*Opti*MOS™ 2 Power-Transistor

Features

• Fast switching MOSFET for SMPS

• Optimized technology for notebook DC/DC

• Qualified according to JEDEC[1] for target applications

Thermal resistance, junction - soldering point
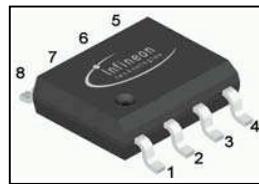
Thermal resistance, junction - ambient

• Excellent gate charge x $R_{DS(on)}$ product (FOM)

• Very low on-resistance $R_{DS(on)}$

• Avalanche rated

• dv/dt rated

• Pb-free plating; RoHS compliant

• Halogen-free according to IEC61249-2-21
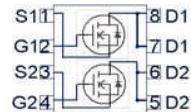
Product Summary

V_{DS}	30	V
$R_{DS(on),max}$	20	mΩ
I_D	7.9	A

P-DSO-8

Type	Package	Marking
BSO200N03	PG-DSO-8	200N3

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value		Unit
			10 secs	**steady state**	
Continuous drain current	I_D	T_A=25 °C[2]	7.9	6.6	A
		T_A=70 °C[2]	6.3	5.3	
Pulsed drain current	$I_{D,pulse}$	T_A=25 °C[3]	32		
Avalanche energy, single pulse	E_{AS}	I_D=7.9 A, R_{GS}=25 Ω	27		mJ
Reverse diode dv/dt	dv/dt	I_D=7.9 A, V_{DS}=20 V, di/dt=200 A/µs, $T_{j,max}$=150 °C	6		kV/µs
Gate source voltage	V_{GS}		±20		V
Power dissipation	P_{tot}	T_A=25 °C[2]	2.0	1.4	W
Operating and storage temperature	T_j, T_{stg}		-55 ... 150		°C
IEC climatic category; DIN IEC 68-1			55/150/56		

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics

Parameter	Symbol	Conditions	min.	typ.	max.	Unit
Thermal resistance, junction - soldering point	R_{thJS}		-	-	50	K/W
Thermal resistance, junction - ambient	R_{thJA}	minimal footprint, $t_p \leq 10$ s	-	-	110	
		minimal footprint, steady state	-	-	150	
		6 cm^2 cooling area[2], $t_p \leq 10$ s	-	-	63	
		6 cm^2 cooling area[2], steady state	-	-	90	

Electrical characteristics, at T_j=25 °C, unless otherwise specified

Static characteristics

Parameter	Symbol	Conditions	min.	typ.	max.	Unit
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=1 mA	30	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=13 µA	1.2	1.6	2	
Zero gate voltage drain current	I_{DSS}	V_{DS}=30 V, V_{GS}=0 V, T_j=25 °C	-	0.1	1	µA
		V_{DS}=30 V, V_{GS}=0 V, T_j=125 °C	-	10	100	
Gate-source leakage current	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	-	10	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=4.5 V, I_D=6.8 A	-	21.7	27	mΩ
		V_{GS}=10 V, I_D=7.9 A	-	16.7	20	
Gate resistance	R_G		-	1.5	-	Ω
Transconductance	g_{fs}	$|V_{DS}|$>2$|I_D|R_{DS(on)max}$, I_D=7.9 A	9	18	-	S

[1] J-STD20 and JESD22

[2] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

[3] See figure 3

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics						
Thermal resistance, ju	C_{iss}	V_{GS}=0 V, V_{DS}=15 V, f=1 MHz	-	756	1010	pF
Thermal resistance, j	C_{oss}		-	270	360	
Reverse transfer capacitance	C_{rss}		-	37	56	
Turn-on delay time	$t_{d(on)}$	V_{DD}=15 V, V_{GS}=10 V, I_{D}=3.9 A, R_{G}=2.7 Ω	-	3.9	5.8	ns
Rise time	t_{r}		-	3.2	4.8	
Turn-off delay time	$t_{d(off)}$		-	14	22	
Fall time	t_{f}		-	2.2	3.3	
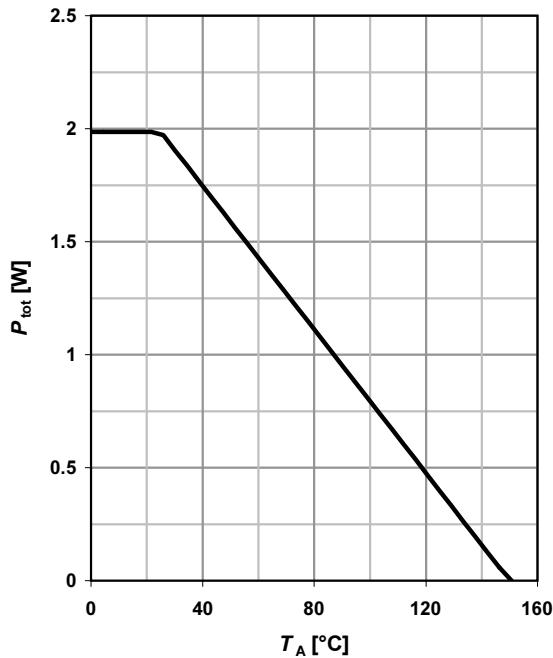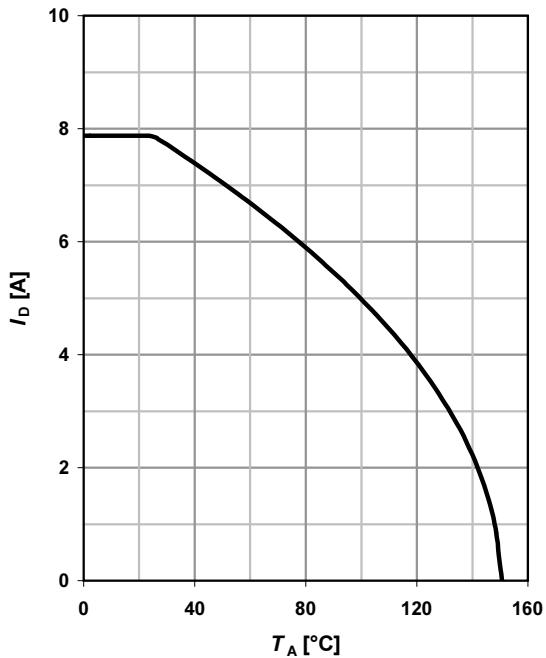
Gate Charge Characteristics[4]

Parameter	Symbol	Conditions	Values			Unit
Gate to source charge	Q_{gs}	V_{DD}=15 V, I_{D}=3.9 A, V_{GS}=0 to 5 V	-	2.2	2.9	nC
Gate charge at threshold	$Q_{g(th)}$		-	1.2	1.6	
Gate to drain charge	Q_{gd}		-	1.5	2.3	
Switching charge	Q_{sw}		-	2.5	3.5	
Gate charge total	Q_{g}		-	6	8	
Gate plateau voltage	$V_{plateau}$		-	2.9	-	V
Gate charge total, sync. FET	$Q_{g(sync)}$	V_{DS}=0.1 V, V_{GS}=0 to 5 V	-	5.1	7	nC
Output charge	Q_{oss}	V_{DD}=15 V, V_{GS}=0 V	-	6	8	

Reverse Diode

Parameter	Symbol	Conditions	Values			Unit
Diode continous forward current	I_{S}	T_{A}=25 °C	-	-	2	A
Diode pulse current	$I_{S,pulse}$		-	-	32	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_{F}=2 A, T_{j}=25 °C	-	0.77	1	V
Reverse recovery charge	Q_{rr}	V_{R}=12 V, I_{F}=I_{S}, di_{F}/dt =400 A/µs	-	-	8	nC
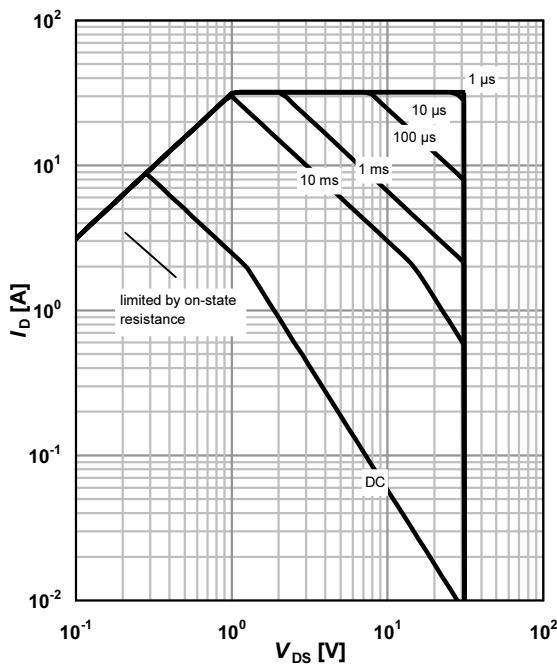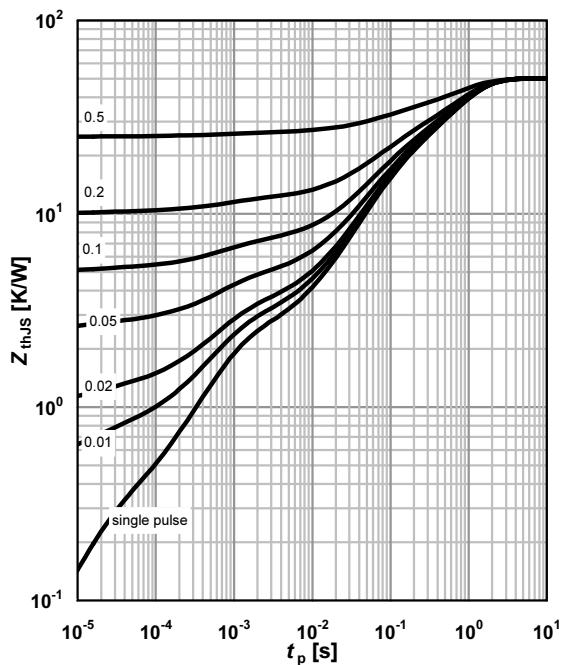
[4] See figure 16 for gate charge parameter definition
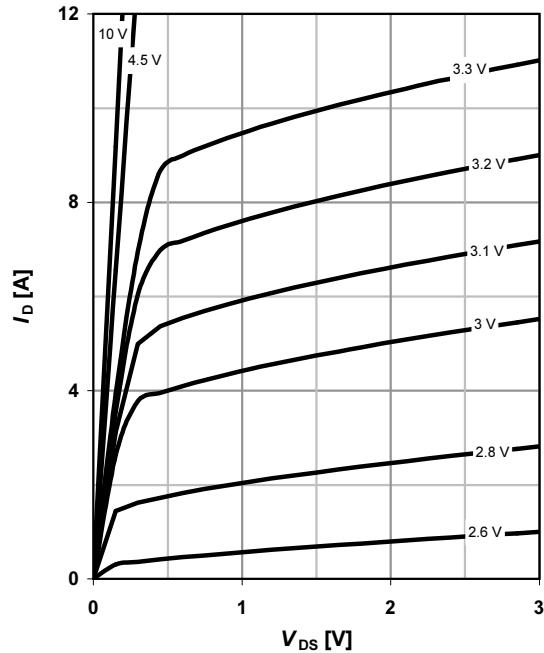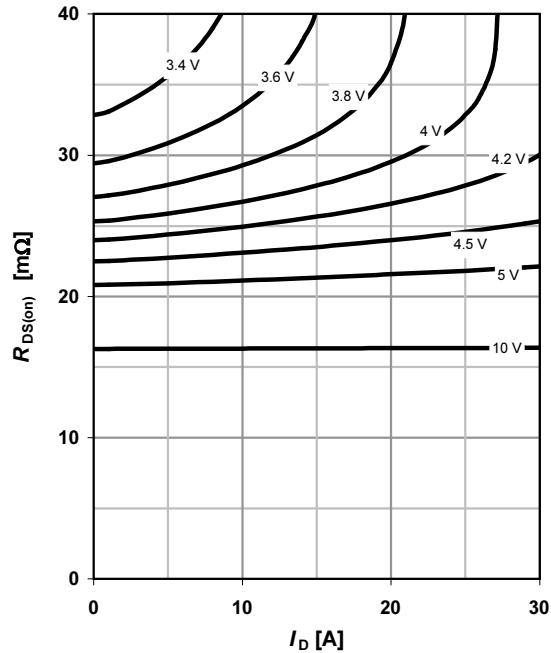
1 Power dissipation

P_{tot}=f(T_A); t_p≤10 s

2 Drain current

I_D=f(T_A); V_{GS}≥10 V; t_p≤10 s

3 Safe operating area

Thermal resistance,

Thermal resistance,

4 Max. transient thermal impedance

junction - solderir Z_{thJS}=f(t_p)
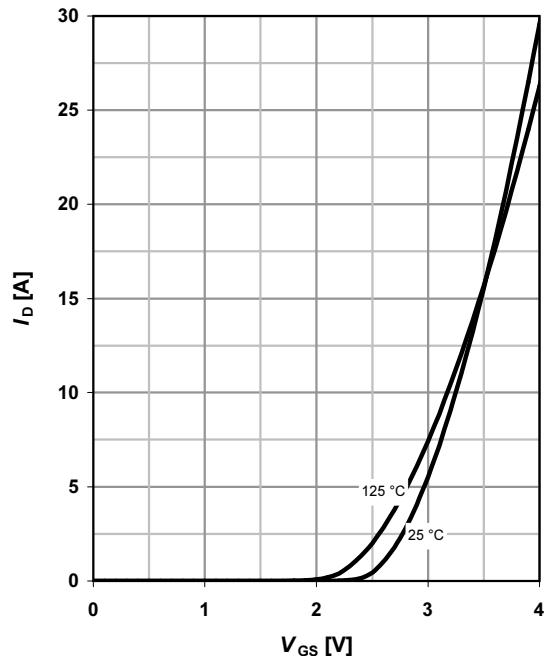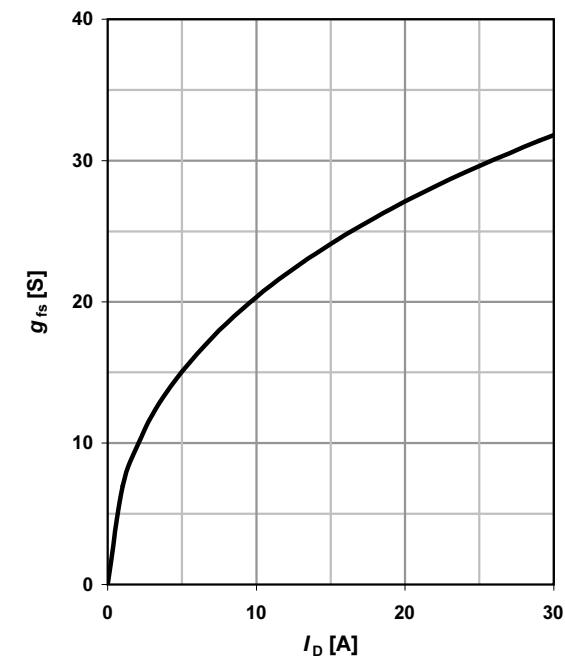
junction - ambier parameter: D=t_p/T
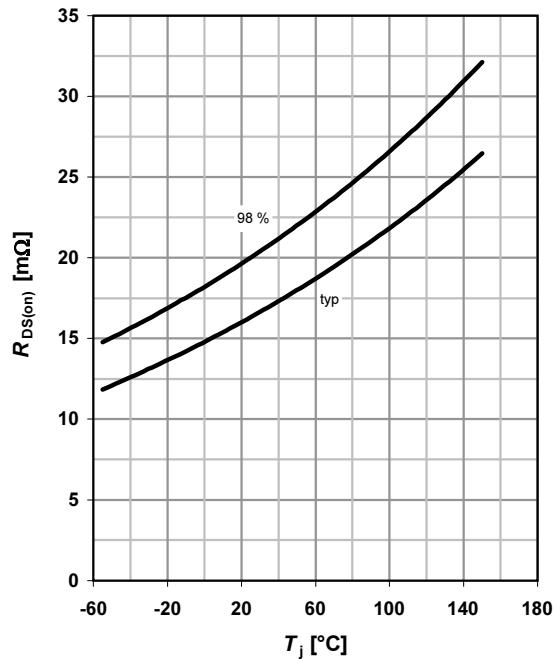
5 Typ. output characteristics

I_D=f(V_{DS}); T_j=25 °C

parameter: V_{GS}

6 Typ. drain-source on resistance

$R_{DS(on)}$=f(I_D); T_j=25 °C

parameter: V_{GS}

7 Typ. transfer characteristics

Thermal resistance,

Thermal resistance,
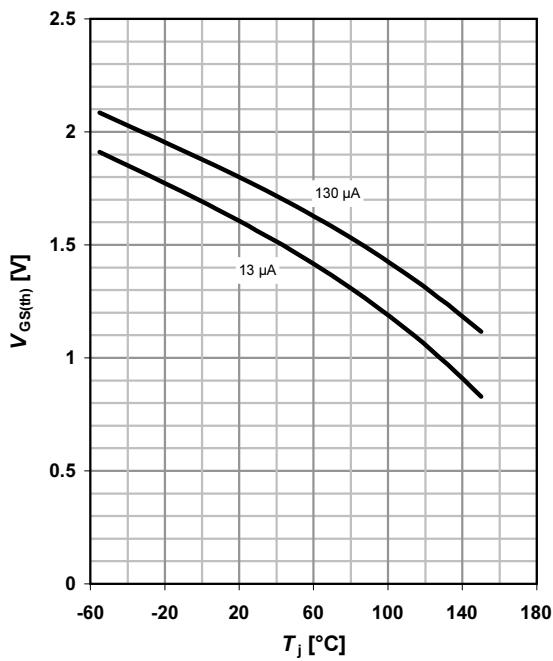
8 Typ. forward transconductance

junction - solderir g_{fs}=f(I_D); T_j=25 °C
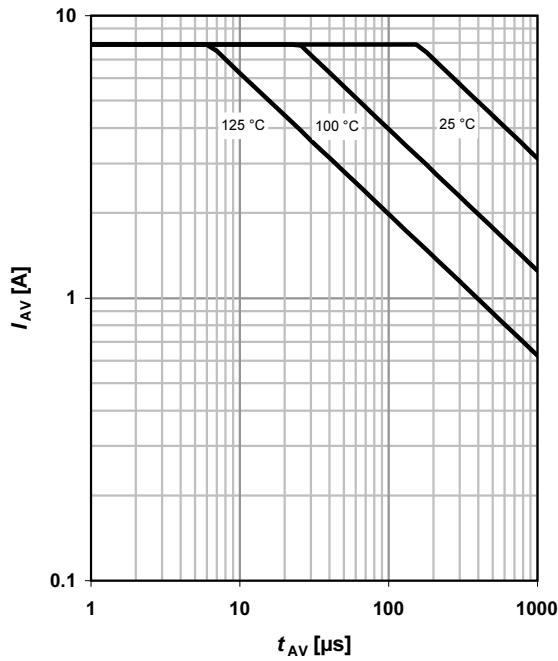
junction - ambient

9 Drain-source on-state resistance

$R_{DS(on)}$=f(T_j); I_D=7.9 A; V_{GS}=10 V

10 Typ. gate threshold voltage

$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}
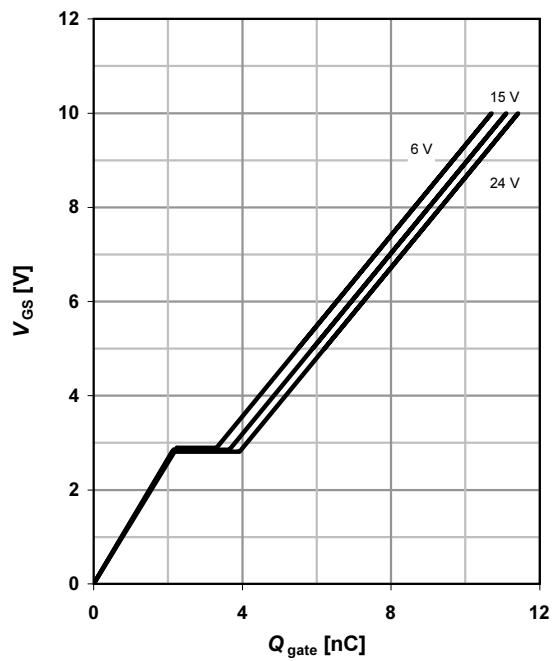
parameter: I_D

11 Typ. capacitances

Thermal resistance,

Thermal resistance,

12 Forward characteristics of reverse diode

junction - solderir I_F=f(V_{SD})

junction - ambier parameter: T_j
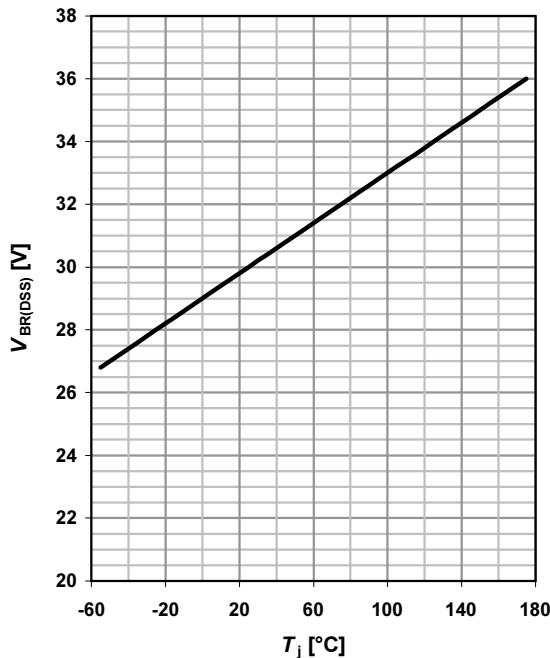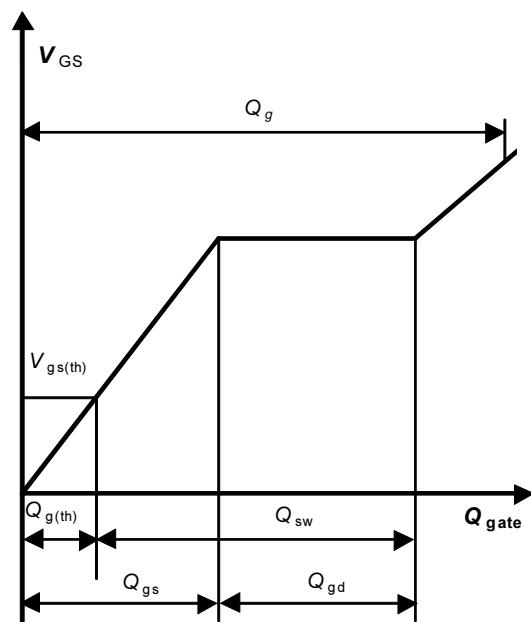
13 Avalanche characteristics

I_{AS}=f(t_{AV}); R_{GS}=25 Ω

parameter: $T_{j(start)}$

14 Typ. gate charge

V_{GS}=f(Q_{gate}); I_D=3.9 A pulsed

parameter: V_{DD}

15 Drain-source breakdown voltage
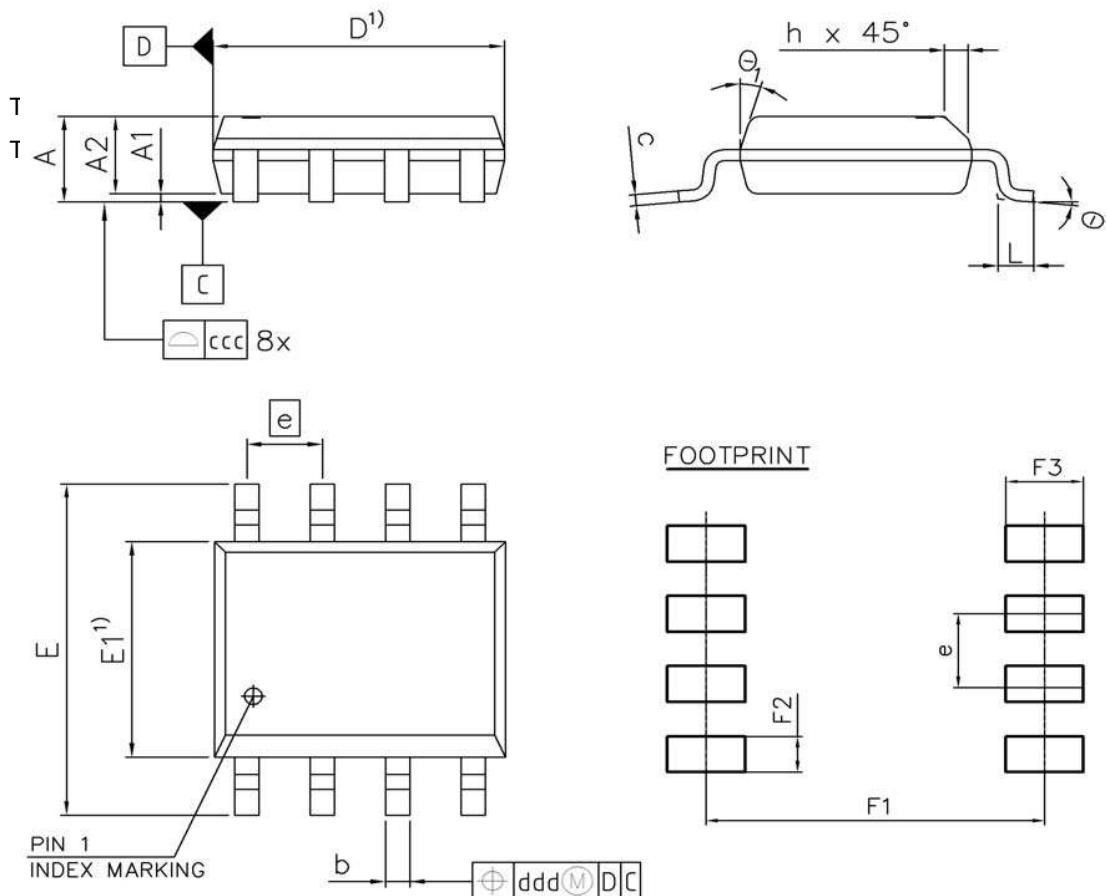
Thermal resistance, junction - soldering point

Thermal resistance, junction - ambient

16 Gate charge waveforms

Package Outline   **PG-DSO-8**

1) DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	1.75	-	0.069
A1	0.10	-	0.004	-
A2	1.25	1.65	0.049	0.065
b	0.35	0.51	0.014	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27		0.050	
N	8		8	
L	0.39	0.89	0.015	0.035
h	0.23	0.50	0.009	0.020
Θ	0°	8°	0°	8°
Θ₁	-	19°	-	19°
ccc	0.10		0.004	
ddd	0.25		0.010	
F1	5.59	5.79	0.220	0.228
F2	0.55	0.75	0.022	0.030
F3	1.21	1.41	0.048	0.056

DOCUMENT NO. Z8B00003333
SCALE
EUROPEAN PROJECTION
ISSUE DATE 09.01.2008
REVISION 02

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (www.infineon.com).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office. The Infineon Technologies component described in this Data Sheet may be used in life-support devices or systems and/or automotive, aviation and aerospace applications or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support, automotive, aviation and aerospace device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.