A DIVISION OF CIRRUS LOGIC

CS4225

Digital Audio Conversion System

Features

- Stereo 16-bit A/D Converters
- Quad 16-bit D/A Converters
- Sample Rates From 4 kHz to 50 kHz
- >100 dB DAC Signal-to-Noise Ratio
- Variable Bandwidth Auxiliary 12-bit A/D
- Programmable Input Gain & Output Attenuation
- +5V Power Supply
- On-chip Anti-aliasing and Output Smoothing Filters
- Error Correction and De-Emphasis

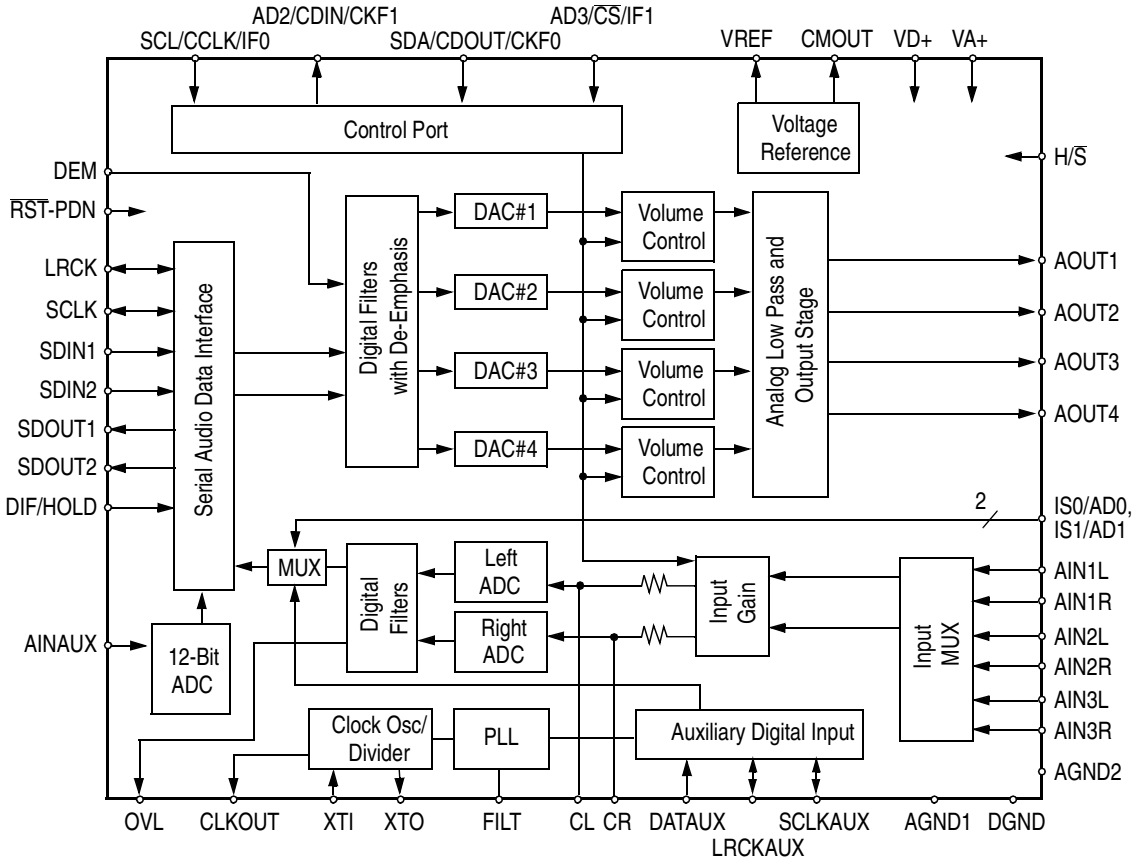
Description

The CS4225 is a single-chip, stereo analog-to-digital and quad digital-to-analog converter using delta-sigma conversion techniques. Applications include CD-quality music, FM radio quality music, telephone-quality speech. Four D/A converters make the CS4225 ideal for surround sound and automotive applications.

The CS4225 is supplied in a 44-pin plastic package with J-leads (PLCC) or as a die.

ORDERING INFORMATION

CS4225-KL	0° to 70° C	44-pin PLCC
CS4225-BL	-40° to 85° C	44-pin PLCC
CS4225-YU	-40° to 85° C	die
CDB4225		Evaluation Board



Preliminary Product Information | This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

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ANALOG CHARACTERISTICS

(T_A = 25°C; VA+, VD+ = +5V; Full Scale Input Sine wave, 1 kHz; Word Clock = 48 kHz (PLL in use); Measurement Bandwidth is 20 Hz to 20 kHz; Local components as shown in "Recommended Connection Diagram"; SPI mode, Format 0, unless otherwise specified.)

Parameter *	Symbol	Min	Typ	Max	Units
Analog Input Characteristics - Minimum gain setting (0 dB); unless otherwise specified.					
ADC Resolution Audio channels Auxiliary channel		16 12	-	-	Bits Bits
ADC Differential Nonlinearity		-	-	±0.9	LSB
Dynamic Range Audio channels(A weighted):		82	85	-	dB
Total Harmonic Distortion + Noise (A weighted)	THD+N	-	-85	-82	dB
Interchannel Isolation		-	85	-	dB
Interchannel Gain Mismatch		-	-	.1	dB
Frequency Response Audio channels(0 to 0.454 Fs):		-3.0	-	+0.2	dB
Programmable Input Gain		-0.2	-	46.7	dB
Gain Step		1.3	1.5	1.7	dB
Offset Error		-	10	-	LSB
Full Scale Input Voltage (Auxiliary and Audio channels):		2.66	2.8	2.94	V_{pp}
Gain Drift		-	100	-	ppm/°C
Input Resistance (Note 1)		10	-	-	kΩ
Input Capacitance		-	-	15	pF
CMOUT Output Voltage		1.9	2.1	2.3	V

Notes: 1. Input resistance is for the input selected. Non-selected inputs have a very high (>1MΩ) input resistance. The input resistance will vary with gain value selected, but will always be greater than the min. value specified.

***** Parameter definitions are given at the end of this data sheet.

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (Continued)

Parameter *		Symbol	Min	Typ	Max	Units
Analog Output Characteristics - Minimum Attenuation; Unless Otherwise Specified.						
DAC Resolution			16	-	-	Bits
DAC Differential Nonlinearity			-	-	±0.9	LSB
Total Dynamic Range	(DAC muted,A weighted)		100	-	-	dB
Total Harmonic Distortion	(Note 2)	THD	-	-	0.01	%
Instantaneous Dynamic Range (DAC not muted, Note 2, A weighted)			85	88	-	dB
Interchannel Isolation	(Note 2)		-	85	-	dB
Interchannel Gain Mismatch			-	-	0.2	dB
Frequency Response	(0 to 0.476 Fs)		-3.0	-	+0.2	dB
Programmable Attenuation	(All Outputs)		0.2	-	-117	dB
Attenuation Step			0.88	1.0	1.12	dB
Offset Voltage			-	10	-	mV
Full Scale Output Voltage	(Note 2)		2.66	2.8	2.94	V_{pp}
Gain Drift			-	100	-	ppm/°C
Deviation from Linear Phase			-	-	5	Degrees
Out of Band Energy	(Fs/2 to 2Fs)		-	-60	-	dB
Analog Output Load	Resistance: Capacitance:		8 -	- -	- 100	kΩ pF
Power Supply						
Power Supply Current	Operating Power Down		- -	120 1	TBD TBD	mA mA
Power Supply Rejection	(1 kHz)		-	40	-	dB

Notes: 2. 10 kΩ, 100 pF load.

16-Bit Audio A/D Decimation Filter Characteristics

(See graphs towards the end of this data sheet)

Parameter	Symbol	Min	Typ	Max	Units
Passband (to -3 dB corner) (Fs is conversion freq.)		0	-	0.454Fs	Hz
Passband Ripple		-	-	±0.1	dB
Transition Band		0.40Fs	-	0.60Fs	Hz
Stop Band		≥ 0.60Fs	-	-	Hz
Stop Band Rejection		75	-	-	dB
Group Delay		-	10/Fs	-	s
Group Delay Variation vs. Frequency		-	-	0.0	µs

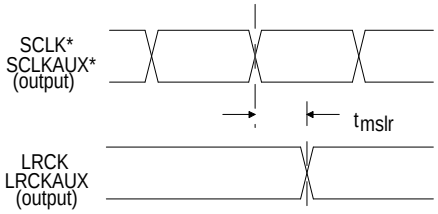
D/A Interpolation Filter Characteristics (See graphs toward the end of this data sheet)

Parameter	Symbol	Min	Typ	Max	Units
Passband (to -3 dB corner) (Fs is conversion freq.)		0	-	0.476Fs	Hz
Passband Ripple		-	-	±0.1	dB
Transition Band		0.442Fs	-	0.567Fs	Hz
Stop Band		≥0.567Fs	-	-	Hz
Stop Band Rejection		50	-	-	dB
Stop Band Rejection with Ext. 2Fs RC filter		57	-	-	dB
Group Delay		-	12/Fs	-	s
Group Delay Variation vs. Frequency		-	-	TBD	µs

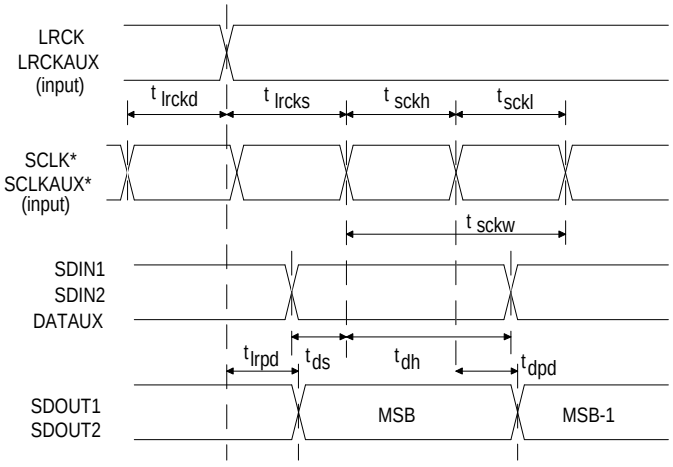
SWITCHING CHARACTERISTICS (T_A = 25°C; VA+, VD+ = +5V, outputs loaded with 30pF)

Parameter		Symbol	Min	Typ	Max	Units
SCLK period		t_{sckw}	80	-	-	ns
SCLK high time		t_{sckh}	25	-	-	ns
SCLK low time		t_{sckl}	25	-	-	ns
Input Transition Time	10% to 90% points		-	-	10	ns
Input Clock Frequency	Crystals XTI		32 32	- -	26000 26000	kHz kHz
Input Clock (XTI) low time			30	-	-	ns
Input Clock (XTI) high time			30	-	-	ns
Input clock jitter tolerance			-	500	-	ps
PLL clock recovery frequency	LRCK, LRCKAUX SCLK, SCLKAUX		32 2.048	- -	50 3.200	kHz MHz
CLKOUT duty cycle			45	50	55	%
Audio ADC's & DAC's sample rate		Fs	4	-	50	kHz
$\overline{RST}$-PDN low time	(Note 5)		500	-	-	ns
MSB output from LRCK edge (Format 1 and 3)		t_{lrpd}	-	-	50	ns
SDOUT output from SCLK edge		t_{dpd}	-	-	50	ns
SDIN setup time before SCLK edge		t_{ds}	-	-	35	ns
SDIN hold time after SCLK edge		t_{dh}	-	-	35	ns
LRCK to SCLK delay (slave mode)		t_{lrckd}	35	-	-	ns
LRCK to SCLK setup (slave mode)		t_{lrcks}	35	-	-	ns
LRCK to SCLK alignment (master mode)		t_{mslr}	-20	-	20	ns

Note: 5. After Powering up the CS4225, $\overline{RST}$-PDN should be held low for 50 ms to allow the voltage reference to settle.



Audio Ports Master Mode Timing



*Active edge of SCLK, SCLKAUX depends on selected format.

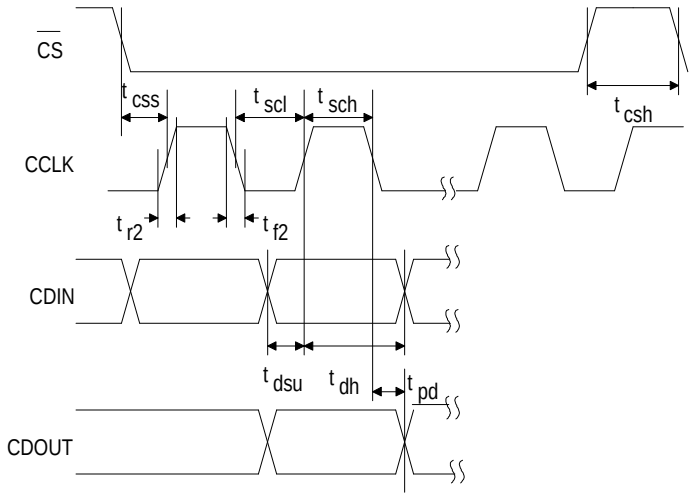
Audio Ports Slave Mode and Data I/O timing

SWITCHING CHARACTERISTICS - CONTROL PORT

(T_A = 25°C VD+, VA+ = 5V±10%; Inputs: logic 0 = DGND, logic 1 = VD+, C_L = 30pF)

Parameter	Symbol	Min	Max	Units
SPI Mode (H/$\overline{S}$=0)				
CCLK Clock Frequency	f_{sck}	0	1	MHz
$\overline{CS}$ High Time Between Transmissions	t_{csh}	1.0		µs
$\overline{CS}$ Falling to SCK Edge	t_{css}	20		ns
CCLK Low Time	t_{scl}	500		ns
CCLK High Time	t_{sch}	500		ns
CDIN to CCLK Rising Setup Time	t_{dsu}	250		ns
CCLK Rising to DATA Hold Time CDIN (Note 9)	t_{dh}	50		ns
CCLK Falling to CDOUT stable	t_{pd}		250	ns
Rise Time of CDOUT	t_{r1}		25	ns
Fall Time of CDOUT	t_{f1}		25	ns
Rise Time of CCLK and CDIN	t_{r2}		100	ns
Fall Time of CCLK and CDIN	t_{f2}		100	ns

Notes: 9. Data must be held for sufficient time to bridge the transition time of CCLK.

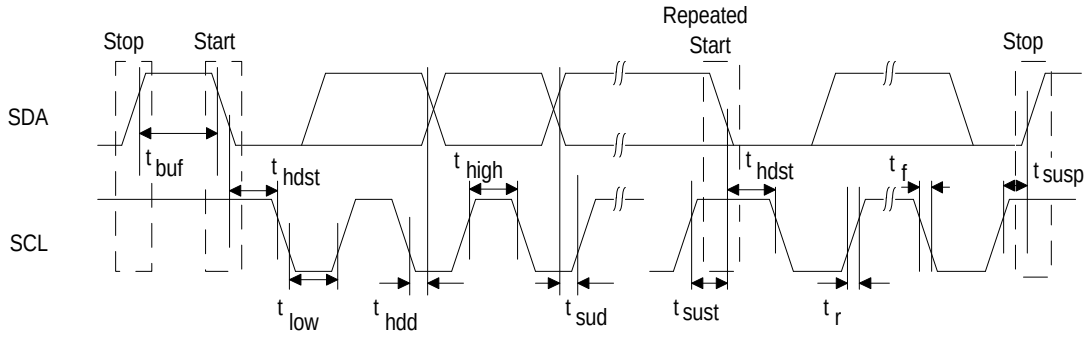


SWITCHING CHARACTERISTICS - CONTROL PORT

(T_A = 25°C; VD+, VA+ = 5V±10%;Inputs: logic 0 = DGND, logic 1 = VD+, C_L = 20pF)

Parameter		Symbol	Min	Max	Units
I^2C® Mode (H/$\overline{S}$ = floating)	Note 10				
SCL Clock Frequency		f_{scl}	0	100	kHz
Bus Free Time Between Transmissions		t_{buf}	4.7		µs
Start Condition Hold Time (prior to first clock pulse)		t_{hdst}	4.0		µs
Clock Low Time		t_{low}	4.7		µs
Clock High Time		t_{high}	4.0		µs
Setup Time for Repeated Start Condition		t_{sust}	4.7		µs
SDA Hold Time from SCL Falling	Note 11	t_{hdd}	0		µs
SDA Setup Time to SCL Rising		t_{sud}	250		ns
Rise Time of Both SDA and SCL Lines		t_r		1	µs
Fall Time of Both SDA and SCL Lines		t_f		300	ns
Setup Time for Stop Condition		t_{susp}	4.7		µs

Notes: 10. Use of the I^2C® bus interface requires a license from Philips.
I^2C® is a registered trademark of Philips Semiconductors.
11. Data must be held for sufficient time to bridge the 300ns transition time of SCL.



ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, all voltages with respect to 0V.)

Parameter		Symbol	Min	Typ	Max	Units
Power Supplies:	Digital	VD	-0.3	-	6.0	V
	Analog	VA	-0.3	-	6.0	V
Input Current	(Except Supply Pins)		-	-	±10.0	mA
Analog Input Voltage			-0.3	-	(VA+)+0.3	V
Digital Input Voltage			-0.3	-	(VD+)+0.3	V
Ambient Temperature	(Power Applied)		-55	-	+125	°C
Storage Temperature			-65	-	+150	°C

Warning: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, all voltages with respect to 0V.)

Parameter		Symbol	Min	Typ	Max	Units
Power Supplies:	Digital	VD	4.6	5.0	5.4	V
	Analog	VA	4.6	5.0	5.4	V
Operating Ambient Temperature	CS4225-KL		0	25	70	°C
	CS4225-BL	T_A	-40	25	+85	°C
	CS4225-YU		-40	25	+85	°C

DIGITAL CHARACTERISTICS (T_A = 25°C; VA+, VD+ = 5V)

Parameter		Symbol	Min	Typ	Max	Units
High-level Input Voltage		V_{IH}	(VD+)-1.0	-	(VD+)+0.3	V
Low-level Input Voltage		V_{IL}	-0.3	-	1.0	V
High-level Output Voltage at I_0 = -2.0 mA		V_{OH}	(VD+)-0.3	-	-	V
Low-level Output Voltage at I_0 = 2.0 mA		V_{OL}	-	-	0.1	V
Input Leakage Current	(Digital Inputs)		-	-	10	µA
Output Leakage Current	(High-Z Digital Outputs)		-	-	10	µA

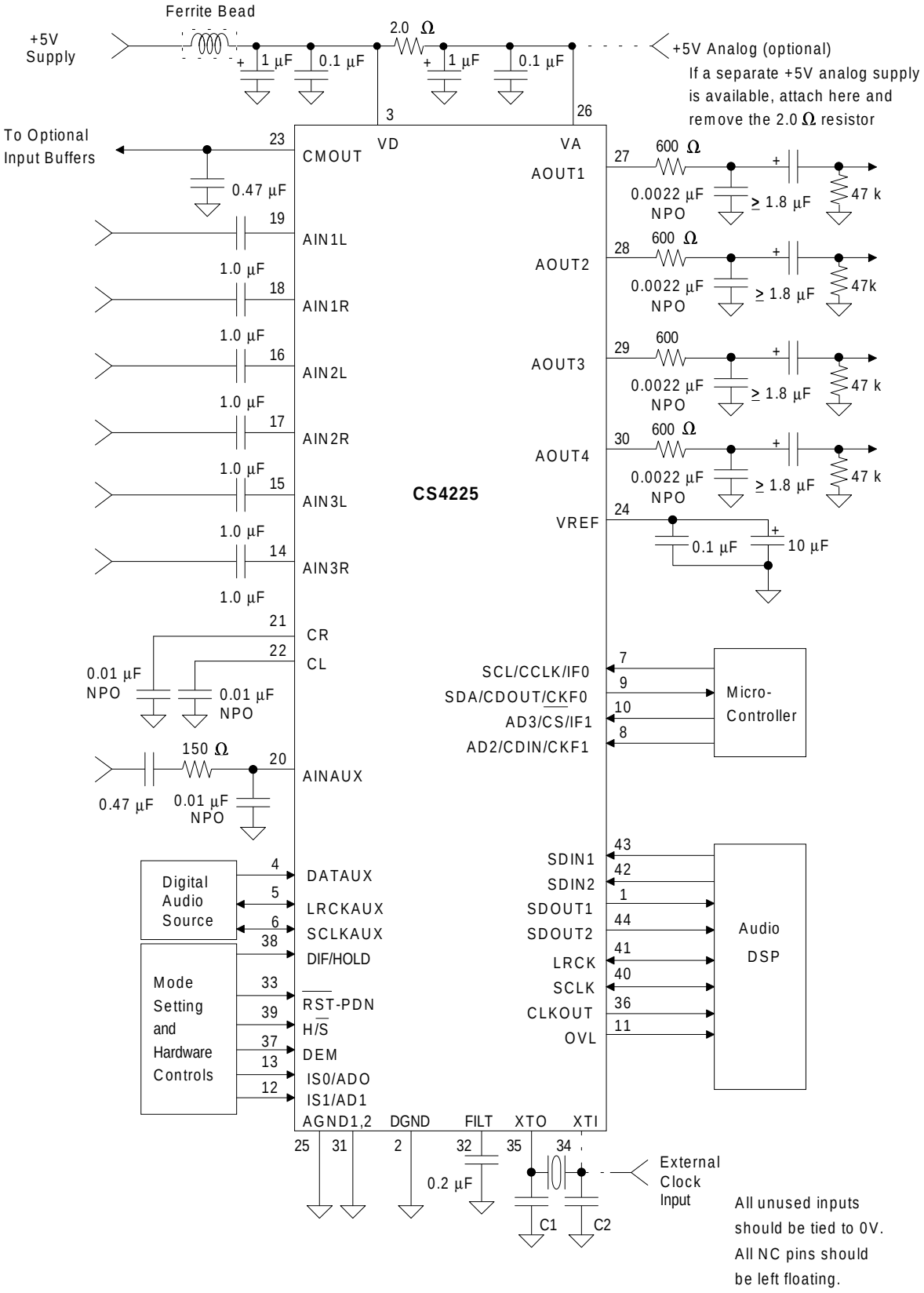


Figure 1 - Recommended Connection Diagram

FUNCTIONAL DESCRIPTION

Overview

The CS4225 has 2 channels of 16-bit analog-to-digital conversion and 4 channels of 16-bit digital-to-analog conversion. An auxiliary 12-bit ADC is also provided. The ADCs and the DACs are delta-sigma type converters. The ADC inputs have adjustable input gain, while the DAC outputs have adjustable output attenuation.

Digital audio data for the DACs and from the ADCs is communicated over a serial port. Separate pins for input and output data are provided, allowing concurrent writing to and reading from the device. Control for the functions available on the CS4225 are communicated over a serial microcontroller style interface, or may be set via dedicated mode pins. Figure 1 shows the recommended connection diagram for the CS4225.

Analog Inputs

Line Level Inputs

AIN1R, AIN1L, AIN2R, AIN2L, AIN3R, AIN3L and AINAUX are the line level input pins (See Figure 1). These pins are internally biased to the CMOUT voltage (nominally 2.1V). A 1µF DC blocking capacitor allows signals centered around 0V to be input. Figure 2 shows an optional dual op amp buffer which combines level shifting with a gain of 0.5 to attenuate the standard line level of $2V_{rms}$ to $1V_{rms}$. The CMOUT reference level is used to bias the op amps to approximately one half the supply voltage.

Series DC blocking capacitors eliminate the contribution of signal offset to the A/D converters. The CS4225 offset calibration scheme yields minimum DC offset values assuming that the inputs are AC coupled (DC blocking capacitor present). If a DC blocking capacitor is not used, a greater DC offset will occur. This offset could be as high as ± 70 codes, with no gain.

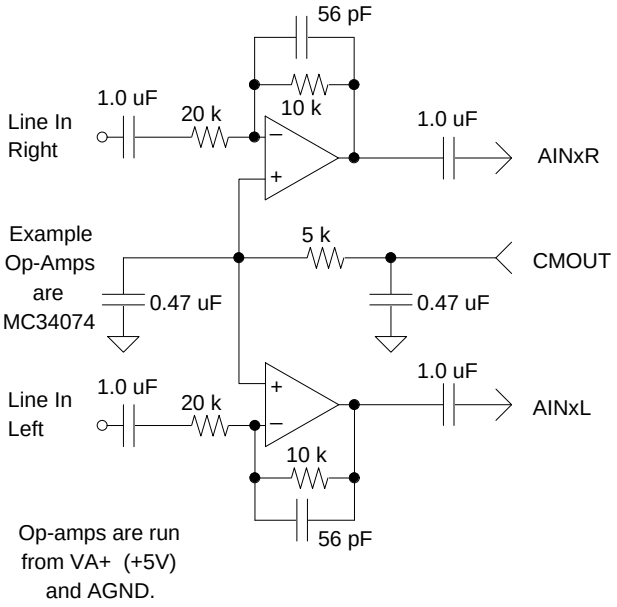


Figure 2 - Optional Line Input Buffer

The input pair for the 16-bit ADCs is selected by IS0 and IS1, which are accessible in the Input Selection Byte in software mode or dedicated pins in the hardware mode. Antialiasing filters follow the input mux, providing antialiasing for the input channels. These filters consist of internal resistors and external capacitors attached to the CR and CL pins. The CR and CL capacitors must be low voltage coefficient type, such as NPO.

The analog signal is input to the 12-bit ADC via the AINAUX pin. An antialiasing filter of 150Ω with 0.01µF to ground is required (See Figure 1) along with a series DC blocking capacitor. The AINAUX signal is normally routed to the 12-bit ADC. This signal may also be routed to the Left 16-bit ADC (replacing the selected left input), under control of the AIM bit in the 12-bit ADC Mode Byte. In this mode, the input antialiasing filters and gain adjustment operates on the AINAUX signal.

Adjustable Input Gain

The signals from the line inputs are routed to a programmable gain circuit which provides up to

46.5dB of gain in 1.5dB steps. The gain is adjustable only by software control. Level changes only take effect on zero crossings to minimize audible artifacts. If there is no zero crossing, then the requested level change will occur after a time-out of 511 frames (10.6ms at 48kHz frame rate). There is a separate zero crossing detector for each channel.

Analog Outputs

Line Level Outputs

AOUT1, AOUT2, AOUT3 and AOUT4 output a $1V_{rms}$ level for full scale, centered around +2.1V. Figure 1 shows the recommended 1.0µF dc blocking capacitor with a 40kΩ resistor to ground. When driving impedances greater than 10kΩ, this provides a high pass corner of 20Hz. These outputs may be muted.

Output Level Attenuator

The DAC outputs are each routed through an attenuator, which is adjustable in 1dB steps. Output attenuation is available via software control only. Level changes are implemented such that the noise is attenuated by the same amount as the signal (equivalent to using an analog attenuator after the signal source), until the residual output noise is equal to the noise floor in the mute state. Level changes only take effect on zero crossings to minimize audible artifacts. If there is no zero crossing, then the requested level change will occur after a time-out of 511 frames (10.6ms at 48kHz frame rate). There is a separate zero crossing detector for each channel.

Each output can be independently muted via mute control bits. In addition, the CS4225 has an optional mute on consecutive zeros feature, where each DAC output will mute if it receives 512 consecutive zeros. A single non-zero value will unmute the DAC output.

ADC and DAC Coding

The CS4225 converters use 2's complement coding. Table 1 shows the ADC and DAC transfer functions.

16-bit ADC/DAC		12-bit ADC	
Input/ Output Voltage*	2's Complement Code	2's Complement Code	Input Voltage*
+1.400000	7FFF	7FF	+1.40000
+1.399957	7FFE	7FE	+139864
+0.000064	0001	001	+0.00204
+0.000021	0000	000	+0.00068
-0.000021	FFFF	FFF	-0.00068
-0.000064	FFFE	FFE	-0.00204
-1.399957	8001	801	-1.39864
-1.400000	8000	800	-1.40000

*Nominal voltage relative to CMOUT (Typ 2.1V), no gain or attenuation. Actual measured voltage will be modified by the gain error and offset error specifications.

Table 1 - ADC/DAC Input and Output Coding Table

Calibration

Both output offset voltage and input offset error are minimized by an internal calibration cycle. At least one calibration cycle must be invoked after power up. A calibration will occur any time the part comes out of reset, including the power-up reset. For the most accurate calibration, some time must be allowed between powering up the CS4225, or exiting the power-down state, and initiating a calibration cycle, to allow the voltage reference to settle. This is achieved by holding $\overline{\text{RST}}$/PDN low for at least 50ms after power up or exiting power-down mode. Input offset error will be calibrated for all inputs and outputs.

A calibration takes 192 frames to complete, based on the frequency of the VCO of the inter-

nal PLL. The calibration that occurs following a reset will proceed at a rate determined by the free running VCO in software mode (which will be at a Fs of about 40kHz), or the selected clock input in hardware mode.

The CS4225 can be calibrated whenever desired. A control bit, CAL, in the Control Byte, is provided to initiate a calibration. The sequence is:
1) Set CAL to 1, the CS4225 sets $\overline{\text{CALD}}$ to 1 and begins to calibrate.
2) Wait for $\overline{\text{CALD}}$ to go to 0. $\overline{\text{CALD}}$ will go to 0 when the calibration is done.
3) Set CAL to 0 for normal operation.

Clock Generation

The master clock to operate the CS4225 may be generated by using the on-chip crystal oscillator, by using the on-chip PLL, or by using an external clock source. If the active clock source stops for 5µs, the CS4225 will enter a power down state to prevent overheating. In all modes it is desirable to have SCLK & LRCK synchronous to the selected master clock.

Clock Source

The CS4225 requires a high frequency (256 Fs) clock to run the internal logic. The Clock Source bits, CS0/1/2, in the Clock Mode Byte determine the source of the clock. A high frequency crystal can be attached to XTI and XTO, or a high frequency clock can be input into XTI. In both these cases, the internal PLL is disabled, with the VCO shut off. The externally supplied high frequency clock can be 256 Fs, 384 Fs or 512 Fs. The CI0/1 bits in the Clock Mode Byte must be set accordingly. When using the on-chip crystal oscillator, external loading capacitors are required (see Figure 1). High frequency crystals (> 8 MHz) should be parallel resonant, fundamental mode and designed for 20pF loading (equivalent to 40pF to ground on each leg). An example crystal supplier is CAL crystal (714) 991-1580.

Alternatively, the on-chip PLL may be used to generate the required high frequency clock. The PLL input clock is either 1 Fs, 32 Fs or 64 Fs and may be input from the Auxiliary Port, (either LRCKAUX or SCLKAUX), the DSP port, (either LRCK or SCLK), or from XTI/XTO. In this last case, a 1 Fs clock may be input into XTI, or a 1 Fs crystal attached across XTI/XTO. The gain of the internal inverter is adjusted for the low crystal frequency. Using a clock at 64 Fs will result in less PLL clock jitter than a clock at 1 Fs. The PLL will lock onto a new 1 Fs clock within 5,000 Fs periods. If the PLL input clock is removed, the VCO will drift to the low frequency end of its frequency range.

In software mode, bits CS2/1/0 in the Clock Mode Byte establish the clock source and frequency. In Hardware mode, either LRCKAUX is the clock reference, at 1 Fs, or the clock may be input to XTI.

Master Clock Output

CLKOUT is a master clock output provided to allow synchronization of external components. Available CLKOUT frequencies of 1 Fs, 256 Fs, 384 Fs, and 512 Fs, are selectable by the CO0/1 bits of the Clock Mode Byte. When switching between clock sources, CLKOUT will always remain low or high for > 10ns.

Synchronization

In normal operation, the DSP port and Auxiliary port operate synchronously to the CS4225 clock source. It is advisable to mute the DACs when changing from one synchronization source to another to avoid the output of undesirable audio signals as the CS4225 resynchronizes. If data which is not synchronous to the clock source is input to the CS4225, then samples will be dropped or repeated, which will cause audible artifacts. Under such conditions, the CS4225 may not meet all data sheet performance specifications.

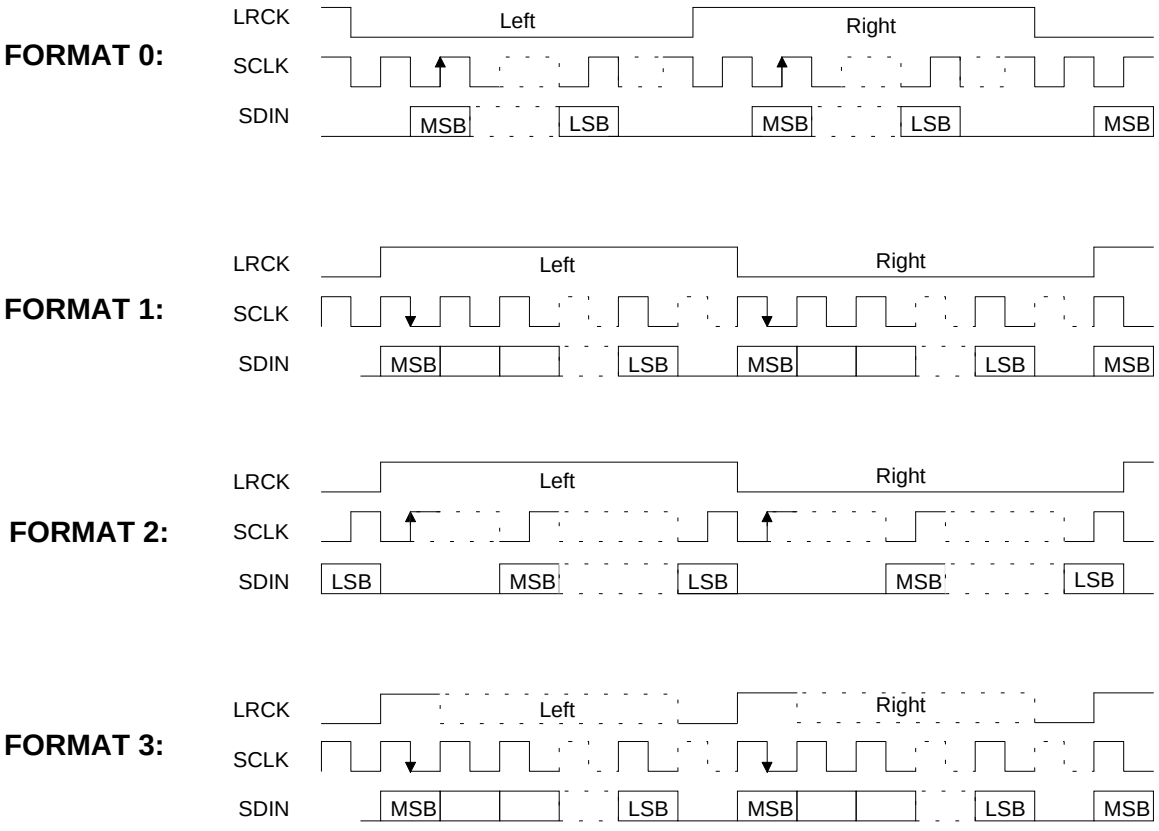


Figure 3 - Audio DSP and Auxiliary Port Data Input Formats.

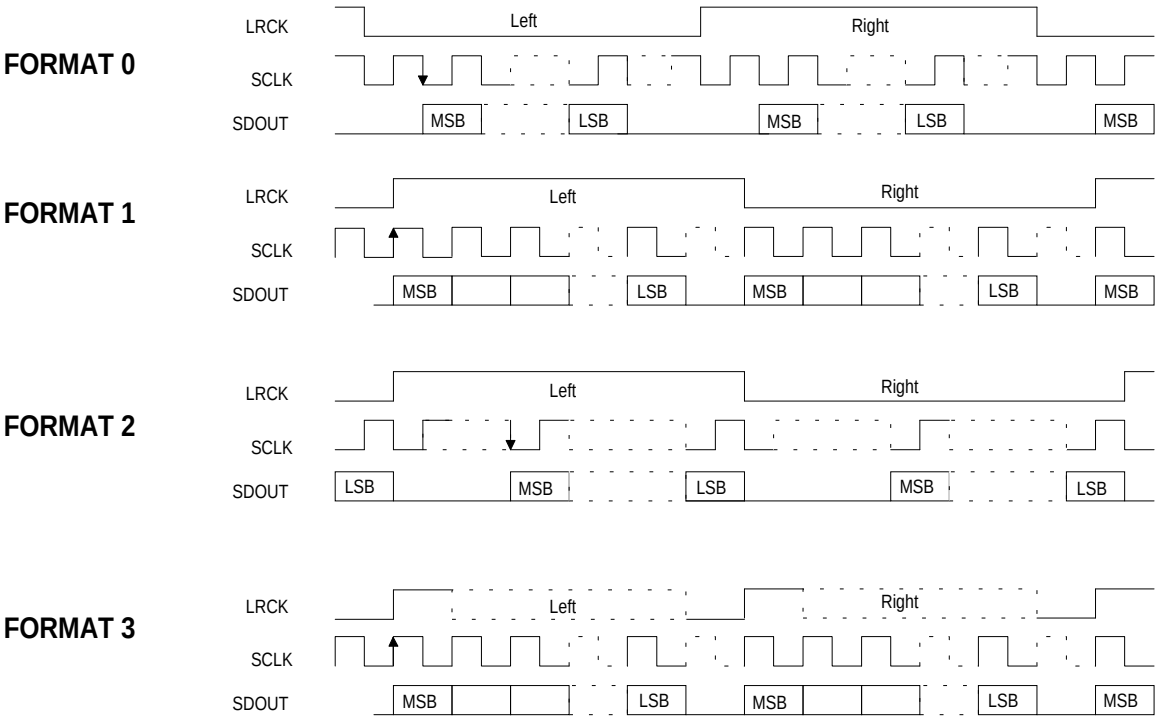


Figure 4 - Audio DSP Port Data Output Formats.

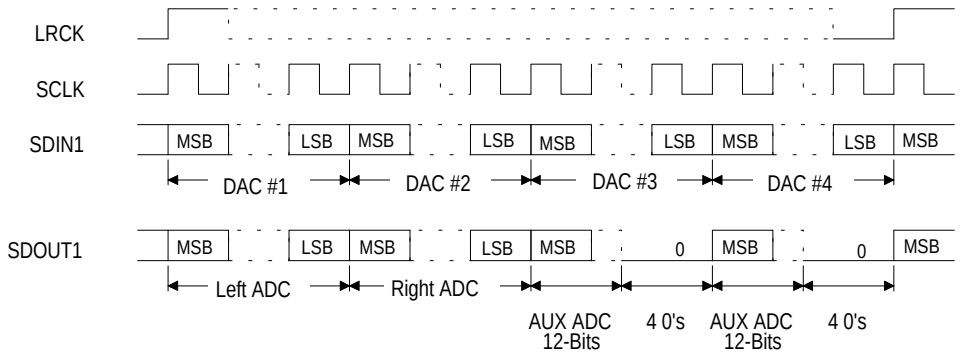


Figure 5 - One data line mode (Format 4)

Digital Interfaces

There are 3 digital interface ports: the audio DSP port, the auxiliary digital audio port and the control port. In hardware mode (H/$\overline{S}$ pin high) the control port is disabled, and various modes can be set via pins. In hardware mode, control of the input gain, output level and some modes are not possible.

Audio DSP Serial Interface Signals

The serial interface clock, SCLK, is used for transmitting and receiving audio data. SCLK can be generated by the CS4225 (master mode) or it can be input from an external SCLK source (slave mode). The number of SCLK cycles in one system sample period is programmable to be 32, 48, or 64. When SCLK is an input, 32 SCLK's per system sample period is not recommended, due to potential interference effects; 64 SCLK's per sample period should be used instead.

The Left/Right clock (LRCK) is used to indicate left and right data, also the start of a new sample period. It may be output from the CS4225, or it may be generated from an external controller. The frequency of LRCK is equal to the system sample rate, Fs.

SDIN1 and SDIN2 are the data input pins, each of which drives a pair of DACs. SDIN1 left data is for DAC #1, SDIN1 right data is for DAC #2, SDIN2 left data is for DAC #3, and SDIN2 right data is for DAC #4. SDOUT1 carries the data from the 2 16-bit ADCs. SDOUT2 carries the data from the 12-bit ADC. The audio DSP port may also be configured so that all 4 DAC's data is input on SDIN1, and all 3 ADC's data is output on SDOUT1.

Audio DSP Serial Interface Formats

The audio DSP port supports 5 alternate formats, shown in Figures 3, 4, and 5. These formats are chosen through the DSP Port Mode Byte in software mode. In hardware mode, four formats are available as selected by the DIF and IF0 pins.

The 12-bit ADC data format is similar to the 16-bit data format. The 12-bit data is positioned to the most significant end of a 16-bit field, with the lower 4 bits set to zero. The resulting 16-bit value is output on SDOUT2 in both the left and right channel positions. The format will be the same as the selected SDOUT1 format.

Figure 5 shows the timing for format 4, where all 4 DAC data words are presented on SDIN1, and the 3 ADC data words are presented on SDOUT1.

Format 5 is a combination mode. The data output is as in Format 1, on the SDOUT1 and SDOUT2 pins. The data input is as in Format 4 on SDIN1. In both format 4 and 5, LRCK duty cycle is 50% if it is an output.

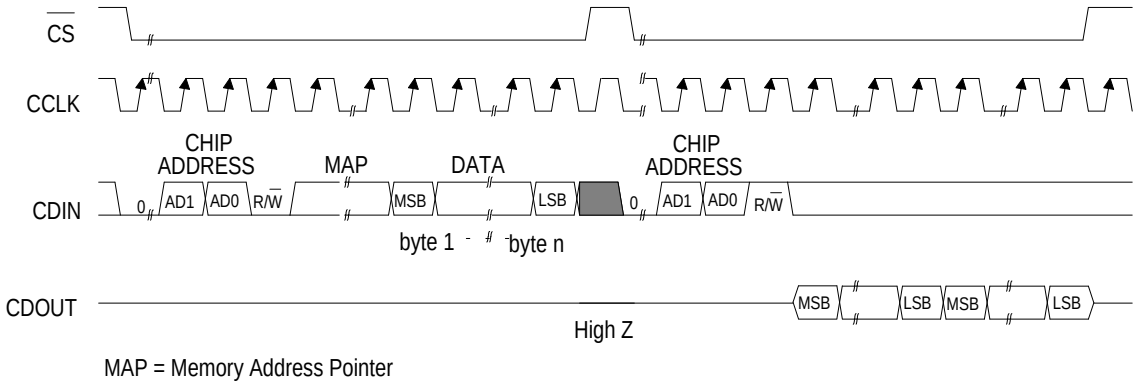


Figure 6 - Control Port Timing, SPI mode

Auxiliary Audio Port Signals

The auxiliary port provides an alternate way to input digital audio signals into the CS4225, and allows the CS4225 to synchronize the system to an external digital audio source. This port consists of clock, data and left/right clock pins named, SCLKAUX, DATAAUX and LRCKAUX. These signals are fed through to the SCLK, SDOUT1 and LRCK pins. There is a two frame delay from DATAAUX to SDOUT1. When the auxiliary port is used, the frequency of LRCKAUX must equal to the system sample rate, Fs, but no particular phase relationship is required.

Auxiliary Audio Port Formats

Input data on DATAAUX is clocked into the part by SCLKAUX using the format selected in the Auxiliary Port Mode Byte. In hardware mode, the auxiliary port format is the same as the DSP port format and is determined by the DIF pin. The auxiliary audio port supports the same 4 formats as the audio DSP port in 2 data line mode. LRCKAUX is used to indicate left and right data samples, and the start of a new sample period. SCLKAUX and LRCKAUX may be output from the CS4225, or they may be generated from an external source, as set by the AMS control bit in Software mode or IF1 in Hardware mode.

Control Port Signals

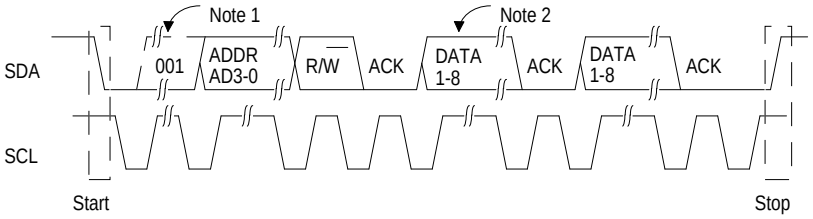
The control port has 2 modes: SPI and $I^2C^®$, with the CS4225 as a slave device. The SPI mode is selected by setting the H/$\overline{S}$ pin low. $I^2C^®$ mode is selected by floating the H/$\overline{S}$ pin. If the H/$\overline{S}$ pin is floated, add a 0.1µF capacitor to ground on the H/$\overline{S}$ pin to minimize noise pickup.

SPI Mode

In SPI mode, $\overline{CS}$ is the CS4225 chip select signal, CCLK is the control port bit clock, (input into the CS4225 from the microcontroller), CDIN is the input data line from the microcontroller, CDOUT is the output data line to the microcontroller, and AD0 and AD1 form the chip address.

The pins AD0, AD1 must be tied to one of 4 possible chip addresses. To write to a particular CS4225, the AD0, AD1 bits must match the state of the AD0, AD1 pins for that chip. This allows up to 4 CS4225 devices to co-exist on one control port bus.

Figure 6 shows the operation of the control port in SPI mode. To write to a register, bring $\overline{CS}$ low. The first 5 bits on CDIN must be zero. The next 2 bits form the chip address. The eighth bit is a read/write indicator (R/$\overline{W}$), which should be



Note 1: The first 3 address bits for the CS4225 must be 001.

Note 2: If operation is a write, this byte contains the Memory Address Pointer, MAP.

Figure 7 - Control Port Timing, I²C® Mode

low to write. The next 8 bits form the Memory Address Pointer (MAP), which is set to the address of the register that is to be updated. The next 8 bits are the data which will be placed into register designated by the MAP. During writes, the CDOUT output stays in the Hi-Z state. It may be externally pulled high or low with a 47kΩ resistor.

The CS4225 has a MAP auto increment capability, enabled by the INCR bit in the MAP register. If INCR is a zero, then the MAP will stay constant for successive reads or writes. If INCR is set to a 1, then MAP will auto increment after each byte is read or written, allowing block reads or writes of successive registers.

To read a register, the MAP has to be set to the correct address by executing a partial write cycle which finishes ($\overline{CS}$ high) immediately after the MAP byte. The auto MAP increment bit (INCR) may be set or not, as desired. To begin a read, bring $\overline{CS}$ low, send out the chip address and set the read/write bit (R/$\overline{W}$) high. The next falling edge of CCLK will clock out the MSB of the addressed register (CDOUT will leave the high impedance state). If the MAP auto increment bit is set to 1, the data for successive registers will appear consecutively.

I²C ®Mode

In I²C® mode, SDA is a bidirectional data line. Data is clocked into and out of the part by the clock, SCL, with the clock to data relationship as shown in Figure 7. There is no $\overline{CS}$ pin. Pins AD0, AD1, AD2, AD3 form the chip address. The upper 3 bits of the 7 bit address field must be 001. To communicate with a CS4225, the LSBs of the chip address field, which is the first byte sent to the CS4225, should match the settings of the AD0, AD1, AD2, AD3 pins. The eighth bit of the address bit is the R/$\overline{W}$ bit (high for a read, low for a write). If the operation is a write, the next byte is the Memory Address Pointer which selects the register to be read or written. If the operation is a read, the contents of the register pointed to by the Memory Address Pointer will be output. Setting the auto increment bit in MAP, allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit. Use of the I²C bus® compatible interface requires a license from Philips. I²C bus® is a registered trademark of Philips Semiconductors.

Control Port Bit Definitions

All registers can be written and read back, except the status report byte, which is read only. See the following bit definition tables for bit assignment information.

Memory Address Pointer (MAP)

B7	B6	B5	B4	B3	B2	B1	B0
INCR	0	0	0	MAP3	MAP2	MAP1	MAP0

MAP3-MAP0 Register Function
- 0 - Reserved
- 1 - Output Attenuator 1
- 2 - Output Attenuator 2
- 3 - Output Attenuator 3
- 4 - Output Attenuator 4
- 5 - Input Gain 1
- 6 - Input Gain 2
- 7 - Auxiliary Port Mode
- 8 - DSP Port Mode
- 9 - Clock Mode
- 10 - Control Byte
- 11 - Status Report Byte
- 12 - Input Channel Select
- 13 - Aux Control Byte
- 14 - Reserved
- 15 - Reserved

INCR Auto Increment Control Bit
- 0 - No auto increment
- 1 - Auto increment on

Output Attenuator Data Byte (1, 2, 3, 4)

B7	B6	B5	B4	B3	B2	B1	B0
0	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0

ATT6 to ATT0 Sets Attenuator Level
- 0 - No attenuation
- 127 - 127 dB attenuation
- ATT0 represents 1.00 dB

Input Gain Setting Data Byte (5, 6)

B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	GN4	GN3	GN2	GN1	GN0

GN4 to GN0 Sets Input Gain
- 0 - No gain
- 31 - 46.5 dB gain
- GN0 represents 1.5 dB

Auxiliary Port Mode Byte (7)

B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	AMS	ACK1	ACK0	ADF1	ADF0

ADF1 - ADF0 Sets Digital Interface Format
- 0 - Format 0 - I^2S
- 1 - Format 1
- 2 - Format 2
- 3 - Format 3

ACK1 - ACK0 Sets number of bit clocks per Fs period
- 0 - 64
- 1 - 48 - gated 64Fs
- 2 - 32 - gated 64Fs
- 3 - 32 - continuous

AMS AUX Master /Slave control bit
- 0 - port is master (SCLKAUX and LRCKAUX are outputs).
- 1 - port is slave (SCLKAUX and LRCKAUX are inputs).

DSP Port Mode Byte (8)

B7	B6	B5	B4	B3	B2	B1	B0
0	0	DMS	DCK1	DCK0	DDF2	DDF1	DDF0

DDF2 - DDF0 Sets Digital Interface Format
- 0 - Format 0 - I^2S
- 1 - Format 1
- 2 - Format 2
- 3 - Format 3
- 4 - One data pin in, One data pin out mode (Format 4).
- 5 - Output is Format 1 on SDOUT1 and SDOUT2, input is Format 4 on SDIN1.

DCK1 - DCK0 Set number of bit clocks per Fs period
- 0 - 64
- 1 - 48 - gated 64 Fs
- 2 - 32 - gated 64 Fs
- 3 - 32 - continuous

DMS DSP Master /Slave control bit
- 0 - port is master (SLCK and LRCK are outputs).
- 1 - port is slave (SLCK and LRCK are inputs).

Clock Mode Byte (9)

B7	B6	B5	B4	B3	B2	B1	B0
0	CO1	CO0	CI1	CI0	CS2	CS1	CS0

CS1 - CS0 Sets the source of the master clock which runs the CS4225.
0 - Crystal Oscillator or XTI (PLL Disabled)
1 - PLL driven by LRCKAUX at 1 Fs
2 - PLL driven by LRCK at 1 Fs
3 - PLL driven by XTI/XTO (XTI at 1 Fs)
4 - PLL driven by SCLK at 32 Fs
5 - PLL driven by SCLK at 64 Fs
6 - PLL driven by SCLKAUX at 32 Fs
7 - PLL driven by SCLKAUX at 64 Fs

CI1 - CI0 Determines frequency of XTI when PLL is disabled.
0 - 256 Fs
1 - 384 Fs
2 - 512 Fs
3 - Reserved

CO1-CO0 Determines CLKOUT frequency
0 - 256 Fs
1 - 384 Fs
2 - 512 Fs
3 - 1 Fs

Control Byte (10)

B7	B6	B5	B4	B3	B2	B1	B0
MUTC	CAL	DEMC	DEM	MUT4	MUT3	MUT2	MUT1

MUT4 to MUT1 Mute Control Bits
0 - Normal Output Level
1 - Selected DAC output muted

DEM Selects De-Emphasis
0 - Normal Flat DAC frequency response
1 - CD De-Emphasis Selected

DEMC Selects De-Emphasis Control Source
0 - De-emphasis is controlled by DEM pin. DEM bit is ignored.
1 - De-emphasis is controlled by DEM bit. DEM pin is ignored.

CAL 0 - Normal Operation
1 - Initiate Calibration

MUTC Controls mute on consecutive zeros function
0 - 512 consecutive zeros will mute DAC
1 - DAC output will not mute on zeros.

Status Report Byte (11)

B7	B6	B5	B4	B3	B2	B1	B0
OVL1	OVL0	OV12	ACK	0	LOCK	$\overline{\text{CALD}}$	0

OVL1 to OVL0 16 - bit ADC overload bits.
00 - Normal ADC input levels
01 - -6 dB level
10 - -3 dB level
11 - Clipping
Indicates one of the ADC's has been overdriven. These bits are "sticky". They will stay set until read, when they will return to 00 if the overload is no longer present.

OV12 12-bit ADC overload bit
0 - normal input
1 - clipped input
This bit is also "sticky"

ACK Control port data check bit
0 - Multiple of 8 clocks received last word (SPI Mode)
1 - Error, not multiple of 8 clocks received.

LOCK PLL lock indicator
0 - PLL not locked. If PLL is selected, DAC outputs will mute
1 - PLL locked

$\overline{\text{CALD}}$
0 - Calibration done
1 - Calibration in progress

Input Selection Byte (12)

B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	0	0	IS1	IS0

IS1 - IS0 Select input channel
0 - Select AIN1
1 - Select AIN2
2 - Select AIN3
3 - Select Auxiliary Digital Input Port

Aux Control Byte (13)

B7	B6	B5	B4	B3	B2	B1	B0
AIM	0	0	0	0	0	0	0

AIM Auxiliary Input Mode Control Bit
0 - AINAUX signal is routed to 12-bit ADC
1 - AINAUX routed to AINL of 16-bit ADC

Reset

$\overline{\text{RST}}$-PDN going low causes all the internal control registers, used in software mode, to be set to the states indicated in Table 1. The reset states are different for hardware mode, see the section on Hardware Mode. $\overline{\text{RST}}$-PDN must be brought low and high at least once after power up. $\overline{\text{RST}}$-PDN returning high causes the CS4225 to execute an offset calibration cycle. $\overline{\text{RST}}$-PDN returning high should occur at least 50ms after the power supply has stabilized.

Power Down Mode

Placing the $\overline{\text{RST}}$-PDN pin into a high impedance state (floating) puts the CS4225 into the power down mode. This may be done by driving the $\overline{\text{RST}}$-PDN pin with a three-state buffer, and setting the buffer to the hi-z state. In power-down mode CMOUT and VREF will not supply current. If the master clock source stops, the CS4225 will power down after 5µs. Power down will change all the control registers to the reset state shown in Table 1.

ATT6 → ATT0	= 127	CS2, CS1,CS0	= 3
GN4 → GN0	= 0	CI1, CI0	= 0
ADF1, ADF0	= 0	CO1, CO0	= 0
ACK1, ACK0	= 0	MUT4 →MUT1	= 1111
AMS	= 1	DEM	= 0
DDF2 → DDF0	= 0	DEMC	= 0
DCK1, DCK1	= 0	MUTC	= 0
DMS	= 1	IS1, IS0	= 0
MAP	= 0	AIM	= 0
CAL	= 0		

Table 1 - Reset State (Software Mode)

After returning to normal operation from power down, an offset calibration cycle must be executed. To leave the power-down state, pull $\overline{\text{RST}}$-PDN low for at least 50ms to allow the internal voltage reference time to settle, then high to initiate an offset calibration cycle.

De-Emphasis

Figure 8 shows the de-emphasis curve. De-emphasis may be enabled under hardware control, using the DEM pin, or by software control using the DEM bit. In software mode, either hardware or software control of de-emphasis may be selected.

The de-emphasis corner frequencies are as shown in Figure 8 for a sample rate of 44.1kHz. Selection of de-emphasis at other sample rates will cause the filter to be applied, but with corner frequencies scaled proportionally to the sample rate.

Hold Function (Software Mode only)

If the digital audio source has an invalid data output pin, then the CS4225 may be configured to cause the last valid analog output level to be held constant. (This sounds much better than a potentially random output level.) HOLD is sampled on the active edge of SCLK. If HOLD is driven high any time during the stereo sample period, both pairs of DAC's hold their current output level, and reject the data currently being input. SDIN input data is ignored while the HOLD pin is high. For normal operation, the HOLD pin must be low.

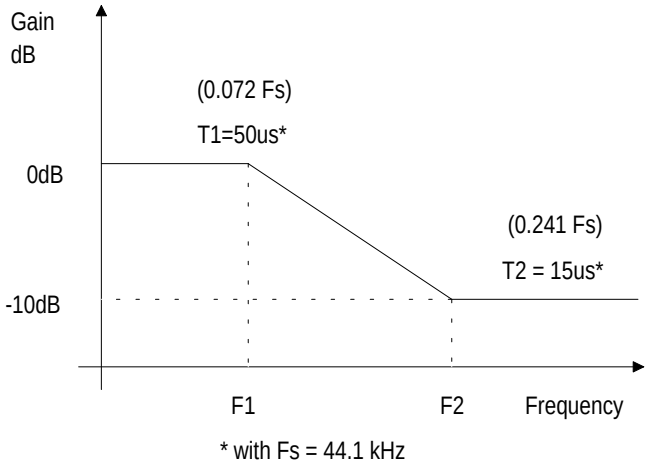


Figure 8 - De-emphasis Curve.

Hardware Mode

Hardware mode is selected by connecting the H/$\overline{S}$ pin to VD. In hardware mode, only certain functions are available:

- de-emphasis,
- digital interface formats 0, 1 and 2, and DSP format 4,
- auxiliary audio port master/slave selection,
- CLKOUT and XTI frequencies are restricted,
- use of PLL is tied to master/slave selection,
- the PLL locks to LRCKAUX only,
- will mute on consecutive zeros.

In addition, the input gain is set to 0dB (no gain), and the attenuator is set to 0dB (no attenuation). The DAC mute bits are set to 0 (not muted). The DSP port and Auxiliary port serial clocks are set to 64 bits per Fs period.

In hardware mode, the DSP port is always in slave mode. The IF1 pin selects the Auxiliary port to be master or slave (low for master, high for slave). When the Auxiliary port is a master, XTI is the clock source and the PLL is off. CKF0 and CKF1 pins define both XTI and CLKOUT frequencies as follows:

CKF1	CKF0	XTI	CLKOUT
0	0	256 Fs	256 Fs
0	1	384 Fs	256 Fs
1	0	512 Fs	256 Fs
1	1	512 Fs	512 Fs

When the Auxiliary port is a slave, LRCKAUX is the clock source at 1 Fs, the PLL is enabled. CKF1 and CKF0 determine CLKOUT as follows:

CKF1	CKF0	CLKOUT
0	0	256 Fs
0	1	384 Fs
1	0	512 Fs
1	1	1 Fs

Functions only available in software mode include:

- input gain adjust & output level adjust,
- digital interface format 3, DSP format 5,
- more clocking flexibility,
- DAC muting,
- setting of number of bit clocks per Fs period,
- turn off mute upon consecutive zeros function,
- 12-bit ADC clipping indicator,
- PLL lock flag,
- routing the AINAUX signal to a 16-bit ADC,
- hold last sample on error.

Power Supply and Grounding

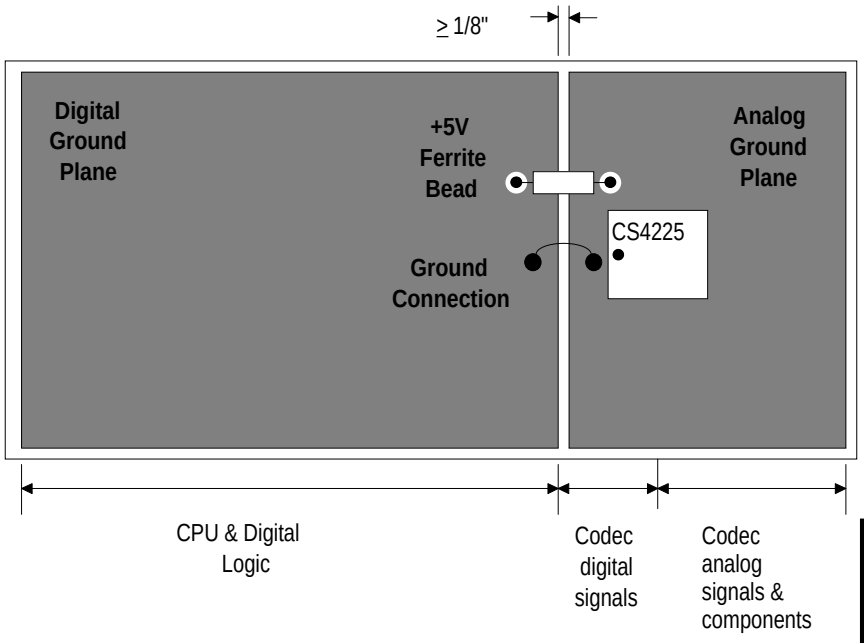
The CS4225, along with associated analog circuitry, should be positioned near to the edge of your circuit board, and have its own, separate, ground plane (see Figure 9). Preferably, it should also have its own power plane. The +5V supply must be connected to the CS4225 via a ferrite bead, positioned closer than 1" to the device. A single connection between the CS4225 ground and the board ground should be positioned as shown in Figure 9. Figure 10 shows the recommended decoupling capacitor layout. Also see Crystal's layout Applications Note, and the CDB4225 evaluation board data sheet for recommended layout of the decoupling components.

The CS4225 will mute the analog outputs if the supply drops below approximately 4 volts.

ADC and DAC Filter Response Plots

Figures 11 through 18 show the overall frequency response, passband ripple and transition band for the CS4225 ADC's and DAC's. Figure 17 shows the DAC's deviation from linear phase.

The 12-bit ADC output is fully decimated to Fs, but is not filtered. Figure 18 shows the noise floor of the output, along with a low frequency full scale signal. External digital filtering is necessary to achieve the desired trade off between measurement bandwidth and dynamic range.



Note that the CS4225 is oriented with its digital pins towards the digital end of the board.

Figure 9. Suggested Layout Guideline

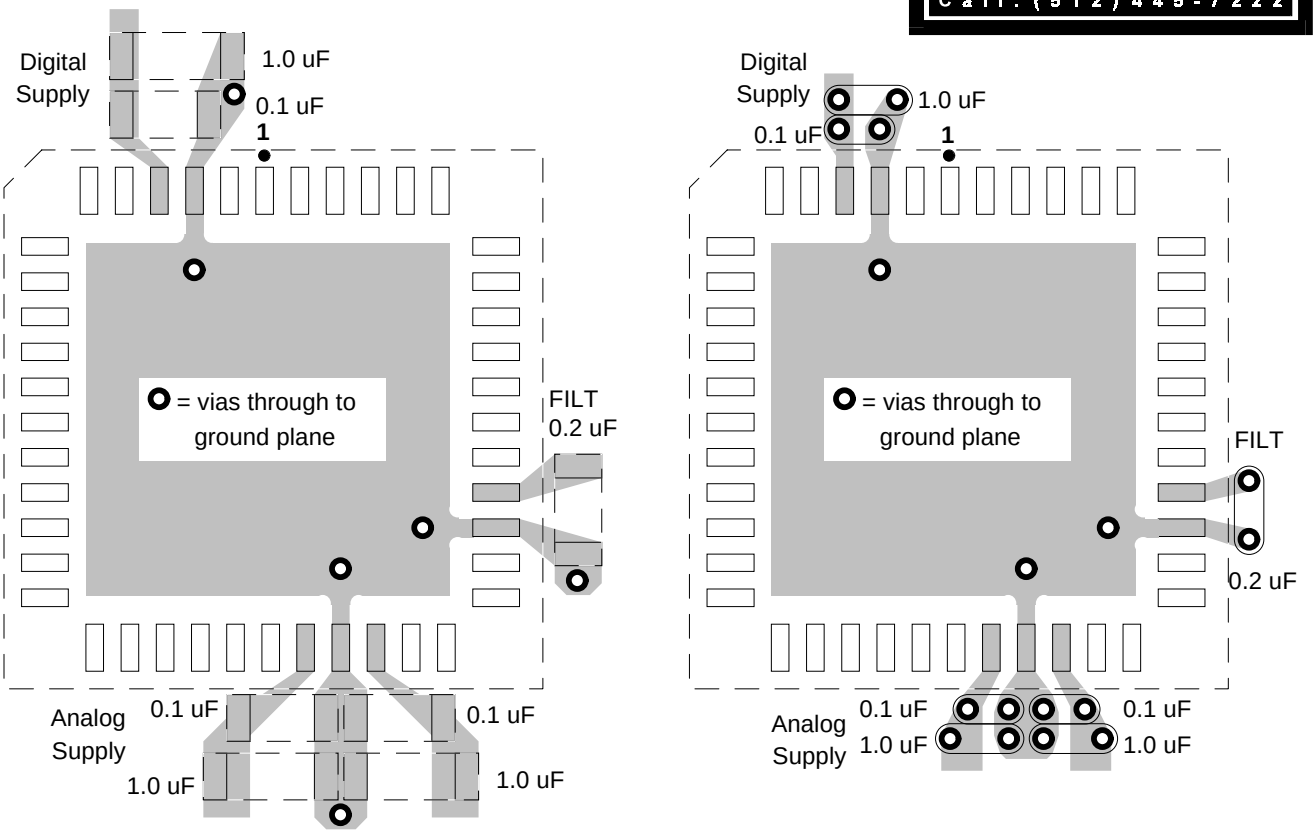


Figure 10. Recommended Decoupling Capacitor Layout

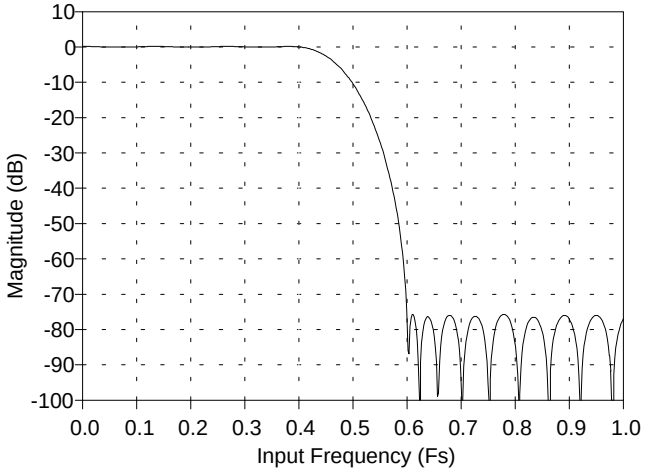


Figure 11. 16-bit ADC Filter Response.

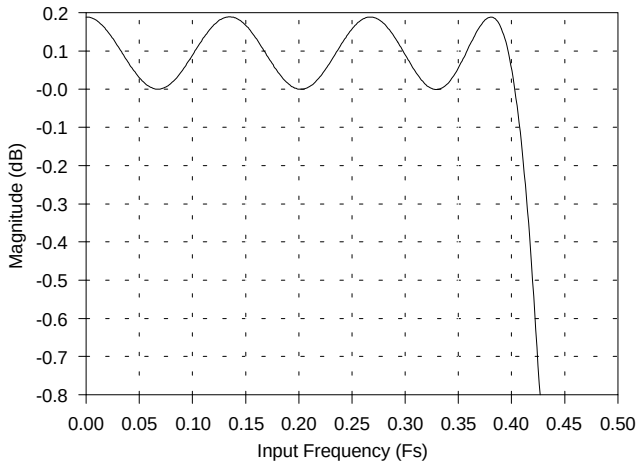


Figure 12. 16-bit ADC Passband Ripple.

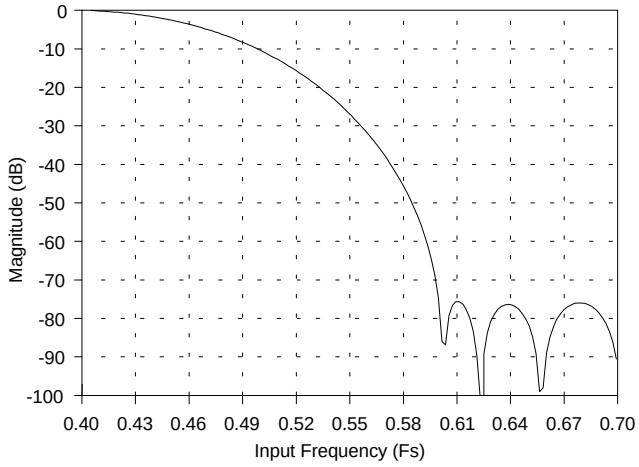


Figure 13. 16-bit ADC Transition Band.

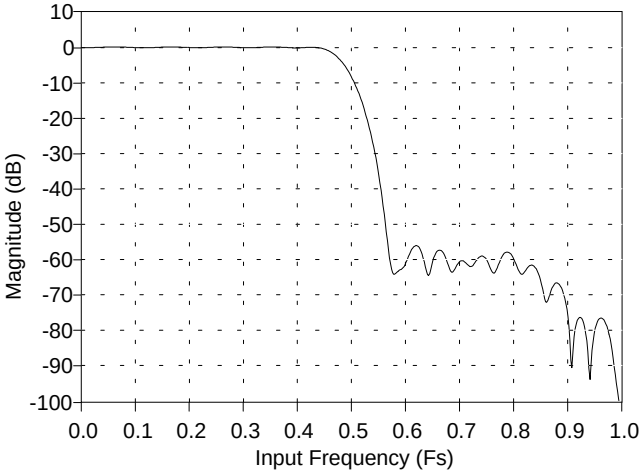


Figure 14. DAC Frequency Response.

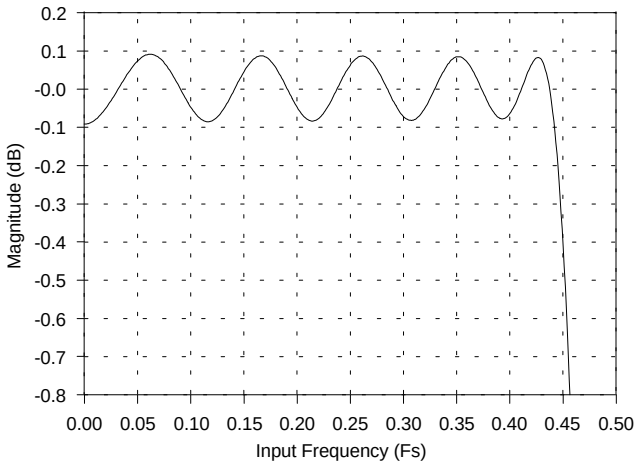


Figure 15. DAC Passband Ripple.

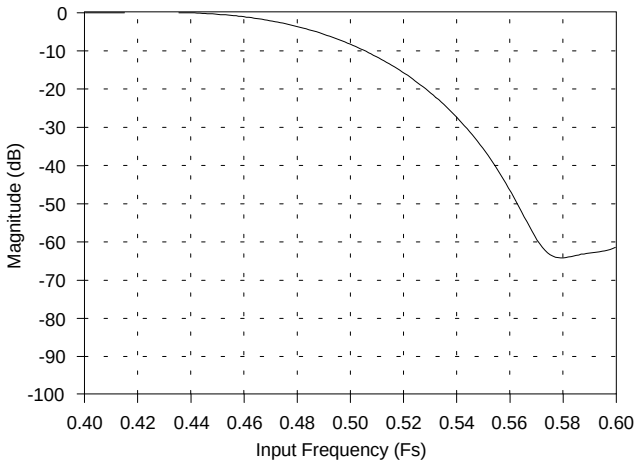


Figure 16. DAC Transition Band.

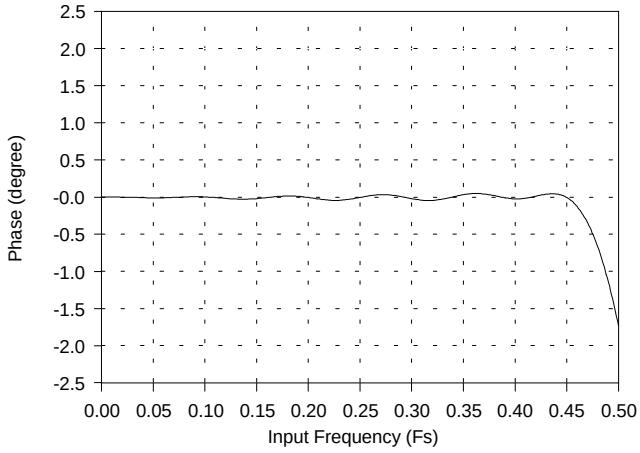


Figure 17. DAC Phase Response.

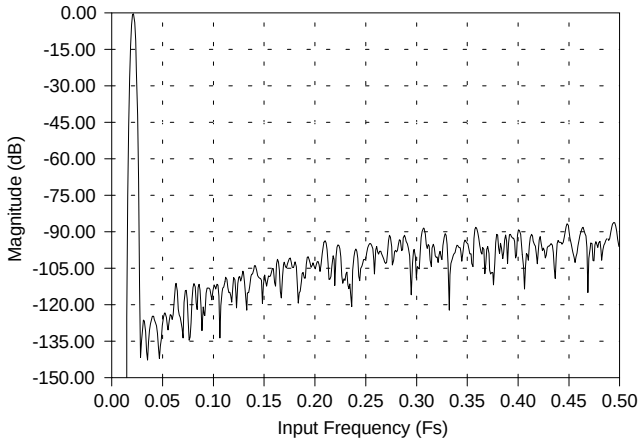
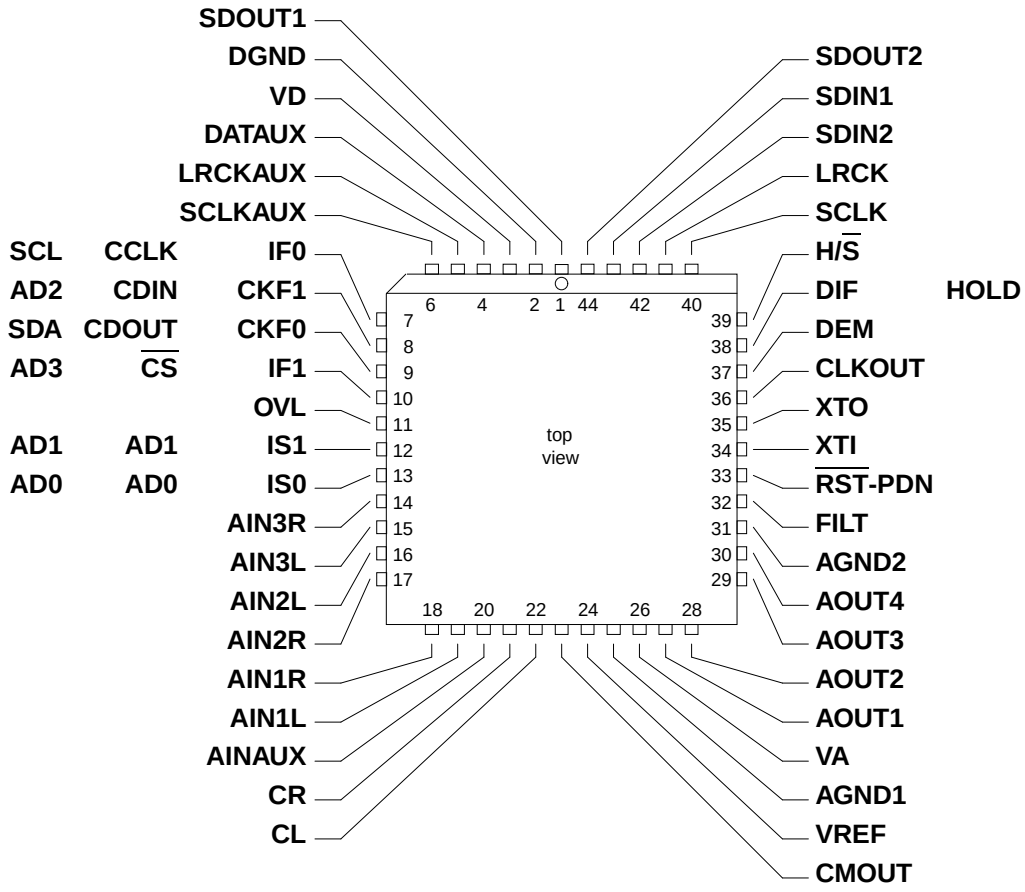


Figure 18. 12-bit ADC Noise with a Low Frequency Full Scale Sine wave input signal.

PIN DESCRIPTIONS



Power Supply

VA - Analog Power Input
+5 V analog supply.

AGND1, AGND2 - Analog Ground
Analog grounds.

VD - Digital Power Input
+ 5 V digital supply.

DGND - Digital Ground
Digital ground.

Analog Inputs

AIN1L, AIN1R - Left and Right Channel Mux Input 1
Analog signal input connections for the right and left channels for multiplexer input 1.

AIN2L, AIN2R - Left and Right Channel Mux Input 2

Analog signal input connections for the right and left channels for multiplexer input 2.

AIN3L, AIN3R - Left and Right Channel Mux Input 3

Analog signal input connections for the right and left channels for multiplexer input 3.

AINAUX - Auxiliary Line Level Input

Analog signal input for the 12-bit A/D converter. In software mode, setting the AIM bit causes AINAUX to replace the left analog input at the multiplexer input.

Analog Outputs

AOUT1, AOUT2, AOUT3, AOUT4 - Audio Outputs

The analog outputs from the 4 D/A converters. Each output can be independently controlled for output amplitude.

CMOUT - Common Mode Output

This common mode voltage output may be used for level shifting when DC coupling is desired. The load on CMOUT must be DC only, with an impedance of not less than 25kΩ. CMOUT should be bypassed with a 0.47µF to AGND.

VREF - Voltage Reference Output, Pin 21

The on-chip generated ADC/DAC reference voltage is brought out to this pin for decoupling purposes. This output must be bypassed with a 10µF capacitor in parallel with a 0.1µF capacitor to the adjacent AGND pin. No other external load may be connected to this output.

Digital Interface Signals

SDIN1 - Serial Data Input 1

Digital audio data for the DACs 1 and 2 is presented to the CS4225 on this pin.

SDIN2 - Serial Data Input 2

Digital audio data for the DACs 3 and 4 is presented to the CS4225 on this pin.

SDOUT1- Serial Data Output 1

Digital audio data from the 16-bit audio ADCs is output from this pin. When selected, DATAAUX is output on SDOUT1.

SDOUT2 - Serial Data Output 2

Digital audio data from the 12-bit audio ADC is output from this pin.

SCLK - DSP Serial Port Clock I/O

SCLK clocks digital audio data into the DACs via SDIN1/2, and clocks data out of the ADCs on SDOUT1/2. Active clock edge depends on the selected format.

LRCK - Left/Right Select Signal I/O

The Left/Right select signal. This signal has a frequency equal to the sample rate. The relationship of LRCK to the left and right channel data depends on the selected format.

$\overline{\text{RST}}$-PDN - Reset and Power-Down Input

The CS4225 must be reset after power up by bringing this pin low, then high. To select power down mode, float this pin, or drive this pin with a three-state buffer, and place the buffer in the Hi-Z state. Low-to-high rise time should be less than 10µs.

DEM - De-emphasis Control

When high, DEM causes the standard Compact Disk de-emphasis frequency response for Fs = 44.1kHz to be applied to the DACs. If H/$\overline{\text{S}}$ is high, this pin is active. If H/$\overline{\text{S}}$ is low, then this pin is enabled by setting the DEMC control bit to 0, and disabled by setting the DEMC control bit to 1.

HOLD/DIF - Digital Interface Format Select Pin / HOLD Control

In software mode, when HOLD is high any time during the sample period, SDIN1 and SDIN2 data is ignored, and the previous "good" sample is presented to the DACs.

In hardware mode, DIF becomes a selection pin which selects audio data I/O formats 0, 1 and 2 (when IF0 is low) using a 3-level selection. Low selects format 0. High selects format 1. Floating selects format 2. Float DIF by tying a 0.01µF capacitor from DIF to ground. In hardware mode, both the auxiliary audio data port and the audio DSP port are set to the same audio format.

SCL/CCLK/IF0 - Serial Control Interface Clock / DSP Interface Mode Select.

In software control mode, SCL/CCLK is the serial control interface clock, and is used to clock control bits into and out of the CS4225.

In hardware control mode, when IF0 is low, the data for DACs 1 and 2 is input on SDIN1, and for DACs 3 and 4 is input on SDIN2. The data from the audio ADCs is presented on SDOUT1 and the data from the 12-bit auxiliary ADC is presented on SDOUT2. In hardware control mode, when IF0 is high, the data for all 4 DACs is input on the SDIN1 pin, and the data from the audio ADCs and the 12-bit auxiliary ADC is output on the SDOUT1 pin. This mode allows a DSP which has only 1 serial input and 1 serial output port to access all the DACs and ADCs.

AD3/$\overline{\text{CS}}$/IF1 - Control Port Chip Select / Interface Control

In $I^2C^®$ software control mode, AD3 is a chip address bit. In SPI software control mode, $\overline{\text{CS}}$ is used to enable the control port interface on the CS4225.

In hardware control mode, IF1 low sets the auxiliary digital audio input port to be master and IF1 high sets the auxiliary digital audio input port to be slave. In slave mode, the PLL is used to generate the internal 256 Fs clock from LRCKAUX, and to generate CLKOUT.

AD2/CDIN/CKF1 - Serial Control Data In / Interface Control

In $I^2C^®$ mode, AD2 is a chip address bit. In SPI software control mode, CDIN is the input data line for the control port interface.

In hardware control mode, CKF0 and CKF1 controls the clock frequency of CLKOUT.

SDA/CDOUT/CKF0 - Serial Control Data Out / Clock Select

In $I^2C^®$ mode, SDA is the control data I/O line. In SPI software control mode, CDOUT is the output data from the control port interface on the CS4225.

In hardware control mode, CKF0 and CKF1 controls the clock frequency of CLKOUT.

DATAUX - Auxiliary Data Input

DATAUX is the auxiliary audio data input line, usually connected to an external digital audio source.

LRCKAUX - Auxiliary Word Clock Input or Output

In auxiliary slave mode, LRCKAUX is a word clock (at Fs) from an external digital audio source. LRCKAUX can be used as the clock reference for the internal PLL. In auxiliary master mode, LRCKAUX is a word clock output (at Fs) to clock an external digital audio source.

SCLKAUX - Auxiliary Bit Clock Input or Output

In auxiliary slave mode, SCLKAUX is the serial data bit clock from an external digital audio source, used to clock in data on DATAAUX. SCLKAUX can be used as the clock reference for the internal PLL. In auxiliary master mode, SCLKAUX is a serial data bit clock output.

AD0/IS0, AD1/IS1 - Input Select Control Pins

In software mode, these pins are part of the chip address.

In hardware mode, IS0 and IS1 select the audio input source from between 4 pairs of signals (AIN1, AIN2 and AIN3) and DATAUX.

H/$\overline{S}$ - Hardware or Software Control

Setting H/$\overline{S}$ high puts the CS4225 into hardware control mode, where many functions are controlled by dedicated pins. When H/$\overline{S}$ is low, many chip functions are controlled via the control port in SPI mode. When H/$\overline{S}$ is open circuit, then software mode $I^2C^®$ protocol is selected for the control port. When floating H/$\overline{S}$, a 100pF capacitor should be connected from the H/$\overline{S}$ pin to ground, to reduce the possibility of external interference influencing the pin.

OVL - Overload Indicator

If either of the 2 16-bit audio ADCs, or the 12-bit ADC, is clipped, then this pin goes high.

Clock and Crystal Pins

XTI, XTO - Crystal connections

Input and output connections for the crystal which may be used to operate the CS4225. Alternatively, a clock may be input into XTI.

CLKOUT - Master Clock Output

CLKOUT allows external circuits to be synchronized to the CS4225. Alternate output frequencies are selectable by the control port or via hardware pins.

Miscellaneous Pins

FILT - PLL Loop Filter Pin

A 0.22 µF capacitor should be connected from FILT to AGND.

PARAMETER DEFINITIONS

Resolution

The number of bits in the input words to the DACs, and in the output words in the ADCs.

Differential Nonlinearity

The worst case deviation from the ideal codewidth; expressed in LSBs.

Total Dynamic Range

The ratio between the DAC full scale output and the noise floor with the DAC muted. Units are in dB.

Total Harmonic Distortion + Noise (THD+N)

THD+N is the ratio of the rms value of the input signal to the rms sum of all other spectral components within the measurement bandwidth (10Hz to 20kHz). THD+N is expressed in dB.

Total Harmonic Distortion (THD)

THD is the ratio of the test signal amplitude to the rms sum of all the in-band harmonics of the test signal.

Instantaneous Dynamic Range

The S/(N+D) with a 1kHz, -60dB input signal, with 60dB added to compensate for the small input signal. Use of a small input signal reduces the harmonic distortion components of the noise to insignificance. Units are in dB.

Interchannel Isolation

The amount of 1kHz signal present on the output of the grounded input channel with 1kHz, 0dB signal present on the other channel. Units are in dB.

Interchannel Gain Mismatch

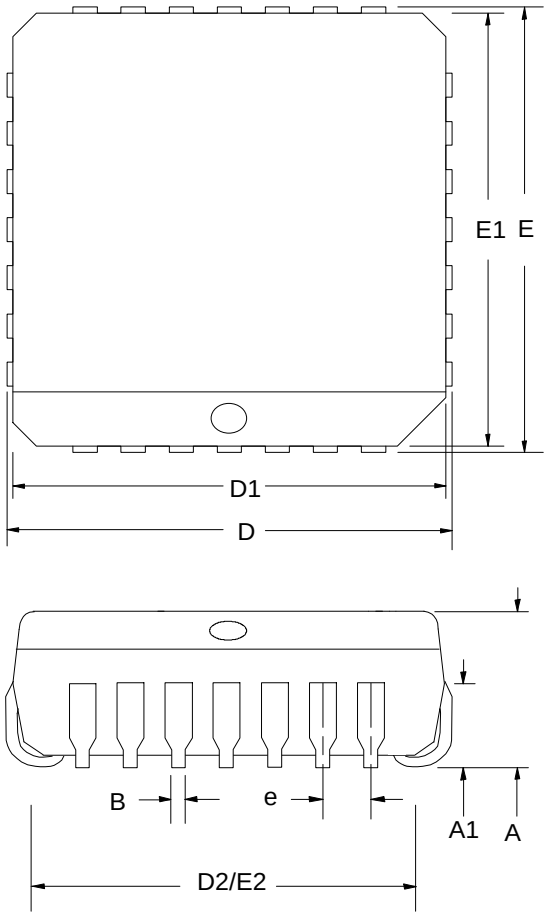
For the ADCs, the difference in input voltage that generates the full scale code for each channel. For the DACs, the difference in output voltages for each channel with a full scale digital input. Units are in dB.

Frequency Response

Worst case variation in output signal level versus frequency over 10Hz to 20kHz. Units in dB.

Offset Error

For the ADCs, the deviation in LSB's of the output from mid-scale with the selected input grounded. For the DAC's, the deviation of the output from zero with mid-scale input code. Units are in volts.



44 pin
PLCC

DIM	NO. OF TERMINALS					
	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	4.20	4.45	4.57	0.165	0.175	0.180
A1	2.29	2.79	3.04	0.090	0.110	0.120
B	0.33	0.41	0.53	0.013	0.016	0.021
D/E	17.40	17.53	17.65	0.685	0.690	0.695
D1/E1	16.51	16.59	16.66	0.650	0.653	0.656
D2/E2	14.99	15.50	16.00	0.590	0.610	0.630
e	1.19	1.27	1.35	0.047	0.050	0.053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