TPA2010D1 2.5-W Mono Filter-Free Class-D Audio Power Amplifier

1 Features

- Maximum Battery Life and Minimum Heat
  - Efficiency with an 8-Ω Speaker:
    - 88% at 400 mW
    - 80% at 100 mW
  - 2.8-mA Quiescent Current
  - 0.5-µA Shutdown Current
- Only Three External Components
  - Optimized PWM Output Stage Eliminates LC Output Filter
  - Internally Generated 250-kHz Switching Frequency Eliminates Capacitor and Resistor
  - Improved PSRR (–75 dB) and Wide Supply Voltage (2.5 V to 5.5 V) Eliminates Need for a Voltage Regulator
  - Fully Differential Design Reduces RF Rectification and Eliminates Bypass Capacitor
  - Improved CMRR Eliminates Two Input Coupling Capacitors
- Die-size ball grid (DSBGA)
  - NanoFree™ Lead-Free (YZF)
  - NanoStar™ SnPb (YEF)

2 Applications

- Wireless or Cellular Handsets and PDAs
- Personal Navigation Devices
- General Portable Audio Devices
- Linear Vibrator Drivers

3 Description

The TPA2010D1 (sometimes referred to as TPA2010) is a 2.5-W high efficiency filter-free class-D audio power amplifier (class-D amp) in a 1,45 mm × 1,45 mm die-size ball grid array (DSBGA) that requires only three external components.

Features like 88% efficiency, –75-dB PSRR, improved RF-rectification immunity, and 8 mm^2 total PCB area make the TPA2010D1 (TPA2010) class-D amp ideal for cellular handsets. A fast start-up time of 1 ms with minimal pop makes the TPA2010D1 (TPA2010) ideal for PDA applications.

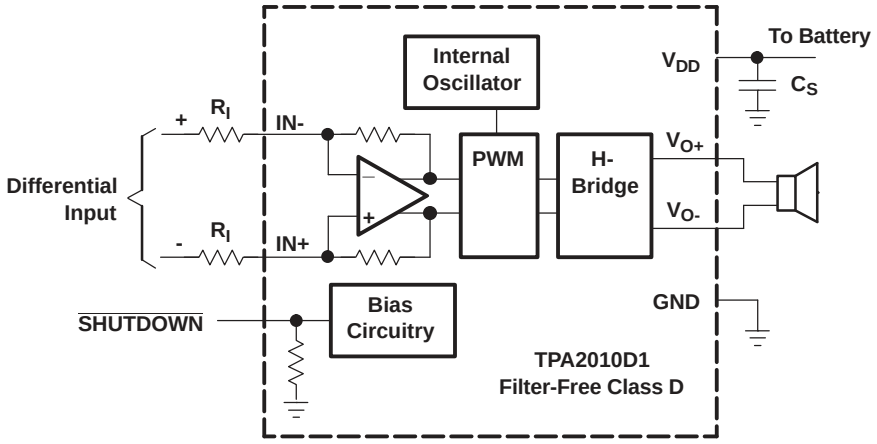
In cellular handsets, the earpiece, speaker phone, and melody ringer can each be driven by the TPA2010D1. The TPA2010D1 allows independent gain while summing signals from separate sources and has a low 36 µV noise floor that is A-weighted.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPA2010D1	DSBGA YEF (9)	1.50 mm × 1.50 mm
	DSBGA YZF (9)	

(1) For all available packages, see the Orderable Addendum at the end of the data sheet.

4 TPA2010D1 With Differential Input For A Wireless Phone



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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

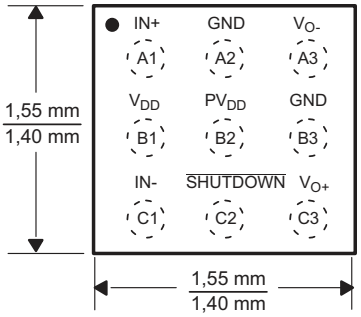
Changes from Revision C (September 2007) to Revision D	Page
• Added *Pin Configuration and Functions* section, *Thermal Information* table, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

6 Device Comparison Table

PART NUMBER	SPEAKER CHANNELS	SPEAKER AMP TYPE	OUTPUT POWER (W)	PSRR (dB)
TPA2010D1	Mono	Class D	2.5	75
TPA2005D1	Mono	Class D	1.4	75
TPA2011D1	Mono	Class D	3.2	86

7 Pin Configuration and Functions

YZF and YEF Package
9-Pin DSBGA
Top View



Note: Pin A1 is marked with a “0” for Pb-free (YZF) and a “1” for SnPb (YEF).

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
A1	IN+	I	Positive differential input
A2	GND	I	High-current ground
A3	VO-	O	Negative BTL output
B1	V_{DD}	I	Power supply
B2	PV_{DD}	I	Power supply
B3	GND	I	High-current ground
C1	IN-	I	Negative differential input
C2	SHUTDOWN	I	Shutdown terminal (active low logic)
C3	VO+	O	Positive BTL output

8 Specifications

8.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{DD}	Supply voltage	In active mode	–0.3	6	V
		In $\overline{\text{SHUTDOWN}}$ mode			
V_I	Input voltage		–0.3	7	V
	Continuous total power dissipation		–0.3	V_{DD} + 0.3	V
T_A	Operating free-air temperature		See *Dissipation Ratings*		°C
T_J	Operating junction temperature		–40	85	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	YZF		260	°C
		YEF		235	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

8.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		2.5		5.5	V
V_{IH}	High-level input voltage	$\overline{\text{SHUTDOWN}}$	1.3		V_{DD}	V
V_{IL}	Low-level input voltage	$\overline{\text{SHUTDOWN}}$	0		0.35	V
R_I	Input resistor	Gain ≤ 20 V/V (26 dB)	15			kΩ
V_{IC}	Common mode input voltage range	V_{DD} = 2.5 V, 5.5 V, CMRR ≤ –49 dB	0.5		V_{DD} – 0.8	V
T_A	Operating free-air temperature		–40		85	°C

8.4 Thermal Information

THERMAL METRIC(1)		TPA2010D1 YZF (DSBGA) 9 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	100.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	24.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	24.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

8.5 Electrical Characteristics

T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{OS}\|$	Output offset voltage (measured differentially)	V_I = 0 V, A_V = 2 V/V, V_{DD} = 2.5 V to 5.5 V		1	25	mV
PSRR	Power supply rejection ratio	V_{DD} = 2.5 V to 5.5 V		–75	–55	dB
CMRR	Common mode rejection ratio	V_{DD} = 2.5 V to 5.5 V, V_{IC} = V_{DD} / 2 to 0.5 V, V_{IC} = V_{DD} / 2 to V_{DD} – 0.8 V		–68	–49	dB
$\|I_{IH}\|$	High-level input current	V_{DD} = 5.5 V, V_I = 5.8 V			100	µA
$\|I_{IL}\|$	Low-level input current	V_{DD} = 5.5 V, V_I = –0.3 V			5	µA
$I_{(Q)}$	Quiescent current	V_{DD} = 5.5 V, no load		3.4	4.9	mA
		V_{DD} = 3.6 V, no load		2.8		
		V_{DD} = 2.5 V, no load		2.2	3.2	
$I_{(SD)}$	Shutdown current	$V_{(\overline{SHUTDOWN})}$ = 0.35 V, V_{DD} = 2.5 V to 5.5 V		0.5	2	µA
$r_{DS(on)}$	Static drain-source on-state resistance	V_{DD} = 2.5 V		700		mΩ
		V_{DD} = 3.6 V		500		
		V_{DD} = 5.5 V		400		
	Output impedance in $\overline{SHUTDOWN}$	$V_{(\overline{SHUTDOWN})}$ = 0.35 V		>1		kΩ
$f_{(sw)}$	Switching frequency	V_{DD} = 2.5 V to 5.5 V	200	250	300	kHz
	Gain	V_{DD} = 2.5 V to 5.5 V	$\frac{285\ k\Omega}{R_I}$	$\frac{300\ k\Omega}{R_I}$	$\frac{315\ k\Omega}{R_I}$	$\frac{V}{V}$
	Resistance from shutdown to GND			300		kΩ

8.6 Operating Characteristics

T_A = 25°C, Gain = 2 V/V, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power	THD + N = 10%, f = 1 kHz, R_L = 4 Ω	V_{DD} = 5 V		2.5		W
			V_{DD} = 3.6 V		1.3		
			V_{DD} = 2.5 V		0.52		
		THD + N = 1%, f = 1 kHz, R_L = 4 Ω	V_{DD} = 5 V		2.08		W
			V_{DD} = 3.6 V		1.06		
			V_{DD} = 2.5 V		0.42		
		THD + N = 10%, f = 1 kHz, R_L = 8 Ω	V_{DD} = 5 V		1.45		W
			V_{DD} = 3.6 V		0.73		
			V_{DD} = 2.5 V		0.33		
		THD + N = 1%, f = 1 kHz, R_L = 8 Ω	V_{DD} = 5 V		1.19		W
			V_{DD} = 3.6 V		0.59		
			V_{DD} = 2.5 V		0.26		
THD+N	Total harmonic distortion plus noise	V_{DD} = 5 V, P_O = 1 W, R_L = 8 Ω, f = 1 kHz			0.18%		
		V_{DD} = 3.6 V, P_O = 0.5 W, R_L = 8 Ω, f = 1 kHz			0.19%		
		V_{DD} = 2.5 V, P_O = 200 mW, R_L = 8 Ω, f = 1 kHz			0.20%		
k_{SVR}	Supply ripple rejection ratio	V_{DD} = 3.6 V, Inputs ac-grounded with C_i = 2 µF	f = 217 Hz, $V_{(RIPPLE)}$ = 200 mV_{pp}		–67		dB
SNR	Signal-to-noise ratio	V_{DD} = 5 V, P_O = 1 W, R_L = 8 Ω			97		dB
V_n	Output voltage noise	V_{DD} = 3.6 V, f = 20 Hz to 20 kHz, Inputs ac-grounded with C_i = 2 µF	No weighting		48		μV_{RMS}
			A weighting		36		
CMRR	Common mode rejection ratio	V_{DD} = 3.6 V, V_{IC} = 1 V_{pp}	f = 217 Hz		–63		dB
Z_I	Input impedance			142	150	158	kΩ
	Start-up time from shutdown	V_{DD} = 3.6 V			1		ms

8.7 Dissipation Ratings

PACKAGE	DERATING FACTOR(1)	$T_A \le 25°C$ POWER RATING	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
YZF	7.8 mW/°C	780 mW	429 mW	312 mW

(1) Derating factor measure with High K board.

8.8 Typical Characteristics

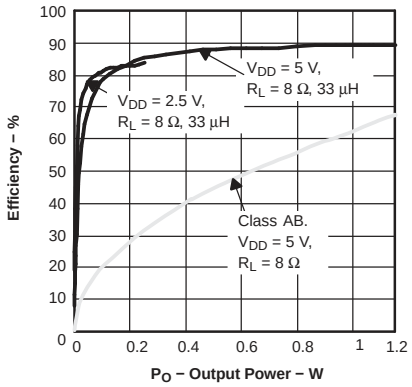


Figure 1. Efficiency versus Output Power

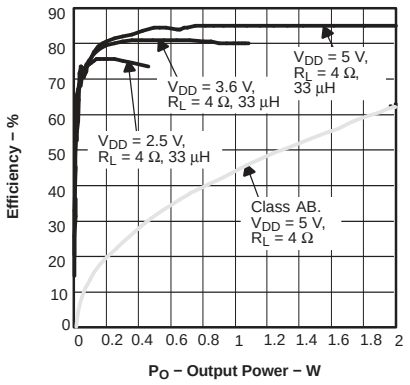


Figure 2. Efficiency versus Output Power

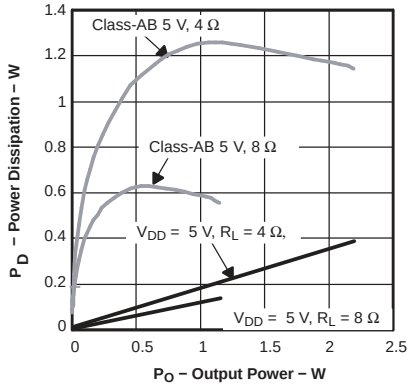


Figure 3. Power Dissipation versus Output Power

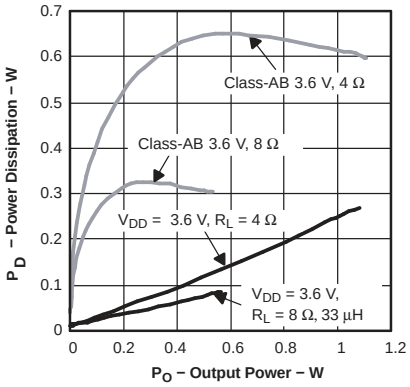


Figure 4. Power Dissipation versus Output Power

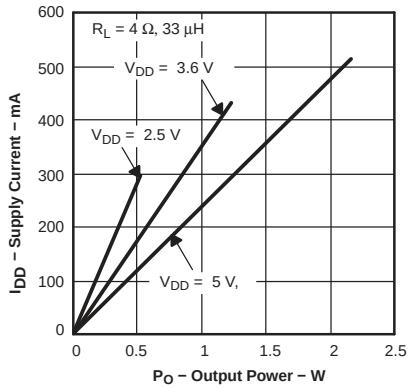


Figure 5. Supply Current versus Output Power

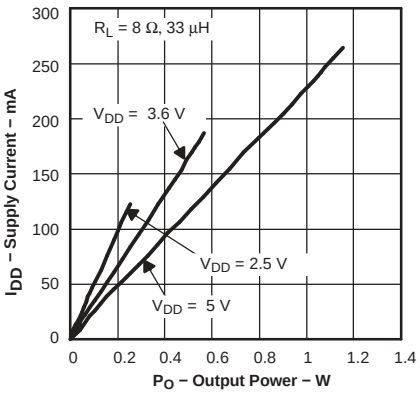


Figure 6. Supply Current versus Output Power

Typical Characteristics (continued)

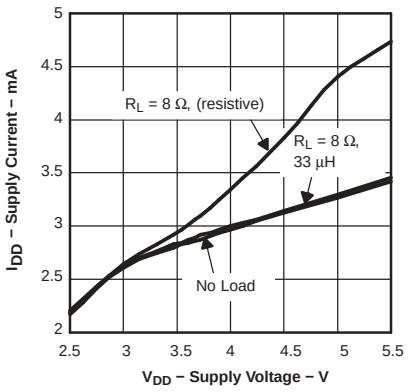


Figure 7. Supply Current versus Supply Voltage

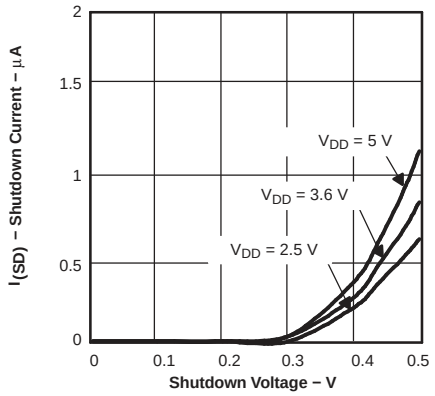


Figure 8. Supply Current versus Shutdown Voltage

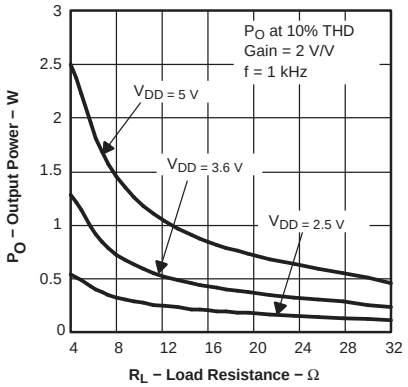


Figure 9. Output Power versus Load Resistance

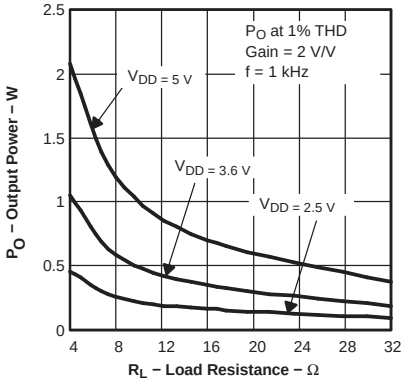


Figure 10. Output Power versus Load Resistance

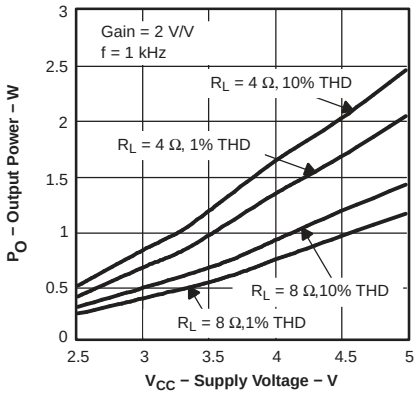


Figure 11. Output Power versus Supply Voltage

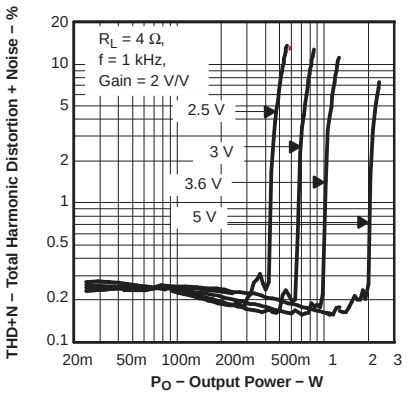


Figure 12. Total Harmonic Distortion + Noise versus Output Power

Typical Characteristics (continued)

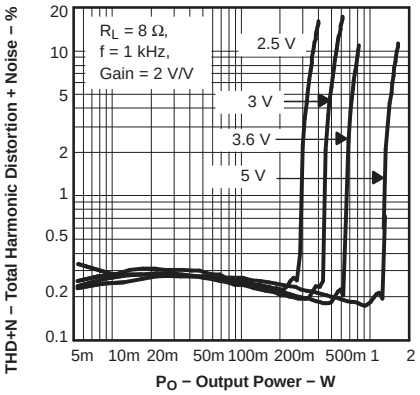


Figure 13. Total Harmonic Distortion + Noise versus Output Power

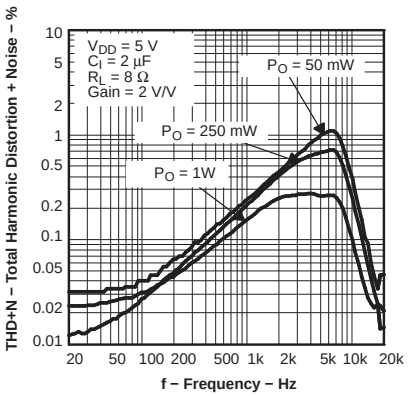


Figure 14. Total Harmonic Distortion + Noise versus Frequency

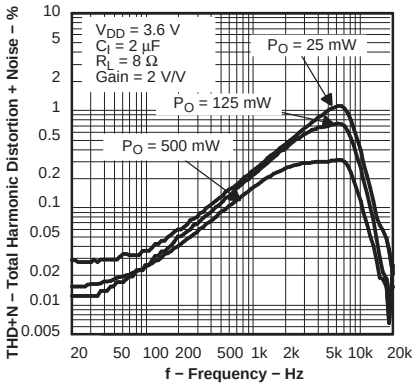


Figure 15. Total Harmonic Distortion + Noise versus Frequency

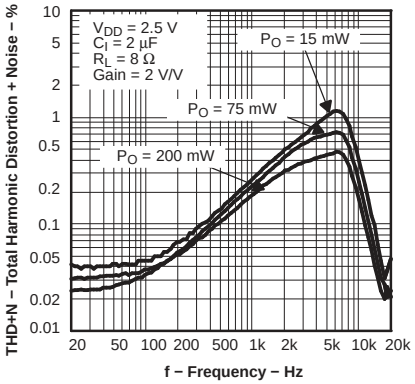


Figure 16. Total Harmonic Distortion + Noise versus Frequency

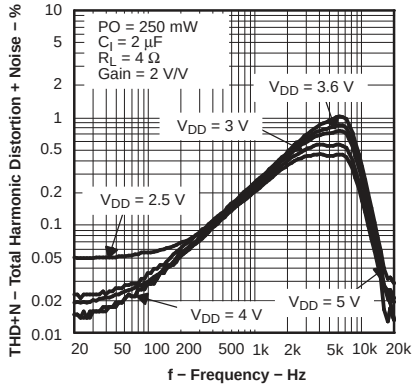


Figure 17. Total Harmonic Distortion + Noise versus frequency

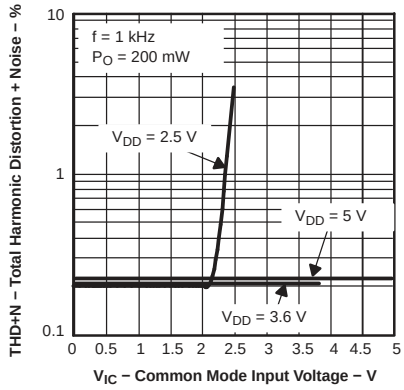


Figure 18. Total Harmonic Distortion + Noise versus Common Mode Input Voltage

Typical Characteristics (continued)

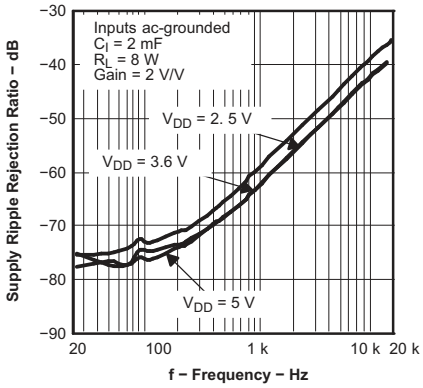


Figure 19. Supply Ripple Rejection Ratio versus Frequency

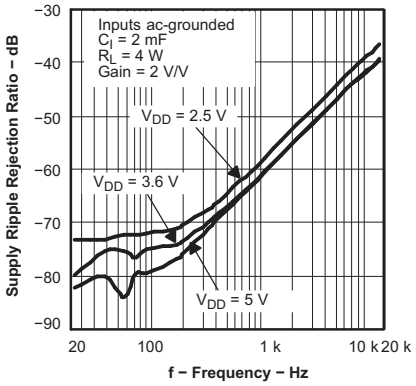


Figure 20. Supply Ripple Rejection Ratio versus Frequency

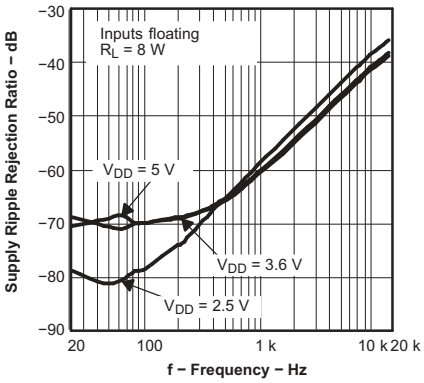


Figure 21. Supply Ripple Rejection Ratio versus Frequency

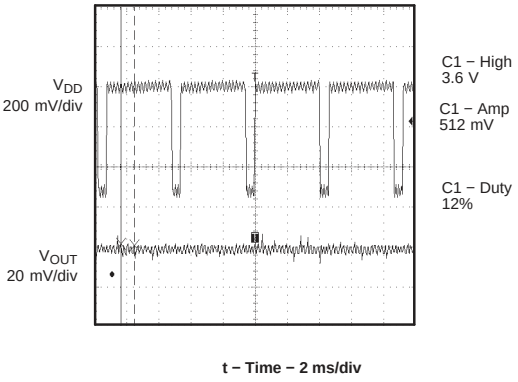


Figure 22. GSM Power Supply Rejection versus Time

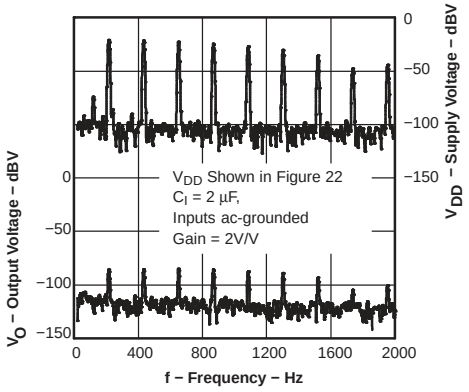


Figure 23. GSM Power Supply Rejection versus Frequency

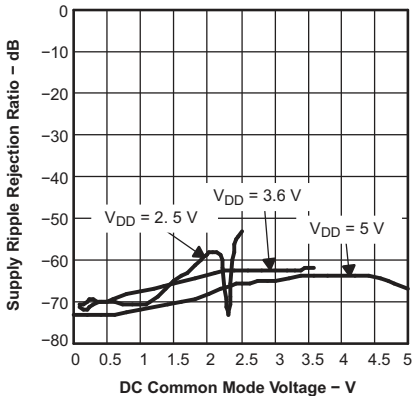


Figure 24. Supply Ripple Rejection Ratio versus DC Common Mode Voltage

Typical Characteristics (continued)

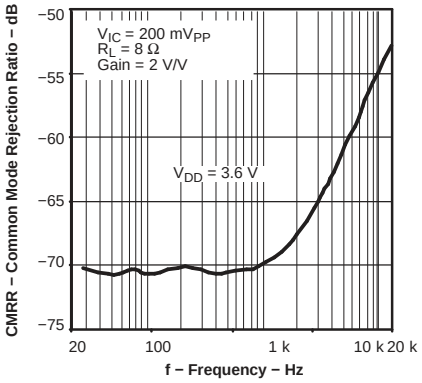


Figure 25. Common-Mode Rejection Ratio versus Frequency

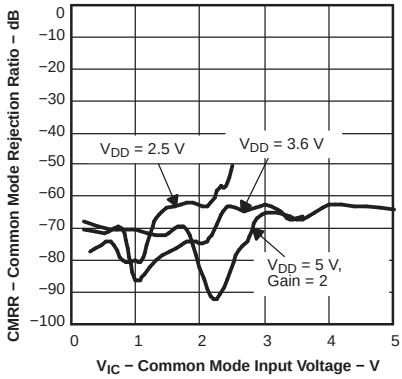


Figure 26. Common-Mode Rejection Ratio versus Common-Mode Input Voltage

9 Parameter Measurement Information

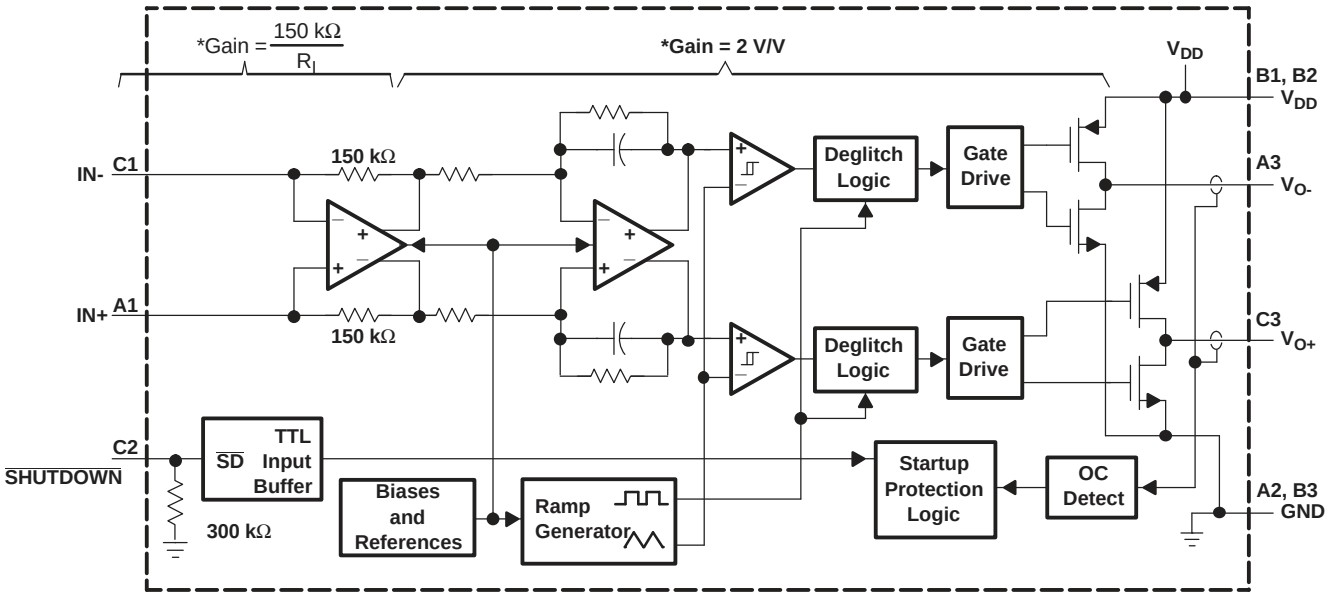
All parameters are measured according to the conditions described in the *Specifications* section.

10 Detailed Description

10.1 Overview

The TPA2010D1 is a high-efficiency filter-free Class-D audio amplifier capable of delivering up to 2.5 W into 4-Ω loads with 5-V power supply. The fully-differential design of this amplifier avoids the usage of bypass capacitors and the improved CMRR eliminates the usage of input-coupling capacitors. This makes the device size a perfect choice for small, portable applications because only three external components are required. The advanced modulation used in the TPA2010D1 PWM output stage eliminates the need for an output filter.

10.2 Functional Block Diagram



Notes:
* Total gain = $2 \times \frac{150\ k\Omega}{R_I}$

10.3 Feature Description

10.3.1 Fully Differential Amplifier

The TPA2010D1 is a fully differential amplifier with differential inputs and outputs. The fully differential amplifier consists of a differential amplifier and a common-mode amplifier. The differential amplifier ensures that the amplifier outputs a differential voltage on the output that is equal to the differential input times the gain. The common-mode feedback ensures that the common-mode voltage at the output is biased around $V_{DD}/2$ regardless of the common-mode voltage at the input. The fully differential TPA2010D1 can still be used with a single-ended input; however, TI recommends using the TPA2010D1 with differential inputs when in a noisy environment, like a wireless handset, to ensure maximum noise rejection.

Feature Description (continued)

10.3.2 Advantages of Fully Differential Amplifiers

- Input-coupling capacitors not required:
  - The fully differential amplifier allows for input bias at voltage other than mid-supply. For example, if a codec has a midsupply lower than the midsupply of the TPA2010D1, the common-mode feedback circuit adjusts, and the TPA2010D1 outputs remain biased at midsupply of the TPA2010D1. The inputs of the TPA2010D1 can be biased from 0.5 V to V_{DD} –0.8 V. If the inputs are biased outside of that range, input-coupling capacitors are required.
- Midsupply bypass capacitor, $C_{(BYPASS)}$, not required:
  - The fully differential amplifier does not require a bypass capacitor because any shift in the midsupply affects both positive and negative channels equally and cancels at the differential output.
- Better RF-immunity:
  - GSM handsets save power by turning on and shutting off the RF transmitter at a rate of 217 Hz. The transmitted signal is picked up on input and output traces. The fully differential amplifier cancels the signal better than the typical audio amplifier.

10.3.3 Efficiency and Thermal Information

The maximum ambient temperature depends on the PCB system heatsinking ability. The derating factor for the YEF and YEZ packages appear in the dissipation rating table. Converting this to θ_{JA}:

$$\theta_{JA} = \frac{1}{\text{Derating Factor}} = \frac{1}{0.0078} = 128.2°C/W \quad (1)$$

Given θ_{JA} of 128.2°C/W, the maximum allowable junction temperature of 150°C, and the maximum internal dissipation of 0.4 W (2.25 W, 4-Ω load, 5-V supply, from Figure 3), the maximum ambient temperature can be calculated with the following equation.

$$T_{A(max)} = T_{J(max)} - \theta_{JA} \times P_{D(max)} = 150 - 128 \times (0.4) = 98.72°C \quad (2)$$

Equation 2 shows that the calculated maximum ambient temperature is 98.72°C at maximum power dissipation with a 5-V supply and 4-Ω a load. See Figure 3. The TPA2010D1 is designed with thermal protection that turns the device off when the junction temperature surpasses 165°C ~ 190°C to prevent damage to the IC. Using speakers more resistive than 4-Ω dramatically increases the thermal performance by reducing the output current and increasing the efficiency of the amplifier.

10.3.4 Eliminating the Output Filter With the TPA2010D1

This section describes why the user can eliminate the output filter with the TPA2010D1.

10.3.4.1 Effect on Audio

The class-D amplifier outputs a pulse-width modulated (PWM) square wave, which is the sum of the switching waveform and the amplified input audio signal. The human ear acts as a band-pass filter such that only the frequencies between approximately 20 Hz and 20 kHz are passed. The switching frequency components are much greater than 20 kHz, so the only signal heard is the amplified input audio signal.

10.3.4.2 Traditional Class-D Modulation Scheme

The traditional class-D modulation scheme, which is used in the TPA005Dxx family, has a differential output where each output is 180 degrees out of phase and changes from ground to the supply voltage, V_{DD}. Therefore, the differential pre-filtered output varies between positive and negative V_{DD}, where filtered 50% duty cycle yields 0 volts across the load. The traditional class-D modulation scheme with voltage and current waveforms is shown in Figure 27.

NOTE

Even at an average of 0 volts across the load (50% duty cycle), the current to the load is high causing a high loss and thus causing a high supply current.

Feature Description (continued)

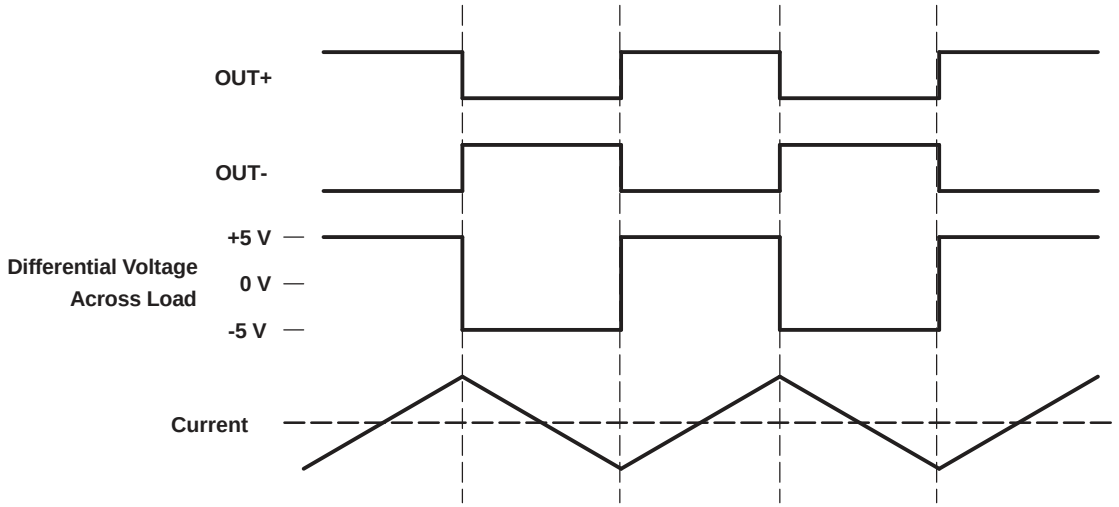


Figure 27. Traditional Class-D Modulation Scheme's Output Voltage and Current Waveforms into an Inductive Load with No Input

10.3.4.3 TPA2010D1 Modulation Scheme

The TPA2010D1 uses a modulation scheme that still has each output switching from 0 to the supply voltage. However, OUT+ and OUT– are now in phase with each other with no input. The duty cycle of OUT+ is greater than 50% and OUT– is less than 50% for positive voltages. The duty cycle of OUT+ is less than 50% and OUT– is greater than 50% for negative voltages. The voltage across the load sits at 0 volts throughout most of the switching period greatly reducing the switching current, which reduces any I^2R losses in the load.

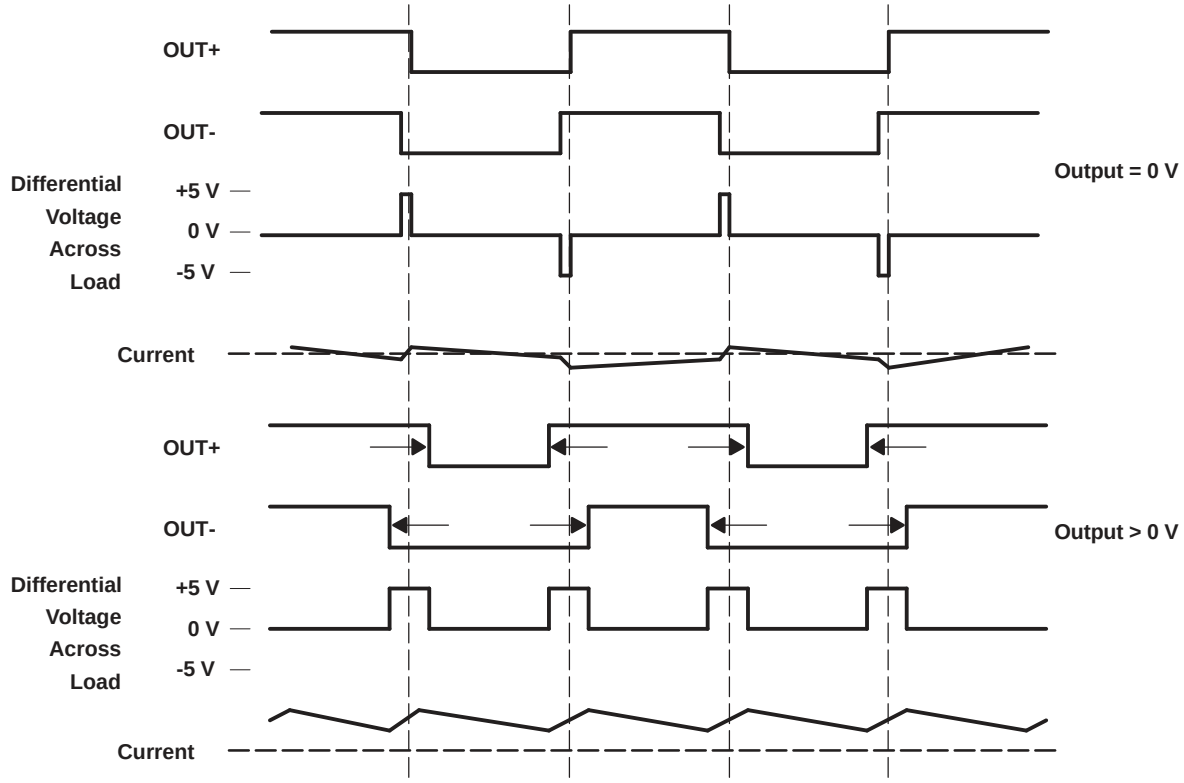


Figure 28. The TPA2010D1 Output Voltage and Current Waveforms into an Inductive Load

Feature Description (continued)

10.3.4.4 Efficiency: Use a Filter With the Traditional Class-D Modulation Scheme

The main reason that the traditional class-D amplifier needs an output filter is that the switching waveform results in maximum current flow. This causes more loss in the load, causing lower efficiency. The ripple current is large for the traditional modulation scheme because the ripple current is proportional to voltage multiplied by the time at that voltage. The differential voltage swing is $2 \times V_{DD}$ and the time at each voltage is half the period for the traditional modulation scheme. An ideal LC filter is needed to store the ripple current from each half cycle for the next half cycle, while any resistance causes power dissipation. The speaker is both resistive and reactive, whereas an LC filter is almost purely reactive.

The TPA2010D1 modulation scheme has very little loss in the load without a filter because the pulses are very short and the change in voltage is V_{DD} instead of $2 \times V_{DD}$. As the output power increases, the pulses widen making the ripple current larger. Ripple current can be filtered with an LC filter for increased efficiency, but for most applications the filter is not needed.

An LC filter with a cutoff frequency less than the class-D switching frequency allows the switching current to flow through the filter instead of the load. The filter has less resistance than the speaker that results in less power dissipated, which increases efficiency.

10.3.4.5 Effects of Applying a Square Wave into a Speaker

If the amplitude of a square wave is high enough and the frequency of the square wave is within the bandwidth of the speaker, a square wave causes the voice coil to jump out of the air gap and/or scar the voice coil. However, a 250-kHz switching frequency is not significant because the speaker cone movement is proportional to $1/f^2$ for frequencies beyond the audio band. Therefore, the amount of cone movement at the switching frequency is very small. However, damage could occur to the speaker if the voice coil is not designed to handle the additional power. To size the speaker for added power, the ripple current dissipated in the load needs to be calculated by subtracting the theoretical supplied power, $P_{SUP\ THEORETICAL}$, from the actual supply power, P_{SUP}, at maximum output power, P_{OUT}. The switching power dissipated in the speaker is the inverse of the measured efficiency, $\eta_{MEASURED}$, minus the theoretical efficiency, $\eta_{THEORETICAL}$.

$$P_{SPKR} = P_{SUP} - P_{SUP\ THEORETICAL}$$

where

- the speaker is operating at maximum power (3)

$$P_{SPKR} = \frac{P_{SUP}}{P_{OUT}} - \frac{P_{SUP\ THEORETICAL}}{P_{OUT}} \quad (4)$$

$$P_{SPKR} = P_{OUT} \times \left(\frac{1}{\eta_{MEASURED}} - \frac{1}{\eta_{THEORETICAL}} \right) \quad (5)$$

$$\eta_{THEORETICAL} = \frac{R_L}{R_L + 2 \times r_{DS(on)}} \quad (6)$$

The maximum efficiency of the TPA2010D1 with a 3.6 V supply and an 8-Ω load is 86% from Equation 6. Using equation Equation 5 with the efficiency at maximum power (84%), we see that there is an additional 17 mW dissipated in the speaker. The added power dissipated in the speaker is not an issue as long as it is taken into account when choosing the speaker.

10.3.4.6 When to Use an Output Filter

Design the TPA2010D1 without an output filter if the traces from amplifier to speaker are short. The TPA2010D1 passed FCC and CE radiated emissions with no shielding with speaker trace wires 100 mm long or less. Wireless handsets and PDAs are great applications for class-D without a filter.

A ferrite bead filter can often be used if the design is failing radiated emissions without an LC filter, and the frequency sensitive circuit is greater than 1 MHz. This is good for circuits that just have to pass FCC and CE because FCC and CE only test radiated emissions greater than 30 MHz. If choosing a ferrite bead, choose one with high impedance at high frequencies, but very low impedance at low frequencies.

Use an LC output filter if there are low frequency (< 1 MHz) EMI sensitive circuits and/or there are long leads from amplifier to speaker.

Feature Description (continued)

Figure 29 and Figure 30 show typical ferrite bead and LC output filters.

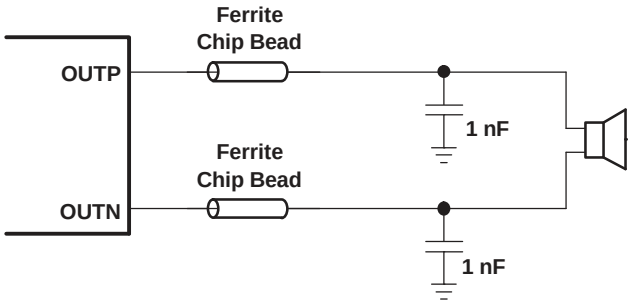


Figure 29. Typical Ferrite Chip Bead Filter (Chip Bead Example: NEC/Tokin: N2012zps121)

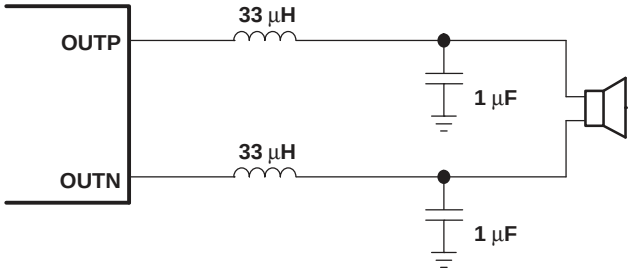


Figure 30. Typical LC Output Filter, Cutoff Frequency Of 27 kHz

10.4 Device Functional Modes

10.4.1 Summing Input Signals with the TPA2010D1

Most wireless phones or PDAs must sum signals at the audio power amplifier or have two signals sources that need separate gain. The TPA2010D1 makes it easy to sum signals or use separate signal sources with different gains. Many phones now use the same speaker for the ear-piece and ringer, where the wireless phone would require a much lower gain for the phone ear-piece than for the ringer. PDAs and phones that have stereo headphones require summing of the right and left channels to output the stereo signal to the mono speaker.

10.4.1.1 Summing Two Differential Inputs

Two extra resistors are needed for summing differential signals (a total of 5 components). The gain for each input source can be set independently (see Equation 7 and Equation 8, and Figure 31).

$$\text{Gain } 1 = \frac{V_O}{V_{I1}} = \frac{2 \times 150\ \text{k}\Omega}{R_{I1}} \left(\frac{V}{V}\right) \tag{7}$$

$$\text{Gain } 2 = \frac{V_O}{V_{I2}} = \frac{2 \times 150\ \text{k}\Omega}{R_{I2}} \left(\frac{V}{V}\right) \tag{8}$$

If summing left and right inputs with a gain of 1 V/V, use $R_{I1} = R_{I2} = 300\ \text{k}\Omega$.

If summing a ring tone and a phone signal, set the ring-tone gain to Gain 2 = 2 V/V, and the phone gain to gain 1 = 0.1 V/V. The resistor values would be: $R_{I1} = 3\ \text{M}\Omega$, and = $R_{I2} = 150\ \text{k}\Omega$.

Device Functional Modes (continued)

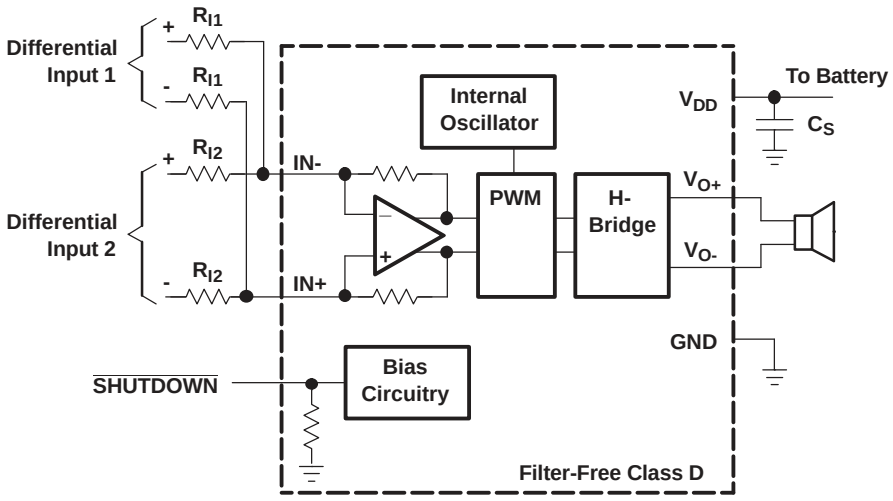


Figure 31. TPA2010D1 Summing Two Differential Inputs

10.4.1.2 Summing a Differential Input Signal and a Single-Ended Input Signal

Figure 32 shows how to sum a differential input signal and a single-ended input signal. Ground noise can couple in through IN+ with this method. It is better to use differential inputs. The corner frequency of the single-ended input is set by C_{I2}, shown in Equation 11. To assure that each input is balanced, the single-ended input must be driven by a low-impedance source even if the input is not in use.

$$\text{Gain } 1 = \frac{V_O}{V_{I1}} = 2 \times \frac{150\ \text{k}\Omega}{R_{I1}} \left(\frac{V}{V}\right) \tag{9}$$

$$\text{Gain } 2 = \frac{V_O}{V_{I2}} = 2 \times \frac{150\ \text{k}\Omega}{R_{I2}} \left(\frac{V}{V}\right) \tag{10}$$

$$C_{I2} = \frac{1}{2\pi \times R_{I2} \times f_{C2}} \tag{11}$$

If summing a ring tone and a phone signal, the phone signal should use a differential input signal while the ring tone might be limited to a single-ended signal. Phone gain is set at Gain 1 = 0.1 V/V, and the ring-tone gain is set to Gain 2 = 2 V/V, the resistor values would be: R_{I1} = MΩ, and R_{I2} = 150 kΩ.

The high pass corner frequency of the single-ended input is set by capacitor C_{I2}. If the desired corner frequency is less than 20 Hz.

$$C_{I2} > \frac{1}{2\pi \times 150\ \text{k}\Omega \times 20\ \text{Hz}} > 53\ \text{pF} \tag{12}$$

Device Functional Modes (continued)

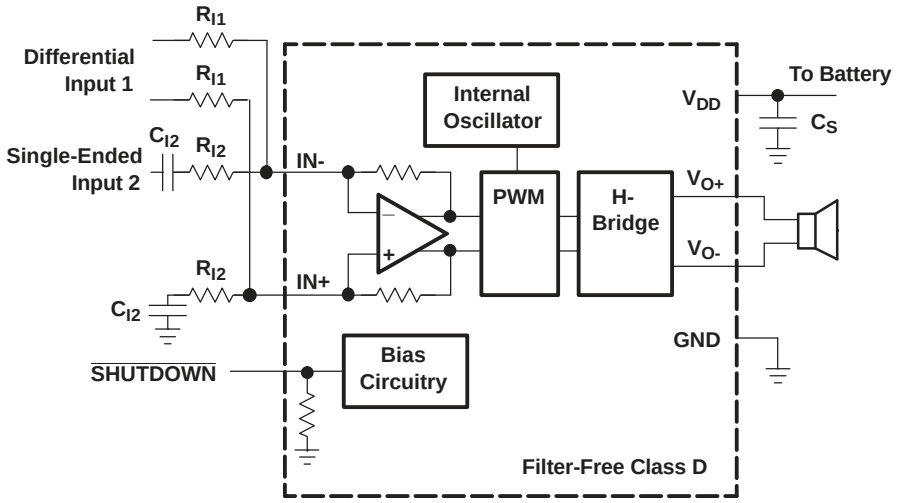


Figure 32. TPA2010D1 Summing Differential Input and Single-Ended Input Signals

10.4.1.3 TPA2010D1 Summing Two Single-Ended Inputs

Four resistors and three capacitors are needed for summing single-ended input signals. The gain and corner frequencies (f_{c1} and f_{c2}) for each input source can be set independently (see Equation 13 through Equation 16, and Figure 33). Resistor, R_P, and capacitor, C_P, are needed on the IN+ terminal to match the impedance on the IN– terminal. The single-ended inputs must be driven by low impedance sources even if one of the inputs is not outputting an AC signal.

$$\text{Gain } 1 = \frac{V_O}{V_{I1}} = 2 \times \frac{150\ \text{k}\Omega}{R_{I1}} \left(\frac{V}{V}\right) \tag{13}$$

$$\text{Gain } 2 = \frac{V_O}{V_{I2}} = 2 \times \frac{150\ \text{k}\Omega}{R_{I2}} \left(\frac{V}{V}\right) \tag{14}$$

$$C_{I1} = \frac{1}{(2\pi \times R_{I1} \times f_{C1})} \tag{15}$$

$$C_{I2} = \frac{1}{(2\pi \times R_{I2} \times f_{C2})} \tag{16}$$

$$C_P = C_{I1} + C_{I2} \tag{17}$$

$$R_P = \frac{R_{I1} \times R_{I2}}{(R_{I1} + R_{I2})} \tag{18}$$

Device Functional Modes (continued)

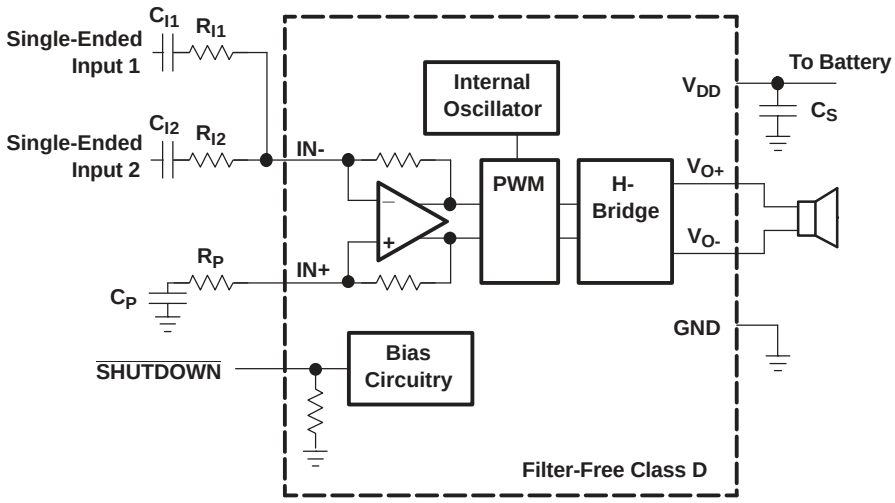


Figure 33. TPA2010D1 Summing Two Single-Ended Inputs

10.4.2 Shutdown Mode

The TPA2010D1 can be put in shutdown mode when asserting SHUTDOWN pin to a logic LOW. While in shutdown mode, the device output stage is turned off and set into high impedance, making the current consumption very low. The device exits shutdown mode when a HIGH logic level is applied to the SHUTDOWN pin.

11 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1 Application Information

These typical connection diagrams highlight the required external components and system level connections for proper operation of the device in several popular use cases. Each of these configurations can be created using the Evaluation Modules (EVMs) for the device. These flexible modules allow full evaluation of the device in the most common modes of operation. Any design variation can be supported by TI through schematic and layout reviews. Visit TI.com for design assistance and join the audio amplifier discussion forum for additional information.

11.2 Typical Applications

Figure 34 shows the TPA2010D1 typical schematic with differential inputs and Figure 38 shows the TPA2010D1 with differential inputs and input capacitors, and Figure 39 shows the TPA2010D1 with single-ended inputs. Differential inputs should be used whenever possible because the single-ended inputs are more susceptible to noise.

11.2.1 TPA200110D1 With Differential Input

Use the values listed in Table 1 as the design requirements. The TPA2010D1 can be used with differential input without input capacitors. This section describes the design considerations for this application.

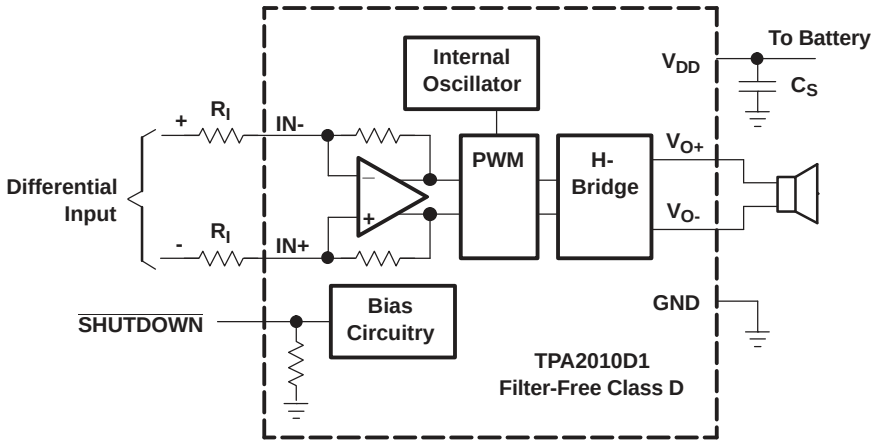


Figure 34. TPA2010D1 with Differential Input

11.2.1.1 Design Requirements

Use the values listed in Table 1 as the design requirements.

Table 1. Design Requirements

PARAMETER	EXAMPLE VALUE
Power supply	5 V
Shutdown input	High > 2 V
	Low < 0.8 V
Speaker	8 Ω

11.2.1.2 Detailed Design Procedure

Table 2 lists the typical components values.

Table 2. Typical Component Values

REF DES	VALUE	EIA SIZE	MANUFACTURER	PART NUMBER
R_I	150 kΩ (±0.5%)	0402	Panasonic	ERJ2RHD154V
C_S	1 µF (+22%, –80%)	0402	Murata	GRP155F50J105Z
C_I (1)	3.3 nF (±10%)	0201	Murata	GRP033B10J332K

(1) C_I is only needed for single-ended input or if V_{ICM} is not between 0.5 V and V_{DD} – 0.8 V. C_I = 3.3 nF (with R_I = 150 kΩ) gives a high-pass corner frequency of 321 Hz.

11.2.1.2.1 Input Resistors (R_I)

The input resistors (R_I) set the gain of the amplifier according to Equation 19.

$$\text{Gain} = \frac{2 \times 150\ \text{k}\Omega}{R_I}\left(\frac{V}{V}\right) \tag{19}$$

Resistor matching is very important in fully differential amplifiers. The balance of the output on the reference voltage depends on matched ratios of the resistors. CMRR, PSRR, and cancellation of the second harmonic distortion diminish if resistor mismatch occurs. Therefore, TI recommends to use 1% tolerance resistors or better to keep the performance optimized. Matching is more important than overall tolerance. Resistor arrays with 1% matching can be used with a tolerance greater than 1%.

Place the input resistors very close to the TPA2010D1 to limit noise injection on the high-impedance nodes.

For optimal performance, set the gain to 2 V/V or lower. Lower gain allows the TPA2010D1 to operate at its best, and keeps a high voltage at the input making the inputs less susceptible to noise.

11.2.1.2.2 Decoupling Capacitor (C_S)

The TPA2010D1 is a high-performance class-D audio amplifier that requires adequate power supply decoupling to ensure the efficiency is high and total harmonic distortion (THD) is low. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1 µF, placed as close as possible to the device V_{DD} lead works best. Placing this decoupling capacitor close to the TPA2010D1 is very important for the efficiency of the class-D amplifier, because any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency. For filtering lower-frequency noise signals, a 10 µF or greater capacitor placed near the audio power amplifier would also help, but it is not required in most applications because of the high PSRR of this device.

11.2.1.3 Application Curves

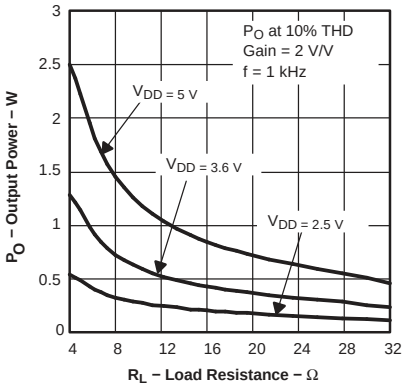


Figure 35. Output Power versus Load Resistance

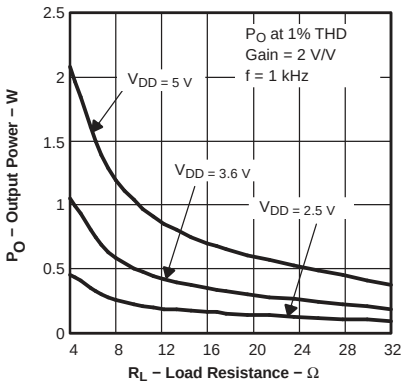


Figure 36. Output Power versus Load Resistance

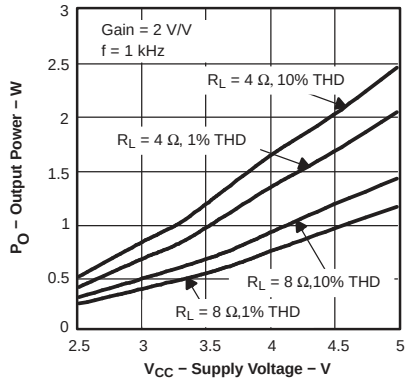


Figure 37. Output Power versus Load Resistance

11.2.2 TPA20010D1 With Differential Input and Input Capacitors

The TPA20010D1 supports differential input operation with input capacitors. This section describes the design considerations for this application.

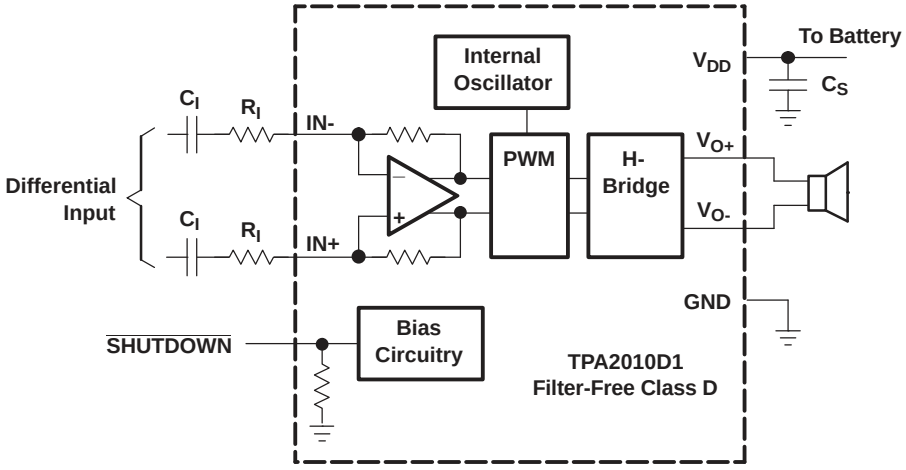


Figure 38. TPA2010D1 With Differential Input and Input Capacitors

11.2.2.1 Design Requirements

Refer to the *Design Requirements* section.

11.2.2.2 Detailed Design Procedure

Refer to the *Detailed Design Procedure* section.

11.2.2.2.1 Input Capacitors (C_I)

The TPA2010D1 does not require input coupling capacitors if the design uses a differential source that is biased from 0.5 V to V_{DD} –0.8 V (shown in Figure 34). If the input signal is not biased within the recommended common-mode input range, if needing to use the input as a high pass filter (shown in Figure 38), or if using a single-ended source (shown in Figure 39), input coupling capacitors are required.

The input capacitors and input resistors form a high-pass filter with the corner frequency, f_c, determined in Equation 20.

$$f_C = \frac{1}{(2\pi \times R_I \times C_I)} \tag{20}$$

The value of the input capacitor is important to consider as it directly affects the bass (low frequency) performance of the circuit. Speakers in wireless phones cannot usually respond well to low frequencies, so the corner frequency can be set to block low frequencies in this application.

Equation 21 is reconfigured to solve for the input coupling capacitance.

$$C_I = \frac{1}{(2\pi \times R_I \times f_C)} \quad (21)$$

If the corner frequency is within the audio band, the capacitors should have a tolerance of ±10% or better, because any mismatch in capacitance causes an impedance mismatch at the corner frequency and below.

For a flat low-frequency response, use large input coupling capacitors (1 µF). However, in a GSM phone the ground signal is fluctuating at 217 Hz, but the signal from the codec does not have the same 217 Hz fluctuation. The difference between the two signals is amplified, sent to the speaker, and heard as a 217 Hz hum.

11.2.2.3 Application Curves

Refer to the *Application Curves* section.

11.2.3 TPA20010D1 with Single-Ended Input

The TPA20010D1 can be used with Single-Ended inputs, using Input capacitors. This section describes the design considerations for this application.

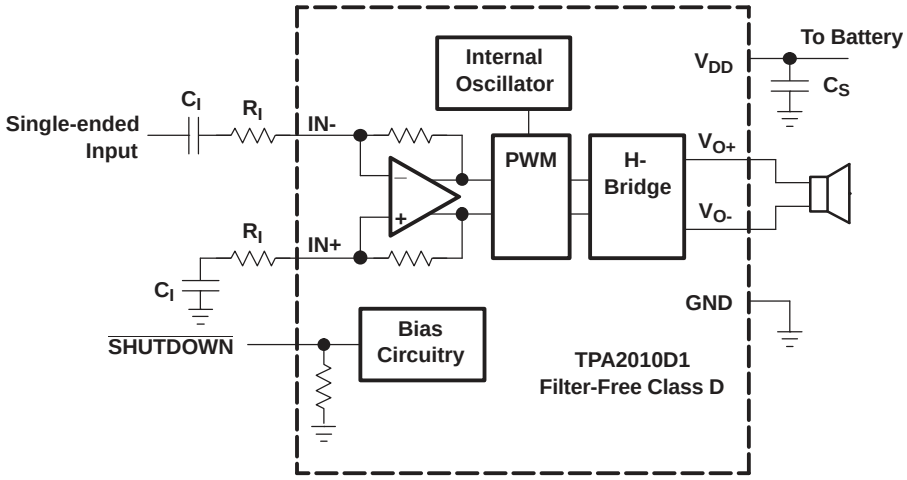


Figure 39. TPA2010D1 with Single-Ended Input

11.2.3.1 Design Requirements

Refer to the *Design Requirements* section.

11.2.3.2 Detailed Design Procedure

Refer to the *Detailed Design Procedure* section.

11.2.3.3 Application Curves

Refer to the *Application Curves* section.

12 Power Supply Recommendations

The TPA2010D1 is designed to operate from an input voltage supply range between 2.5-V and 5.5-V. Therefore, the output voltage range of power supply should be within this range and well regulated. The current capability of upper power should not exceed the maximum current limit of the power switch.

12.1 Power Supply Decoupling Capacitors

The TPA2010D1 requires adequate power supply decoupling to ensure a high efficiency operation with low total harmonic distortion (THD). Place a low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 µF, within 2 mm of the V_{DD} pin. This choice of capacitor and placement helps with higher frequency transients, spikes, or digital hash on the line. In addition to the 0.1 µF ceramic capacitor, is recommended to place a 2.2 µF to 10 µF capacitor on the V_{DD} supply trace. This larger capacitor acts as a charge reservoir, providing energy faster than the board supply, thus helping to prevent any drop in the supply voltage.

13 Layout

13.1 Layout Guidelines

13.2 Board Layout

In making the pad size for the DSBGA balls, TI recommends that the layout use nonsolder mask defined (NSMD) land. With this method, the solder mask opening is made larger than the desired land area, and the opening size is defined by the copper pad width. Figure 42 and Table 3 show the appropriate diameters for a DSBGA layout. The TPA2010D1 evaluation module (EVM) layout is shown in the next section as a layout example.

Follow these guidelines:

- Circuit traces from NSMD defined PWB lands should be 75 µm to 100 µm wide in the exposed area inside the solder mask opening. Wider trace widths reduce device stand off and impact reliability.
- Recommend solder paste is Type 3 or Type 4.
- Best reilability results are achieved when the PWB laminate glass transition temperature is above the operating the range of the intended application.
- For a PWB using a Ni/Au surface finish, the gold thickness should be less 0.5 µm to avoid a reduction in thermal fatigue performance.
- Solder mask thickness should be less than 20 µm on top of the copper circuit pattern.
- Best solder stencil performance is achieved using laser cut stencils with electro polishing. Use of chemically etched stencils results in inferior solder paste volume control.
- Trace routing away from DSBGA device should be balanced in X and Y directions to avoid unintentional component movement due to solder wetting forces.

13.2.1 Component Location

Place all the external components very close to the TPA2010D1. The input resistors need to be very close to the TPA2010D1 input pins so noise does not couple on the high impedance nodes between the input resistors and the input amplifier of the TPA2010D1. Placing the decoupling capacitor, CS, close to the TPA2010D1 is important for the efficiency of the class-D amplifier. Any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency.

13.2.2 Trace Width

Recommended trace width at the solder balls is 75 µm to 100 µm to prevent solder wicking onto wider PCB traces. Figure 40 shows the layout of the TPA2010D1 evaluation module (EVM).

For high current pins (V_{DD}, GND V_{O+}, and V_{O-}) of the TPA2010D1, use 100-µm trace widths at the solder balls and at least 500-µm PCB traces to ensure proper performance and output power for the device.

For input pins (IN–, IN+, and $\overline{\text{SHUTDOWN}}$) of the TPA2010D1, use 75-µm to 100-µm trace widths at the solder balls. IN– and IN+ pins need to run side-by-side to maximize common-mode noise cancellation. Placing input resistors, R_{IN}, as close to the TPA2010D1 as possible is recommended.

Board Layout (continued)

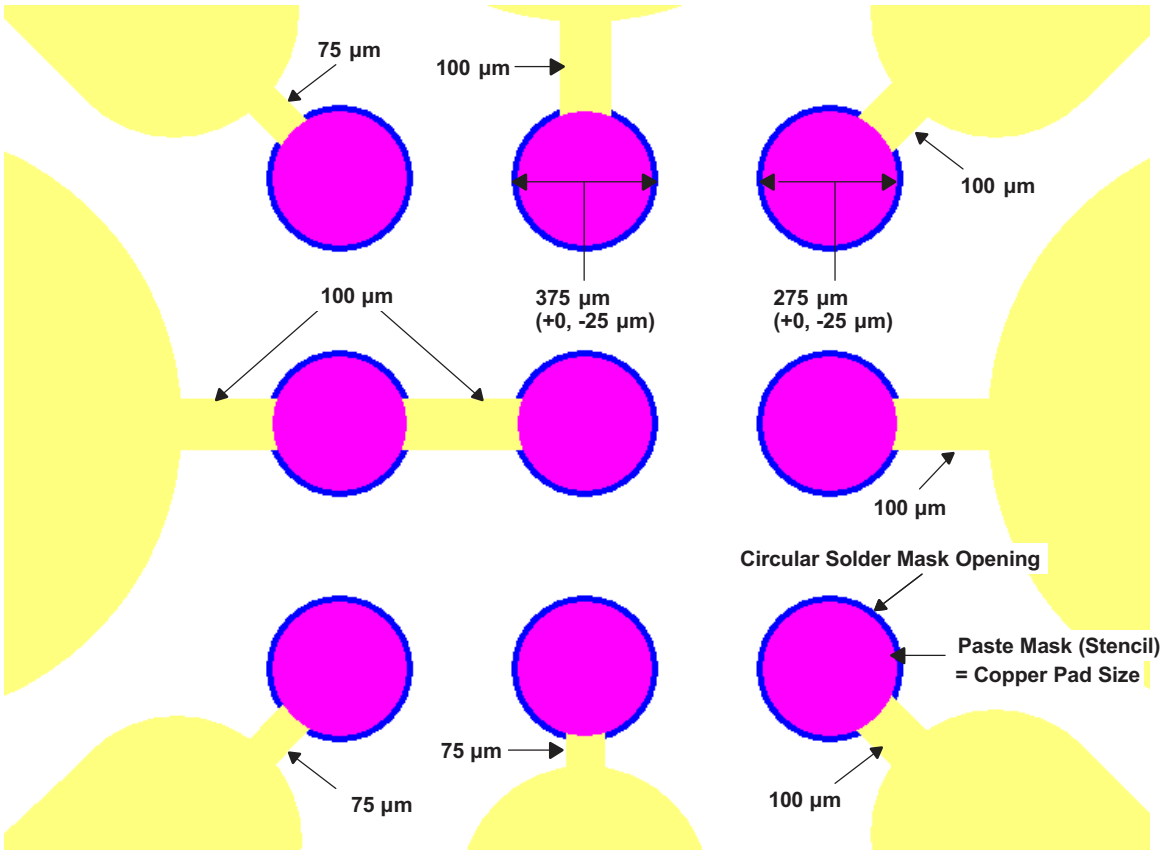


Figure 40. Close Up of TPA2010D1 Land Pattern from TPA2010D1 EVM

13.3 Layout Example

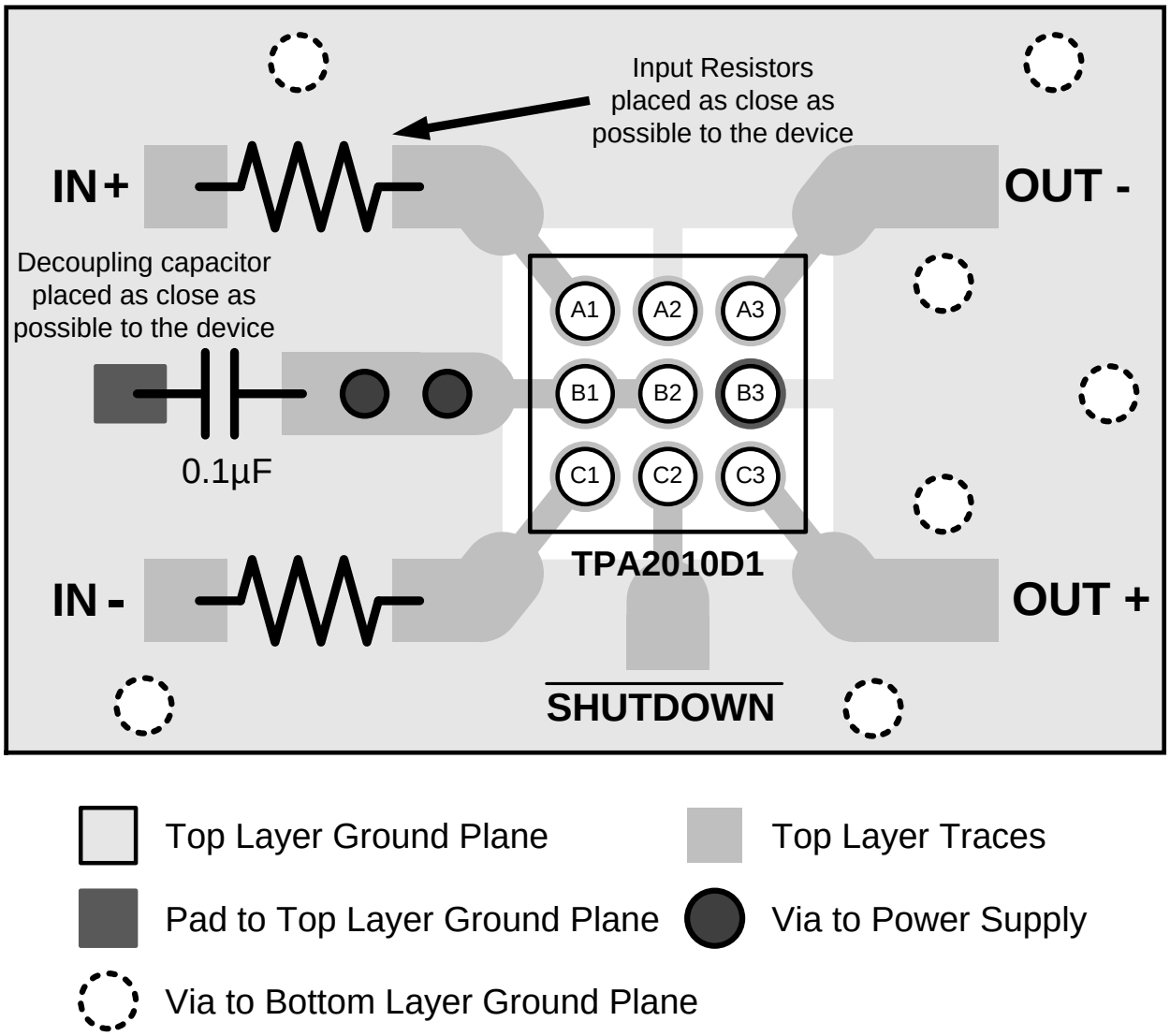


Figure 41. TPA2010D1 Layout Example

14 Device and Documentation Support

14.1 Device Support

14.1.1 Third-Party Products Disclaimer

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14.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

14.3 Trademarks

NanoFree, NanoStar, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

14.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

14.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

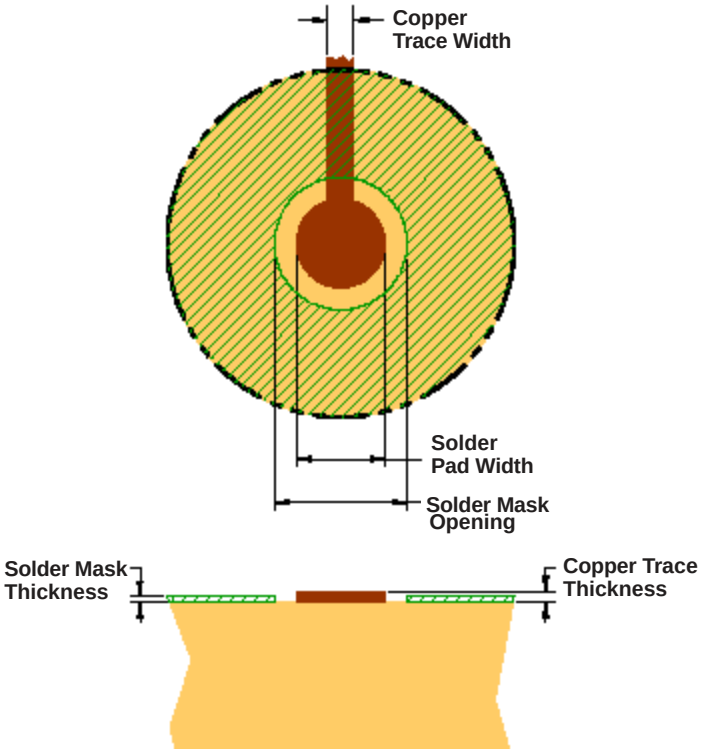


Figure 42. Land Pattern Dimensions

Table 3. Land Pattern Dimensions

SOLDER PAD DEFINITIONS	COPPER PAD	SOLDER MASK OPENING	COPPER THICKNESS	STENCIL OPENING	STENCIL THICKNESS
Nonsolder mask defined (NSMD)	275 µm (+0.0, –25 µm)	375 µm (+0.0, –25 µm)	1 oz max (32 µm)	275 µm × 275 µm Sq. (rounded corners)	125 µm thick

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPA2010D1YZFR	ACTIVE	DSBGA	YZF	9	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	AK0	Samples
TPA2010D1YZFT	ACTIVE	DSBGA	YZF	9	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	AK0	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

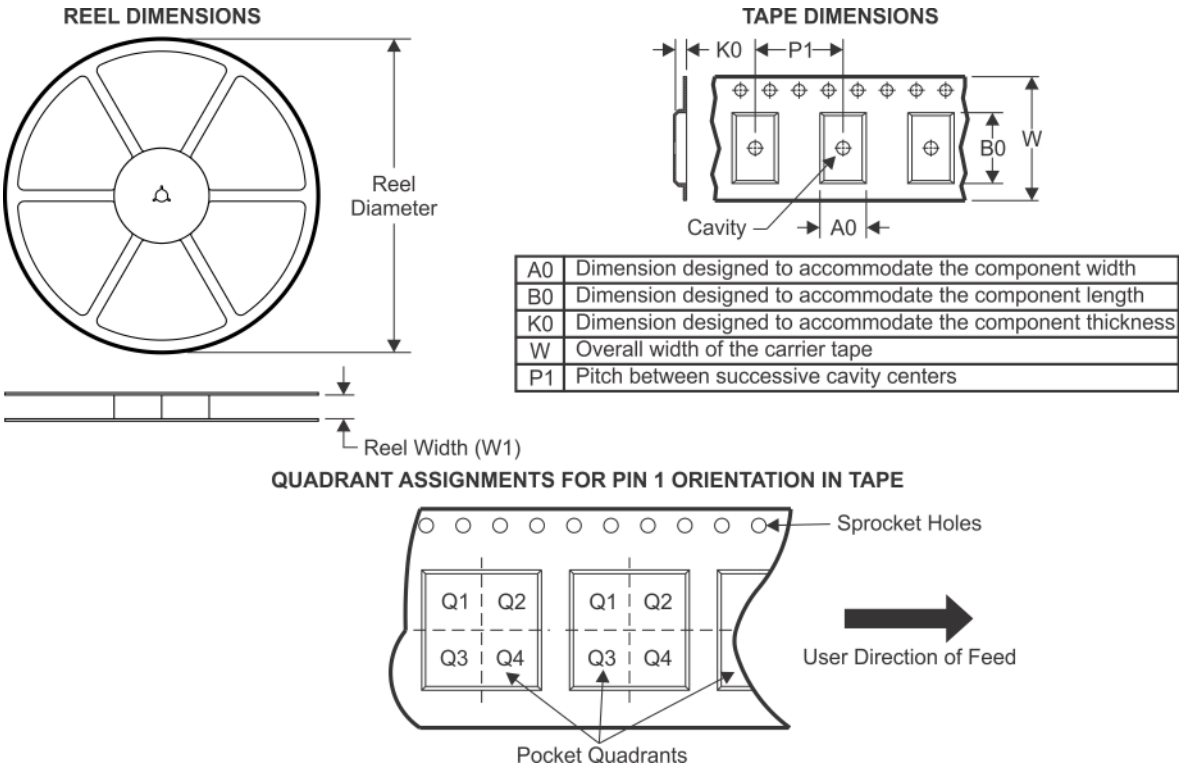
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

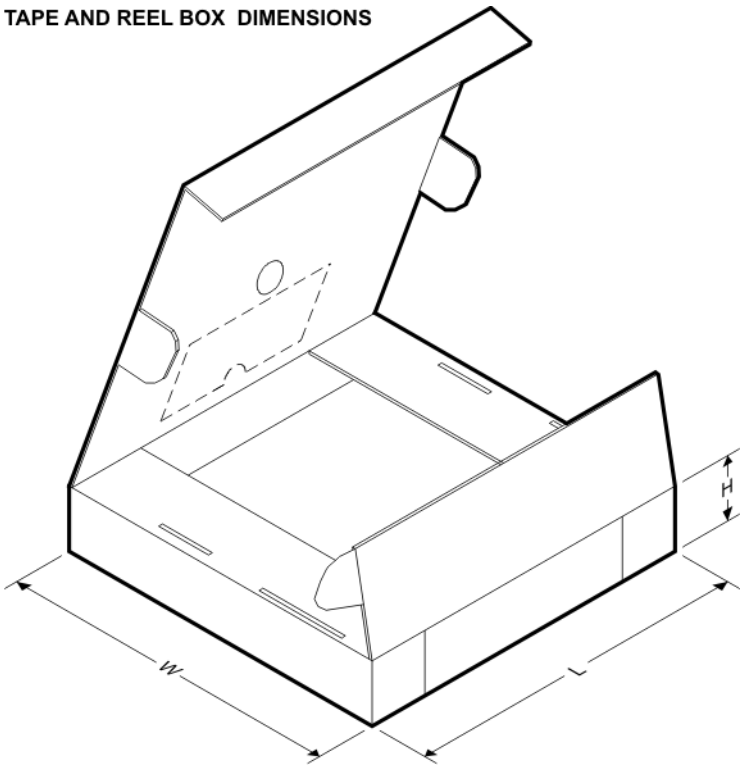


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

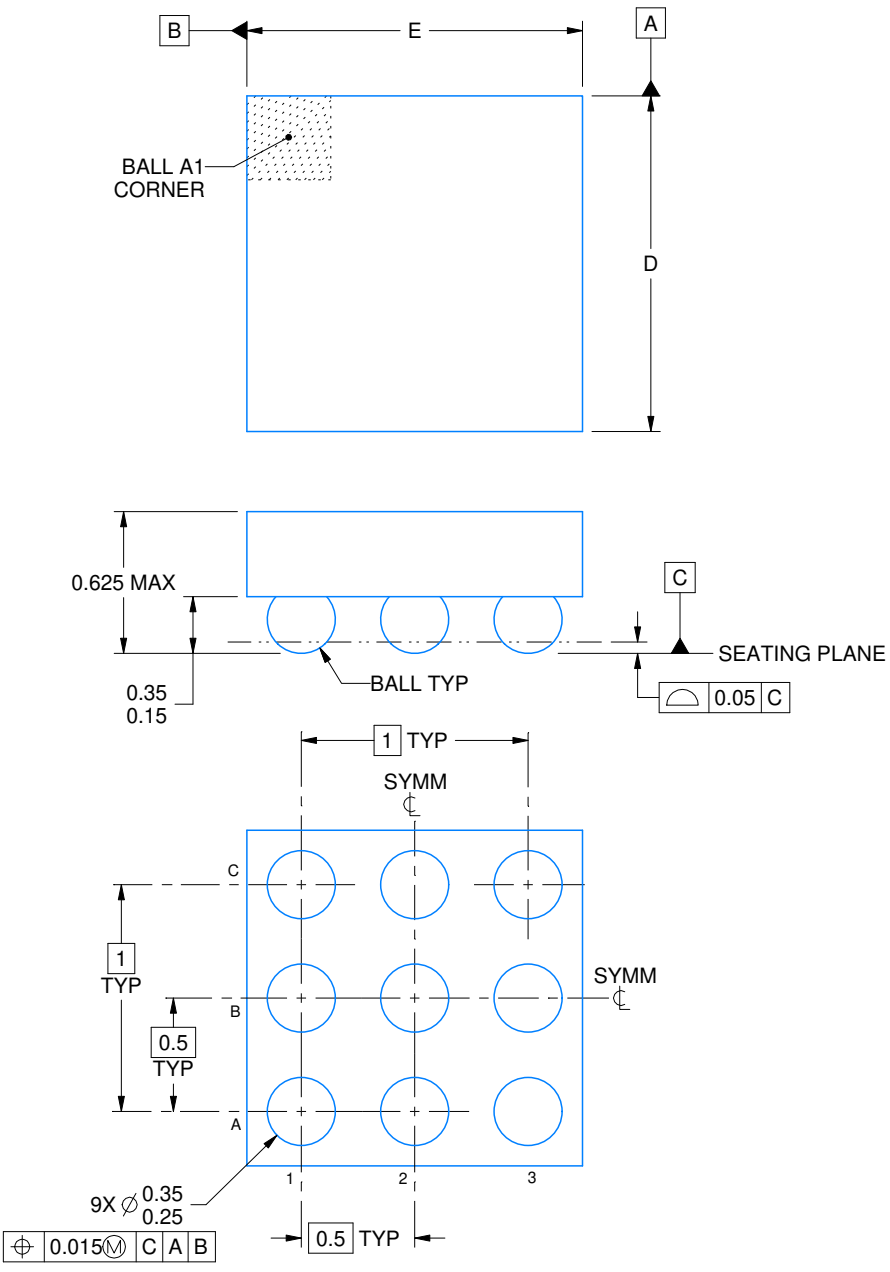
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA2010D1YZFR	DSBGA	YZF	9	3000	180.0	8.4	1.65	1.65	0.81	4.0	8.0	Q1
TPA2010D1YZFT	DSBGA	YZF	9	250	180.0	8.4	1.65	1.65	0.81	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA2010D1YZFR	DSBGA	YZF	9	3000	182.0	182.0	20.0
TPA2010D1YZFT	DSBGA	YZF	9	250	182.0	182.0	20.0



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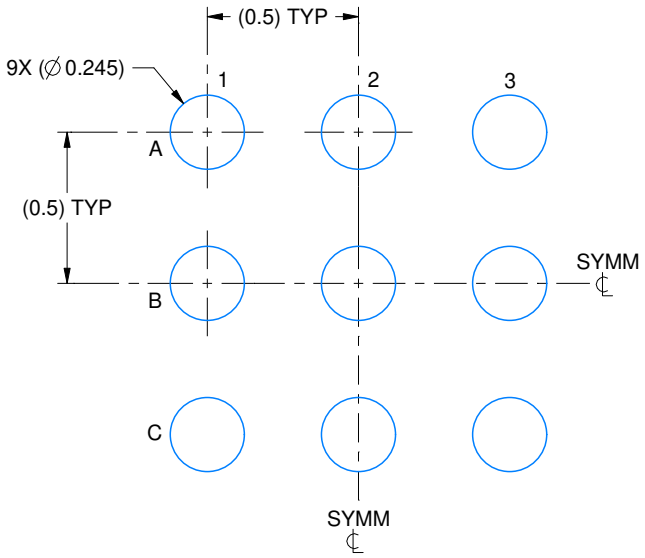
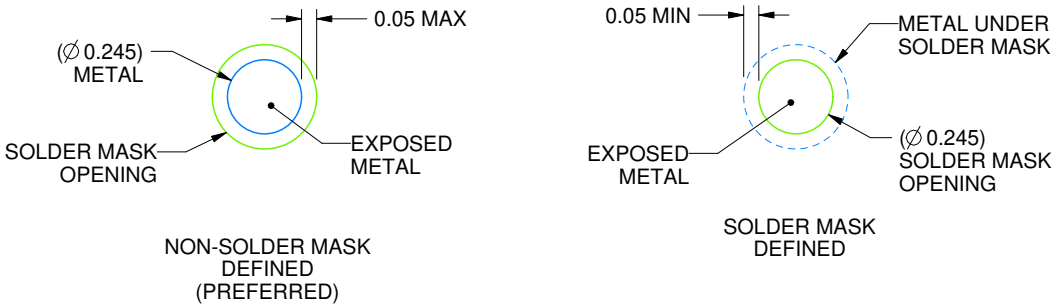
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 40X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

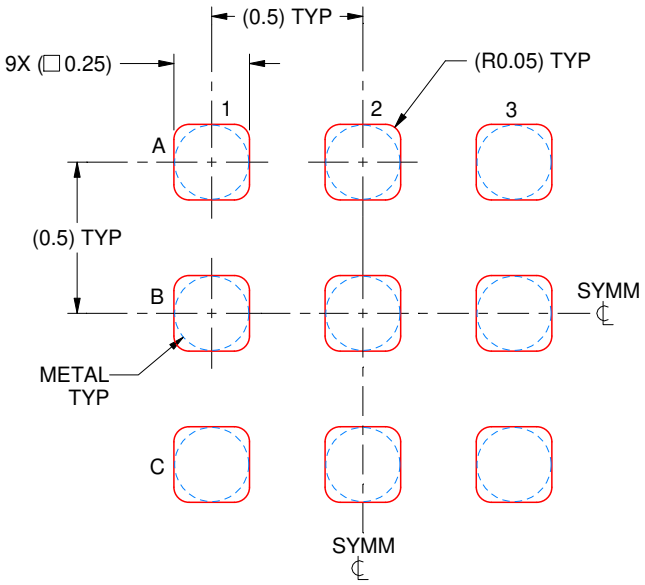
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YZF0009

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 40X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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