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April 1st, 2010 Renesas Electronics Corporation

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MOS FIELD EFFECT TRANSISTOR 2SK3634

SWITCHING N-CHANNEL POWER MOS FET

DESCRIPTION			ORDERING INFORMATION			
The 2SK3634 is N-channel MOS FET device that features			PART NUMBER	PACKAGE		
a low on-state resistance and excellent switching			2SK3634	TO-251 (MP-3)		
characteristics, and designed for high voltage applications			2SK3634-Z	TO-252 (MP-3Z)		
such as DC/DC converter.				X.		
FEATURES						
 High voltage: V_{DSS} = 200 V 						
 Gate voltage rating: ±30 V 			40			
RDS(on) = 0.60 Ω MAX. (VGS = 10 V, ID = 3	-		0			
• Low Ciss: Ciss = 270 pF TYP. (VDS = 10 V	, Vgs = 0 V)	aced	RIOGIU			
Built-in gate protection diode						
• TO-251/TO-252 package		0		(TO-251)		
 Avalanche capability rated 				•		
ABSOLUTE MAXIMUM RATINGS (TA	. = 25°C)					
Drain to Source Voltage ($V_{GS} = 0 V$)	VDSS	200	V			
Gate to Source Voltage (VDS = 0 V)	Vgss	±30	V	Ŵ		
Drain Current (DC) (Tc = 25°C)	ID(DC)	±6.0	А			
Drain Current (Pulse) Note1	D(pulse)	±18	А	(TO-252)		
Total Power Dissipation ($T_{c} = 25^{\circ}C$)	P T1	20	W	(
Total Power Dissipation ($T_A = 25^{\circ}C$)	P T2	1.0	W			
Channel Temperature	Tch	150	°C			
Storage Temperature	Tstg	–55 to +150	°C	(free		
Single Avalanche Current Note2	las	6.0	А			
Single Avalanche Energy Note2	Eas	3.6	mJ			
Repetitive Avalanche Current Note3	lar	6.0	А			
Repetitive Pulse Avalanche Energy Note3	Ear	2.0	mJ			

Notes 1. PW \leq 10 μ s, Duty Cycle \leq 1%

- **2.** Starting T_{ch} = 25°C, V_{DD} = 100 V, R_G = 25 Ω , V_{GS} = 20 \rightarrow 0 V, L = 100 μ H
- 3. $T_{ch} \leq 125^{\circ}C$, R_{G} = 25 $\Omega,~V_{DD}$ = 100 V

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Document No. D15936EJ3V0DS00 (3rd edition) Date Published August 2006 NS CP(K) Printed in Japan

The mark <R> shows major revised points.

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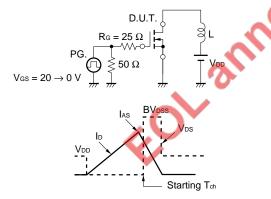
The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

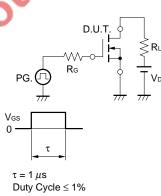
ELECTRICAL CHARACTERISTICS (TA = 25°C)

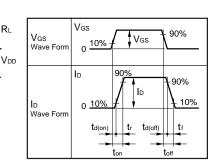
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
CHARACTERISTICS	STIVIDUL	TEST CONDITIONS	IVIIIN.	ITF.	WAA.	UNIT
Zero Gate Voltage Drain Current	loss	V _{DS} = 200 V, V _{GS} = 0 V			10	μA
Gate Leakage Current	lgss	$V_{GS} = \pm 30 \text{ V}, \text{ V}_{DS} = 0 \text{ V}$			±10	μA
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	2.5	3.5	4.5	V
Forward Transfer Admittance	y _{fs}	Vds = 10 V, Id = 3.0 A	2	4		S
Drain to Source On-state Resistance	RDS(on)	Vgs = 10 V, Id = 3.0 A		0.47	0.60	Ω
Input Capacitance	Ciss	V _{DS} = 10 V		270		pF
Output Capacitance	Coss	V _{GS} = 0 V		75		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		33		pF
Turn-on Delay Time	td(on)	Vdd = 100 V, Id = 3.0 A		4		ns
Rise Time	tr	V _{GS} = 10 V		8		ns
Turn-off Delay Time	td(off)	$R_G = 0 \Omega$.C	14		ns
Fall Time	tr		3	6		ns
Total Gate Charge	QG	Vdd = 160 V		9		nC
Gate to Source Charge	Q _{GS}	Vgs = 10 V		1.5		nC
Gate to Drain Charge	Qgd	ID = 6.0 A		4.5		nC
Body Diode Forward Voltage	VF(S-D)	IF = 16 A, VGS = 0 V		1.0		V
Reverse Recovery Time	trr	IF = 6 A, Vgs = 0 V		100		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/µs		320		nC

TEST CIRCUIT 1 AVALANCHE CAPABILITY

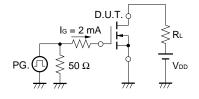
TEST CIRCUIT 2 SWITCHING TIME

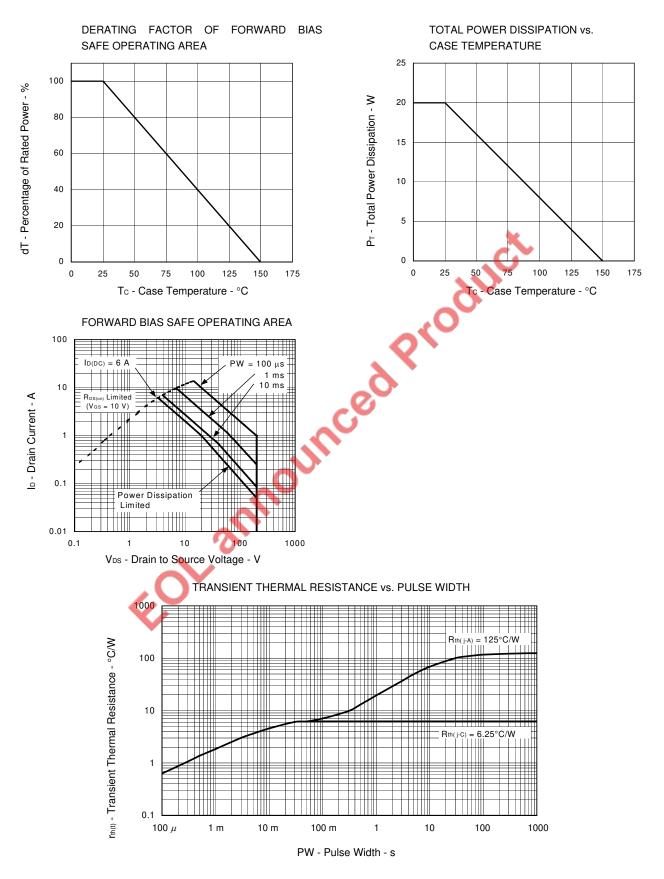




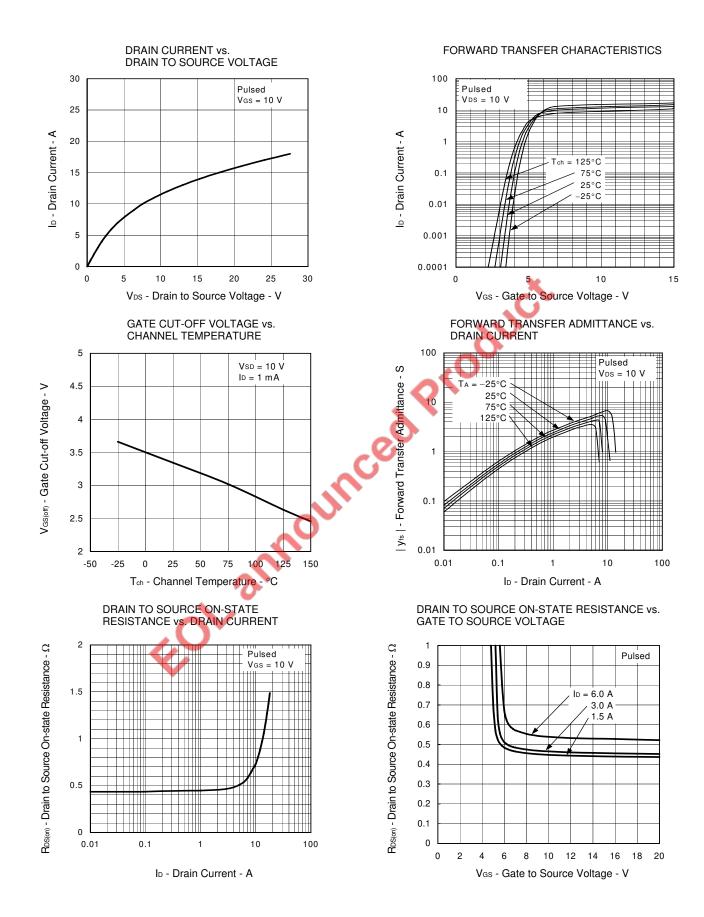


TEST CIRCUIT 3 GATE CHARGE

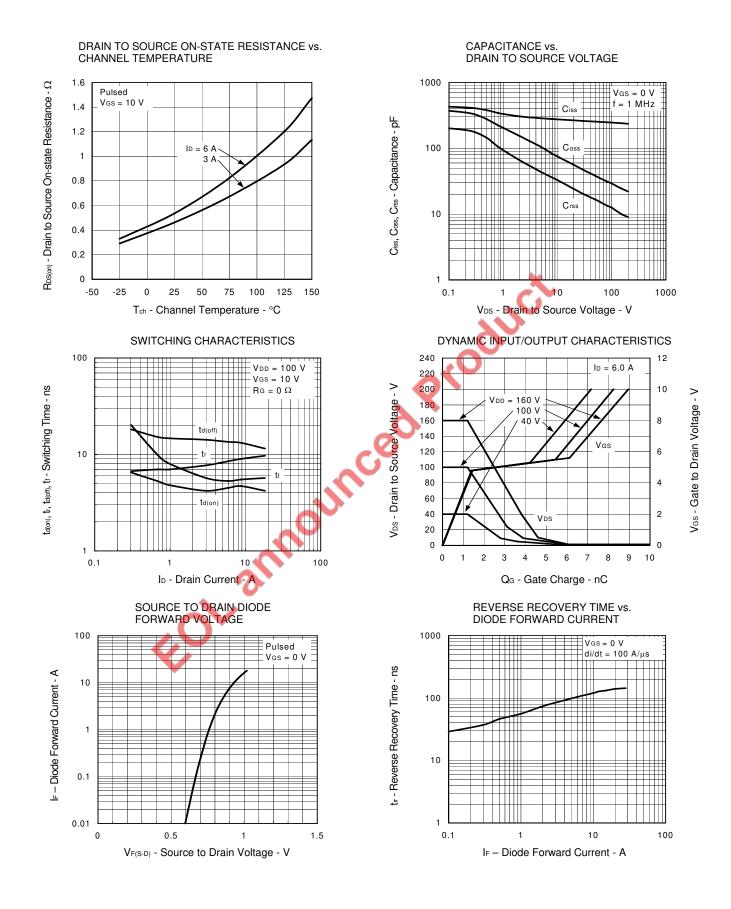




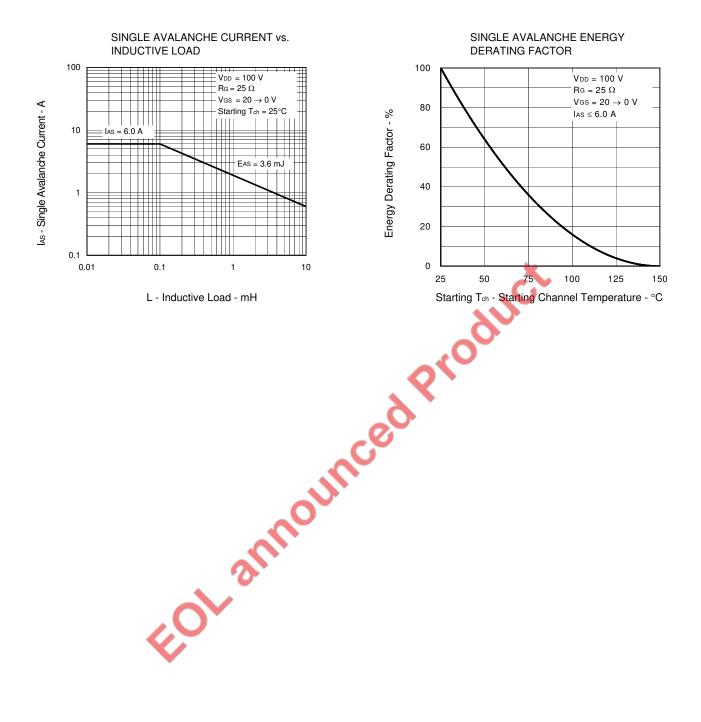
TYPICAL CHARACTERISTICS ($T_A = 25^{\circ}C$)



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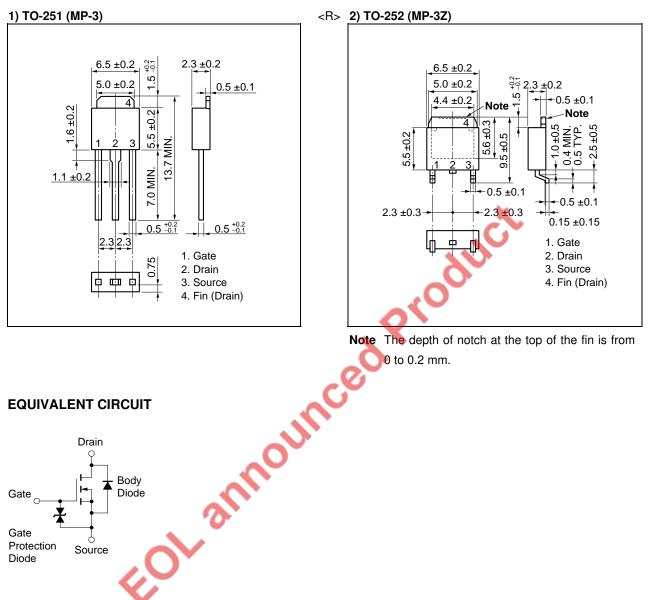


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PACKAGE DRAWINGS (Unit: mm)



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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