LTC3310S-1
3.3V to 1.0V at 10A, 2MHz Low EMI Buck Regulator in a 2.11cm² Solution

DESCRIPTION

Demonstration circuit 3021A shows the LTC®3310S-1 10A, 1V fixed output, synchronous step-down Silent Switcher®2 operating as a 2MHz 3.3V to 1.0V 10A buck regulator. The LTC3310S-1 supports operating frequencies from 500kHz up to 5MHz. The LTC3310S-1 is a compact, ultralow emission, high efficiency, and high speed synchronous monolithic step-down switching regulator. The integrated bypass capacitors optimize all the fast-current loops and make it easier to minimize EMI/EMC emissions by reducing layout sensitivity. The LTC3310S-1 has Active Voltage Positioning (AVP) where the output voltage is dependent on load current. At light loads, the output voltage is regulated above the nominal value. At full load, the output voltage is regulated below the nominal value. The DC load regulation is adjusted to improve transient performance and reduce output capacitor requirements.

DC3021A is set up to run in forced continuous mode with a 2MHz switching frequency but can be configured to pulse-skipping mode and different switching frequencies. RT is connected to V_{IN} which sets the MODE/SYNC pin as an input and allows the LTC3310S-1 to sync from an external clock. Connecting the MODE/SYNC pin to V_{IN} sets the mode to pulse-skipping mode and connecting the MODE/SYNC pin to GND sets the mode to forced continuous mode.

The DC3021A also has an EMI filter to reduce conducted EMI. This EMI filter can be included by applying the input voltage at the V_{IN} EMI terminal. The EMI performance of the board is shown in the EMI Test Results section. The red lines in the EMI performance graphs illustrate the CISPR25 Class 5 peak limits for the conducted and radiated emission tests.

The LTC3310S/LTC3310S-1 data sheet gives a complete description of the part, operation and application information. The data sheet must be read in conjunction with this demo manual. The LTC3310S-1 is assembled in a 3mm × 3mm LQFN package with exposed pad for low thermal resistance. The layout recommendations for low EMI operation and maximum thermal performance are available in the data sheet section Low EMI PCB Layout.

Design files for this circuit board are available.

PERFORMANCE SUMMARY Specifications are at $T_A = 25°C$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DC3021A Input Voltage Range		2.25		5.5	V
DC3021A V_{OUT} Voltage Range	I_{OUT} = 4A		1.0		V
DC3021A Output Current				10	A
Switching Frequency		1.8	2.0	2.2	MHz
V_{OUT} Active Voltage Positioning		1.7	2.4	3.1	mV/A

BOARD PHOTO

CIRCUIT SCHEMATIC

L = COILCRAFT, XEL4030-101ME
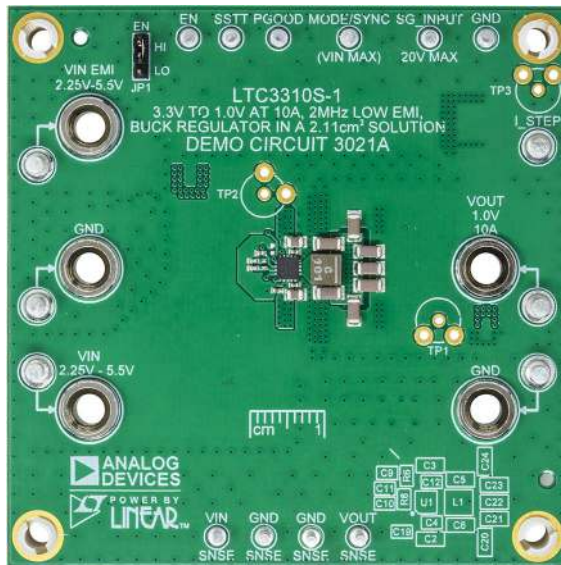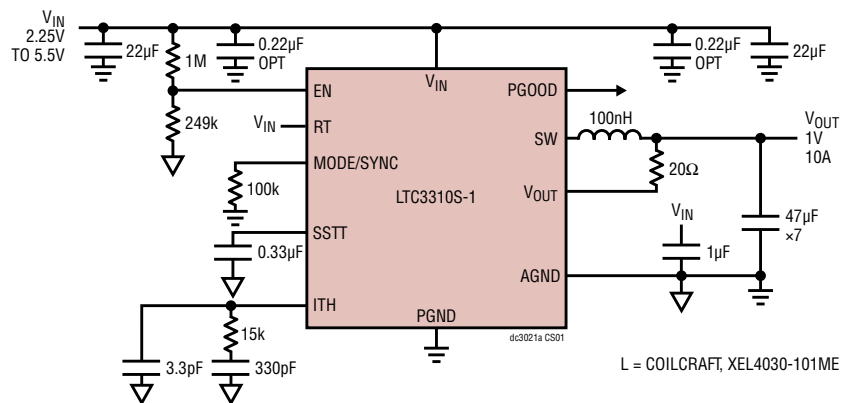
Efficiency and Power Loss vs Load Current

V_{IN} = 3.3V
V_{OUT} = 1.0V
F_{OSC} = 2MHz
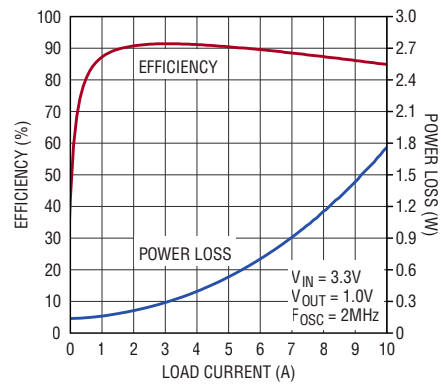
V_{OUT} Load Regulation (LTC3310S-1, LTC3310-1)

- 125°C
- 25°C
- −45°C
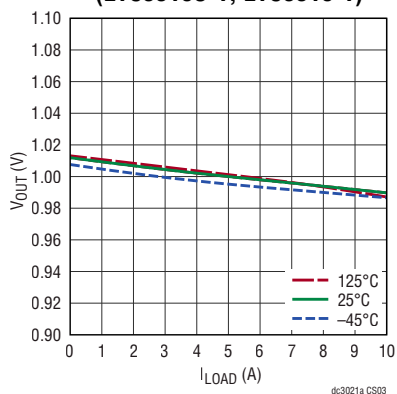
Load Transient Response Forced Continuous Moe

I_{OUT} 2A/DIV

1.0V V_{OUT} 10mV/DIV

10µs/DIV
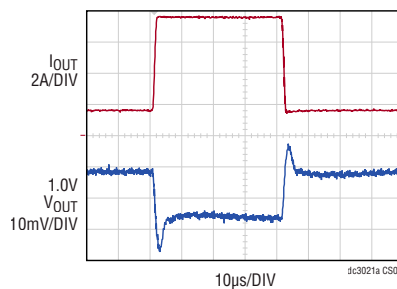
LTC3310S-1
3.3V_{IN} TO 1.0V_{OUT}
LOAD STEP 1.5A TO 7.5A 6A/µs
V_{OUTMIN} = 0.984V, V_{OUTMAX} = 1.018V
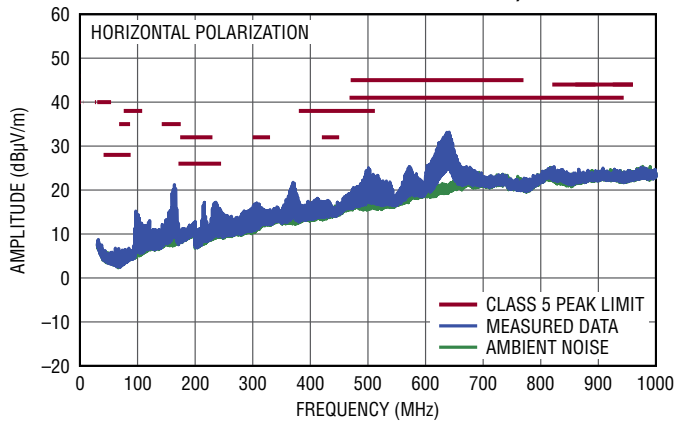
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EMI TEST RESULTS

Conducted EMI Performance (CISPR25 Conducted Emission Test with Class 5 Peak Limits)
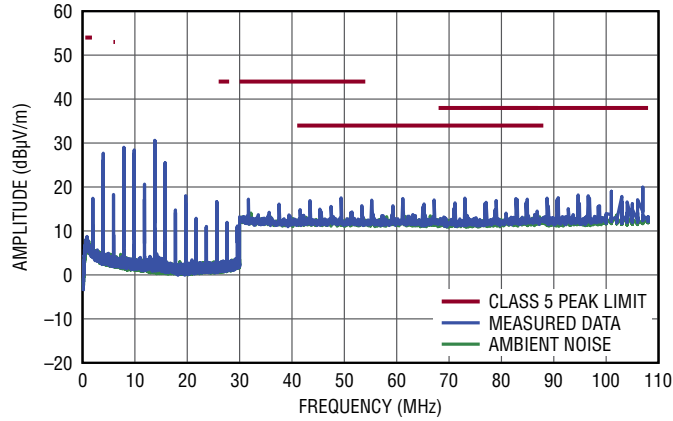
DC3021A DEMO BOARD
(WITH EMI FILTER INSTALLED)
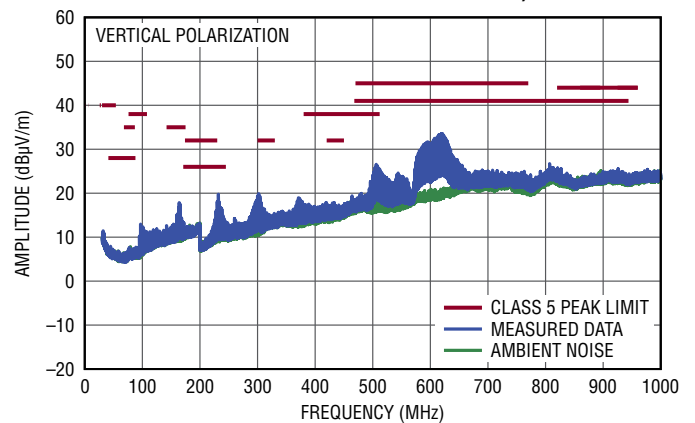3.3V INPUT TO 1V OUTPUT AT 8A, f_{SW} = 2MHz

dc3021a ET01

Radiated EMI Performance (CISPR25 Radiated Emission Test with Class 5 Peak Limits)

DC3021A DEMO BOARD
(WITH EMI FILTER INSTALLED)
3.3V INPUT TO 1V OUTPUT AT 8A, f_{SW} = 2MHz

dc3021a ET02

Radiated EMI Performance (CISPR25 Radiated Emission Test with Class 5 Peak Limits)

DC3021A DEMO BOARD
(WITH EMI FILTER INSTALLED)
3.3V INPUT TO 1V OUTPUT AT 8A, f_{SW} = 2MHz

dc3021a ET03

QUICK START PROCEDURE

Demonstration circuit 3021A is easy to set up to evaluate the performance of the LTC3310S-1. Refer to Figure 2 for proper measurement equipment setup and follow the procedure below.

> **NOTE:** For accurate V_{IN}, V_{OUT} and efficiency measurements, measure V_{IN} at the V_{IN} SNSE and GND SNSE turrets and V_{OUT} at the V_{OUT} SNSE and GND SNSE turrets as illustrated as VM1 and VM2 in Figure 2. When measuring the input or output voltage ripple, care must be taken to avoid a long ground lead on the oscilloscope probe. Measure the output voltage ripple by touching the probe tip directly across the output turrets or to TP1 as shown in Figure 3.

1. Set the JP1 Jumper to the HI position.

2. With power off, connect the input power supply to V_{IN} and GND. If the input EMI filter is desired, connect the input power supply to V_{IN} EMI and GND. Connect LD1 with the load set to 0A.

3. Slowly increase PS1 to 1.0V. If AM1 reads less than 20mA, increase PS1 to 3.3V. Verify that VM1 reads 3.3V and VM2 reads 1.2V. Record VM1, VM2, VM3 AM1 and AM2. Connect an oscilloscope voltage probe as shown in Figure 3. Set Channel to AC-coupled, voltage scale to 20mV and time base to 10µs. Record V_{OUT} ripple voltage. Verify that PGOOD voltage is above 3V. Calculate die temperature using Equation 1.

$$T_J \ (°C) = \frac{V_{SSTT}}{4mV} - 273 \tag{1}$$

4. Increase the load by 1A intervals up to 10A and observe the voltage output regulation, ripple voltage, and the voltage on the SSTT turret.

5. If pulse-skipping mode is desired, set PS1 to 0V. Install a 0Ω in the R5 location or short the MODE/SYNC turret to GND. Repeat Steps 1 through 4. In Step 4 observe that the switching waveform is now operating in pulse-skipping mode at low currents.

6. To change the frequency, remove R4 and install the desired R_T resistor in the R6 location. Note, the MODE/SYNC pin is an output when R6 is installed and the MODE/SYNC pin should have high impedance to GND and V_{IN}. Size the inductor, output capacitors and compensation components to provide the desired inductor ripple and a stable output.

7. To test the transient response with a base load, add the desired resistor to produce a minimum load between V_{OUT} and I_STEP turrets (RL shown on Figure 2). Note that the total load resistance will be RL plus R10 (50mΩ). Adjust a signal generator with a 10ms period, 10% duty-cycle and an amplitude from 1V to 2V to start.

8. Measure the I_STEP voltage to observe the current, $V_{I\_STEP}/50m\Omega$. Adjust the amplitude of the pulse to provide the desired transient. Adjust the rising and falling edge of the pulse to provide the desired ramp rate using Equation 2. The Load Transient Response Measurement (Figure 1) shows a load step from 1.5A (R_L = 0.62Ω) to 7.5A.

$$I_{OUT} = \frac{V_{I\_STEP}}{50m\Omega} \tag{2}$$

$$V_{GS} = V_{SG\_INPUT} - V_{I\_STEP}$$

When done, turn off SG1, PS1 and Load. Remove all connections to demo board.

V_{SG_INPUT} 2V/DIV

V_{I_STEP} 100mV/DIV

V_{OUT} 20mV/DIV

10µs/DIV
dc3021a F03

LTC3310S-1
3.3V_{IN} TO 1.0V_{OUT}
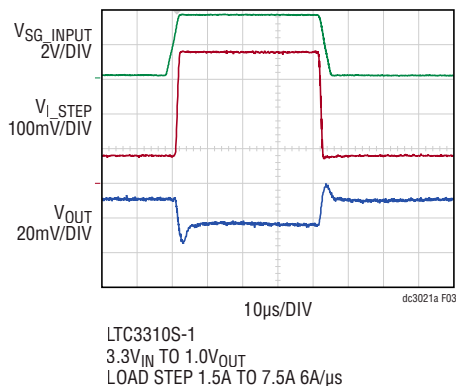LOAD STEP 1.5A TO 7.5A 6A/µs

Figure 1. Load Transient Response Measurement
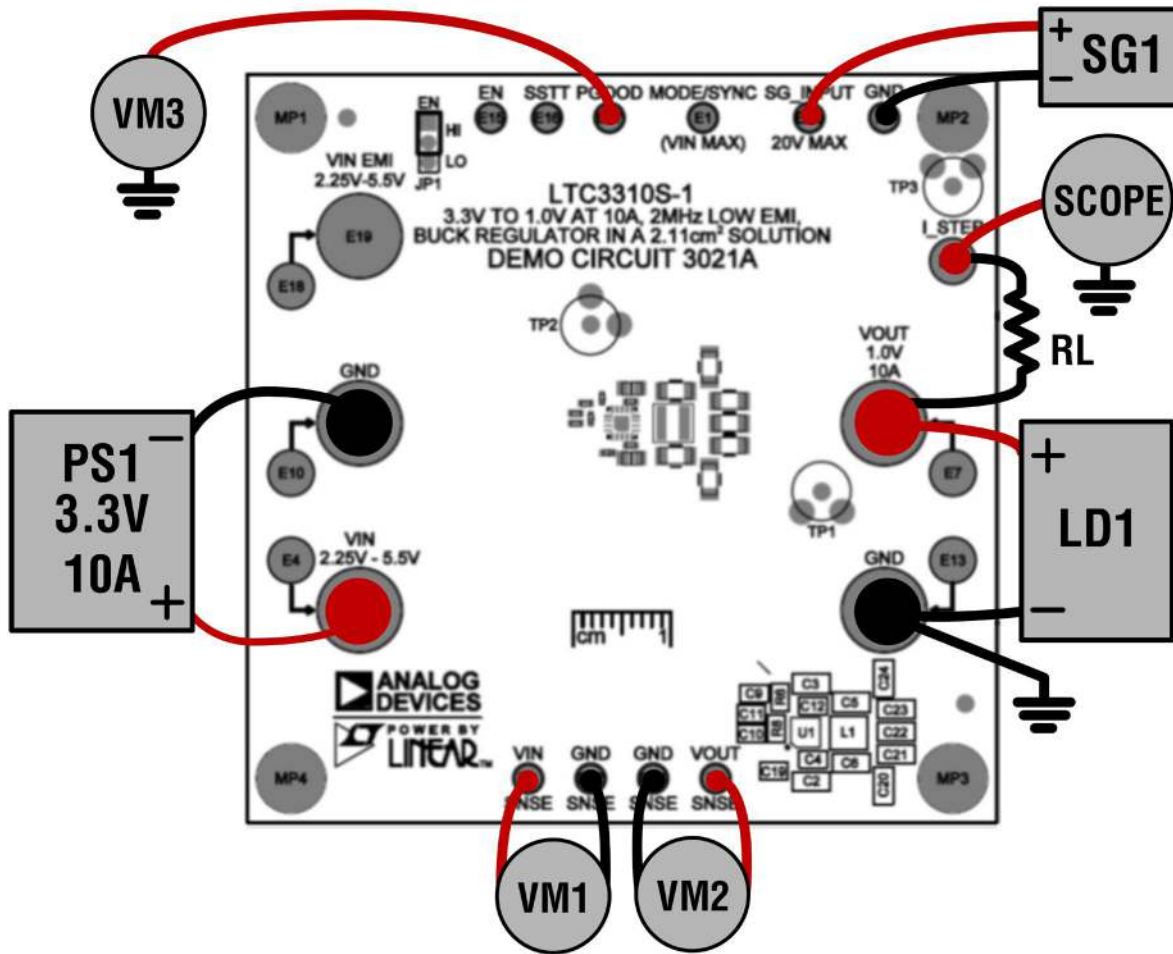
QUICK START PROCEDURE

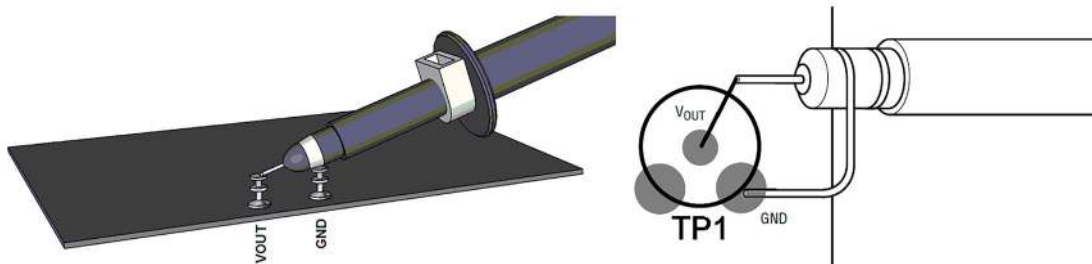Figure 2. Test Setup for the DC3021A Demo Board

Figure 3. Technique for Measuring Output Ripple and Step Response

THEORY OF OPERATION

Introduction to the DC3021A

The DC3021A demonstration circuit features the LTC3310S-1, a fixed 1V output, synchronous step-down Silent Switcher 2. The LTC3310S-1 is a monolithic, constant frequency, current mode step-down DC/DC converter. An oscillator, with frequency set using a resistor on the RT pin, turns on the internal top power switch at the beginning of each clock cycle. Current in the inductor then increases until the top switch comparator trips and turns off the top power switch. The peak inductor current, at which the top switch turns off, is controlled by the voltage on the internal ITH node. The error amplifier servos the ITH node by comparing the voltage on the internal V_{FB} pin with an internal 500mV reference. When the load current increases, it causes a reduction in the feedback voltage relative to the reference leading the error amplifier to raise the ITH voltage until the average inductor current matches the new load current. When the top switch turns off, the synchronous power switch turns on until the next clock cycle begins or the inductor current falls to zero. If overload conditions result in excessive current flowing through the bottom switch, the next clock cycle will be delayed until the switch current returns to a safe level.

The LTC3301S-1 includes active voltage positioning (AVP) where the output voltage is dependent on load current. At light loads the output is regulated above the nominal. At full load the output is regulated below the nominal. The DC regulation is degraded to improve transient performance and reduce output capacitance requirements.

If the EN pin is low, the LT3310S-1 is in shutdown and in a low quiescent current state. When the EN pin is above its threshold, the switching regulator will be enabled.

The MODE/SYNC pin synchronizes the switching frequency to an external clock, is a clock output or sets the PWM mode. The PWM modes of operation are either pulse-skipping or forced continuous mode. See the LTC3310S/LTC3310S-1 data sheet for more detailed information.

The maximum allowable operating frequency is influenced by the minimum on time of the top switch, the ratio of V_{OUT} to V_{IN} and the available inductor values. The maximum allowable operating frequency may be calculated using Equation 3.

$$f_{SW(MAX)} = \frac{V_{OUT}}{V_{IN(MAX)} \cdot t_{ON(MIN)}} \tag{3}$$

Select an operating switching frequency below $F_{SW(MAX)}$. Typically, it is desired to obtain an inductor current of 30% of the maximum LTC3310S-1 operating load, 10A. Use Equation 4 to calculate the inductor value to obtain a 30% (3A) inductor ripple for the operating frequency.

$$L \approx \frac{V_{OUT}}{3A \cdot f_{SW}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}} \right) \text{ for } \frac{V_{OUT}}{V_{IN(MAX)}} \leq 0.5$$

$$L \approx \frac{0.25 \cdot V_{IN(MAX)}}{3A \cdot f_{SW}} \text{ for } \frac{V_{OUT}}{V_{IN(MAX)}} > 0.5 \tag{4}$$

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THEORY OF OPERATION

When determining the compensation components, C10, C11 and R8, controlling the loop stability and transient response are the two main considerations. The LTC3310S-1 has been designed to operate at a high bandwidth for fast transient response capabilities. This reduces output capacitance required to meet the desired transient response. The mid-band gain of the loop increases with R8 and the bandwidth of the loop increases with decreasing C11. C10 along with R8 provides a high frequency pole to reduce the high frequency gain.

Loop stability is generally measured using the Bode plot method of plotting loop gain in dB and phase in degrees. The 0dB crossover frequency should be less the 1/6 of the operating frequency to reduce the effects of added phase of the modulator. The control loop phase margin goal should be 45° or greater and a gain margin goal of 8dB or greater.

Ceramic capacitors with a X5R or X7R dielectric should be used for both input and output capacitors. It is important to review the impedance versus frequency when selecting a capacitor for the application. Ceramic capacitors have a resonant frequency in the 1MHz to 3MHz range. Setting the operating frequency above the resonant frequency will result in higher output ripple voltage due to the ESL of the capacitor. Low inductance capacitors are available at a higher cost but can improve the ripple voltage by 30%. Low inductance capacitors are available from Murata, TDK, Taiyo Yuden and AVX.

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	2	C2, C3	CAP, 22µF, X7S, 6.3V, 20%, 0805	TDK, C2012X7S0J226M125AC
2	7	C5, C6, C20-C24	CAP, 47µF, X7S, 6.3V, 20%, 1206, NO SUBS. ALLOWED	TDK, C3216X7S0J476M160AC
3	1	C7	CAP, 0.1µF, X7R, 10V, 10%, 0402, AEC-Q200	MURATA, GCM155R71A104KA55D
4	1	C9	CAP, 0.033µF, X7R, 25V, 10%, 0402	WURTH ELEKTRONIK, 885012205053
5	1	C10	CAP, 3.3pF, C0G, 50V, ±0.25pF, 0402	AVX, 04025A3R3CAT2A
6	1	C11	CAP, 330pF, X7R, 50V, 20%, 0402	AVX, 04025C331MAT2A
7	1	L1	IND., 0.1µH, PWR, SHIELDED, 20%, 25.8A, 1.8mΩ, 4.3mm × 4.3mm, XEL4030, AEC-Q200	COILCRAFT, XEL4030-101MEB
8	1	R8	RES., 15k, 1%, 1/16W, 0402	VISHAY, CRCW040215K0FKED
9	1	U1	IC, 5V, FIXED 1V OUTPUT, 10A SYNCHRONOUS STEP-DOWN SILENT SWITCHER 2, 18-PIN LQFN	ANALOG DEVICES, LTC3310SEV-1#PBF
Additional Demo Board Circuit Components				
1	2	C1, C18	CAP, 470µF, TANT. POSCAP, 6.3V, 20%, 7343, 10mΩ, TCF	PANASONIC, 6TCF470MAH
2	2	C4, C12	CAP, 0.22µF, X7R, 16V, 10%, 0402, AEC-Q200	MURATA, GCM155R71C224KE02D
3	1	C8	CAP, 22µF, X7S, 6.3V, 20%, 0805	TDK, C2012X7S0J226M125AC
4	4	C13, C14, C16, C17	CAP, 10µF, X7S, 6.3V, 20%, 0603	TDK, C1608X7S0J106M080AC
5	1	C15	CAP, 0.1µF, X7R, 10V, 10%, 0402, AEC-Q200	MURATA, GCM155R71A104KA55D
6	1	C19	CAP, 1µF, X7S, 10V, 10%, 0402	MURATA, GRM155C71A105KE11D
7	1	L2	IND., 100Ω AT 100MHz, FERRITE BEAD, 25%, 8A, 6mΩ, 1812	WURTH ELEKTRONIK, 74279226101
8	1	Q1	XSTR., MOSFET, N-CH, 40V, 14A, DPAK (TO-252)	VISHAY, SUD50N04-8M8P-4GE3
9	1	R1	RES., 1M, 1%, 1/16W, 0402, AEC-Q200	VISHAY, CRCW04021M00FKED
10	1	R2	RES., 249k, 1%, 1/16W, 0402, AEC-Q200	VISHAY, CRCW0402249KFKED
11	2	R3, R9	RES., 100k, 5%, 1/16W, 0402, AEC-Q200	VISHAY, CRCW0402100KJNED
12	1	R4	RES., 0Ω, 1/16W, 0402, AEC-Q200	VISHAY, CRCW04020000Z0ED
13	0	R5, R6	RES., OPTION, 0402	
14	1	R7	RES., 20Ω, 1%, 1/16W, 0402, AEC-Q200	VISHAY, CRCW040220R0FKED
15	1	R10	RES., 0.05Ω, 1%, 10W, 2818, AEC-Q200, METAL, HP	VISHAY, WSHP2818R0500FEA
16	1	R11	RES., 10k, 5%, 1/16W, 0402, AEC-Q200	VISHAY, CRCW040210K0JNED
Hardware				
1	10	E1-E3, E5, E12, E14-E17, E20	TEST POINT, TURRET, 0.064" MTG. HOLE, PCB 0.062" THK	MILL-MAX, 2308-2-00-80-00-00-07-0
2	6	E4, E7, E10, E13, E18, E21	TEST POINT, TURRET, 0.094" MTG. HOLE, PCB 0.062" THK	MILL-MAX, 2501-2-00-80-00-00-07-0
3	5	E6, E8, E9, E11, E19	CONN., BANANA JACK, FEMALE, THT, NON-INSULATED, SWAGE, 0.218"	KEYSTONE, 575-4
4	1	JP1	CONN., HDR, MALE, 1 × 3, 2mm, VERT, ST, THT	WURTH ELEKTRONIK, 62000311121
5	4	MP1-MP4	STANDOFF, NYLON, SNAP-ON, 0.50"	KEYSTONE, 8833
6	1	XJP1	CONN., SHUNT, FEMALE, 2 POS, 2mm	WURTH ELEKTRONIK, 60800213421

SCHEMATIC DIAGRAM
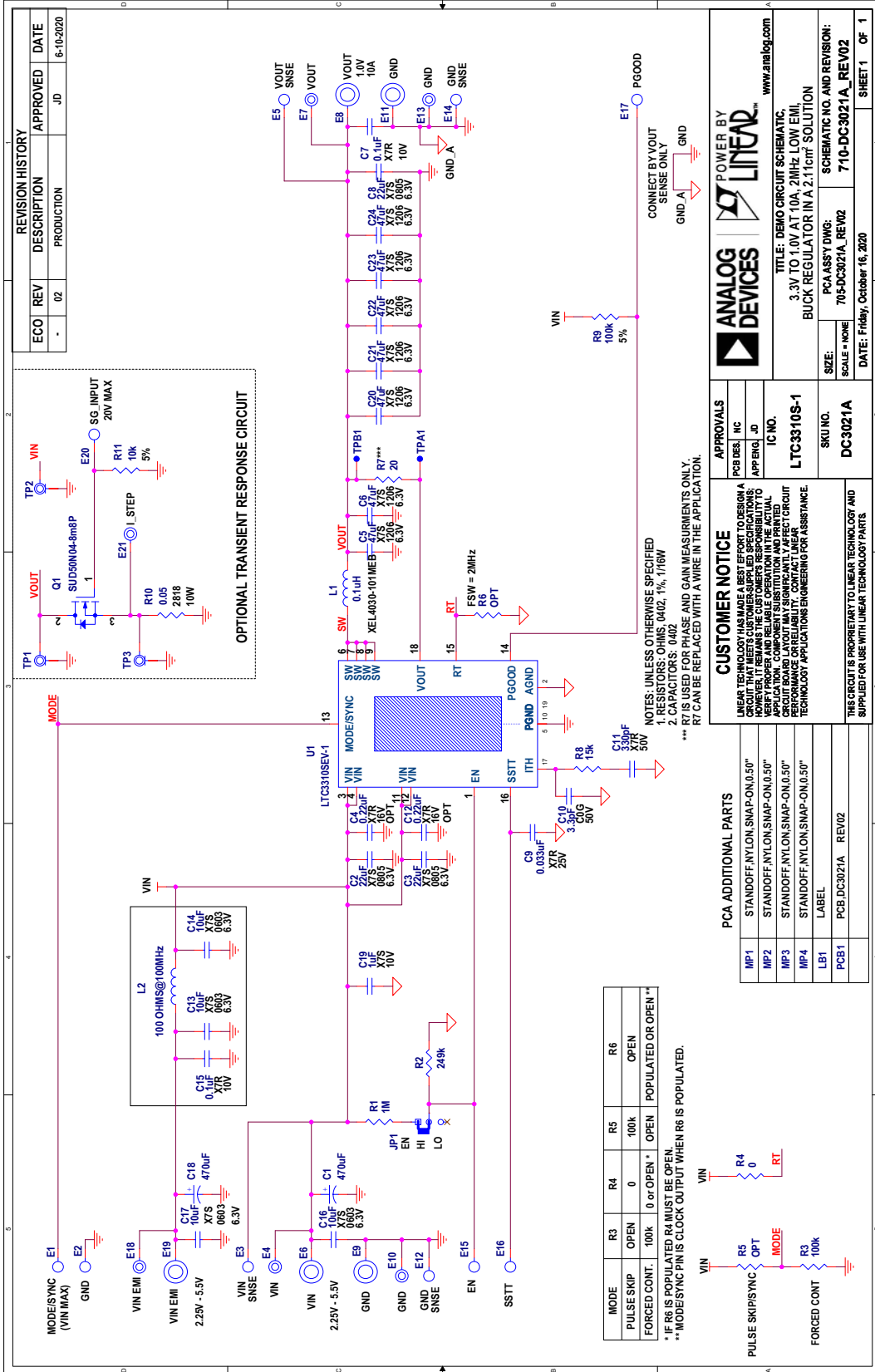
ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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