CY7C1049CV33

4-Mbit (512 K × 8) Static RAM

Features

- Temperature ranges
  - Commercial: 0 °C to 70 °C
  - Industrial: –40 °C to 85 °C
- High speed
  - t_{AA} = 8 ns
- Low active power
  - 360 mW (max)
- 2.0 V data retention
- Automatic power down when deselected
- Transistor- transistor logic (TTL) compatible inputs and outputs
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features

Functional Description

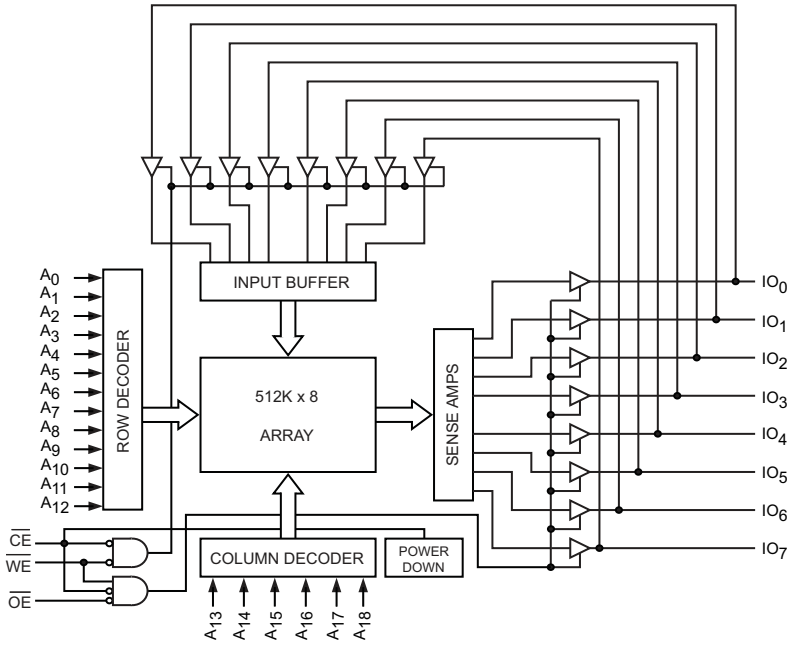
The CY7C1049CV33 is a high performance Complementary metal oxide semiconductor (CMOS) Static RAM organized as 524,288 words by eight bits. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{CE}$), an active LOW Output Enable ($\overline{OE}$), and three-state drivers. Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{18}).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins.

The eight input and output pins (I/O_0 through I/O_7) are placed in a high impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

The CY7C1049CV33 is available in standard 44-pin TSOP II package with center power and ground (revolutionary) pinout.

Logic Block Diagram



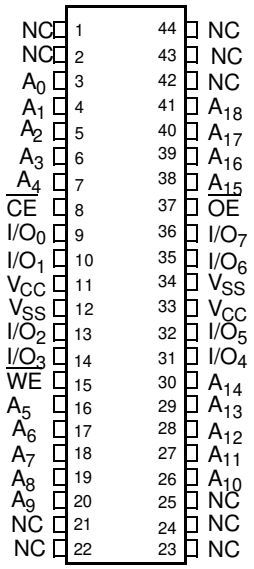
Contents

Selection Guide

Description	-8	-10	Unit
Maximum access time	8	10	ns
Maximum operating current	100	100	mA
Maximum CMOS standby current	10	10	mA

Pin Configuration

Figure 1. 44-pin TSOP II (Top View)



Pin Definitions

Pin Name	44-pin TSOP II Pin Number	I/O Type	Description
A_0–A_{18}	3–7, 16–20, 26–30, 38–41	Input	**Address inputs used to select one of the address locations.**
I/O_0–I/O_7	9, 10, 13, 14, 31, 32, 35, 36	Input/Output	**Bidirectional data I/O lines.** Used as input or output lines depending on operation.
NC[1]	1, 2, 21, 22, 23, 24, 25, 42, 43, 44	No connect	**No connects.** This pin is not connected to the die.
$\overline{WE}$	15	Input/Control	**Write Enable input, active LOW.** When selected LOW, a WRITE is conducted. When selected HIGH, a READ is conducted.
$\overline{CE}$	8	Input/Control	**Chip Enable input, active LOW.** When LOW, selects the chip. When HIGH, deselects the chip.
$\overline{OE}$	37	Input/Control	**Output Enable, active LOW.** Controls the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are three-stated, and act as input data pins.
V_{SS}, GND	12, 34	Ground	**Ground for the device.** Should be connected to ground of the system.
V_{CC}	11, 33	Power supply	**Power supply inputs to the device.**

Note
1. NC pins are not connected on the die.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage on V_{CC} to Relative GND[2] .....–0.5 V to +4.6 V

DC voltage applied to outputs in High Z State[2] .....–0.5 V to V_{CC} + 0.5 V

Input Voltage[2] .....–0.5 V to V_{CC} + 0.5 V

Current into Outputs (LOW) ..... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0 °C to +70 °C	3.3 V ± 0.3 V
Industrial	-40 °C to +85 °C	3.3 V ± 0.3 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	-8		-10		Unit
			Min	Max	Min	Max	
V_{OH}	Output HIGH voltage	V_{CC} = Min; I_{OH} = –4.0 mA	2.4	–	2.4	–	V
V_{OL}	Output LOW voltage	V_{CC} = Min; I_{OL} = 8.0 mA	–	0.4	–	0.4	V
V_{IH}	Input HIGH voltage		2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW voltage[2]		–0.3	0.8	–0.3	0.8	V
I_{IX}	Input load current	GND ≤ V_I ≤ V_C	–1	+1	–1	+1	µA
I_{CC}	V_{CC} operating supply current	V_{CC} = Max, f = f_{MAX} = $1/t_{RC}$	–	100	–	100	mA
I_{SB1}	Automatic CE power down current —TTL inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	–	40	–	40	mA
I_{SB2}	Automatic CE power down current —CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3 V, V_{IN} ≥ V_{CC} – 0.3 V, or V_{IN} ≤ 0.3 V, f = 0	–	10	–	10	mA

Capacitance

Parameter[3]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 3.3 V	8	pF
C_{OUT}	I/O capacitance		8	pF

Thermal Resistance

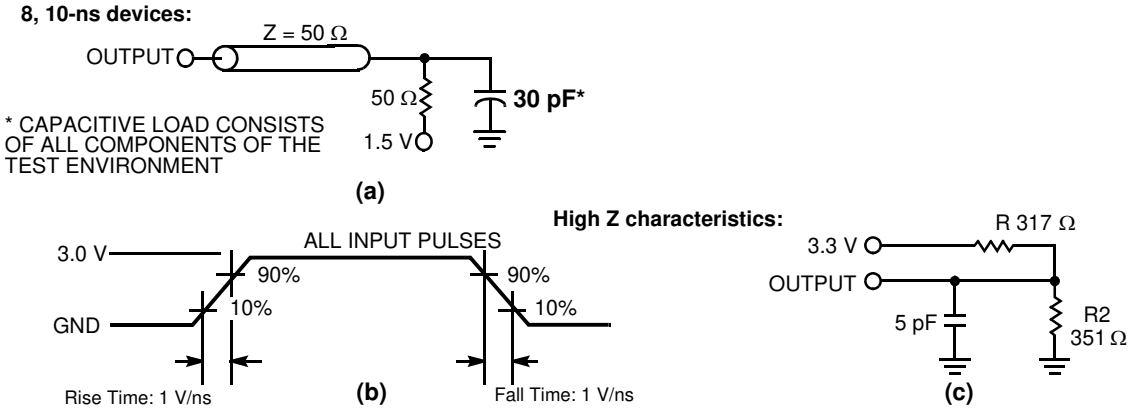
Parameter[3]	Description	Test Conditions	44-pin TSOP-II	Unit
Θ_{JA}	Thermal resistance (Junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	41.66	°C/W
Θ_{JC}	Thermal resistance (Junction to case)		10.56	°C/W

Notes

2. AC characteristics (except High Z) are tested using the load conditions shown in Figure 2 on page 5 (a). High Z characteristics are tested for all speeds using the test load shown in Figure 2 on page 5 (c).
3. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms [4]



Note
4. AC characteristics (except High Z) are tested using the load conditions shown in Figure 2 (a). High Z characteristics are tested for all speeds using the test load shown in Figure 2 (c).

AC Switching Characteristics

Over the Operating Range

Parameter [5]	Description	-8		-10		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{power} [6]	V_{CC}(typical) to the first access	100	–	100	–	µs
t_{RC}	Read cycle time	8	–	10	–	ns
t_{AA}	Address to data valid	–	8	–	10	ns
t_{OHA}	Data Hold from Address Change	3	–	3	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	8	–	10	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	5	–	5	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z [7]	0	–	0	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z [7, 8]	–	4	–	5	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z [7]	3	–	3	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z [7, 8]	–	4	–	5	ns
t_{PU}	$\overline{CE}$ LOW to power up	0	–	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power down	–	8	–	10	ns
Write Cycle [9, 10]						
t_{WC}	Write cycle time	8	–	10	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	6	–	7	–	ns
t_{AW}	Address setup to write end	6	–	7	–	ns
t_{HA}	Address hold from write end	0	–	0	–	ns
t_{SA}	Address setup to write start	0	–	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	6	–	7	–	ns
t_{SD}	Data setup to write end	4	–	5	–	ns
t_{HD}	Data hold from write end	0	–	0	–	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z [7]	3	–	3	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [7, 8]	–	4	–	5	ns

Notes

5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V.
6. t_{POWER} gives the minimum amount of time that the power supply should be at stable, typical V_{CC} values until the first memory access can be performed.
7. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
8. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (c) of Figure 2 on page 5. Transition is measured ±500 mV from steady-state voltage.
9. The internal Write time of the memory is defined by the overlap of $\overline{CE}$ LOW, and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a Write, and the transition of either of these signals can terminate the Write. The input data setup and hold timing should be referenced to the leading edge of the signal that terminates the Write.
10. The minimum Write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms

Figure 3. Read Cycle No. 1 (Address Transition Controlled) [11, 12]

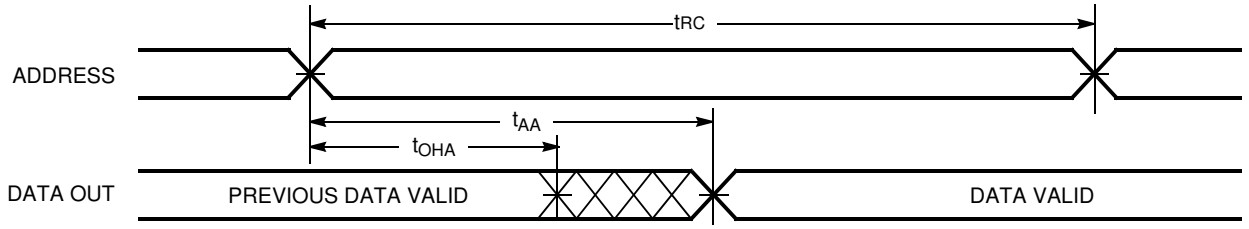
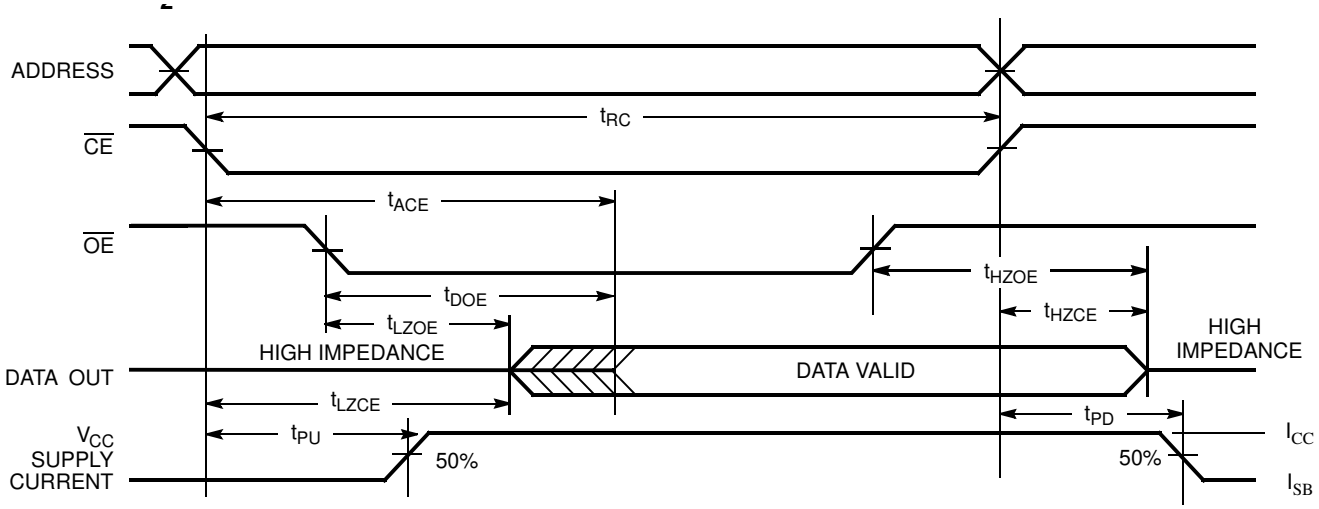


Figure 4. Read Cycle No. 2 ($\overline{OE}$ Controlled) [12, 13]



Notes
11. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
12. $\overline{WE}$ is HIGH for read cycles.
13. Address valid before or similar to $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Figure 5. Write Cycle No. 1 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write) [14, 15]

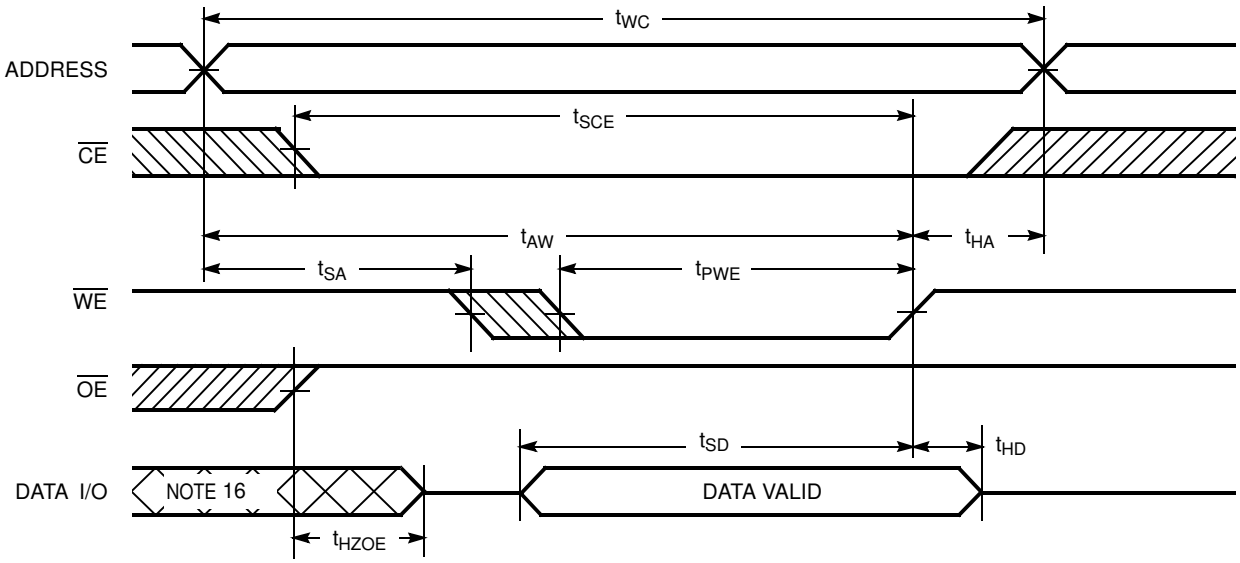
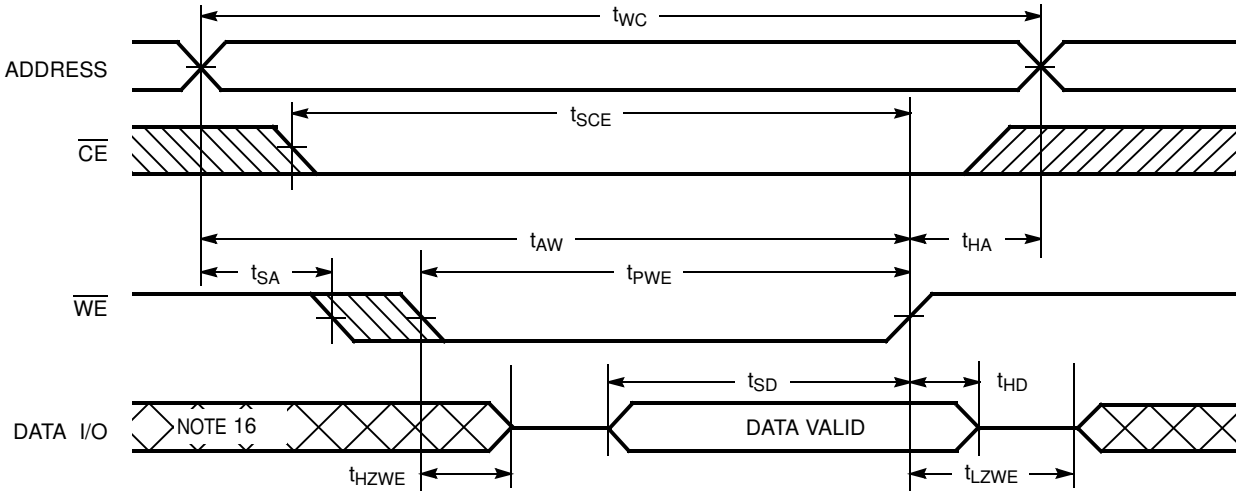


Figure 6. Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [15]



Notes
14. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
15. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in high impedance state.
16. During this period, the I/Os are in output state. Do not apply input signals.

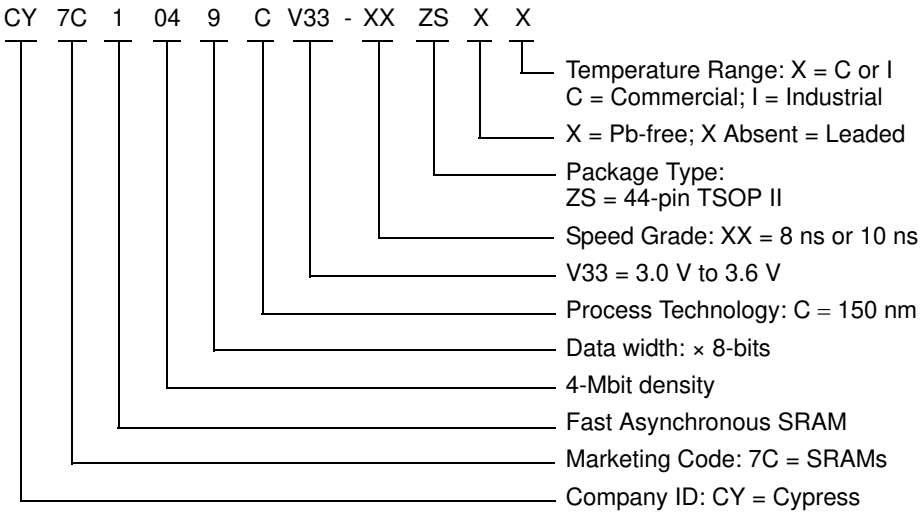
Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O_0–I/O_7	Mode	Power
H	X	X	High Z	Power Down	Standby (I_{SB})
L	L	H	Data Out	Read	Active (I_{CC})
L	X	L	Data In	Write	Active (I_{CC})
L	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

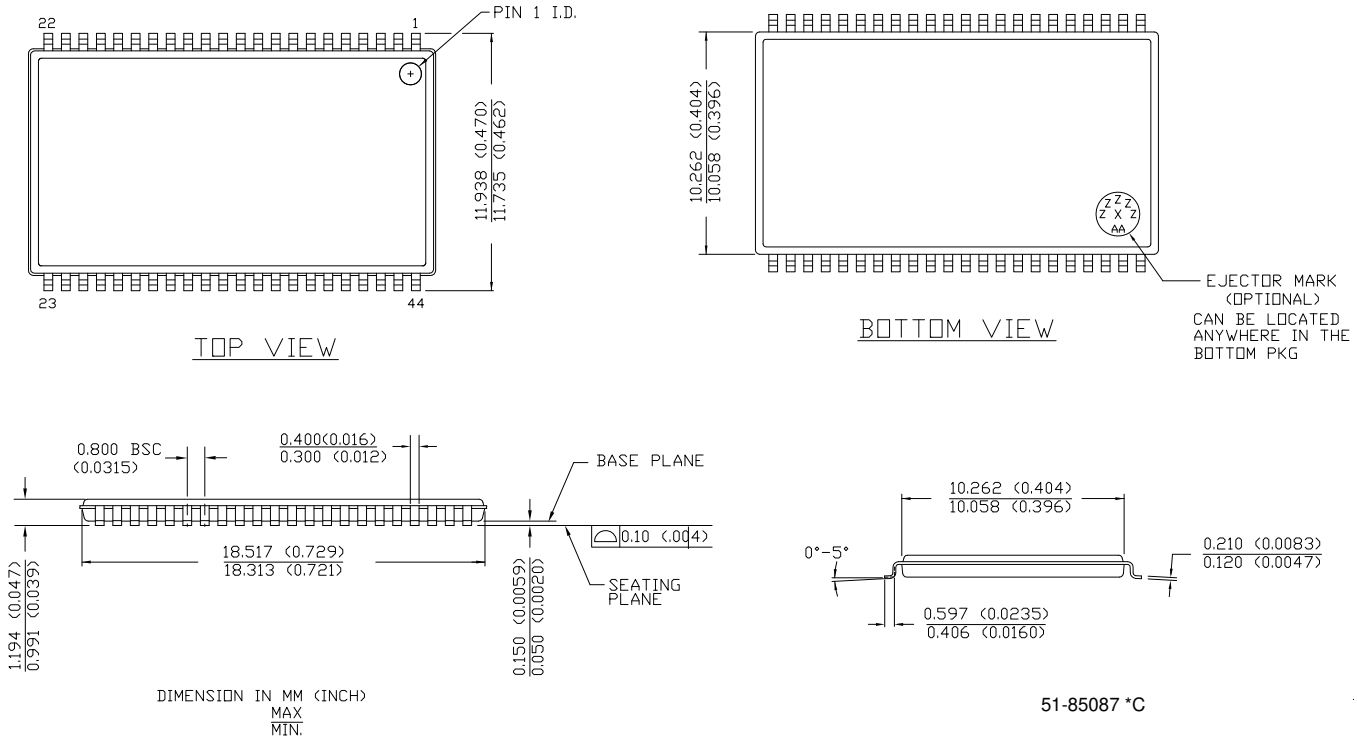
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
8	CY7C1049CV33-8ZSXC	51-85087	44-pin TSOP II (Pb-free)	Commercial
10	CY7C1049CV33-10ZXI	51-85087	44-pin TSOP II (Pb-free)	Industrial

Ordering Code Definitions



Package Diagram

Figure 7. 44-pin TSOP Z44-II, 51-85087



Acronyms

Acronym	Description
$\overline{CE}$	chip enable
CMOS	complementary metal oxide semiconductor
I/O	input/output
$\overline{OE}$	output enable
RAM	random access memory
SRAM	static random access memory
TSOP	thin small outline package
TTL	transistor-transistor logic
$\overline{WE}$	write enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	Mega Hertz
µA	micro Amperes
µs	micro seconds
mA	milli Amperes
mm	milli meter
ms	milli seconds
mW	milli Watts
ns	nano seconds
Ω	ohms
%	percent
pF	pico Farad
V	Volts
W	Watts

Document History Page

Document Title: CY7C1049CV33, 4-Mbit (512 K × 8) Static RAM Document Number: 38-05006				
Rev.	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	112569	HGK	03/06/02	New data sheet
*A	114091	DFP	04/25/02	Changed Tpower unit from ns to μs
*B	116479	CEA	09/16/02	Add applications foot note to data sheet, page 1.
*C	262949	RKF	See ECN	Added Automotive-E Specs Added Θ_{JA} and Θ_{JC} values on Page #3.
*D	300091	RKF	See ECN	Added -20-ns Speed bin
*E	344595	SYT	See ECN	Added Pb-free package on page #8 Removed shading for CY7C1049CV33-15ZSXE in the ordering Information on page 9
*F	2615344	VKN/PYRS	12/03/08	Added Automotive-A information Removed 8 ns and 20 ns speed bins, Changed t_{POWER} spec from 1 μs to 100 μs, Updated Ordering Information table.
*G	2841563	NXR/	01/07/2010	Added CY7C1049CV33-10VXA to Ordering Info table.
*H	2898958	AJU	03/25/10	Removed inactive parts from the ordering information table. Updated package diagrams.
*I	2954734	AJU	06/30/2010	New Part Number added CY7C1049CV33-10ZXC to Ordering Info table.
*J	3072834	PRAS	11/12/2010	Removed obsolete parts and updated package diagram.
*K	3185812	PRAS	03/02/2011	Updated Features. Updated Functional Description. Updated Selection Guide (Added 8 ns speed grade devices and removed 10 ns, 12 ns, and 15 ns speed grade devices). Removed Figure 36-pin SOJ (Top View) in Pin Configuration. Updated Electrical Characteristics (Added 8 ns speed grade devices and removed 10 ns, 12 ns, and 15 ns speed grade devices). Deleted 36-pin SOJ column in Thermal Resistance. Updated AC Switching Characteristics (Added 8 ns speed grade devices and removed 10 ns, 12 ns, and 15 ns speed grade devices). Added Units of Measure. Dislodged Automotive information to 001-67511. Removed SOJ package related information in all instances in the document.
*L	3250938	PRAS	05/25/11	Updated Functional Description (Removed “For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.”). Updated Selection Guide (Added 10 ns speed grade devices). Updated Electrical Characteristics (Added 10 ns speed grade devices). Updated Note 2 in page 4 as “AC characteristics (except High Z) are tested using the load conditions shown in Figure 2 on page 5 (a). High Z characteristics are tested for all speeds using the test load shown in Figure 2 on page 5 (c)”. Updated Figure 2. Updated Note 4 in page 5 as “AC characteristics (except High Z) are tested using the load conditions shown in Figure 2 (a). High Z characteristics are tested for all speeds using the test load shown in Figure 2 (c)”. Updated AC Switching Characteristics (Added 10 ns speed grade devices). Updated Ordering Information (Included CY7C1049CV33-10ZXI).
*M	3282230	AJU	06/14/2011	Updated in new template.

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