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# SCANSTA111

# Enhanced SCAN Bridge Multidrop Addressable IEEE 1149.1 (JTAG) Port

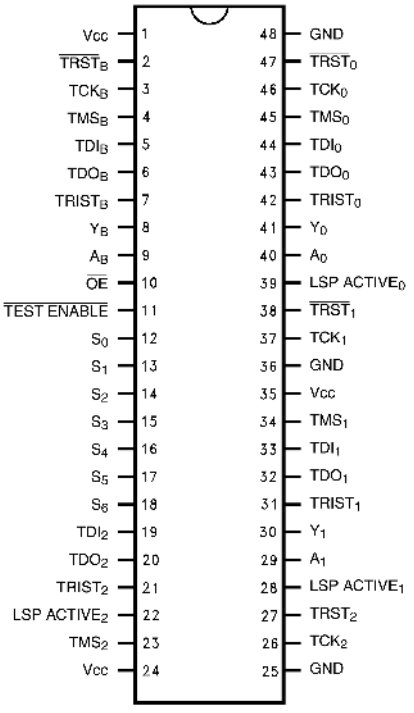
## General Description

The SCANSTA111 extends the IEEE Std. 1149.1 test bus into a multidrop test bus environment. The advantage of a multidrop approach over a single serial scan chain is improved test throughput and the ability to remove a board from the system and retain test access to the remaining modules. Each SCANSTA111 supports up to 3 local IEEE 1149.1 scan rings which can be accessed individually or combined serially. Addressing is accomplished by loading the instruction register with a value matching that of the Slot inputs. Backplane and inter-board testing can easily be accomplished by parking the local TAP Controllers in one of the stable TAP Controller states via a Park instruction. The 32-bit TCK counter enables built in self test operations to be performed on one port while other scan chains are simultaneously tested.

## Features

- True IEEE 1149.1 hierarchical and multidrop addressable capability
- The 7 slot inputs support up to 121 unique addresses, an Interrogation Address, Broadcast Address, and 4 Multicast Group Addresses (address 000000 is reserved)
- 3 IEEE 1149.1-compatible configurable local scan ports
- Mode Register$_0$ allows local TAPs to be bypassed, selected for insertion into the scan chain individually, or serially in groups of two or three
- Transparent Mode can be enabled with a single instruction to conveniently buffer the backplane IEEE 1149.1 pins to those on a single local scan port
- LSP ACTIVE outputs provide local port enable signals for analog busses supporting IEEE 1149.4.
- General purpose local port Pass-through bits are useful for delivering write pulses for FPGA programming or monitoring device status.
- Known Power-up state
- $\overline{\text{TRST}}$ on all local scan ports
- 32-bit TCK counter
- 16-bit LFSR Signature Compactor
- Local TAPs can become TRI-STATE via the $\overline{\text{OE}}$ input to allow an alternate test master to take control of the local TAPs (LSP$_{0\text{-}2}$ have a TRI-STATE notification output)
- 3.0-3.6V $V_{CC}$ Supply Operation
- Power-off high impedance inputs and outputs
- Supports live insertion/withdrawal

## Connection Diagrams

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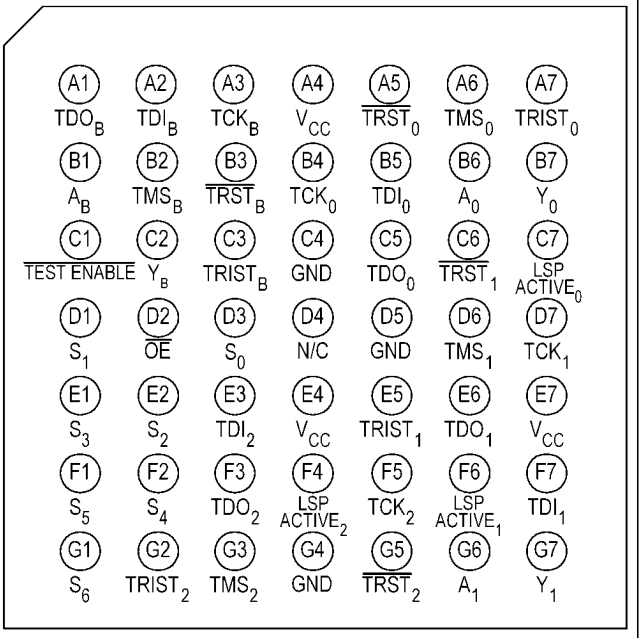


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**TABLE 1. Glossary**

| | |
|---|---|
| LFSR | Linear Feedback Shift Register. When enabled, will generate a 16-bit signature of sampled serial test data. |
| LSP | Local Scan Port. A four signal port that drives a local (i.e. non-backplane) scan chain. (e.g., $TCK_0$, $TMS_0$, $TDO_0$, $TDI_0$). |
| Local | Local is used to describe IEEE Std. 1149.1 compliant scan rings and the SCANSTA111 Test Access Port that drives them. The term local was adopted from the system test architecture that the 'STA111 will most commonly be used in; namely, a system test backplane with a 'STA111 on each card driving up to 3 local scan rings per card. (Each card can contain multiple 'STA111s, with 3 local scan ports per 'STA111.) |
| Park/Unpark/Unparked | Parked, unpark, and unparked, are used to describe the state of the LSP controller and the state of the local TAP controllers (the local TAP controllers refers to the TAP controllers of the scan components that make up a local scan ring). Park is also used to describe the action of parking a LSP (transitioning into one of the Parked LSP controller states). It is important to understand that when a LSP controller is in one of the parked states, $TMS_n$ is held constant, thereby holding or parking the local TAP controllers in a given state. |
| TAP | Test Access Port as defined by IEEE Std. 1149.1. |
| Selected/Unselected | Selected and Unselected refers to the state of the 'STA111 Selection Controller. A selected 'STA111 has been properly addressed and is ready to receive Level 2 protocol. Unselected 'STA111s monitor the system test backplane, but do not accept Level 2 protocol (except for the GOTOWAIT instruction). The data registers and LSPs of unselected 'STA111s are not accessible from the system test master. |
| Active Scan Chain | The Active Scan Chain refers to the scan chain configuration as seen by the test master at a given moment. When a 'STA111 is selected with all of its LSPs parked, the active scan chain is the current scan register only. When a LSP is unparked, the active scan chain becomes: $TDI_B$ → the current 'STA111 register → the local scan ring registers → a PAD bit → $TDO_B$. Refer to Table 7 for Unparked configurations of the LSP network. |
| Level 1 Protocol | Level 1 is the protocol used to address a 'STA111. |
| Level 2 Protocol | Level 2 is the protocol that is used once a 'STA111 is selected. Level 2 protocol is IEEE Std. 1149.1 compliant when an individual 'STA111 is selected. |
| PAD | A one bit register that is placed at the end of each local scan port scan-chain. The PAD bit eliminates the prop delay that would be added by the 'STA111 LSPN logic between $TDI_n$ and $TDO_{(n+1)}$ or $TDO_B$ by buffering and synchronizing the LSP TDI inputs to the falling edge of $TCK_B$, thus allowing data to be scanned at higher frequencies without violating setup and hold times. |
| LSB | Least Significant Bit, the right-most position in a register (bit 0). |
| MSB | Most Significant Bit, the left-most position in a register. |

## Architecture

Figure 1 shows the basic architecture of the 'STA111. The device's major functional blocks are illustrated here. The TAP Controller, a 16-state state machine, is the central control for the device. The instruction register and various test data registers can be scanned to exercise the various functions of the 'STA111 (these registers behave as defined in IEEE Std. 1149.1). The 'STA111 selection controller provides the functionality that allows the 1149.1 protocol to be used in a multidrop environment. It primarily compares the address input to the slot identification and enables the 'STA111 for subsequent scan operations. The Local Scan Port Network (LSPN) contains multiplexing logic used to select different port configurations. The LSPN control block contains the Local Scan Port Controllers (LSPC) for each Local Scan Port ($LSP_0$, $LSP_1$ ... $LSP_n$). This control block receives input from the 'STA111 instruction register, mode registers, and the TAP controller. Each local port contains all four boundary scan signals needed to interface with the local TAPs plus the optional Test Reset signal (TRST).

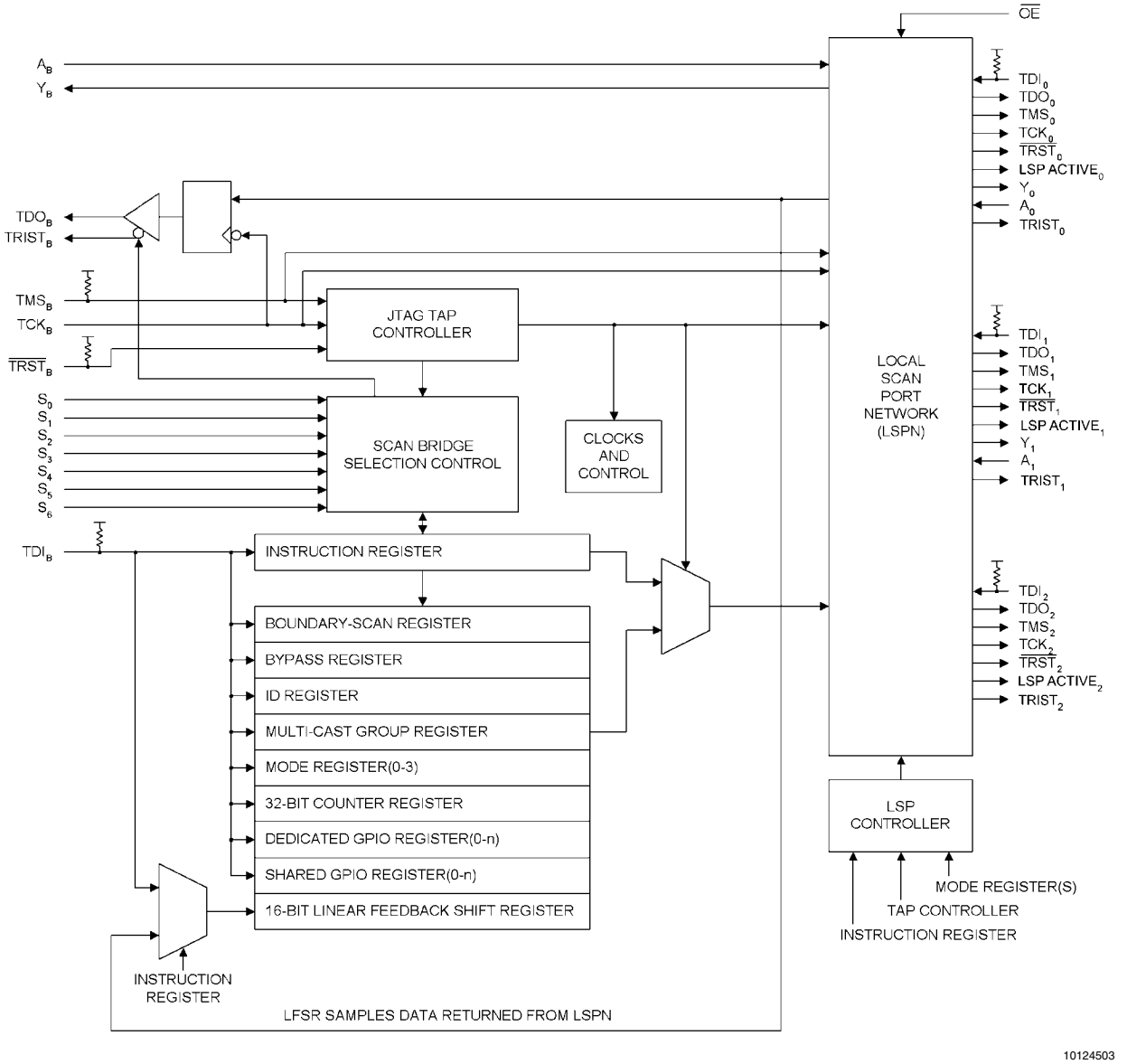


**FIGURE 1. SCANSTA111 Block Diagram**

**TABLE 2. Pin Descriptions**

| Pin Name | No. Pins | I/O | Description |
|---|---|---|---|
| **VCC** | 3 | N/A | Power |
| **GND** | 3 | N/A | Ground |
| **$TMS_B$** | 1 | I | BACKPLANE TEST MODE SELECT: Controls sequencing through the TAP Controller of the 'STA111. Also controls sequencing of the TAPs which are on the local scan chains. This input has a 25KΩ pull-up resistor and no ESD clamp diode (ESD is controlled with an alternate method). When the device is power-off ($V_{DD}$ floating), this input appears to be a capacitive load to ground (Note 1). When $V_{DD}$ = 0V (i.e.; not floating but tied to $V_{SS}$) this input appears to be a capacitive load with the pull-up to ground. |
| **$TDI_B$** | 1 | I | BACKPLANE TEST DATA INPUT: All backplane scan data is supplied to the 'STA111 through this input pin. This input has a 25KΩ pull-up resistor and no ESD clamp diode (ESD is controlled with an alternate method). When the device is power-off ($V_{DD}$ floating), this input appears to be a capacitive load to ground (Note 1). When $V_{DD}$ = 0V (i.e.; not floating but tied to $V_{SS}$) this input appears to be a capacitive load with the pull-up to ground. |
| **$TDO_B$** | 1 | O | BACKPLANE TEST DATA OUTPUT: This output drives test data from the 'STA111 and the local TAPs, back toward the scan master controller. This output has 24mA of drive current. When the device is power-off ($V_{DD}$ = 0V or floating), this output appears to be a capacitive load (Note 1). |
| **$TCK_B$** | 1 | I | TEST CLOCK INPUT FROM THE BACKPLANE: This is the master clock signal that controls all scan operations of the 'STA111 and of the local scan ports. This input has no pull-up resistor and no ESD clamp diode (ESD is controlled with an alternate method). When the device is power-off ($V_{DD}$ floating), this input appears to be a capacitive load to ground (Note 1). When $V_{DD}$ = 0V (i.e.; not floating but tied to $V_{SS}$) this input appears to be a capacitive load to ground. |
| **$\overline{TRST}_B$** | 1 | I | TEST RESET: An asynchronous reset signal (active low) which initializes the 'STA111 logic. This input has a 25KΩ pull-up resistor and no ESD clamp diode (ESD is controlled with an alternate method). When the device is power-off ($V_{DD}$ floating), this input appears to be a capacitive load to ground (Note 1). When $V_{DD}$ = 0V (i.e.; not floating but tied to $V_{SS}$) this input appears to be a capacitive load with the pull-up to ground. |
| **$TRIST_{(B,0-2)}$** | 4 | O | TRI-STATE NOTIFICATION OUTPUT: This signal is asserted high when the associated TDO is TRI-STATEd. Associated means $TRIST_B$ is for $TDO_B$, $TRIST_1$ is for $TDO_1$, etc. This output has 12mA of drive current. |
| **$A_B$** | 1 | I | BACKPLANE PASS-THROUGH INPUT: A general purpose input which is driven to the $Y_n$ of a single selected LSP. (Not available when multiple LSPs are selected). This input has an internal pull-up resistor. |
| **$Y_B$** | 1 | O | BACKPLANE PASS-THROUGH OUTPUT: A general purpose output which is driven from the $A_n$ of a single selected LSP. (Not available when multiple LSPs are selected). This output has 24mA of drive current. |
| **$S_{(0-6)}$** | 7 | I | SLOT IDENTIFICATION: The configuration of these pins is used to identify (assign a unique address to) each 'STA111 on the system backplane . |
| **$\overline{OE}$** | 1 | I | OUTPUT ENABLE for the Local Scan Ports, active low. When high, this active-low control signal TRI-STATEs all local scan ports on the 'STA111, to enable an alternate resource to access one or more of the three local scan chains. |
| **$TDO_{(0-2)}$** | 3 | O | TEST DATA OUTPUTS: Individual output for each of the local scan ports . These outputs have 24mA of drive current. |
| **$TDI_{(0-2)}$** | 3 | I | TEST DATA INPUTS: Individual scan data input for each of the local scan ports . |
| **$TMS_{(0-2)}$** | 3 | O | TEST MODE SELECT OUTPUTS: Individual output for each of the local scan ports. $TMS_n$ does not provide a pull-up resistor (which is assumed to be present on a connected TMS input, per the IEEE 1149.1 requirement) . These outputs have 24mA of drive current. |
| **$TCK_{(0-2)}$** | 3 | O | LOCAL TEST CLOCK OUTPUTS: Individual output for each of the local scan ports. These are buffered versions of $TCK_B$ . These outputs have 24mA of drive current. |
| **$\overline{TRST}_{(0-2)}$** | 3 | O | LOCAL TEST RESETS: A gated version of $\overline{TRST}_B$ . These outputs have 24mA of drive current. |

| Pin Name | No. Pins | I/O | Description |
|---|---|---|---|
| $A_{(0-1)}$ | 2 | I | LOCAL PASS-THROUGH INPUTS: General purpose inputs which can be driven to the backplane pin $Y_B$. (Only on $LSP_0$ and $LSP_1$. Only available when a single LSP is selected) . These inputs have an internal pull-up resistor. |
| $Y_{(0-1)}$ | 2 | O | LOCAL PASS-THROUGH OUTPUT: General purpose outputs which can be driven from the backplane pin $A_B$. (Only on $LSP_0$ and $LSP_1$. Only available when a single LSP is selected) . These outputs have 24mA of drive current. |
| $LSP\_ACTIVE_{(0-2)}$ | 3 | O | LOCAL ANALOG TEST BUS ENABLE: These analog pins serve as enable signals for analog busses supporting the IEEE 1149.4 Mixed-Signal Test Bus standard , or for backplane physical layer changes (i.e.; TTL to LVDS). These outputs have 12mA of drive current. |
| $TRIST_{(0-2)}$ | 3 | O | LOCAL TRI-STATE NOTIFICATION OUTPUTS: This signal is high when the local scan ports are TRI-STATEd . These pins are used for backplane physical layer changes (i.e.; TTL to LVDS). These outputs have 12mA of drive current. |
| $\overline{\text{TEST ENABLE}}$ | 1 | I | TEST ENABLE INPUT: This pin is used for factory test and should be tied to $V_{CC}$ for normal operation. |

**Note 1:** Refer to the IBIS model on our website for I/O characteristics.

## Application Overview

**ADDRESSING SCHEME** - The SCANSTA111 architecture extends the functionality of the IEEE 1149.1 Standard by supplementing that protocol with an addressing scheme which allows a test controller to communicate with specific 'STA111s within a network of 'STA111s. That network can include both multi-drop and hierarchical connectivity. In effect, the 'STA111 architecture allows a test controller to dynamically select specific portions of such a network for participation in scan operations. This allows a complex system to be partitioned into smaller blocks for testing purposes. The 'STA111 provides two levels of test-network partitioning capability. First, a test controller can select individual 'STA111s, specific sets of 'STA111s (multi-cast groups), or all 'STA111s (broadcast). This 'STA111-selection process is supported by a Level-1 communication protocol. Second, within each selected 'STA111, a test controller can select one or more of the chip's three local scan-ports. That is, individual local ports can be selected for inclusion in the (single) scan-chain which a 'STA111 presents to the test controller. This mechanism allows a controller to select specific terminal scan-chains within the overall scan network. The port-selection process is supported by a Level-2 protocol.

**HIERARCHICAL SUPPORT** - Multiple SCANSTA111's can be used to assemble a hierarchical boundary-scan tree. In such a configuration, the system tester can configure the local ports of a set of 'STA111s so as to connect a specific set of local scan-chains to the active scan chain. Using this capability, the tester can selectively communicate with specific portions of a target system. The tester's scan port is connected to the backplane scan port of a root layer of 'STA111s, each of which can be selected using multi-drop addressing. A second tier of 'STA111s can be connected to this root layer, by connecting a local port (LSP) of a root-layer 'STA111 to the backplane port of a second-tier 'STA111. This process can be continued to construct a multi-level scan hierarchy. 'STA111 local ports which are not cascaded into higher-level 'STA111s can be thought of as the terminal leaves of a scan tree. The test master can select one or more target leaves by selecting and configuring the local ports of an appropriate set of 'STA111s in the test tree.

Check with your ATPG tool vendor to ensure support of this feature.

## State Machines

The 'STA111 is IEEE 1149.1-compatible, in that it supports all required 1149.1 operations. In addition, it supports a higher level of protocol, (Level 1), that extends the IEEE 1149.1 Std. to a multi-drop environment.

In multi-drop scan systems, a scan tester can select individual 'STA111s for participation in upcoming scan operations. STA111 selection is accomplished by simultaneously scanning a device address out to multiple 'STA111s. Through an on-chip address matching process, only those 'STA111s whose statically-assigned address matches the scanned-out address become selected to receive further instructions from the scan tester. SCANSTA111 selection is done using a Level-1 protocol, while follow-on instructions are sent to selected 'STA111s by using a Level-2 protocol.

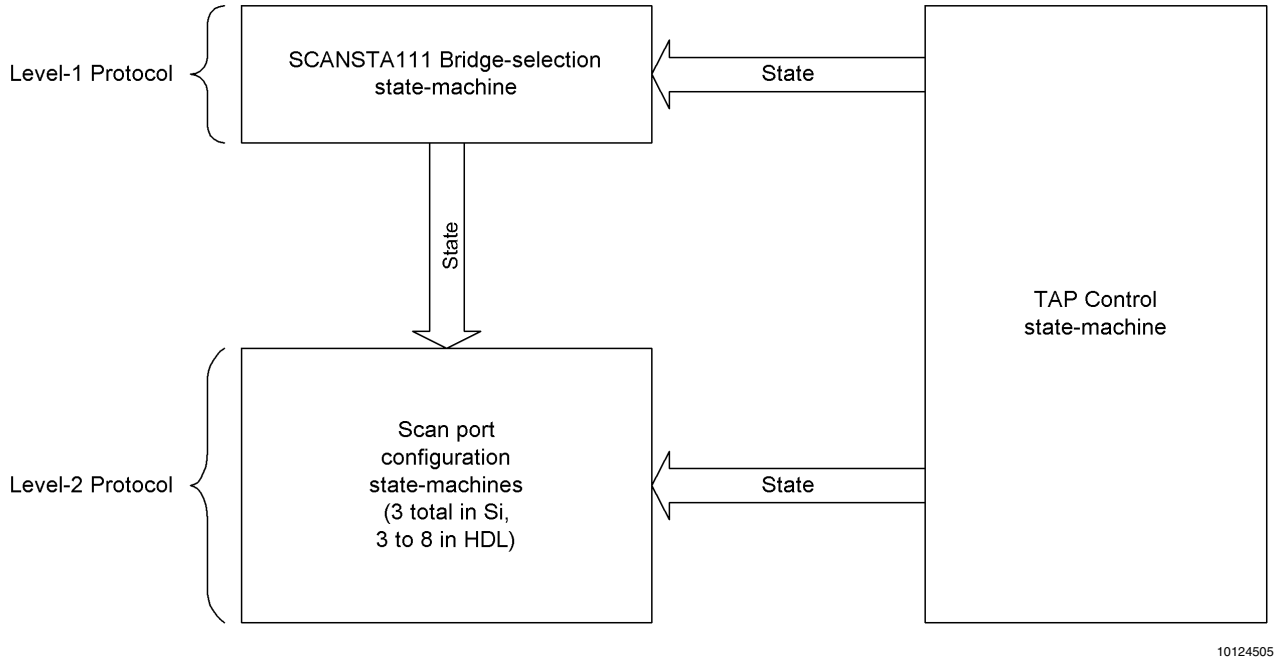


**FIGURE 2. SCANSTA111 State Machines**

The 'STA111 contains three distinct but coupled state-machines (see Figure 2). The first of these is the TAP-control state-machine, which is used to drive the 'STA111's scan ports in conformance with the 1149.1 Standard. The second is the 'STA111-selection state-machine (Figure 3). The third state-machine actually consists of three identical but independent state-machines (see Figure 4), one per 'STA111 local scan port. Each of these scan port selection state-machines allows individual local ports to be inserted into and removed from the 'STA111s overall scan chain.

The 'STA111 selection state-machine performs the address matching which gives the 'STA111 its multi-drop capability. That logic supports single-'STA111 access, multi-cast, and broadcast. The 'STA111-selection state-machine implements the chip's Level-1 protocol.

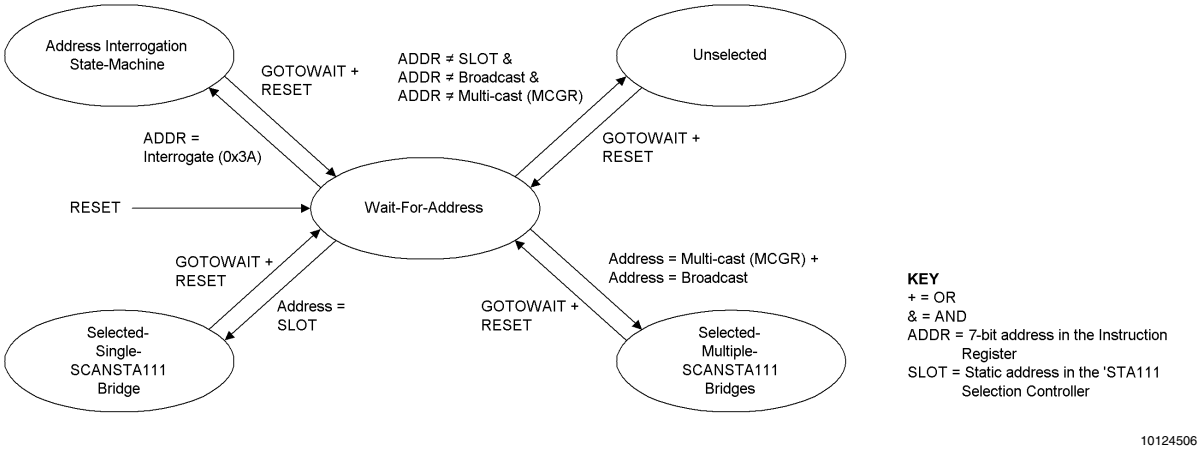


**FIGURE 3. State Machine for SCANSTA111 Selection Controller**

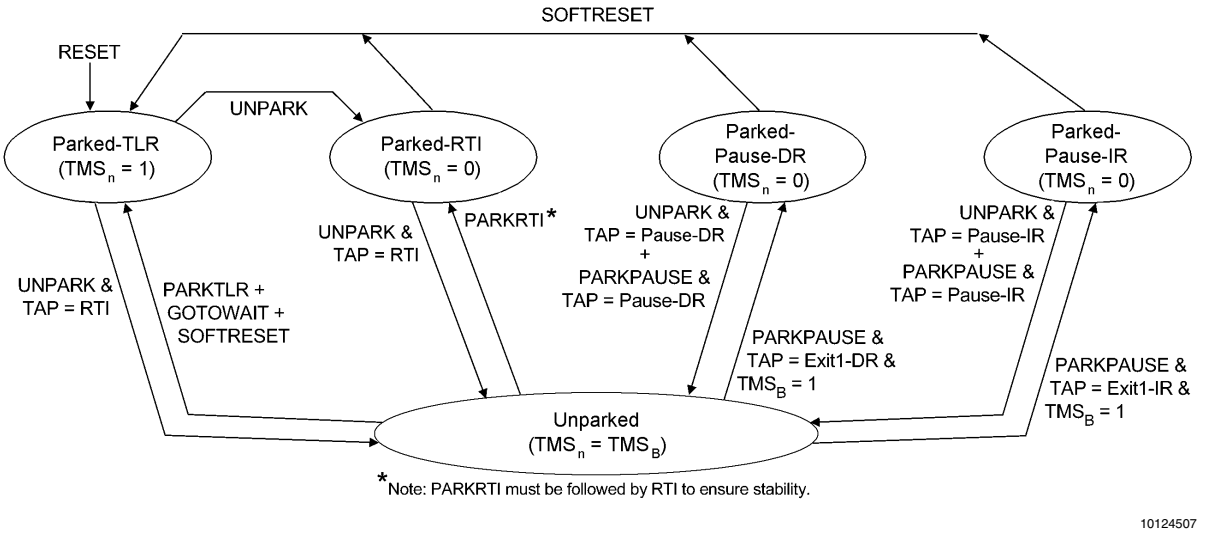


**FIGURE 4. Local SCANSTA111 Port Configuration State Machine**

The 'STA111's scan port-configuration state-machine is used to control the insertion of local scan ports into the overall scan chain, or the isolation of local ports from the chain. From the perspective of a system's (single) scan controller, each 'STA111 presents only one scan chain to the master. The 'STA111 architecture allows one or more of the 'STA111's local ports to be included in the active scan chain.

Each local port can be parked in one of four stable states (Parked-TLR, Parked-RTI, Parked-Pause-DR or Parked-Pause-IR), either individually or simultaneously with other local ports. Parking a chain removes that local chain from the active scan chain. Conversely, a parked chain can be unparked, causing the corresponding local port to be inserted into the active scan chain.

As shown in Figure 4, the 'STA111's three scan port-configuration state-machines allow each of the part's local ports to occupy a different state at any given time. For example, some ports may be parked, perhaps in different states, while other ports participate in scan operations. The state-diagram shows that some state transitions depend on the current state of the TAP-control state-machine. As an example, a local port which is presently in the Parked-RTI state does not become unparked (i.e., enter the Unparked state) until the 'STA111 receives an UNPARK instruction and the 'STA111's TAP state-machine enters the Run-Test/Idle state.

Similarly, certain transitions of the scan port-configuration state-machine can force the 'STA111's LSP-control state-machine into specific states. For example, when a local port is in the Unparked state, the 'STA111 receives the PARKRTI instruction and the TAP is transitioned through Run-Test/Idle state, the Local Port controller enters the Parked-RTI state in which $TMS_n$ will be held low until the port is later unparked.

Once the Park-RTI instruction has been updated into the instruction register the TAP MUST be transitioned through the Run-Test/Idle state. While $TMS_n$ is held low, all devices on that local scan chain remain in their current TAP State (the RTI TAP controller state in this example).

The 'STA111's scan port-configuration state-machine implements part of the 'STA111's Level-2 protocol. In addition, the 'STA111 provides a number of Level-2 instructions for functions other than local scan port configuration. These instructions provide access to and control of various registers within the 'STA111. This set of instructions includes:

| | |
|---|---|
| BYPASS | CNTRSEL |
| EXTEST | LFSRON |
| SAMPLE/PRELOAD | LFSROFF |
| IDCODE | CNTRON |
| MODESEL | CNTROFF |
| MCGRSEL | GOTOWAIT |
| LFSRSEL | |

Figure 5 illustrates how the 'STA111's state-machines interact. The 'STA111-selection state-machine enables or disables operation of the chip's three port-selection state-machines. In 'STA111s which are selected via Level-1 protocol (either as individual 'STA111s or as members of broadcast or multi-cast groups), Level-2 protocol commands can be used to park or unpark local scan ports. Note that most transitions of the port-configuration state-machines are gated by particular states of the 'STA111's TAP-control state-machine, as shown in Figure 4 or Figure 5.

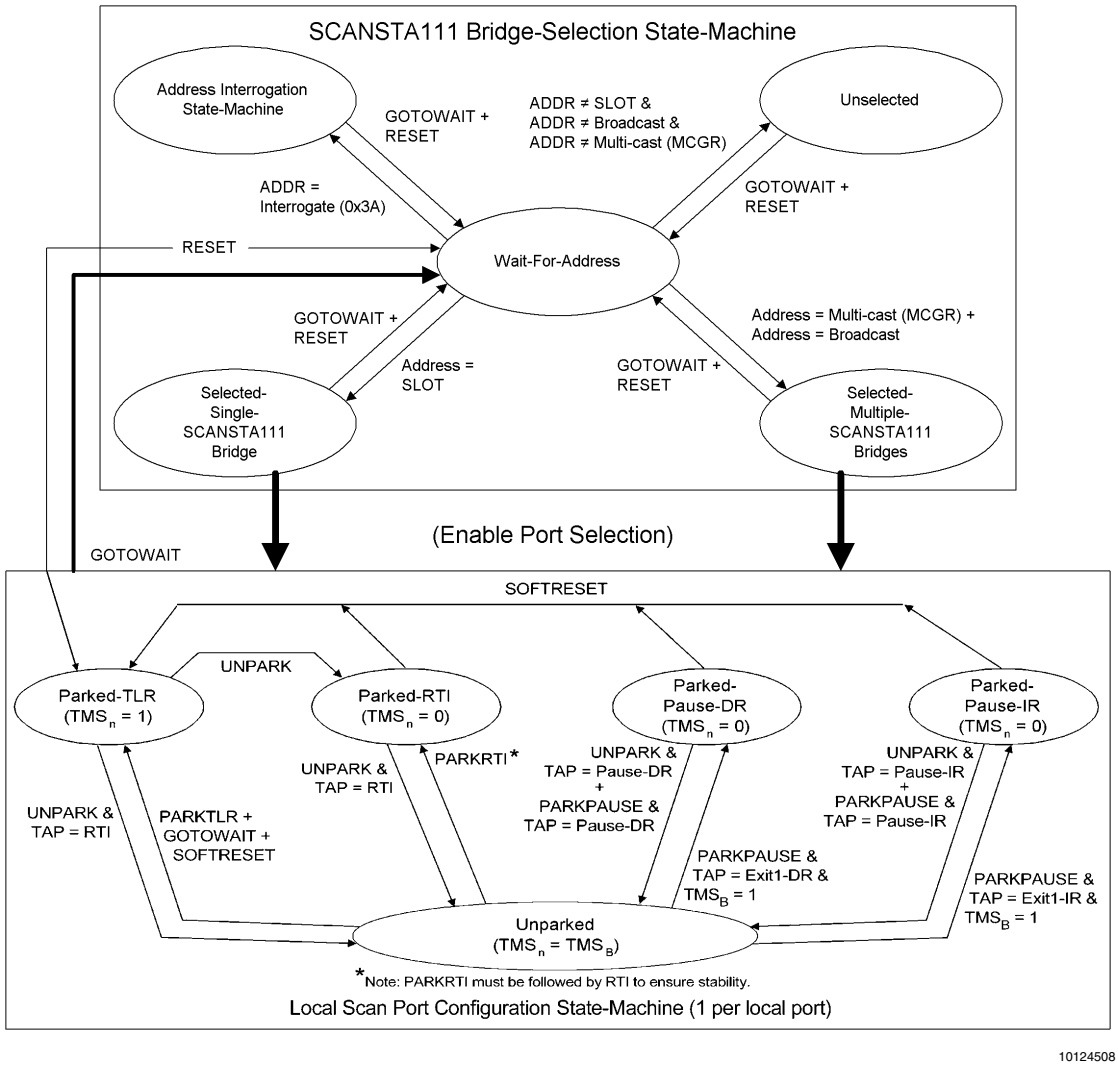


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**FIGURE 5. Relationship Between SCANSTA111 State Machines**

Following a hardware reset, the TAP controller state-machine is in the Test-Logic-Reset (TLR) state; the 'STA111-selection state-machine is in the Wait-For-Address state; and each of the three port-selection state-machines is in the Parked-TLR state. The 'STA111 is then ready to receive Level-1 protocol, followed by Level-2 protocol.

## Tester/SCANSTA111 Interface

An IEEE 1149.1 system tester sends instructions to a 'STA111 via that 'STA111's backplane scan-port. Following test logic reset, the 'STA111's selection state-machine is in the Wait-For-Address state. When the 'STA111's TAP controller is sequenced to the Shift-IR state, data shifted in through the $TDI_B$ input is shifted into the 'STA111's instruction register. Note that prior to successful selection of a 'STA111, data is not shifted out of the instruction register and out through the 'STA111's $TDO_B$ output, as it is during normal scan operations. Instead, as each new bit enters the instruction register's most-significant bit, data shifted out from the least-significant bit is discarded.

When the instruction register is updated with the address data, the 'STA111's address-recognition logic compares the seven least-significant bits of the instruction register with the 7-bit assigned address which is statically present on the $S_{(0\text{-}6)}$ inputs. Simultaneously, the scanned-in address is compared with the reserved Broadcast and Multi-cast addresses. If an address match is detected, the 'STA111-selection state-machine enters one of the two selected states. If the scanned address does not match a valid single-slot address or one of the reserved broadcast/multi-cast addresses, the 'STA111-selection state-machine enters the Unselected state.

Note that the SLOT inputs should not be set to a value corresponding to a multi-cast group, or to the broadcast address. Also note that the single 'STA111 selection process must be performed for all 'STA111s which are subsequently to be addressed in multi-cast mode. This is required because each such device's Multicast Group Register (MCGR) must be programmed with a multi-cast group number, and the MCGR is not accessible to the test controller until that 'STA111 has first entered the Selected-Single-'STA111 state.

Once a 'STA111 has been selected, Level-2 protocol is used to issue commands and to access the chip's various registers.

## Register Set

The SCANSTA111 includes a number of registers which are used for 'STA111 selection and configuration, scan data manipulation, and scan-support operations. These registers can be grouped as shown in Table 3.

The specific fields and functions of each of these registers are detailed in the section of this document titled Data Register Descriptions.

Note that when any of these registers is selected for insertion into the 'STA111's scan-chain, scan data enters through that register's most-significant bit. Similarly, data that is shifted out of the register is fed to the scan input of the next-downstream device in the scan-chain.

**TABLE 3. Register Descriptions**

| Register Name | BSDL Name | Description |
|---|---|---|
| Instruction Register | INSTRUCTION | 'STA111 addressing and instruction-decode IEEE Std. 1149.1 required register |
| Boundary-Scan Register | BOUNDARY | IEEE Std. 1149.1 required register |
| Bypass Register | BYPASS | IEEE Std. 1149.1 required register |
| Device Identification Register | IDCODE | IEEE Std. 1149.1 optional register |
| Multi-Cast Group Register | MCGR | 'STA111-group address assignment |
| Mode Register$_0$ | MODE | 'STA111 local-port configuration and control bits |
| Mode Register$_1$ | N/A | 'STA111 local-port configuration and control bits (Note 2, Note 3) |
| Mode Register$_2$ | MODE2 | 'STA111 Shared GPIO configuration bits |
| Linear-Feedback Shift Register | LFSR | 'STA111 scan-data compaction (signature generation) |
| TCK Counter Register | CNTR | Local-port TCK clock-gating (for BIST) |
| Dedicated GPIO Register$_{(0\text{-}n)}$ | N/A | 'STA111 Dedicated GPIO control bits (Note 3) |
| Shared GPIO Register$_{(0\text{-}n)}$ | SGPIOn | 'STA111 Shared GPIO control bits |

**Note 2:** One dedicated and one shared GPIO register exists for each LSP that supports dedicated and/or shared GPIO (maximum of eight shared and eight dedicated GPIO registers).

**Note 3:** HDL version only

# Level 1 Protocol (Addressing Modes)

**TABLE 4. SCANSTA111 Address Modes**

| Address Type | Hex Address | Binary Address | $TDO_B$ State |
|---|---|---|---|
| Direct Address | 00 to 39,<br>40 to 7F.<br>(80 to FF (Note 4)) | 00000000 to 00111010<br>01000000 to 01111111<br>(10000000 to 11111111(Note 4)) | Normal IEEE Std. 1149.1 |
| Interrogation Address | 3A | 00111010 | Force strong 0' or weak 1' as ones-complement address is shifted out. |
| Broadcast Address | 3B | 00111011 | Always TRI-STATED |
| Multi-Cast Group 0 | 3C | 00111100 | Always TRI-STATED |
| Multi-Cast Group 1 | 3D | 00111101 | Always TRI-STATED |
| Multi-Cast Group 2 | 3E | 00111110 | Always TRI-STATED |
| Multi-Cast Group 3 | 3F | 00111111 | Always TRI-STATED |

**Note 4:** Hex addresses 80' to FF' are only available when using the eighth address bit in the HDL version of the SCANSTA111. The Silicon part has seven address lines and will treat the most-significant address bit as a don't care.

The SCANSTA111 supports single and multiple modes of addressing a 'STA111. The single mode selects one 'STA111 and is called Direct Addressing. More than one 'STA111 device can be selected via the Broadcast and Multi-Cast Addressing modes.

**DIRECT ADDRESSING:** The 'STA111 enters the Wait-For-Address state when:

1. its TAP Controller enters the Test-Logic-Reset state, or
2. its instruction register is updated with the GOTOWAIT instruction (while either selected or unselected).

Each 'STA111 within a scan network must be statically configured with a unique address via its $S_{(0-6)}$ inputs. While the 'STA111 controller is in the Wait-For-Address state, data shifted into bits 6 through 0 of the instruction register is compared with the address present on the $S_{(0-6)}$ inputs in the Update-IR state. If the seven (7) LSBs of the instruction register match the address on the $S_{(0-6)}$ inputs, (see Figure 6) the 'STA111 becomes selected, and is ready to receive Level 2 Protocol (i.e., further instructions). When the 'STA111 is selected, its device identification register is inserted into the active scan chain.

All 'STA111s whose $S_{(0-6)}$ address does not match the instruction register address become unselected. An unselected 'STA111 will remain unselected until either its TAP Controller enters the Test-Logic-Reset state, or its instruction register is updated with the GOTOWAIT instruction.

**BROADCAST ADDRESSING:**

The Broadcast Address allows a tester to simultaneously select all 'STA111s in a test network. This mode is useful in testing systems which contain multiple identical boards. To avoid bus contention between scan-path output drivers on different boards, each 'STA111's $TDO_B$ buffer is always TRI-STATEd while in Broadcast mode. In this configuration, the on-chip Linear Feedback Shift Register (LFSR) can be used to accumulate a test result signature for each board that can be read back later by direct-addressing each board's 'STA111.

**MULTICAST ADDRESSING:**

As a way to make the broadcast mechanism more selective, the 'STA111 provides a Multi-cast addressing mode. A 'STA111's multi-cast group register (MCGR) can be programmed to assign that 'STA111 to one of four (4) Multi-Cast groups. When 'STA111s in the Wait-For-Address state are updated with a Multi-Cast address, all 'STA111s whose MCGR matches the Multi-Cast group will become selected. As in Broadcast mode, $TDO_B$ is always TRI-STATEd while in Multicast mode.

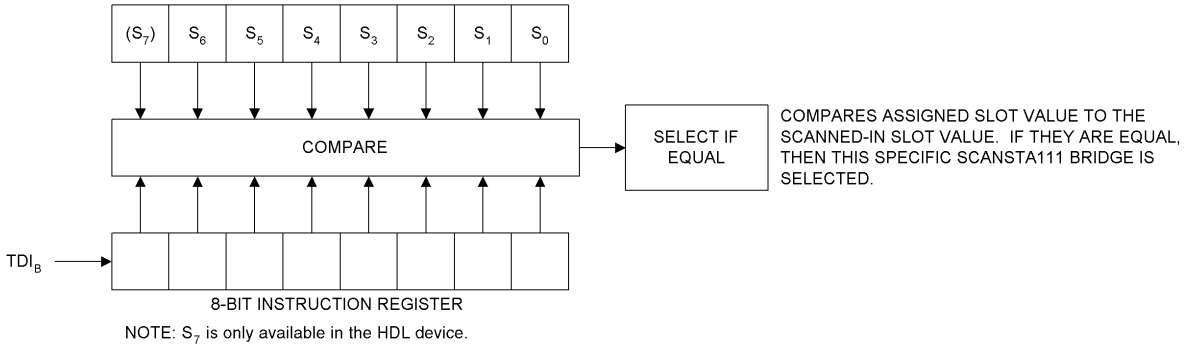



**FIGURE 6. Direct Addressing: Device Address Loaded into Instruction Register**

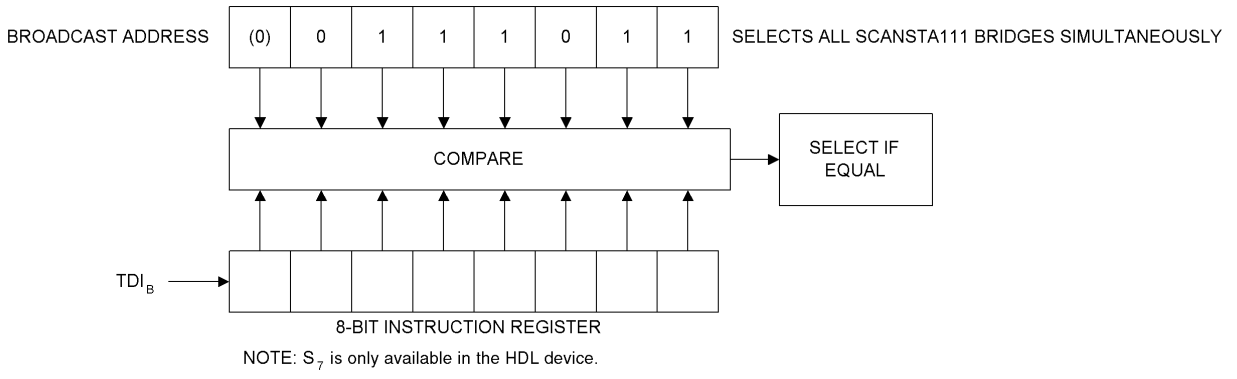



**FIGURE 7. Broadcast Addressing: Address Loaded into Instruction Register**

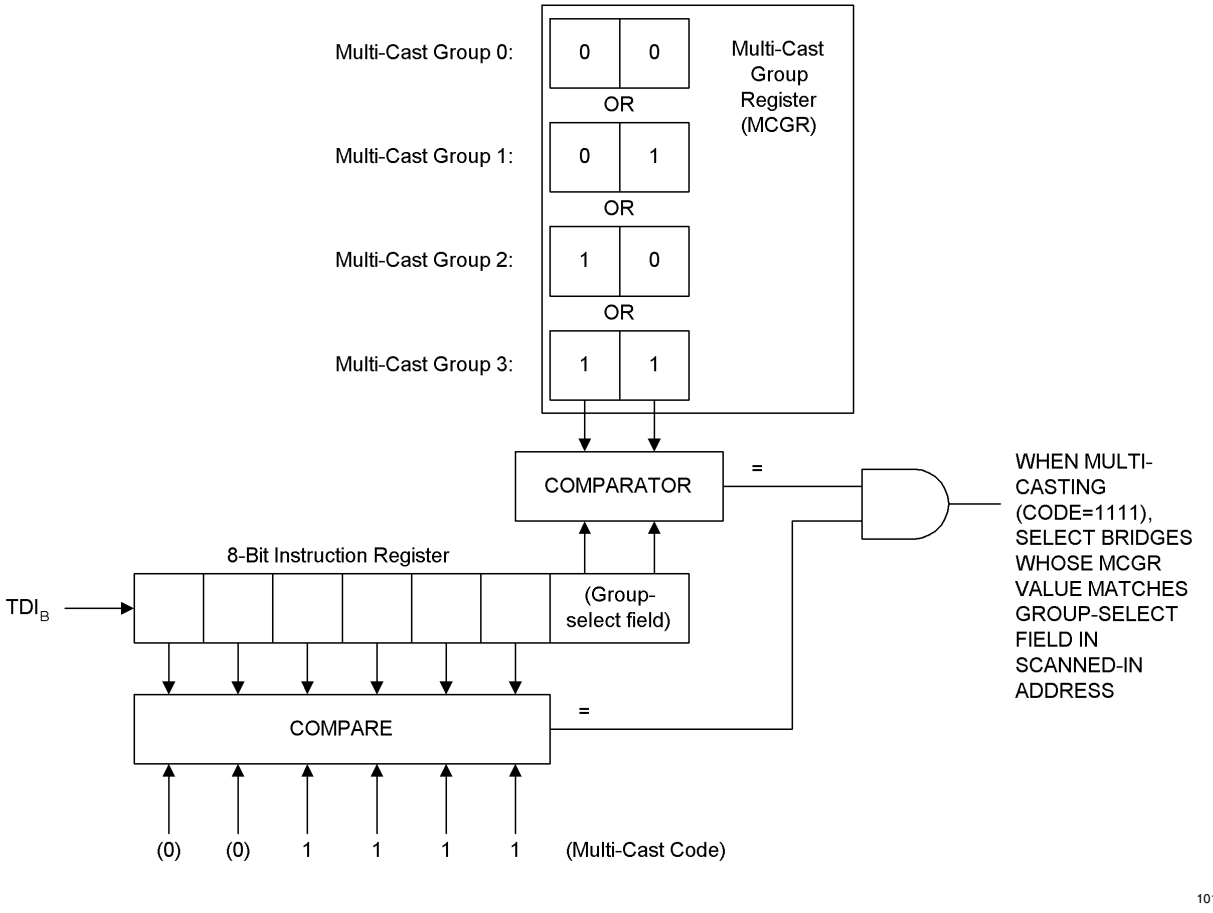



**FIGURE 8. Multi-Cast Addressing: Address Loaded into Instruction Register**

## Level 2 Protocol

Once the SCANSTA111 has been successfully addressed and selected, its internal registers may be accessed via Level-2 Protocol. Level-2 Protocol is compliant to IEEE Std. 1149.1 TAP protocol with one exception: if the 'STA111 is selected via the Broadcast or Multi-Cast address, $TDO_B$ is always TRI-STATED. (The $TDO_B$ buffer must be implemented this way to prevent bus contention.) Upon being selected, (i.e., the 'STA111 Selection controller transitions from the Wait-For-Address state to one of the Selected states), each of the local scan ports ($LSP_0$ , $LSP_1$ , $LSP_2$) remains parked in one of the following four TAP Controller states: Test-Logic-Reset, Run-Test/Idle, Pause-DR, or Pause-IR and the active scan chain consists of: $TDI_B$ through the instruction register (or the IDCODE register) and out through $TDO_B$.

$TDI_B \rightarrow$ Instruction Register $\rightarrow TDO_B$

The UNPARK instruction (described later) is used to insert one or more local scan ports into the active scan chain. Table 7 describes which local ports are inserted into the chain, and in what order.

**LEVEL 2 INSTRUCTION TYPES** There are two types of instructions (reference Table 5):

1. Instructions that insert a 'STA111 register into the active scan chain so that the register can be captured or updated (BYPASS, SAMPLE/PRELOAD, EXTEST, IDCODE, MODESEL, MCGRSEL, LFSR-SEL, CNTRSEL).
2. Instructions that configure local ports or control the operation of the linear feedback shift register and counter registers (UNPARK, PARKTRL, PARKRTI, PARK-PAUSE, GOTOWAIT, SOFTRESET, LFSRON, LFSROFF, CNTRON, CNTROFF). These instructions, along with any other yet undefined Op-Codes, will cause the device identification register to be inserted into the active scan chain.

**TABLE 5. Level 2 Protocol and Op-Codes**

| Instructions | Hex Op-Code | Binary Op-Code | Data Register |
|---|---|---|---|
| BYPASS | FF | 1111 1111 | Bypass Register |
| EXTEST | 00 | 0000 0000 | Boundary-Scan Register |
| SAMPLE/PRELOAD | 81 | 1000 0001 | Boundary-Scan Register |
| IDCODE | AA | 1010 1010 | Device Identification Register |
| UNPARK | E7 | 1110 0111 | Device Identification Register |
| PARKTLR | C5 | 1100 0101 | Device Identification Register |
| PARKRTI | 84 | 1000 0100 | Device Identification Register |
| PARKPAUSE | C6 | 1100 0110 | Device Identification Register |
| GOTOWAIT (Note 5) | C3 | 1100 0011 | Device Identification Register |
| MODESEL | 8E | 1000 1110 | Mode Register$_0$ |
| MODESEL$_1$ | 82 | 1000 0010 | Mode Register$_1$ |
| MODESEL$_2$ | 83 | 1000 0011 | Mode Register$_2$ |
| MODESEL$_3$ | 85 | 1000 0101 | Mode Register$_3$ |
| MCGRSEL | 03 | 0000 0011 | Multi-Cast Group Register |
| SOFTRESET | 88 | 1000 1000 | Device Identification Register |
| LFSRSEL | C9 | 1100 1001 | Linear Feedback Shift Register |
| LFSRON | 0C | 0000 1100 | Device Identification Register |
| LFSROFF | 8D | 1000 1101 | Device Identification Register |
| CNTRSEL | CE | 1100 1110 | 32-Bit TCK Counter Register |
| CNTRON | 0F | 0000 1111 | Device Identification Register |
| CNTROFF | 90 | 1001 0000 | Device Identification Register |
| DEFAULT_BYPASS (Note 6) | 07 | 0000 0111 | Set Bypass_reg as default data register |
| TRANSPARENT0 | A0 | 1010 0000 | Transparent Enable Register$_0$ |
| TRANSPARENT1 | A1 | 1010 0001 | Transparent Enable Register$_1$ |
| TRANSPARENT2 | A2 | 1010 0010 | Transparent Enable Register$_2$ |
| TRANSPARENT3 | A3 | 1010 0011 | Transparent Enable Register$_3$ |
| TRANSPARENT4 | A4 | 1010 0100 | Transparent Enable Register$_4$ |
| TRANSPARENT5 | A5 | 1010 0101 | Transparent Enable Register$_5$ |
| TRANSPARENT6 | A6 | 1010 0110 | Transparent Enable Register$_6$ |
| TRANSPARENT7 | A7 | 1010 0111 | Transparent Enable Register$_7$ |
| DGPIO$_0$ | B0 | 1011 0000 | Dedicated GPIO Register$_0$ |
| DGPIO$_1$ | B1 | 1011 0001 | Dedicated GPIO Register$_1$ |
| DGPIO$_2$ | B2 | 1011 0010 | Dedicated GPIO Register$_2$ |
| DGPIO$_3$ | B3 | 1011 0011 | Dedicated GPIO Register$_3$ |

| Instructions | Hex Op-Code | Binary Op-Code | Data Register |
|---|---|---|---|
| $DGPIO_4$ | B4 | 1011 0100 | Dedicated GPIO $Register_4$ |
| $DGPIO_5$ | B5 | 1011 0101 | Dedicated GPIO $Register_5$ |
| $DGPIO_6$ | B6 | 1011 0110 | Dedicated GPIO $Register_6$ |
| $DGPIO_7$ | B7 | 1011 0111 | Dedicated GPIO $Register_7$ |
| $SGPIO_0$ | B8 | 1011 1000 | Shared GPIO $Register_0$ |
| $SGPIO_1$ | B9 | 1011 1001 | Shared GPIO $Register_1$ |
| $SGPIO_2$ | BA | 1011 1010 | Shared GPIO $Register_2$ |
| $SGPIO_3$ | BB | 1011 1011 | Shared GPIO $Register_3$ |
| $SGPIO_4$ | BC | 1011 1100 | Shared GPIO $Register_4$ |
| $SGPIO_5$ | BD | 1011 1101 | Shared GPIO $Register_5$ |
| $SGPIO_6$ | BE | 1011 1110 | Shared GPIO $Register_6$ |
| $SGPIO_7$ | BF | 1011 1111 | Shared GPIO $Register_7$ |
| Other Undefined | TBD | TBD | Device Identification Register |

**Note 5:** All other instructions act on selected 'STA111s only.

**Note 6:** Commands added to HDL version of 'STA111.

**LEVEL 2 INSTRUCTON DESCRIPTIONS:**

**BYPASS:** The BYPASS instruction selects the bypass register for insertion into the active scan chain when the 'STA111 is selected.

**EXTEST:** The EXTEST instruction selects the boundary-scan register for insertion into the active scan chain. The boundary-scan register consists of seven sample only shift cells connected to the $S_{(0\text{-}6)}$ and $\overline{OE}$ inputs. On the 'STA111, the EXTEST instruction performs the same function as the SAMPLE/PRELOAD instruction, since there aren't any scannable outputs on the device.

**SAMPLE/PRELOAD:** The SAMPLE/PRELOAD instruction selects the boundary-scan register for insertion into the active scan chain. The boundary-scan register consists of seven sample only shift cells connected to the $S_{(0\text{-}6)}$ and $\overline{OE}$ inputs.

**IDCODE:** The IDCODE instruction selects the device identification register for insertion into the active scan chain. When IDCODE is the current active instruction the device identification 0FC0F01F Hex is captured upon exiting the Capture-DR state.

**UNPARK:** This instruction unparks the Local Scan Port Network and inserts it into the active scan chain as configured by Mode $Register_0$ (and Mode $Register_1$ in the HDL) (see Table 7). Unparked LSPs are sequenced synchronously with the 'STA111's TAP controller. When a LSP has been parked in the Test-Logic-Reset or Run-Test/Idle state, it will not become unparked until the 'STA111's TAP Controller enters the Run-Test/Idle state following the UNPARK instruction. An LSP which has been parked in Test-Logic-Reset will be parked in Run-Test/Idle upon update of an UNPARK instruction. If an LSP has been parked in one of the stable pause states (Pause-DR or Pause-IR), it will not become unparked until the 'STA111's TAP Controller enters the respective pause state. (See Figure 9, Figure 10, Figure 11, and Figure 12).

**PARKTLR:** This instruction causes all unparked LSPs to be parked in the Test-Logic-Reset TAP controller state and removes the LSP network from the active scan chain. The LSP controllers keep the LSPs parked in the Test-Logic-Reset state by forcing their respective $TMS_n$ output with a constant logic 1 while the LSP controller is in the Parked-TLR state (see Figure 4).

**PARKRTI:** This instruction causes all unparked LSPs to be parked in the Run-Test/Idle state. The update of the PARKRTI instruction MUST immediately be followed by a $TMS_B$=0 (to enter the RTI state) in order to assure stability. When a $LSP_n$ is active (unparked), its $TMS_n$ signals follow $TMS_B$ and the $LSP_n$ controller state transitions are synchronized with the TAP Controller state transitions of the 'STA111. When the instruction register is updated with the PARKRTI instruction, $TMS_n$ will be forced to a constant logic 0, causing the unparked local TAP Controllers to be parked in the Run-Test/Idle state. When an $LSP_n$ is parked, it is removed from the active scan chain.

**PARKPAUSE:** The PARKPAUSE instruction has dual functionality. It can be used to park unparked LSPs or to unpark parked LSPs. The instruction places all unparked LSPs in one of the TAP Controller pause states. A local port does not become parked until the 'STA111's TAP Controller is sequenced through Exit1-DR/IR into the Update-DR/IR state. When the 'STA111 TAP Controller is in the Exit1-DR or Exit1-IR state and TMSB is high, the LSP controller forces a constant logic 0 onto TMSL thereby parking the port in the Pause-DR or Pause-IR state respectively (see Figure 4). Another instruction can then be loaded to reconfigure the local ports or to deselect the 'STA111 (i.e., MODESEL, GOTOWAIT, etc.).

If the PARKPAUSE instruction is given to a whose LSPs are parked in Pause-IR or Pause-DR, the parked LSPs will become unparked when the 'STA111's TAP controller is sequenced into the respective Pause state.

The PARKPAUSE instruction was implemented with this dual functionality to enable backplane testing (interconnect testing between boards) with simultaneous Updates and Captures.

Simultaneous Update and Capture of several boards can be performed by parking LSPs of the different boards in the Pause-DR TAP controller state, after shifting the data to be updated into the boundary registers of the components on each board. The broadcast address is used to select all 'STA111s connected to the backplane. The PARKPAUSE instruction is scanned into the selected 'STA111s and the 'STA111 TAP controllers are sequenced to the Pause-DR state where the LSPs of all 'STA111s become unparked. The local TAP controllers are then sequenced through the Update-DR, Select-DR, Capture-DR, Exit1-DR, and parked in the Pause-DR state, as the 'STA111 TAP controller is sequenced into the Update-DR state. When a LSP is parked, it is removed from the active scan chain.

**GOTOWAIT:** This instruction is used to return all 'STA111s to the Wait-For-Address state. All unparked LSPs will be parked in the Test-Logic-Reset TAP controller state (see Figure 5).

**MODESEL:** The MODESEL instruction inserts Mode Register$_0$ into the active scan chain. Mode Register$_0$ determines the LSPN configuration for a device with up to five (5) LSPs (only three in Silicon). Bit 7 of Mode Register$_0$ is a read-only counter status flag.

**MODESEL$_n$:** The MODESEL$_n$ instruction inserts Mode Register$_n$ (n = 1 to 3) into the active scan chain. Mode Register$_1$ determines the LSPN configuration for LSP 5, 6 and 7 (if they exist), and Mode Register$_2$ determines the Shared GPIO configuration.

**MCGRSEL:** This instruction inserts the multi-cast group register (MCGR) into the active scan chain. The MCGR is used to group 'STA111s into multi-cast groups for parallel TAP sequencing (i.e., to simultaneously perform identical scan operations).

**SOFTRESET:** This instruction causes all 3 Port configuration controllers (see Figure 4) to enter the Parked-TLR state, which forces TMS$_n$ high; this parks each local port in the Test-Logic-Reset state within 5 TCK$_B$ cycles.

**LFSRSEL:** This instruction inserts the linear feedback shift register (LFSR) into the active scan chain, allowing a compacted signature to be shifted out of the LFSR during the Shift-DR state. (The signature is assumed to have been computed during earlier LFSRON shift operations.) This instruction disables the LFSR register's feedback circuitry, turning the LFSR into a standard 16-bit shift register. This allows a signature to be shifted out of the register, or a seed value to be shifted into it.

**LFSRON:** Once this instruction is executed, the linear feedback shift register samples data from the active scan path (including all unparked TDI$_n$) during the Shift-DR state. Data from the scan path is shifted into the linear feedback shift register and compacted. This allows a serial stream of data to be compressed into a 16-bit signature that can subsequently be shifted out using the LFSRSEL instruction. The linear feedback shift register is not placed in the scan chain during this mode. Instead, the register samples the active scan-chain data as it flows from the LSPN to TDO$_B$.

**LFSROFF:** This instruction terminates linear feedback shift register sampling. The LFSR retains its current state after receiving this instruction.

**CNTRSEL:** This instruction inserts the 32-bit TCK counter shift register into the active scan chain. This allows the user to program the number of n TCK cycles to send to the parked local ports once the CNTRON instruction is issued (e.g., for BIST operations). Note that to ensure completion of countdown, the 'STA111 should receive at least n TCK$_B$ pulses.

**CNTRON:** This instruction enables the TCK counter. The counter begins counting down on the first rising edge of TCK$_B$ following the Update-IR TAP controller state and is decremented on each rising edge of TCK$_B$ thereafter. When the TCK counter reaches terminal count, 00000000 Hex, TCK$_n$ of all parked LSP's is held low. This function overrides Mode Register$_0$ TCK control bit (bit-3).

If the CNTRON instruction is issued when the TCK counter is 00000000 (terminal count) the local TCKs of parked LSPs will be gated. The counter will begin counting on the rising edge of TCK$_B$ when the TCK counter is loaded with a non-zero value following a CNTRSEL instruction (see BIST Support in Special Features section for an example).

**CNTROFF:** This instruction disables the TCK counter, and TCK$_n$ control is returned to Mode Register$_0$ (bit 3).

**DEFAULT_BYPASS:** This instruction selects the Bypass register to be the default for SCANSTA111 commands that do not explicitly require a data register. The default after RESET is the Device ID register.

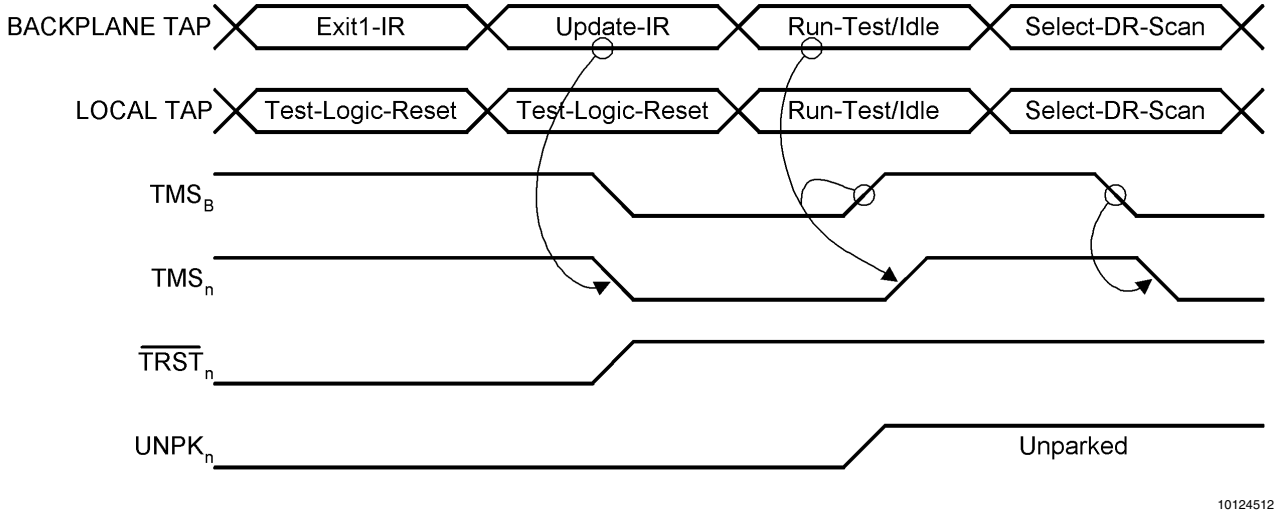



**FIGURE 9. Local Scan Port Synchronization from Parked-TLR State**

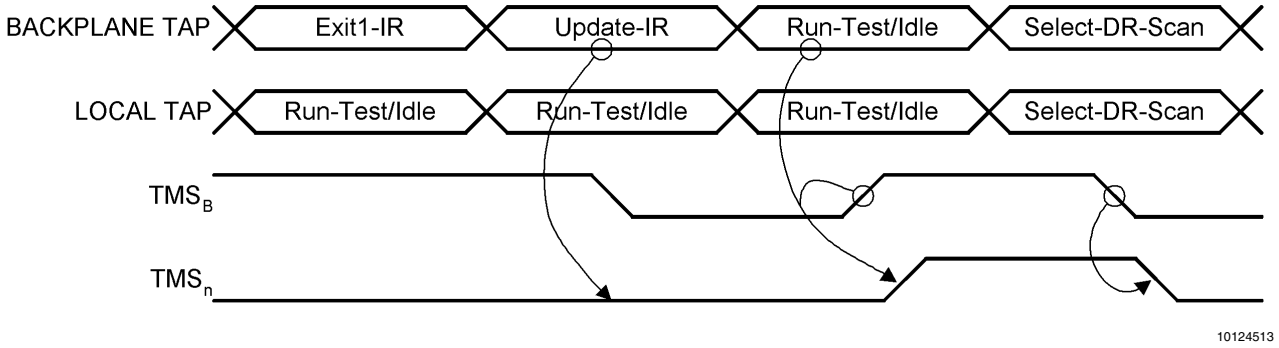



**FIGURE 10. Local Scan Port Synchronization from Parked-RTI State**

## Register Descriptions

**INSTRUCTION REGISTER:** The instruction shift register is an 8-bit register that is in series with the scan chain whenever the TAP Controller of the SCANSTA111 is in the Shift-IR state. Upon exiting the Capture-IR state, the value XXXXXX01 is captured into the instruction register, where XXXXXX represents the value on the $S_{(0-6)}$ inputs. When the 'STA111 controller is in the Wait-For-Address state, the instruction register is used for 'STA111 selection via address matching. In addressing individual 'STA111s, the chip's addressing logic performs a comparison between a statically-configured (hard-wired) value on that 'STA111's slot inputs, and an address which is scanned into the chip's instruction register. Binary address codes 000000 through 111010 (00 through 3A Hex) are reserved for addressing individual 'STA111s. Address 3B Hex is for Broadcast mode.

During multi-cast (group) addressing, a scanned-in address is compared against the (previously scanned-in) contents of a 'STA111's Multi-Cast Group register. Binary address codes 111110 through 111111 (3A through 3F Hex) are reserved for multi-cast addressing, and should not be assigned as 'STA111 slot-input values.

**BOUNDARY-SCAN REGISTER:** The boundary-scan register is a sample only shift register containing cells from the $S_{(0-6)}$ and $\overline{OE}$ inputs. The register allows testing of circuitry external to the 'STA111. It permits the signals flowing between the system pins to be sampled and examined without interfering with the operation of the on-chip system logic.

The scan chain is arranged as follows:

$TDI_B \rightarrow \overline{OE} \rightarrow S_6 \rightarrow S_5 \rightarrow S_4 \rightarrow S_3 \rightarrow S_2 \rightarrow S_1 \rightarrow S_0 \rightarrow TDO_B$

**BYPASS REGISTER:** The bypass register is a 1-bit register that operates as specified in IEEE Std. 1149.1 once the 'STA111 has been selected. The register provides a minimum length serial path for the movement of test data between $TDI_B$ and the LSPN. This path can be selected when no other test data register needs to be accessed during a board-level test operation. Use of the bypass register shortens the serial access-path to test data registers located in other components on a board-level test data path.

**MULTI-CAST GROUP REGISTER:** Multi-cast is a method of simultaneously communicating with more than one selected 'STA111. The multi-cast group register (MCGR) is a 2-bit register used to determine which multi-cast group a particular 'STA111 is assigned to. Four addresses are reserved for multi-cast addressing. When a 'STA111 is in the Wait-For-Address state and receives a multi-cast address, and if that 'STA111's MCGR contains a matching value for that multi-cast address, the 'STA111 becomes selected and is ready to receive Level 2 Protocol (i.e., further instructions).

The MCGR is initialized to 00 upon entering the Test-Logic-Reset state.

**TABLE 6. Multi-Cast Group Register Addressing**

| MCGR Bits 1,0 | Hex Address | Binary Address |
|---|---|---|
| 00 | 3C | 00111100 |
| 01 | 3D | 00111101 |
| 10 | 3E | 00111110 |
| 11 | 3F | 00111111 |

The following actions are used to perform multi-cast addressing:

1. Assign all target 'STA111s to a multi-cast group by writing each individual target 'STA111's MCGR with the same multi-cast group code (see Table 6). This configuration step must be done by individually addressing each target 'STA111, using that chip's assigned slot value.
2. Scan out the multi-cast group address through the $TDI_B$ input of all 'STA111s. Note that this occurs in parallel, resulting in the selection of only those 'STA111s whose MCGR was previously programmed with the matching multi-cast group code.

**MODE REGISTER$_0$:** Mode Register$_0$ is an 8-bit data register used primarily to configure the Local Scan Port Network. Mode Register$_0$ is initialized to 00000001 binary upon entering the Test-Logic-Reset state. Bits 0, 1, 2, and 4 are used for scan chain configuration as described in Table 7. When the UNPARK instruction is executed, the scan chain configuration is as shown in Table 7 below. When all LSPs are parked, the scan chain configuration is $TDI_B$ → 'STA111-register → $TDO_B$. Bit 3 is used for $TCK_n$ configuration, see Table 8.

**TABLE 7. Mode Register Control of LSPN**

| Mode Register(s) | Scan Chain Configuration (if unparked) |
|---|---|
| MR0: X000X000 | $TDI_B \rightarrow$ Register $\rightarrow TDO_B$ |
| MR0: X000X001 | $TDI_B \rightarrow$ Register $\rightarrow LSP_0 \rightarrow$ PAD $\rightarrow TDO_B$ |
| MR0: X000X010 | $TDI_B \rightarrow$ Register $\rightarrow LSP_1 \rightarrow$ PAD $\rightarrow TDO_B$ |
| MR0: X000X011 | $TDI_B \rightarrow$ Register $\rightarrow LSP_0 \rightarrow$ PAD $\rightarrow LSP_1 \rightarrow$ PAD $\rightarrow TDO_B$ |
| MR0: X000X100 | $TDI_B \rightarrow$ Register $\rightarrow LSP_2 \rightarrow$ PAD $\rightarrow TDO_B$ |
| MR0: X000X101 | $TDI_B \rightarrow$ Register $\rightarrow LSP_0 \rightarrow$ PAD $\rightarrow LSP_2 \rightarrow$ PAD $\rightarrow TDO_B$ |
| MR0: X000X110 | $TDI_B \rightarrow$ Register $\rightarrow LSP_1 \rightarrow$ PAD $\rightarrow LSP_2 \rightarrow$ PAD $\rightarrow TDO_B$ |
| MR0: X000X111 | $TDI_B \rightarrow$ Register $\rightarrow LSP_0 \rightarrow$ PAD $\rightarrow LSP_1 \rightarrow$ PAD $\rightarrow LSP_2 \rightarrow$ PAD $\rightarrow TDO_B$ |
| MR0: X010X000 | $TDI_B \rightarrow$ Register $\rightarrow LSP_3 \rightarrow$ PAD $\rightarrow TDO_B$ |
| MR0: X010X001 | $TDI_B \rightarrow$ Register $\rightarrow LSP_0 \rightarrow$ PAD $\rightarrow LSP_3 \rightarrow$ PAD $\rightarrow TDO_B$ |
| MR0: X010X010 | $TDI_B \rightarrow$ Register $\rightarrow LSP_1 \rightarrow$ PAD $\rightarrow LSP_3 \rightarrow$ PAD $\rightarrow TDO_B$ |
| MR0: X010X011 | $TDI_B \rightarrow$ Register $\rightarrow LSP_0 \rightarrow$ PAD $\rightarrow LSP_1 \rightarrow$ PAD $\rightarrow LSP_5 \rightarrow$ PAD $\rightarrow TDO_B$ |
| MR0: X010X100 | $TDI_B \rightarrow$ Register $\rightarrow LSP_2 \rightarrow$ PAD $\rightarrow LSP_3 \rightarrow$ PAD $\rightarrow TDO_B$ |
| ... | ... |
| MR0: X110X111 | $TDI_B \rightarrow$ Register $\rightarrow LSP_0 \rightarrow$ PAD $\rightarrow LSP_1 \rightarrow$ PAD $\rightarrow LSP_2 \rightarrow$ PAD $\rightarrow LSP_3 \rightarrow$ PAD $\rightarrow LSP_4 \rightarrow$ PAD $\rightarrow TDO_B$ |
| MR0: X000X000<br>MR1: XXXXX001<br>(Note 7) | $TDI_B \rightarrow$ Register $\rightarrow LSP_5 \rightarrow$ PAD $\rightarrow TDO_B$ |
| MR0: X000X001<br>MR1: XXXXX001<br>(Note 7) | $TDI_B \rightarrow$ Register $\rightarrow LSP_0 \rightarrow$ PAD $\rightarrow LSP_5 \rightarrow$ PAD $\rightarrow TDO_B$ |
| MR0: X000X010<br>MR1: XXXXX001<br>(Note 7) | $TDI_B \rightarrow$ Register $\rightarrow LSP_1 \rightarrow$ PAD $\rightarrow LSP_5 \rightarrow$ PAD $\rightarrow TDO_B$ |
| ... | ... |
| MR0: X110X111<br>MR1: XXXXX001<br>(Note 7) | $TDI_B \rightarrow$ Register $\rightarrow LSP_0 \rightarrow$ PAD $\rightarrow\rightarrow LSP_1 \rightarrow$ PAD $\rightarrow LSP_2 \rightarrow$ PAD $\rightarrow LSP_3 \rightarrow$ PAD $\rightarrow LSP_4 \rightarrow$ PAD $\rightarrow LSP_5 \rightarrow$ PAD $\rightarrow TDO_B$ |
| MR0: X000X000<br>MR1: XXXXX010<br>(Note 7) | $TDI_B \rightarrow$ Register $\rightarrow LSP_6 \rightarrow$ PAD $\rightarrow TDO_B$ |
| ... | ... |
| MR0: X110X111<br>MR1: XXXXX111<br>(Note 7) | $TDI_B \rightarrow$ Register $\rightarrow LSP_0 \rightarrow$ PAD $\rightarrow LSP_1 \rightarrow$ PAD $\rightarrow LSP_2 \rightarrow$ PAD $\rightarrow LSP_3 \rightarrow$ PAD $\rightarrow LSP_4 \rightarrow$ PAD $\rightarrow LSP_5 \rightarrow$ PAD $\rightarrow LSP_6 \rightarrow$ PAD $\rightarrow LSP_7 \rightarrow$ PAD $\rightarrow TDO_B$ |
| MR0: XXX1XXXX<br>MR1: XXXXXXXX<br>(Note 7) | $TDI_B \rightarrow$ Register $\rightarrow TDO_B$ (Loopback) |

**Note 7:** Mode Register$_1$ is only available in the HDL version (up to eight LSPs). The Silicon version has three LSPs and uses Mode Register$_0$ for LSP selection.

**Note 8:** In a device with 8 LSPs there are $2^8$ possible LSPN configurations: No LSPs, each individual LSP, combinations of 2 to 7 LSPs, and all 8 LSPs.

**TABLE 8. Test Clock Configuration**

| Bit 3 | LSP n | TCK n |
|---|---|---|
| 1 | Parked | Stopped |
| 0 | Parked | Free-running |
| 1 | Unparked | Free-running |
| 0 | Unparked | Free-running |
| X | Parked-TLR | Stopped after 512 clock pulses |

Bit 3 is normally set to logic 0 so that $TCK_n$ is free-running when the local scan ports are parked in the Parked-RTI, Parked-Pause-DR or Parked-Pause-IR state. When the local ports are parked, bit 3 can be programmed with logic 1, forcing all of the LSP $TCK_n$'s to stop. This feature can be used in power sensitive applications to reduce the power consumed by the test circuitry in parts of the system that are not under test. When in the Parked-TLR state, $TCK_n$ is gated (stopped) after 512 clock pulses have been received on $TCK_B$ independent of the bit 3 value.

Bit 7 is a status bit for the TCK counter. Bit 7 is only set (logic 1) when the TCK counter is on and has reached terminal count (zero). It is cleared (logic 0) when the counter is loaded following a CNTRSEL instruction. The power-on value for bit 7 is 0.

Bits 5 and 6 are optional in the HDL to support five LSPs with a single Mode Register$_0$ . A second Mode Register$_1$ may be added to allow support of up to eight LSPs.

**TABLE 9. Mode Register$_0$**

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Description | TCK Counter Status | $LSP_4$ | $LSP_3$ | $TDI_B$ to $TDO_B$ Loopback | TCK Free Running Disable | $LSP_2$ | $LSP_1$ | $LSP_0$ |
| Used in Silicon | Y | N | N | Y | Y | Y | Y | Y |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

**TABLE 10. Mode Register$_1$**

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Description | Reserved | Reserved | Reserved | Reserved | Reserved | $LSP_7$ | $LSP_6$ | $LSP_5$ |
| Used in Silicon | N | N | N | N | N | N | N | N |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**TABLE 11. Mode Register$_2$**

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Description | $LSP_7$/$GPIO_7$ | $LSP_6$/$GPIO_6$ | $LSP_5$/$GPIO_5$ | $LSP_4$/$GPIO_4$ | $LSP_3$/$GPIO_3$ | $LSP_2$/$GPIO_2$ | $LSP_1$/$GPIO_1$ | $LSP_0$/$GPIO_0$ |
| Used in Silicon | N | N | N | N | N | Y | Y | Y |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**DEVICE IDENTIFICATION REGISTER:** The device identification register (IDREG) is a 32-bit register compliant with IEEE Std. 1149.1. When the IDCODE instruction is active, the identification register is loaded with the Hex value upon leaving the Capture-DR state (on the rising edge of the $TCK_B$). Refer to the currently available BSDL file on our website for the most accurate Device ID.

**LINEAR FEEDBACK SHIFT REGISTER:** The 'STA111 contains a signature compactor which supports test result evaluation in a multi-chain environment. The signature compactor consists of a 16-bit linear-feedback shift register (LFSR) which can monitor local-port scan data as it is shifted upstream from the 'STA111's local-port network. Once the LFSR is enabled, the LFSR's state changes in a reproducible way as each local-port data bit is shifted in from the local-port network. When all local-port data has been scanned in, the LFSR contains a 16-bit signature value which can be compared against a signature computed for the expected results vector.

The LFSR uses the following feedback polynomial:

$$F(x) = X^{16} + X^{12} + X^3 + X + 1$$

This signature compactor is used to compress serial data shifted in from the local scan chain, into a 16-bit signature. This signature can then be shifted out for comparison with an expected value. This allows users to test long scan chains in parallel, via Broadcast or Multi-Cast addressing modes, and check only the 16-bit signatures from each module. The LFSR is initialized with a value of 0000 Hex upon reset.

**32-BIT TCK COUNTER REGISTER:** The 32-bit TCK counter register enables BIST testing that requires n TCK cycles, to be run on a parked LSP while another 'STA111 port is being tested. The CNTRSEL instruction can be used to load a count-down value into the counter register via the active scan chain. When the counter is enabled (via the CNTRON instruction), and the LSP is parked, the local TCKs will stop and be held low when terminal count is reached.

The TCK counter is initialized with a value of 00000000 Hex upon reset.

**TABLE 12. Dedicated GPIO Register$_n$ (HDL only)**

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Description | Input | Input | Input | Input | Output | Output | Output | Output |

**TABLE 13. Shared GPIO Register$_n$**

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Description | Reserved | Reserved | Reserved | Reserved | Reserved | Input (TDI) | Output (TDO) | Output (TMS) |
| Used in Silicon | N | N | N | N | N | Y | Y | Y |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

# Special Features

## TRANSPARENT MODE

While this mode is activated, the selected LSP n ports will follow the backplane ports. $\overline{TRST}_n$ is a buffered version of $\overline{TRST}_B$, $TCK_n$ is a buffered version of $TCK_B$, $TMS_n$ is a buffered version of $TMS_B$, $TDO_n$ is a buffered version of $TDI_B$ and $TDO_B$ is a buffered version of $TDI_n$. $TRIST_B$ and $TRIST_n$ are asserted when the state machine is in either the Shift-DR or Shift-IR states. The unselected LSPs are placed in the PARKTLR state, and their clocks are gated after 512 $TCK_B$ clock cycles.

Transparent Mode is controlled by 8 new instructions, TRANSPARENT0 through TRANSPARENT7. Transparent Mode overrides any other active mode. When one of the transparent mode instruction is shifted into the instruction register and the tap controller goes through the UPDATE-IR state, $\overline{TRST}_n$ will go high, and $TMS_n$ will go low. This will force the targets connected to the $LSP_n$ ports to go into the RTI state. Then as the 'STA111 state machine goes into the RTI state, all of the $LSP_n$ signals will follow the back-plane signals. This is identical to the method that is typically used to unpark an LSP. The 'STA111 will remain in this mode until a $\overline{TRST}_B$ is asserted or a power cycle forces a reset. Once in the Transparent Mode, the 'STA111 will not be able to be reset by a 5 TMS high reset.

The sequence of operations to use Transparent Mode on an LSP are as follows (example uses $LSP_0$ ):

1. IR-Scan the 'STA111 address into the instruction register (address a 'STA111).
2. IR-Scan the TRANSPARENT0 instruction to enable Transparent Mode on $LSP_0$. Transparent Mode is enabled when the TAP enters the RTI state at the end of this shift operation ($\overline{TRST}_0$, $TDO_0$, $TMS_0$ and $TCK_0$ become buffered versions of $\overline{TRST}_B$, $TDI_B$, $TMS_B$ and $TCK_B$ and $TDO_B$ becomes a buffered version of $TDI_0$).

NOTE: Transparent Mode will persist until the 'STA111 is reset using $\overline{TRST}_B$ . The GOTOWAIT and SOFTRESET instructions will not work in this mode.

## BIST SUPPORT

The sequence of instructions to run BIST testing on a parked SCANSTA111 port is as follows:

1. Pre-load the Boundary register of the device under test if needed.
2. Issue the CNTRSEL instruction and initialize (load) the TCK counter to 00000000 Hex. Note that the TCK counter is initialized to 00000000 Hex upon Test-Logic-Reset, so this step may not be necessary.
3. Issue the CNTRON instruction to the 'STA111, to enable the TCK counter.
4. Shift the PARKRTI instruction into the 'STA111 instruction register and BIST instruction into the instruction register of the device under test. With the counter on (at terminal count) and the LSP parked, the local TCK is gated.
5. Issue the CNTRSEL instruction to the 'STA111.
6. Load the TCK counter (Shift the 32-bit value representing the number of $TCK_n$ cycles needed to execute the BIST operation into the TCK counter register). The Self test will begin on the rising edge of $TCK_B$ following the Update-DR TAP controller state.
7. Bit 7 of $Mode\ Register_0$ can be scanned to check the status of the TCK counter, (MODESEL instruction followed by a Shift-DR). Bit 7 logic 0 means the counter has not reached terminal count, logic 1 means that the counter has reached terminal count and the BIST operation has completed.
8. Execute the CNTROFF instruction.
9. Unpark the LSP and scan out the result of the BIST operation

## RESET

Reset operations can be performed at three levels. The highest level resets all 'STA111 registers and all of the local scan chains of selected and unselected 'STA111s. This Level 1 reset is performed whenever the 'STA111 TAP Controller enters the Test-Logic-Reset state. Test-Logic-Reset can be entered synchronously by forcing $TMS_B$ high for at least five (5) $TCK_B$ pulses, or asynchronously by asserting the $TRST_B$ pin. A Level 1 reset forces all 'STA111s into the Wait-For-Address state, parks all local scan chains in the Test-Logic-Reset state, and initializes all 'STA111 registers.

The SOFTRESET instruction is provided to perform a Level 2 reset of all LSP's of selected 'STA111s. SOFTRESET forces all $TMS_n$ signals high, placing the corresponding local TAP Controllers in the Test-Logic-Reset state within five (5) $TCK_B$ cycles.

The third level of reset is the resetting of individual local ports. An individual LSP can be reset by parking the port in the Test-Logic-Reset state via the PARKTLR instruction. To reset an individual LSP that is parked in one of the other parked states, the LSP must first be unparked via the UNPARK instruction.

## PORT SYNCHRONIZATION

When a LSP is not being accessed, it is placed in one of the four TAP Controller states: Test-Logic-Reset, Run-Test/Idle, Pause-DR, or Pause-IR. The 'STA111 is able to park a local chain by controlling the local Test Mode Select outputs ($TMS_{(0\text{-}2)}$) (see Figure 4). $TMS_n$ is forced high for parking in the Test-Logic-Reset state, and forced low for parking in Run-Test/Idle, Pause-IR, or Pause-DR states. Local chain access is achieved by issuing the UNPARK instruction. The LSPs do not become unparked until the 'STA111 TAP Controller is sequenced through a specified synchronization state. Synchronization occurs in the Run-Test/Idle state for LSPs parked in Test-Logic-Reset or Run-Test/Idle; and in the Pause-DR or Pause-IR state for ports parked in Pause-DR or Pause-IR, respectively.

Figure 11 and Figure 12 show the waveforms for synchronization of a local chain that was parked in the Test-Logic-Reset state. Once the UNPARK instruction is received in the instruction register, the LSPC forces $TMS_n$ low on the falling edge of $TCK_B$ .

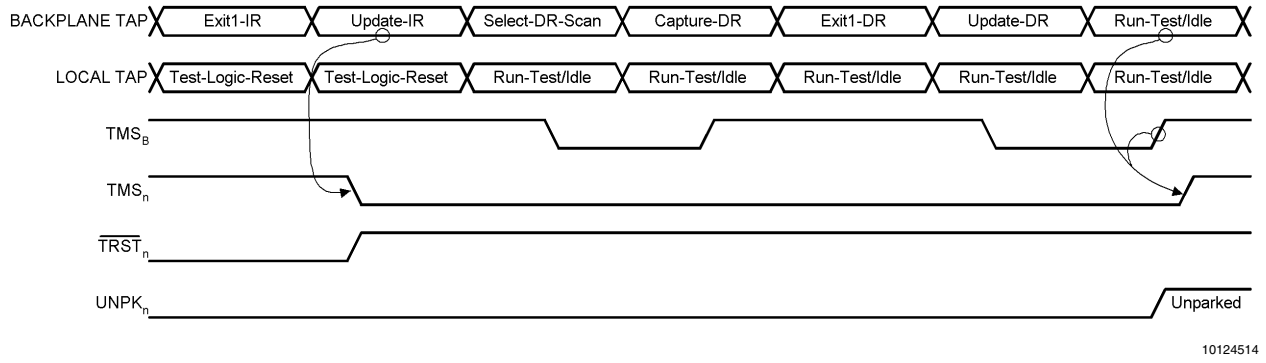



**FIGURE 11. Local Scan Port Synchronization on Second Pass**

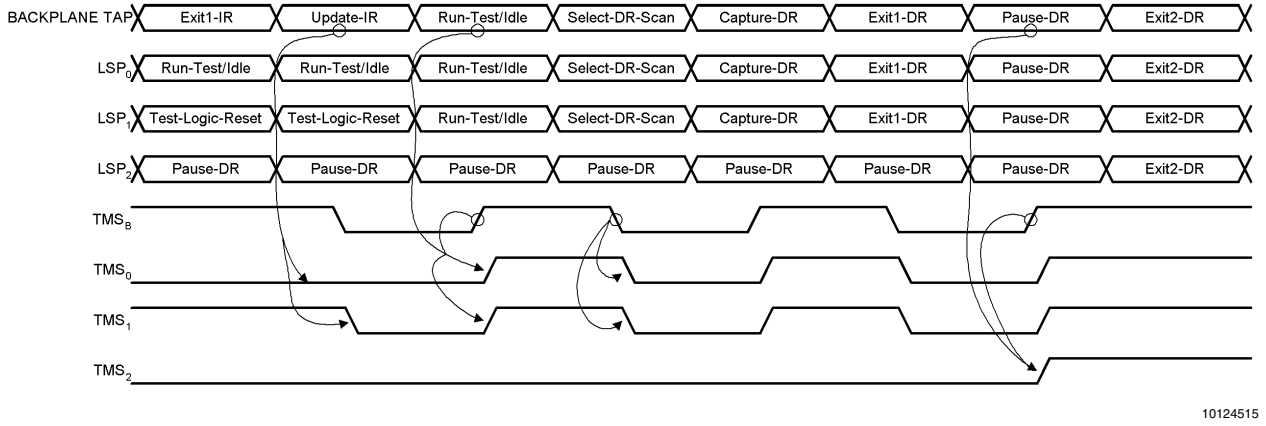



**FIGURE 12. Synchronization of the Three Local Scan Ports**

This moves the local chain TAP Controllers to the synchronization state (Run-Test/Idle), where they stay until synchronization occurs. If the next state of the 'STA111 TAP Controller is Run-Test/Idle, $TMS_n$ is connected to $TMS_B$ and the local TAP Controllers are synchronized to the 'STA111 TAP Controller as shown in Figure 12. If the next state after Update-IR were Select-DR, $TMS_n$ would remain low and synchronization would not occur until the 'STA111 TAP Controller entered the Run-Test/Idle state, as shown in Figure 11.

Each local port has its own Local Scan Port Controller. This is necessary because the LSPN can be configured in any one of eight (8) possible combinations. Either one, some, or all of the local ports can be accessed simultaneously. Configuring the LSPN is accomplished with Mode $Register_0$, in conjunction with the UNPARK instruction.

The LSPN can be unparked in one of seven different configurations (Si device), as specified by bits 0-2 of Mode $Register_0$ . Using multiple ports presents not only the task of synchronizing the 'STA111 TAP Controller with the TAP Controllers of an individual local port, but also of synchronizing the individual local ports to one another.

When multiple local ports are selected for access, it is possible that two ports are parked in different states. This could occur when previous operations accessed the two ports separately and parked them in the two different states. The LSP Controllers handle this situation gracefully. Figure 12 shows the UNPARK instruction being used to access $LSP_0$, $LSP_1$, and $LSP_2$ in series (Mode $Register_0$ = XXX0X111 binary). $LSP_0$ and $LSP_1$ become active as the 'STA111 controller is sequenced through the Run-Test/Idle state. $LSP_2$ remains parked in the Pause-DR state until the 'STA111 TAP Controller is sequenced through the Pause-DR state. At that point, all three local ports are synchronized for access via the active scan chain.

## PARAMETERIZED DESIGN (HDL)

In order to support a large number of applications, the 'STA111 HDL is parameterized as described:

- **Number of Local Scan Ports (LSPs):** The 'STA111 HDL is able to simulate/synthesize a device that contains from 1 to 8 LSPs. $LSP_0$ through $LSP_4$ are controlled via Mode $Register_0$ and $LSP_5$ through $LSP_7$ are controlled via Mode $Register_1$. The silicon version of the 'STA111 is synthesized with three LSPs, $LSP_0$ through $LSP_2$.
- **Number of Address Pins:** The 'STA111 has a selectable number of address bits ($S_0$ - $S_n$, where n can range from 5 to 7). Addresses 3A through 3F hex are reserved for address interrogation, broadcast and multi-cast addressing. The silicon version of the 'STA111 is synthesized with seven address pins.
- **Pass-Through Pins:** Each of the LSPs (0-n) may selectively have or not have Pass-through pins. Pass-through pins are described in more detail below. The silicon version of the 'STA111 is synthesized with Pass-through pins on $LSP_0$ and $LSP_1$.

- **Number/Type of GPIO bits:** The 'STA111 has both dedicated and shared GPIO (General Purpose I/O). Each dedicated group of GPIO bits supports from 0 to 4 dedicated inputs and 0 to 4 dedicated outputs. There are provisions for specifying the default (power-up) value. $TMS_{(0-n)}$, $TDO_{(0-n)}$ and $TDI_{(0-n)}$ are also dual purpose pins functioning as LSP or GPIO. $TMS_n$ and $TDO_n$ are outputs, $TDI_n$ is an input in the GPIO mode. The silicon version of the 'STA111 is synthesized with shared GPIO on all three available LSPs. The silicon version of the 'STA111 does not support dedicated GPIO.

Throughout this datasheet, notations exist to clarify the differences between features available on the Silicon version and the HDL version.

## KNOWN POWER-UP STATE

The 'STA111 has a known power-up condition. This is the same state that the device is in after a $\overline{TRST}$ reset. This happens at power-up without the presence of a $TCK_B$.

Reset can also occur via a 5 TMS high reset or a SOFTRESET command.

## POWER-OFF HIGH IMPEDANCE INPUTS AND OUTPUTS

The 'STA111 backplane test port features power-off high impedance inputs and outputs.

The $TDI_B$, $TMS_B$, and $\overline{TRST}_B$ inputs have a 25KΩ pull-up resistor and no ESD clamp diode (ESD is controlled with an alternate method). When the device is power-off ($V_{DD}$ floating), these inputs appear to be a capacitive load to ground. When $V_{DD}$ = 0V (i.e.; not floating but tied to $V_{SS}$) these inputs appear to be capacitive with the pull-up to ground.

The $TCK_B$ input has no pull-up resistor and no ESD clamp diode (ESD is controlled with an alternate method). When the device is power-off ($V_{DD}$ floating), the input appears to be a capacitive load to ground. When $V_{DD}$ = 0V (i.e.; not floating but tied to $V_{SS}$) the input appears to be a capacitive load to ground.

When the device is power-off ($V_{DD}$ = 0V or floating), the $TDO_B$ output appears to be a capacitive load.

Refer to the device IBIS model on our website for more details about the I/O characteristics at http://www.national.com/apinfo/scan/ibis.html.

## TRST

**$\overline{TRST}_B$:** Assertion of $\overline{TRST}_B$ will return the device back to its known power-up state.

**$\overline{TRST}_n$:** $\overline{TRST}_n$ is an output on the LSP side of the 'STA111. While the LSP state-machine (level 2 protocol) is in the Parked-TLR state the $\overline{TRST}_n$ pin will be driven low. In all other states the $\overline{TRST}_n$ pin will be driven high.

## PHYSICAL LAYER CHANGES

TRIST for $TDO_B$ and $TDO_n$ are signals for enabling an external buffer circuit between the 'STA111 and the backplane/LSP. This would allow, for example, a CMOS-to-LVDS converter to drive an LVDS JTAG backplane test bus. These signals are always driving. A separate TRIST is provided for each LSP to report a TRI-STATE on TDO when the LSP is not in a shift state.

## SVF DRIVEN, SELF-CHECKING TEST BENCH

The 'STA111 consists of 3 types of pins, dot1 backplane pins, dot1 LSP pins and support pins. The command interpreter of the test bench is able to translate a limited set of SVF commands to the dot1 backplane pins. The SVF shift commands contain both the stimulus ($TDI_B$) and expected response ($TDO_B$).

The interpreter is able to parse the following commands: ENDDR, ENDIR, RUNTEST, SDR, SIR, STATE, TRST.

## PASS-THROUGH PINS

Each LSP may selectively have two pass-through pins. The pair of pass-through pins consist of an input ($A_n$) and an output ($Y_n$). The LSP pass-through output ($Y_n$) drives the level being received by the backplane pass-through input ($A_B$). Conversely, the level on the LSP pass-through input ($A_n$) drives the backplane pass-through output ($Y_B$).

The Pass-through pins are available only when a single LSP is selected. For each LSP these pins will be enabled when the level 2 protocol state-machine is not in the Parked-TLR state. When not enabled they are TRI-STATED.

## LSP GATING

While the LSP state-machine (level 2 protocol) is in the Parked-TLR state, the four LSP signals shall be controlled as shown in Table 14 below. Upon entry into the Parked-TLR state (power-up, reset, PARKTLR or GOTOWAIT) a counter in the LSP state-machine allows 512 $TCK_B$ clock pulses to occur on $TCK_n$ before gating. Once gated, $TCK_n$ will drive a logic 0.

Letting 512 $TCK_B$ pulses pass through to $TCK_n$ allows a five high TMS reset to occur on over 100 levels of hierarchy before the 'STA111 gates $TCK_n$ (for power saving in a free-running clock system).

**TABLE 14. Gated LSP Drive States**

| LSP Connection | Drive State |
|---|---|
| $TDO_n$ | Pull-up resistor to provide a weak HIGH |
| $TMS_n$ | Pull-up resistor to provide a weak HIGH |
| $TDI_n$ | Pull-up resistor to provide a weak HIGH |
| $TCK_n$ | $TCK_B$ for 512 pulses, then gated LOW |

The 'STA111 does not require that any clock pulses are received on $TCK_B$ while in the Parked-TLR state.

Setting Bit 3 of $Mode\ Register_0$ to 1 gates $TCK_n$ when in the Parked-RTI, Parked-Pause-DR and Parked-Pause-IR states. Default is free-running (bit 3 = 0). The value stored in bit 3 of $Mode\ Register_0$ does not effect the requirement of 512 clock pulses before gating $TCK_n$ in the Parked-TLR state. (See section on $Mode\ Register_0$).

## IEEE 1149.4 SUPPORT

The 'STA111 provides support for a switched analog bus. Each LSP has an unparked-TLR notification pin ($LSP\_ACTIVE_{(0-2)}$) which is low (0) when the LSP is in Parked-TLR and high (1) otherwise. This signal can be used to enable/disable analog switches external to the 'STA111.

## GPIO CONNECTIONS

General Purpose I/O (GPIO) pins are registered inputs and outputs that are parameterized in the HDL. The two types of GPIOs than can be used in the 'STA111 are described in the next two sections. The silicon version of the 'STA111 supports shared GPIO on all three available LSPs. The silicon version of the 'STA111 does not support dedicated GPIO.

**DEDICATED:** Each LSP supports up to four (4) dedicated inputs and up to four (4) dedicated outputs. These are separate, dedicated GPIO signals controlled by dedicated GPIO registers (one register per LSP). The GPIO outputs are updated

during the UPDATE-DR state and the GPIO input values are written to the corresponding GPIO register during the CAPTURE-DR state. Dedicated GPIO operation is not supported in the silicon version of the 'STA111.

**LSP SHARED:** In the shared mode of operation, the dot1 LSP pins $TDI_n$, $TDO_n$ and $TMS_n$ pins become GPIO pins. $TMS_n$ and $TDO_n$ are outputs, $TDI_n$ is an input in the GPIO mode.

The sequence of operations to use shared GPIOs on an LSP are as follows (example uses $LSP_0$):

1. IR-Scan the 'STA111 address into the instruction register (address a 'STA111).
2. IR-Scan the $MODESEL_3$ instruction into the instruction register to select Mode $Register_3$ (Shared GPIO configuration register) as the data register.
3. DR-Scan 00000001 into Mode $Register_3$ to enable GPIOs on $LSP_0$. The GPIOs will be enabled when the TAP enters the RTI state at the end of this shift operation ($TDO_0$ and $TMS_0$ will be forced to logic 0 as defined by the default value in the Shared GPIO $Register_0$).
4. IR-Scan the $SGPIO_0$ instruction into the instruction register to select the Shared GPIO $Register_0$ as the data register.
5. DR-Scan 00000011 into the Shared GPIO $Register_0$ to set $TDO_0$ and $TMS_0$ to a logic 1 (when TAP enters Update-DR). During this operation, when the TAP enters Capture-DR, the present value on the $TDI_0$ pin and the values of $TDO_0$ and $TMS_0$ (as set by Shared GPIO $Register_0$) will be captured into bits 2, 1 and 0 of the shift register and will be scanned out 00000X00 (X = value present on $TDI_0$ when TAP enters Capture-DR).
6. Step 5 can be repeated to generate waveforms on $TDO_0$ and $TMS_0$. If step 5 was repeated with 00000000 as data, $TDO_0$ and $TMS_0$ would be set to a logic 0 (when TAP state = Update-DR) and 00000X11 would be scanned out (X = value present on $TDI_0$ when TAP enters Capture-DR).
7. IR-Scan the GOTOWAIT or SOFTRESET instruction, or generate a $\overline{TRST}_B$ reset to disable the GPIOs.

## ADDRESS INTERROGATION

The 'STA111 has four states that it can go to from the Wait-For-Address state: Unselected, Singularly-selected, Multi/Broadcast-selected, and Address-interrogation (see Figure 13).

After a reset (or GOTOWAIT command) has been issued, the 'STA111 TAP is sequenced to the Capture-IR state where XXXXXX01 is loaded into the shift register. Upon entering the Shift-IR state, the instruction register is filled with the address interrogation value (3A hex) which is loaded into the address register as the TAP is sequenced into the Update-IR state. On the next loop through Capture-IR the shift register is loaded with the ones-complement of the slot address. In the Shift-IR state the address interrogation value is loaded into the instruction register. The value presented on $TDO_B$ will be a wired-and address of all of the 'STA111s on the bus. As this value is being shifted out, each 'STA111 will monitor its $TDO_B$ to see if it is receiving the same value it is driving. If the device shifts all bits of its ones-complement address and never gets a compare error it will tri-state $TDO_B$ and go to the Wait-For-Reset state. Alternately, if the device sees a compare error while it is shifting its ones-complement address it will stop shifting its address and tri-state $TDO_B$ until the next shift operation; during the next Shift-IR operation it will again try to present its address (if the previous instruction was 3A hex) while monitoring $TDO_B$.

Shifting 3A hex into the instruction registers of the 'STA111s will continue until all 'STA111s have presented their address. At this time all devices will be waiting to be reset, and if a 3A is shifted into the 'STA111 instruction registers the address read by the tester will be all weak 1s due to all $TDO_B$'s being tri-stated. Reading all ones will signal the tester that address interrogation is complete. Since all ones signifies the end of Address-Interrogation, no device can have an address of all zeros (ones-complement).

If at any time, during the address interrogation mode, any other instruction besides 3A hex is shifted into the instruction register, then the 'STA111 will exit the interrogation mode. Also, the 'STA111's state machine will go to the Wait-For-Address state.

This address interrogation scheme presumes that $TDO_B$ is capable of driving a weak 1 and that an 'STA111 driving a 0 will overdrive an 'STA111 driving a weak 1.

The following is an example of the Address-Interrogation function. Assume there are three 'STA111s (U1, U2 and U3) on a dot1 backplane with slot addresses 010100, 100000 and 000001 respectively (assuming 6 address pins).

1. The 'STA111s are reset and the interrogation address/op-code (3A hex) is shifted into the instruction registers.
2. At the end of the instruction shift (Update-IR) the 'STA111 address registers are loaded with 3A hex.
3. The TAPs are sequenced to Capture-IR and the shift registers latch the ones-complement slot addresses (U1=101011, U2=011111 and U3=111110).
4. The TAPs are sequenced to Shift-IR and the LSB of the interrogation address is presented on the $TDI_B$'s. Concurrently, the LSBs of the ones-complement slot addresses are presented on the respective $TDO_B$'s.
5. The weak 1 being driven on U1 and U2 is overdriven by the 0 from U3. U1 and U2 enter the Wait-For-Next-Interrogation state.
6. The shift operation continues and U3 finishes shifting its ones-complement address (111110) out on $TDO_B$. U3 enters the Wait-For-Reset state when the TAP enters Update-IR.
7. The TAPs are again sequenced to Capture-IR and U1 and U2 shift registers latch the ones-complement addresses (U1=101011, U2=011111).
8. The TAPs are sequenced to Shift-IR and the LSB of the interrogation address is presented on the $TDI_B$'s. Concurrently, the LSBs of the ones-complement addresses are presented on the respective $TDO_B$'s.
9. Since both U1 and U2 are driving a weak 1 the shift continues.
10. Again U1 and U2 drive weak 1 and the shift continues.
11. U2s weak 1 is overdriven by U1s 0 and U2 enters the Wait-For-Next-Interrogation state.
12. The shift operation continues and U1 finishes shifting its ones-complement address (101011) out on $TDO_B$. U1 enters theWait-For-Reset state.
13. The instruction shift operation is repeated and U2 shifts its ones-complement address (011111) out on $TDO_B$. U2 enters the Wait-For-Reset state.
14. The instruction shift operation is repeated, however, all devices have been interrogated and are waiting for a reset. The master device will receive all ones. This implies that there can not be an STA111 with address 0!

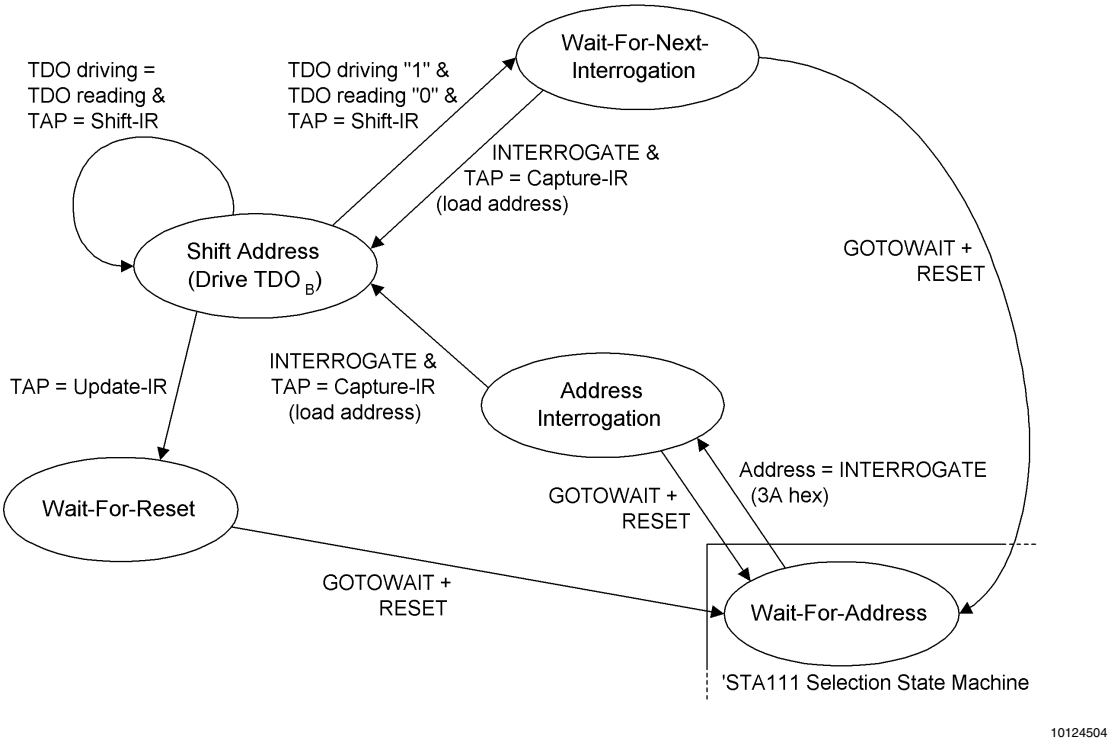



**FIGURE 13. Address Interrogation State Machine**

## Absolute Maximum Ratings (Note 9)

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | −0.3V to +4.0V |
| DC Input Diode Current ($I_{IK}$) | |
| $V_I$ = −0.5V | −20 mA |
| DC Input Voltage ($V_I$) | −0.5V to +3.9V |
| DC Output Diode Current ($I_{OK}$) | |
| $V_O$ = −0.5V | −20 mA |
| DC Output Voltage ($V_O$) | −0.3V to +3.9V |
| DC Output Source/Sink Current ($I_O$) | ±50 mA |
| DC $V_{CC}$ or Ground Current per Output Pin | ±50 mA |
| DC Latchup Source or Sink Current | ±300 mA |
| Junction Temperature (Plastic) | +150°C |
| Storage Temperature | −65°C to +150°C |
| Lead Temperature (Solder, 4sec) | |
| 49L BGA | 235°C |
| 48L TSSOP | 260°C |
| Max Pkg Power Capacity @ 25°C | |
| 49L BGA | 1.47 W |
| 48L TSSOP | 1.47 W |
| Thermal Resistance ($\theta_{JA}$) | |
| 49L BGA | 85°C/W |
| 48L TSSOP | 85°C/W |
| Package Derating | 11.8 mW/°C above 25°C |
| ESD Last Passing Voltage (Min) | |
| I/O | 2000V |
| Inputs | 1000V |

## Recommended Operating Conditions

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | |
| 'STA111 | 3.0V to 3.6V |
| Input Voltage ($V_I$) | 0V to $V_{CC}$ |
| Output Voltage ($V_O$) | 0V to $V_{CC}$ |
| Operating Temperature ($T_A$) | |
| Industrial | −40°C to +85°C |

**Note 9:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of SCAN STA products outside of recommended operation conditions.

## DC Electrical Characteristics

Over recommended operating supply voltage and temperature ranges unless otherwise specified

| Symbol | Parameter | Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| $V_{IH}$ | Minimum High Input Voltage | $V_{OUT}$ = 0.1V or $V_{CC}$ −0.1V | 2.1 | | V |
| $V_{IL}$ | Maximum Low Input Voltage | $V_{OUT}$ = 0.1V or $V_{CC}$ −0.1V | | 0.8 | V |
| $V_{OH}$ | Minimum High Output Voltage ($TDO_B$, $TCK_{(0-2)}$, $TMS_{(0-2)}$, $TDO_{(0-2)}$, $Y_{(0-1)}$) | $I_{OUT}$ = −100 µA $V_{IN}$ ($TDI_B$, $TMS_B$, $TCK_B$) = $V_{IH}$ | $V_{CC}$ - 0.2v | | V |
| $V_{OH}$ | Minimum High Output Voltage ($TDO_B$, $TCK_{(0-2)}$, $TMS_{(0-2)}$, $TDO_{(0-2)}$, $Y_{(0-1)}$, $Y_B$, $\overline{TRST}_{(0-2)}$) | $I_{OUT}$ = −24 mA, $V_{IN}$ on $S_{(0-6)}$ and $TDI_{(0-2)}$ = $V_{IH}$, $V_{IL}$All Outputs Loaded | 2.2 | | V |
| $V_{OH}$ | Minimum High Output Voltage ($TRIST_B$, $TRIST_{(0-2)}$, $Y_B$) | $I_{OUT}$ = −100µA | $V_{CC}$ - 0.2v | | V |
| $V_{OH}$ | Minimum High Output Voltage ($TRIST_B$, $TRIST_{(0-2)}$, $LSP\_ACTIVE_{(0-2)}$) | $I_{OUT}$ = −12mA. All Outputs Loaded | 2.4 | | V |
| $V_{OL}$ | Maximum Low Output Voltage ($TDO_B$, $TCK_{(0-2)}$, $TMS_{(0-2)}$, $TDO_{(0-2)}$, $Y_{(0-1)}$) | $I_{OUT}$ = +100 µA, $V_{IN}$ ($TDI_B$, $TMS_B$, $TCK_B$) = $V_{IL}$ | | 0.2 | V |
| $V_{OL}$ | Maximum Low Output Voltage ($TDO_B$, $TCK_{(0-2)}$, $TMS_{(0-2)}$, $TDO_{(0-2)}$, $Y_{(0-1)}$, $Y_B$, $\overline{TRST}_{(0-2)}$) | $I_{OUT}$ = +24 mA, $V_{IN}$ on $S_{(0-6)}$ and $TDI_{(0-2)}$ = $V_{IH}$, $V_{IL}$, All Outputs Loaded | | 0.55 | V |
| $V_{OL}$ | Maximum Low Output Voltage ($TRIST_B$, $TRIST_{(0-2)}$, $Y_B$) | $I_{OUT}$ = +100 µA | | 0.2 | V |

| Symbol | Parameter | Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| $V_{OL}$ | Maximum Low Output Voltage ($TRIST_B$, $TRIST_{(0-2)}$, $LSP\_ACTIVE_{(0-2)}$) | $I_{OUT}$ = +12 mA All Outputs Loaded | | 0.4 | V |
| $I_{IN}$ | Maximum Input Leakage Current ($TCK_B$, $S_{(0-6)}$) | $V_{IN} = V_{CC}$ or GND | | ±5.0 | µA |
| $I_{CCT}$ | Maximum $I_{CC}$/Input | $V_{IN} = V_{CC} - 0.6V$ | | 250 | µA |
| $I_{CC}$ | Maximum Quiescent Supply Current | $TDI_B$, $TMS_B$, $\overline{TRST}_B$, $TDI_{(0-2)} = V_{CC}$ or GND | | 1.65 | mA |
| $I_{CCD}$ | Maximum Dynamic Supply Current | | | 130 | mA |
| $I_{OFF}$ | Power Off Leakage Current $TDO_B$, $TCK_{(0-2)}$, $TMS_{(0-2)}$, $TDO_{(0-2)}$, $\overline{TRST}_{(0-2)}$ | $V_{CC}$ = GND, $V_{IN}$ = 3.6V | | ±5.0 | µA |
| $I_{ILR}$ | $TDI_{(0-2)}$, $TDI_B$, $\overline{OE}$, $\overline{TRST}_B$, $A_{(0-1)}$, $A_B$, $TMS_B$ | $V_{IN}$ = GND | -45 | -180 | µA |
| $I_{IH}$ | $TDI_{(0-2)}$, $TDI_B$, $\overline{OE}$, $\overline{TRST}_B$, $A_{(0-1)}$, $A_B$, $TMS_B$ | $V_{IN} = V_{CC}$ | | +5.0 | µA |
| $I_{OZ}$ | Maximum TRI-STATE Leakage Current | $V_{IN}$ ($\overline{OE}$) = $V_{IH}$, $V_{IN}$ ($\overline{TRST}_B$) = $V_{IL}$, $V_O = V_{CC}$, GND | | ±5.0 | µA |

## AC Electrical Characteristics

Over recommended operating supply voltage and temperature ranges unless otherwise specified.

| Symbol | Parameter | Conditions | Typ | Max | Units |
|---|---|---|---|---|---|
| $t_{PHL1}$, $t_{PLH1}$ | Propagation Delay $TCK_B$ to $TCK_{(0-2)}$ | | 8.0 | 12.0 | ns |
| $t_{PHL2}$, $t_{PLH2}$ | Propagation Delay $TCK_B$ to $TDO_{(0-2)}$ | | 11.5 | 16.0 | ns |
| $t_{PLH3}$ | Propagation Delay $\overline{TRST}_B$ to $TMS_{(0-2)}$ | | 13.5 | 19.0 | ns |
| $t_{PHL4}$ | Propagation Delay $\overline{TRST}_B$ to $\overline{TRST}_{(0-2)}$ | | 13.0 | 19.0 | ns |
| $t_{PHL5}$, $t_{PLH5}$ | Propagation Delay $TCK_B$ to $TDO_B$ | | 10.5 | 15.0 | ns |
| $t_{PHL6}$, $t_{PLH6}$ | Propagation Delay $A_B$ to $Y_{(0-1)}$ | | 5.0 | 9.0 | ns |
| $t_{PHL7}$, $t_{PLH7}$ | Propagation Delay $A_{(0-1)}$ to $Y_B$ | | 6.5 | 10.0 | ns |
| $t_{PHL8}$, $t_{PLH8}$ | Propagation Delay $TCK_B$ to $LSP\_ACTIVE_{(0-2)}$ | | 13.0 | 19.0 | ns |
| $t_{PZL9}$, $t_{PZH9}$ | Enable Time $TCK_B$ to $TDO_{(0-2)}$ | | 12.0 | 17.0 | ns |
| $t_{PLZ10}$, $t_{PHZ10}$ | Disable Time $TCK_B$ to $TDO_{(0-2)}$ | | 11.5 | 16.0 | ns |
| $t_{PHL11}$, $t_{PLH11}$ | Propagation Delay $TCK_B$ to $TRIST_{(0-2)}$ | | 11.5 | 17.0 | ns |
| $t_{PZL12}$, $t_{PZH12}$ | Enable Time $TCK_B$ to $TDO_B$ | | 12.5 | 17.0 | ns |
| $t_{PLZ13}$, $t_{PHZ13}$ | Disable Time $TCK_B$ to $TDO_B$ | | 12.5 | 17.0 | ns |
| $t_{PHL14}$, $t_{PLH14}$ | Propagation Delay $TCK_B$ to $TRIST_B$ | | 12.5 | 18.0 | ns |

| Symbol | Parameter | Conditions | Typ | Max | Units |
|---|---|---|---|---|---|
| $t_{PHL15}$, $t_{PLH15}$ | Propagation Delay $TMS_B$ to $TMS_{(0-2)}$ | | 7.0 | 11.0 | ns |
| $t_{PHL16}$, $t_{PLH16}$ | Propagation Delay $TDI_B$ to $TDO_{(0-2)}$ | | 7.0 | 11.0 | ns |
| $t_{PZL17}$, $t_{PZH17}$ | Enable Time $\overline{OE}$ to $TMS_{(0-2)}$ | | 7.5 | 11.0 | ns |
| $t_{PLZ17}$, $t_{PHZ17}$ | Disable Time $\overline{OE}$ to $TMS_{(0-2)}$ | | 5.0 | 10.0 | ns |
| $t_{PZL18}$, $t_{PZH18}$ | Enable Time $\overline{OE}$ to $\overline{TRST}_{(0-2)}$ | | 8.0 | 11.0 | ns |
| $t_{PLZ18}$, $t_{PHZ18}$ | Disable Time $\overline{OE}$ to $\overline{TRST}_{(0-2)}$ | | 6.5 | 10.0 | ns |
| $t_{PZL19}$, $t_{PZH19}$ | Enable Time $\overline{OE}$ to $TDO_{(0-2)}$ | | 8.5 | 12.0 | ns |
| $t_{PLZ19}$, $t_{PHZ19}$ | Disable Time $\overline{OE}$ to $TDO_{(0-2)}$ | | 7.5 | 12.0 | ns |
| $t_{PHL20}$, $t_{PLH20}$ | Propagation Delay $\overline{OE}$ to $TRIST_{(0-2)}$ | | 8.0 | 13.0 | ns |
| $t_{PZL21}$, $t_{PZH21}$ | Enable Time $\overline{OE}$ to $TCK_{(0-2)}$ | | 7.5 | 11.0 | ns |
| $t_{PLZ21}$, $t_{PHZ21}$ | Disable Time $\overline{OE}$ to $TCK_{(0-2)}$ | | 6.5 | 10.0 | ns |

## AC Electrical Characteristics

Over recommended operating supply voltage and temperature ranges unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Units |
|---|---|---|---|---|
| $t_S$ | Setup Time $TMS_B$ to $TCK_B$ | | 2.0 | ns |
| $t_H$ | Hold Time $TMS_B$ to $TCK_B$ | | 1.0 | ns |
| $t_S$ | Setup Time $TDI_B$ to $TCK_B$ | | 2.0 | ns |
| $t_H$ | Hold Time $TDI_B$ to $TCK_B$ | | 1.0 | ns |
| $t_S$ | Setup Time $TDI_{(0-2)}$ to $TCK_B$ | | 1.5 | ns |
| $t_H$ | Hold Time $TDI_{(0-2)}$ to $TCK_B$ | | 1.5 | ns |
| $t_W$ | Clock Pulse Width $TCK_B$ (H or L) | | 10.0 | ns |
| $t_{WL}$ | Reset Pulse Width $\overline{TRST}_B$ (L) | | 2.5 | ns |
| $t_{REC}$ | Recovery Time $TCK_B$ from $\overline{TRST}_B$ | | 2.0 | ns |
| $F_{MAX}$ | Maximum Clock Frequency | | 25.0 | MHz |

## AC Loading and Waveforms

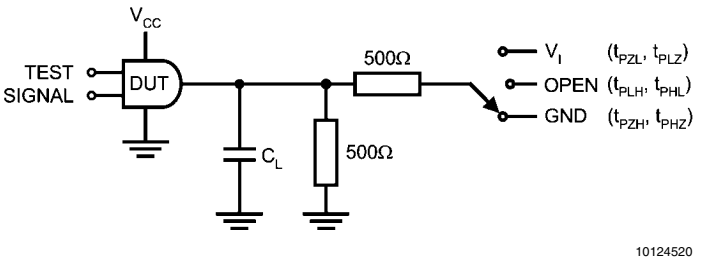



**FIGURE 14. AC Test Circuit ($C_L$ includes probe and jig capacitance)**

| $V_I$ | $C_L$ |
|---|---|
| 6.0V | 50pF |

**AC Waveforms**

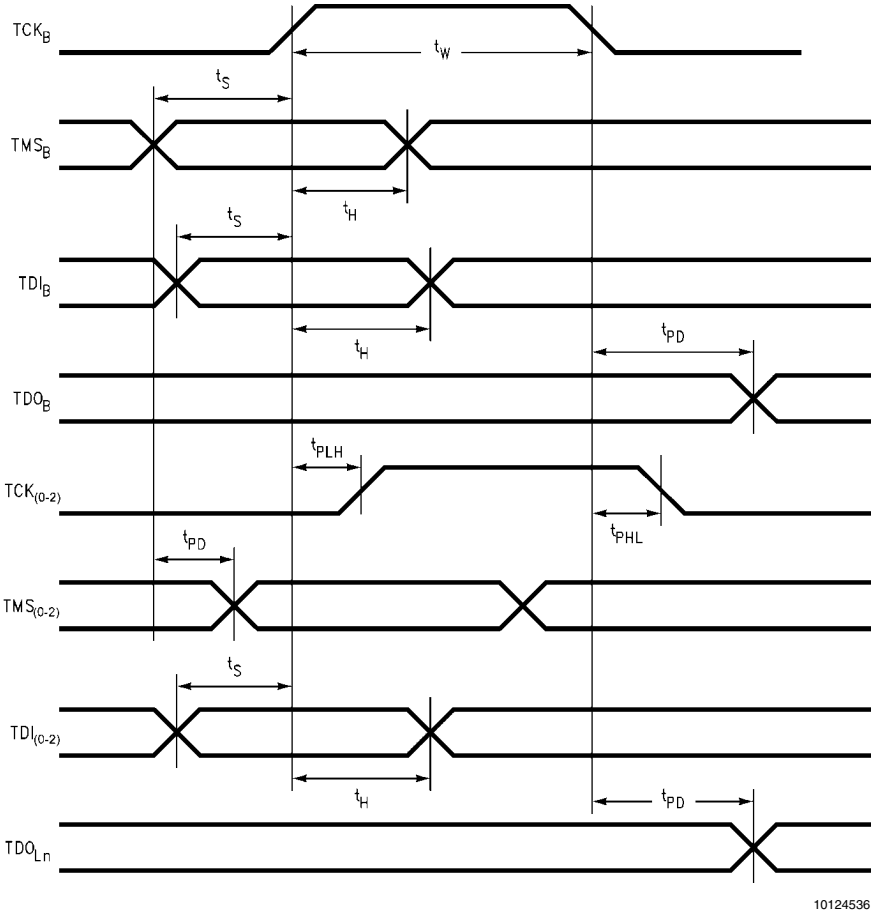



**FIGURE 15. Waveforms for an Unparked STA111 in the Shift-DR (IR) TAP Controller State**

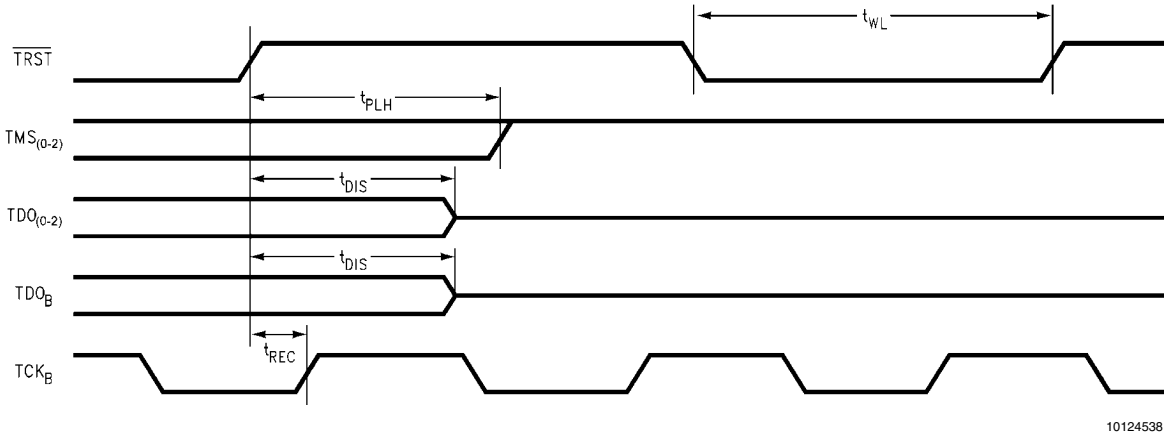



**FIGURE 16. Reset Waveforms**

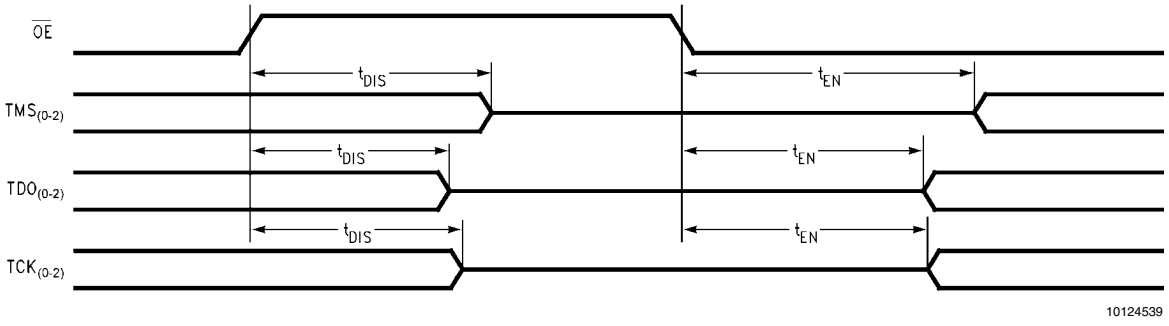
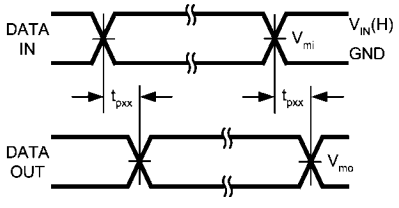
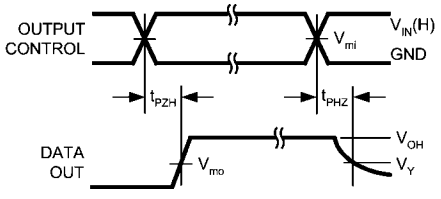


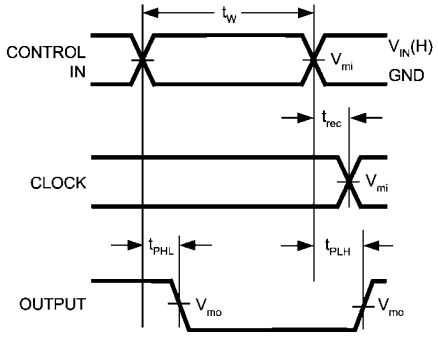

**FIGURE 17. Output Enable Waveforms**



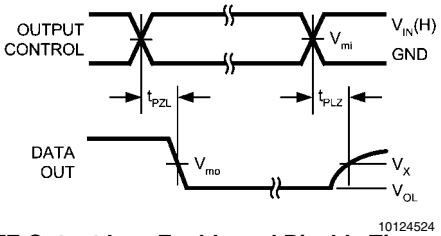

**Waveform for Inverting and Non-inverting Functions**




**TRI-STATE Output High Enable and Disable Times for Logic**




**Propagation Delay, Pulse Width and $t_{REC}$ Waveforms**




**TRI-STATE Output Low Enable and Disable Times for Logic**

**FIGURE 18. Timing Waveforms**
**(Input Characteristics; f = 1MHz, $t_r = t_f = 2.5$ns)**

| Symbol | $V_{CC}$ |
|---|---|
| | **2.7 - 3.6V** |
| $V_{IN}(H)$ | 2.7V |
| $V_{mi}$ | 1.5V |
| $V_{mo}$ | 1.5V |
| $V_x$ | $V_{OL}$ + 0.3V |
| $V_y$ | $V_{OH}$ - 0.3V |

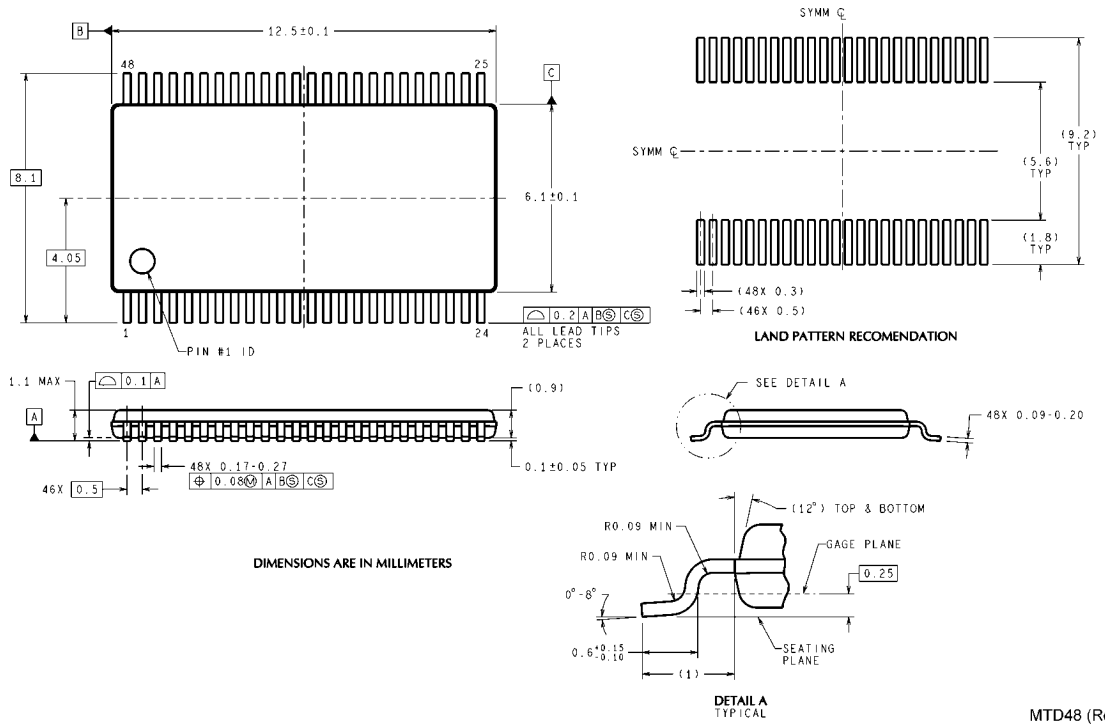
## Capacitance & I/O Characteristics

Refer to National's website for IBIS models at http://www.national.com/scan

## Revision History

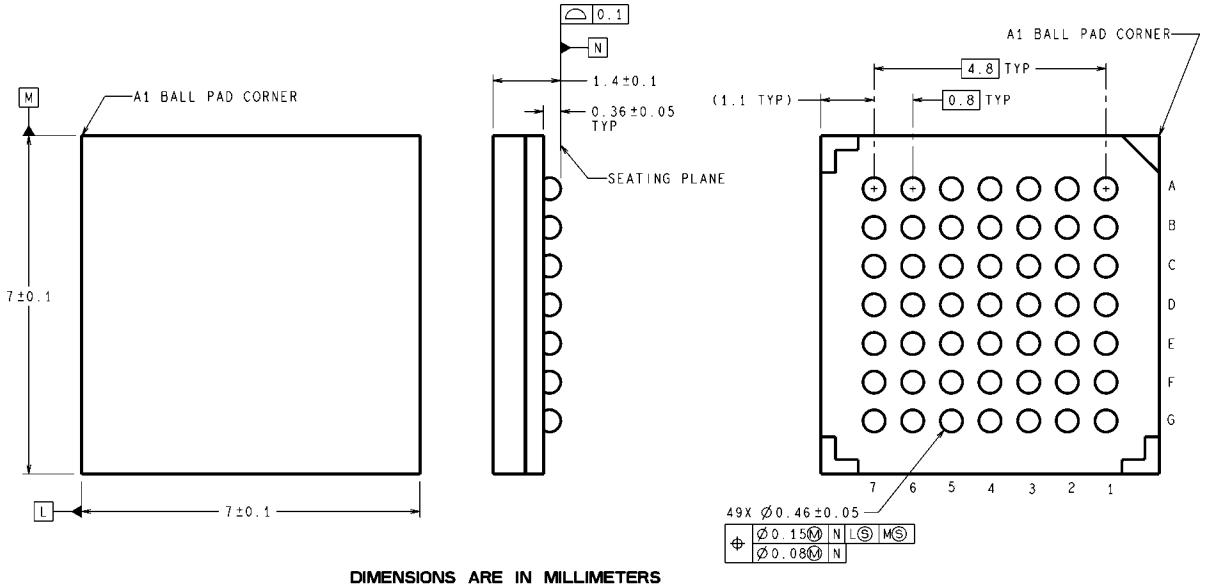
February, 2010 – Revisions to clarify shared GPIO operation in the silicon version. No specification changes or changes to operation.

## Physical Dimensions inches (millimeters) unless otherwise noted




MTD48 (Rev E)

**48-Pin TSSOP**
**NS Package Number MTD48**
**Ordering Code SCANSTA111MT**




DIMENSIONS ARE IN MILLIMETERS

SLC49A (Rev B)

**49-Pin BGA**
**NS Package Number SLC49a**
**Ordering Code SCANSTA111SM**

# Notes

# Notes

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