ANALOG DEVICES

LC²MOS Voiceband Reconstruction and Antialiasing Filter Set

AD7341/AD7371

FEATURES

AD7341 – Transmit (Reconstruction) Filter for 14-Bit DAC (AD7840)
Programmable Attenuation (0dB to −38dB)
AD7371 – Receive Filter for 14-Bit ADC (AD7871)
Programmable Gain (0dB to 24dB)
70dB Stopband Attenuation
75dB In-Band Signal-to-Noise Ratio
Better Than −75dB Total Harmonic Distortion
CCITT V.32 and V.33 Compatible
Small, 0.3", 24-Pin Plastic Package and 28-Pin PLCC

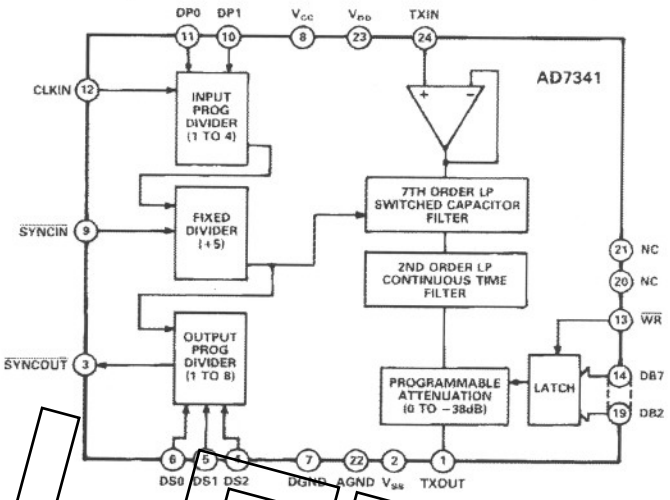
GENERAL DESCRIPTION

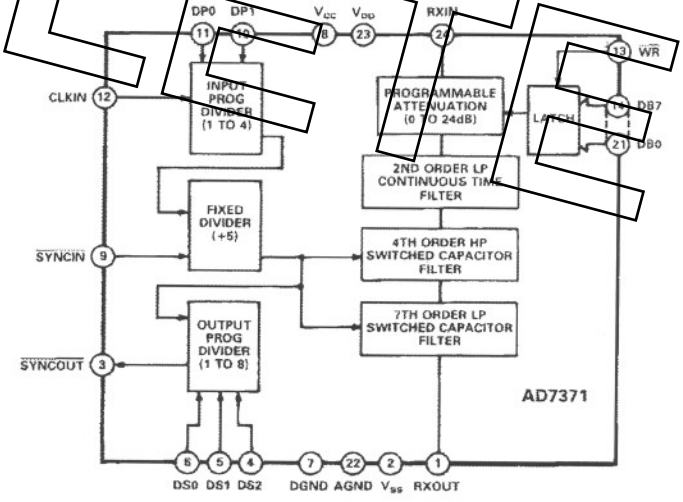
The AD7341 and AD7371 are reconstruction and antialiasing filters designed for use in high speed voiceband modems with speeds up to 14.4 kbits/sec, in accordance with CCITT V.32 and V.33 recommendations. These filters, along with the AD7840 DAC, the AD7871 ADC and a digital signal processor (DSP) can be used to implement a complete modem.

The AD7341 is the transmit or reconstruction filter. It implements the filter function using a seventh order low pass switched capacitor filter and a second order low pass continuous time filter. The cutoff frequency is 3.5kHz.

The AD7371 is the receive filter. It is a high order bandpass filter with a lower cutoff frequency of 180Hz and an upper cutoff frequency of 3.5kHz. The filter function is implemented using a second order low pass continuous time filter, a fourth order high pass switched capacitor filter and a seventh order low pass switched capacitor filter.

FUNCTIONAL BLOCK DIAGRAMS





REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106
Tel: 617/329-4700 Fax: 617/326-8703 Twx: 710/394-6577
West Coast 714/641-9391 Central 214/231-5094 Atlantic 215/643-7790

AD7341/AD7371—SPECIFICATIONS

TRANSMIT FILTER[1] (V_{DD} = V_{CC} = 5V ± 5%; V_{SS} = −5V ± 5%; AGND = DGND = 0V; CLKIN = 288kHz (M/S Ratio = 40/60 to 60/40. T_A = +25°C. Attenuator set at 0dB, unless otherwise stated.)

Parameter	AD7341JN AD7341JP	Units	Test Conditions/Comments
INPUT CHARACTERISTICS			
Input Signal Range	±3	V max	
Input Impedance	100	MΩ typ	
FILTER CHARACTERISTICS[2, 3]			
CLKIN Frequency	288	kHz	N1 = 1 (i.e., DP0 = 1, DP1 = 0)
Cutoff Frequency	3.5	kHz	0.1dB Down from the Lowest Point in the Passband
Second Harmonic	−80	dB typ	
Third and Higher Harmonics	−80	dB typ	
Passband Ripple	0.4	dB max	0≤f≤3.3kHz
Passband Gain Error	±0.5	dB max	Deviation from Nominal Setting on Programmable Attenuator
Signal-to-Noise Ratio	72	dB min	0≤f≤3.5kHz
	75	dB typ	SNR Includes Noise and Harmonics
	70	dB typ	Attenuator Set at −30dB, 0≤f≤3.5kHz
Stopband Rejection	70	dB min	f≥6.1kHz
Differential Group Delay	350	µs typ	0≤f≤3.3kHz and Referenced to the Absolute Group Delay at 1kHz
OUTPUT CHARACTERISTICS			
Output Voltage	±3	V max	R_L = 3kΩ, C_L = 100pF
Offset Voltage	±70	mV max	
Attenuation Range	0 to −36	dB	Determined by DB2–DB7, See Table III
Relative Accuracy[3, 4]	±0.1	dB typ	
Output Resistance	0.2	Ω typ	
LOGIC INPUTS $\overline{WR}$, DB2–DB7, DP0, DP1, DS0–DS2, $\overline{SYNCIN}$, CLKIN			
V_{INH}, Input High Voltage	2.0	V min	
V_{INL}, Input Low Voltage	0.8	V max	
I_{INH}, Input Current	10	µA max	
C_{IN}, Input Capacitance	10	pF max	
CLKIN Divider Range (N1)[5]	1 to 4		CLKIN Can Be Set to 288kHz, 576kHz, 864kHz or 1.152MHz. N1 Is Set by DP0, DP1.
LOGIC OUTPUTS $\overline{SYNCOUT}$[6]			
Divider Range (N2)	1 to 8		N2 Is Set by DS0–DS2.
Frequency	$f_{CLKIN}/(N1\times5\times N2)$	kHz	
Pulse Width	$1/f_{CLKIN}$	µs	
V_{OH}, Output High Voltage	2.4	V min	I_{SOURCE} = 400µA
V_{OL}, Output Low Voltage	0.4	V max	I_{SINK} = 1.6mA
POWER SUPPLIES			
V_{DD}	4.75/5.25	V min/V max	
V_{CC}	4.75/5.25	V min/V max	
V_{SS}	−4.75/−5.25	V min/V max	
I_{DD} + I_{CC}	25	mA max	
I_{SS}	25	mA max	
Power Dissipation	265	mW max	

NOTES
[1]Operating temperature ranges as follows: J versions: 0 to +70°C.
[2]Specified for an input frequency of 288kHz. This is internally divided by 5 to produce a switched capacitor filter frequency of 57.6kHz. For input frequencies lower than 288kHz, the filter response is shifted down by the ratio of this input frequency to 288kHz.
[3]Measured using a ±3V, 1kHz sine wave.
[4]Measured over the full attenuation range.
[5]Required to derive internal frequency of 288kHz from CLKIN.
[6]Determined by data transmission rate.

Specifications subject to change without notice.

RECEIVE FILTER[1] (V_{DD} = V_{CC} = 5V ± 5%; V_{SS} = −5V ± 5%; AGND = DGND = 0V; CLKIN = 288kHz M/S Ratio = 40/60 to 60/40. T_A = +25°C. PGA set at 0dB, unless otherwise stated.)

Parameter	AD7371JN AD7371JP	Units	Test Conditions/Comments
INPUT CHARACTERISTICS			
Input Signal Range	±3	V max	
Input Impedance	10	kΩ typ	
FILTER CHARACTERISTICS[2, 3]			
CLKIN Frequency	288	kHz	N1 = 1 (i.e., DP0 = 1, DP1 = 0)
Lower Cutoff Frequency	180	Hz	0.1dB Down from the Lowest Point in the Passband
Upper Cutoff Frequency	3.5	kHz	0.1dB Down from the Lowest Point in the Passband
Second Harmonic	−80	dB typ	
Third and Higher Harmonics	−80	dB typ	
Passband Ripple	0.4	dB max	200Hz≤f≤3.3kHz
Passband Gain Error	±0.5	dB max	Deviation from Nominal Setting on PGA
Signal-to-Noise Ratio	72	dB min	180Hz≤f≤3.5kHz
	75	dB typ	
	60	dB typ	Input Signal Level of −24dB; PGA Gain Set at +24dB
Stopband Rejection	66	dB min	f≥6.1kHz
	40	dB typ	f≥60kHz
Differential Group Delay	300	µs typ	500Hz≤f≤3.3kHz and Referenced to the Absolute Group Delay at 1kHz
OUTPUT CHARACTERISTICS			
Output Voltage	±3	V max	R_L = 3kΩ, C_L = 100pF
Offset Voltage	±70	mV max	
Gain Range	0 to +24	dB	Determined by DB0–DB7, see Table VI
Relative Accuracy[3, 4]	±0.1	dB typ	
Output Resistance	0.2	Ω typ	
LOGIC INPUTS			
$\overline{WR}$, DB0–DB7, DP0, DP1, DS0–DS2, $\overline{SYNCIN}$, CLKIN			
V_{INH}, Input High Voltage	2.0	V min	
V_{INL}, Input Low Voltage	0.8	V max	
I_{INH}, Input Current	10	µA max	
C_{IN}, Input Capacitance	10	pF max	
CLKIN Divider Range (N1)[5]	1 to 4		CLKIN Can Be Set to 288kHz, 576kHz, 864kHz or 1.152MHz. N1 Is Set by DP0, DP1.
LOGIC OUTPUTS $\overline{SYNCOUT}$[6]			
Divider Range (N2)	1 to 8		N2 Is Set by DS0–DS2.
Frequency	$f_{CLKIN}/(N1\times5\times N2)$	kHz	
Pulse Width	$1/f_{CLKIN}$	µs	
V_{OH}, Output High Voltage	2.4	V min	I_{SOURCE} = 400µA
V_{OL}, Output Low Voltage	0.4	V max	I_{SINK} = 1.6mA
POWER SUPPLIES			
V_{DD}	4.75/5.25	V min/V max	
V_{CC}	4.75/5.25	V min/V max	
V_{SS}	−4.75/−5.25	V min/V max	
I_{DD} + I_{CC}	25	mA max	
I_{SS}	25	mA max	
Power Dissipation	265	mW max	

NOTES
[1]Operating temperature ranges as follows: J versions: 0 to +70°C.
[2]Specified for an input frequency of 288kHz. This is internally divided by 5 to produce a switched capacitor filter frequency of 57.6kHz. For input frequencies lower than 288kHz, the filter response is shifted down by the ratio of this input frequency to 288kHz.
[3]Measured using a ±3V, 1kHz sine wave.
[4]Measured over the full attenuation range.
[5]Required to derive a switched capacitor filter frequency of 288kHz from CLKIN.
[6]Determined by data transmission rate.

Specifications subject to change without notice.

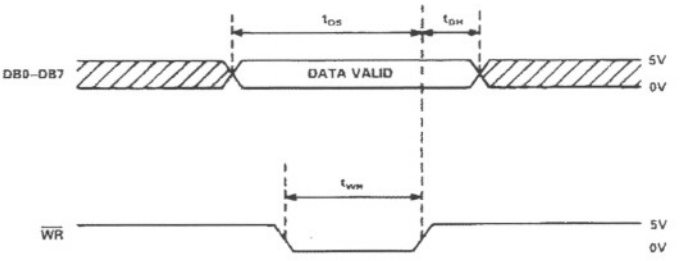
AD7341/AD7371

TIMING CHARACTERISTICS[1]

($V_{DD} = V_{CC} = +5V \pm 5\%$, $V_{SS} = -5V \pm 5\%$)

Parameter	Limit at $T_A = +25°C$	Units	Comments
t_{WR}	80	ns min	Write Pulse Width
t_{DS}	60	ns min	Data Setup Time
t_{DH}	20	ns min	Data Hold Time
t_{SYNCIN}	80	ns min	$\overline{SYNCIN}$ Pulse Width

NOTE
[1]Timing specifications are sample tested at +25°C to ensure compliance. All input control signals are specified with $t_R = t_F = 20ns$ (10% to 90% of +5V) and timed from a voltage level of +1.6V.
Specifications subject to change without notice.



NOTES
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% to 90% of +5V. tr = tf = 20ns.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $(V_{IH} + V_{IL})/2$.

Figure 1. AD7341/AD7371 Timing Diagram

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to AGND . . . . . −0.3V to +7V
V_{CC} to DGND . . . . . −0.3V to +7V
V_{DD} to V_{CC} . . . . . −0.6V to +0.6V
V_{SS} to DGND . . . . . +0.3V to −7V
AGND to DGND . . . . . −0.3V to V_{CC}
RXIN, TXIN to AGND . . . . . V_{SS} −0.3V to V_{DD} + 0.3V
RXOUT, TXOUT to AGND[1] . . . V_{SS} −0.3V to V_{DD} + 0.3V
Digital Input Voltage to DGND . . . . −0.3V to V_{CC} + 0.3V
Power Dissipation (Any Package) to +75°C 1000mW
Operating Temperature Range
J Versions . . . . . 0 to +70°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10secs) . . . . . +300°C

NOTE
[1]RXOUT, TXOUT may be shorted to AGND, DGND, V_{DD}, V_{CC}, V_{SS} provided that the power dissipation of the package is not exceeded.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability. Only one absolute maximum rating may be applied at any one time.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

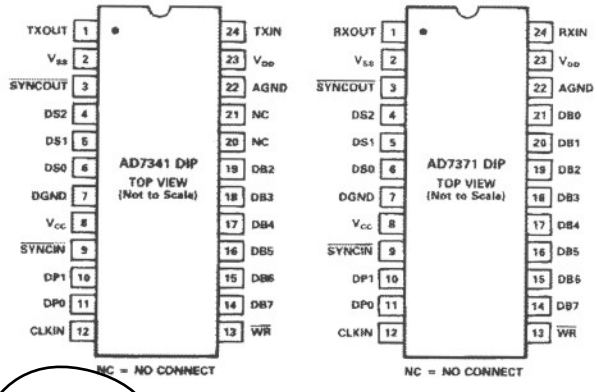
ORDERING GUIDE

Model	Function	Temperature Range	Package Option*
AD7341JN	Transmit Filter	0°C to +70°C	N-24
AD7341JP	Transmit Filter	0°C to +70°C	P-28A
AD7371JN	Receive Filter	0°C to +70°C	N-24
AD7371JP	Receive Filter	0°C to +70°C	P-28A

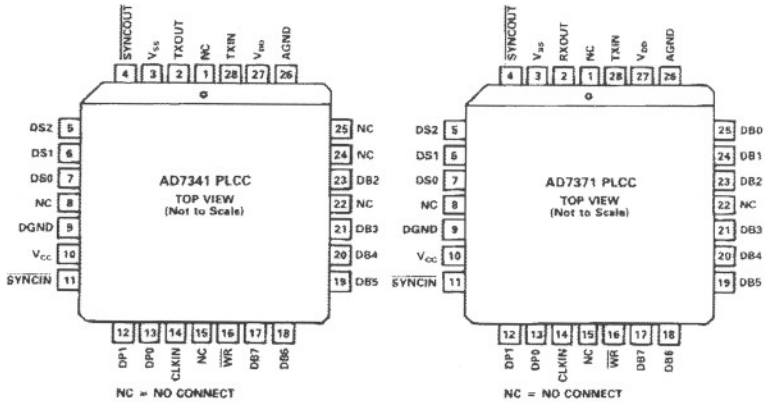
*N = Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC).

PIN CONFIGURATIONS

DIP



PLCC



TERMINOLOGY

Cutoff Frequency

The filter cutoff frequency is the point in the response where the amplitude begins to fall off. For the AD7341 and AD7371 it is defined as 0.1dB down from the lowest point in the passband. The AD7341 low pass filter has one cut off frequency at 3.5kHz while the AD7371 band pass filter has a lower cutoff frequency of 180Hz and an upper cutoff frequency of 3.5kHz.

Signal-to-Noise Ratio (SNR)

Signal-to-noise ratio (SNR) is the measured signal to noise at the output of the filter. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all nonfundamental signals (including harmonics) up to 3.5kHz.

Second Harmonic

Second harmonic is the ratio of the second harmonic amplitude to the fundamental amplitude, expressed in dBs.

Third and Higher Harmonics

This is the amplitude ratio of the rms sum of the third and higher harmonics to the fundamental, expressed in dBs. Total harmonic distortion (THD) is the rms sum of the second harmonic and the third and higher harmonics.

Passband Ripple

This is the ripple in the passband section of the frequency response and is expressed in dBs. For the AD7341, it is measured in the band 0 to 3.3kHz, and for the AD7371 it is measured in the band 200Hz to 3.3kHz.

Passband Gain Error

Passband gain error is the deviation of the actual passband level from the ideal passband level. For the AD7341, it is measured with the attenuation set to 0dB (DB2–DB7 = 1); for the AD7371, it is measured with the gain set to 0dB (DB0–DB7 = 1).

Stopband Rejection

This is the magnitude of the stopband response relative to the passband magnitude. The stopband is specified for frequencies greater than 6.1kHz.

Differential Group Delay

Absolute group delay is the rate of change of phase versus frequency, d0/df. For the AD7341 and AD7371, differential group delay is the absolute group delay in a specified band relative to the absolute group delay at 1kHz. The specified band for the AD7341 is 0 to 3.3kHz and for the AD7371 it is 500Hz to 3.3kHz.

Offset Voltage

This is the amount of offset introduced into the input signal by the filter. For the AD7341 it is measured with the attenuation set at 0dB, and for the AD7371 it is measured with the gain set at 0dB.

Attenuation Range

For the AD7341, this is the amount by which the output can be attenuated, using the digital inputs DB7–DB2. Table I gives a selection of attenuations for various values of digital input.

Gain Range

For the AD7371, this is the amount by which the input can be amplified, using the digital inputs DB7–DB0. Table VI gives gain versus digital input code.

Relative Accuracy

This is a measure of the accuracy with which either the AD7341 attenuation or the AD7371 gain can be programmed, having allowed for the passband gain error. It is expressed in dBs relative to attenuation or gain setting with a digital input code of all 1s.

AD7341/AD7371

TYPICAL PERFORMANCE CURVES ($V_{DD} = V_{CC} = +5V$, $V_{SS} = -5V$, $f_{CLKIN} = 288kHz$, $T_A = +25°C$ unless otherwise stated)

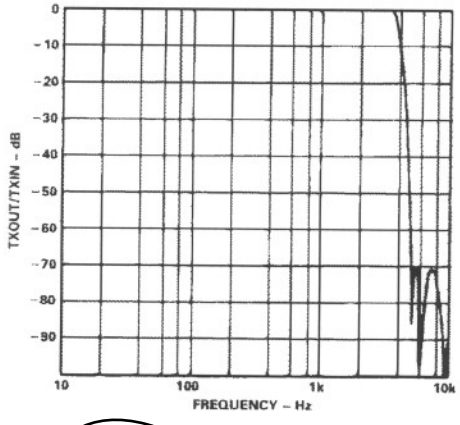


Figure 2. AD7341 Amplitude Response

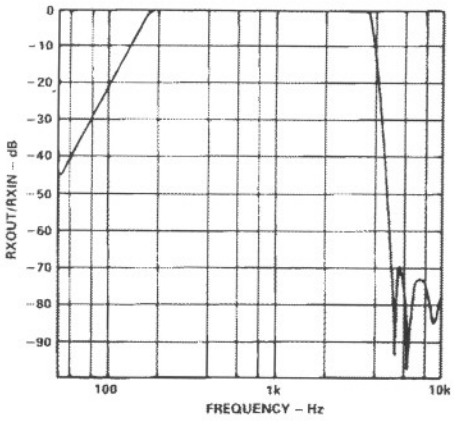


Figure 3. AD7371 Amplitude Response

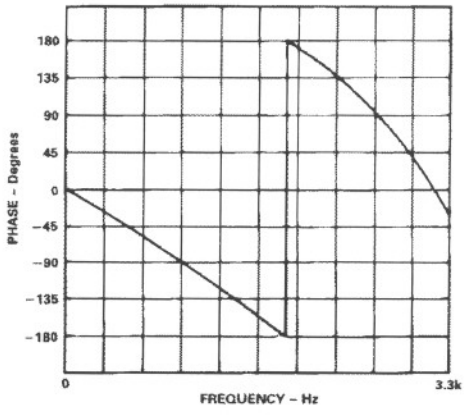


Figure 4. AD7341 Phase Response

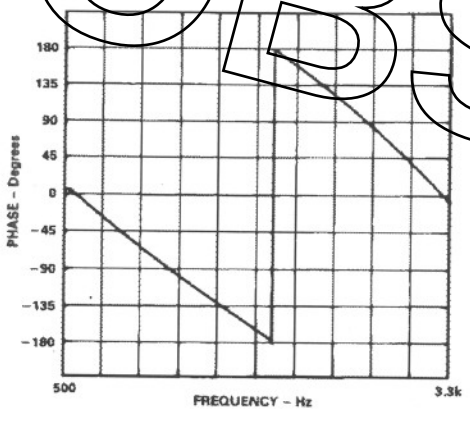


Figure 5. AD7371 Phase Response

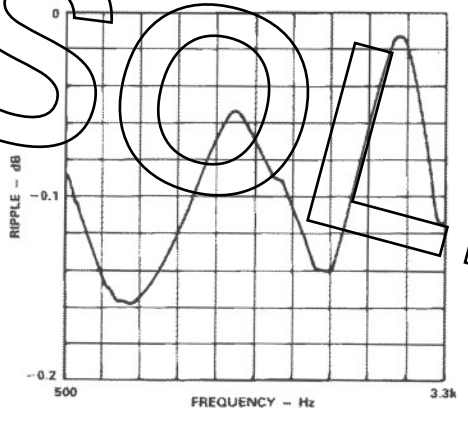


Figure 6. Passband Ripple in the AD7341/AD7371

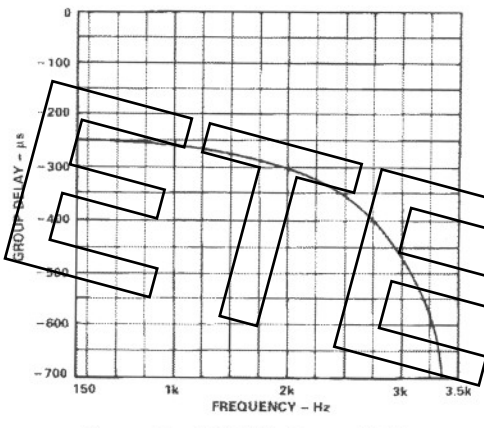


Figure 7. AD7341 Group Delay

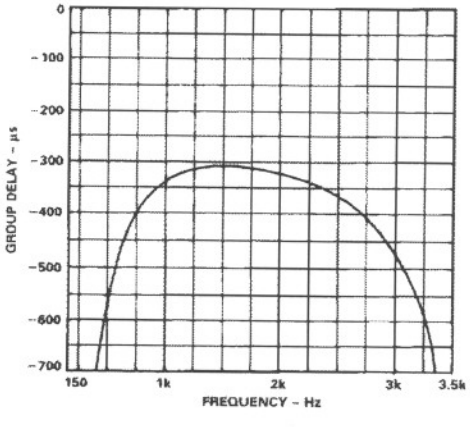


Figure 8. AD7371 Group Delay

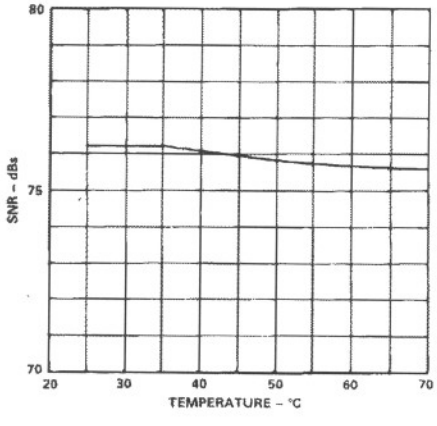


Figure 9. AD7341 SNR vs. Temperature

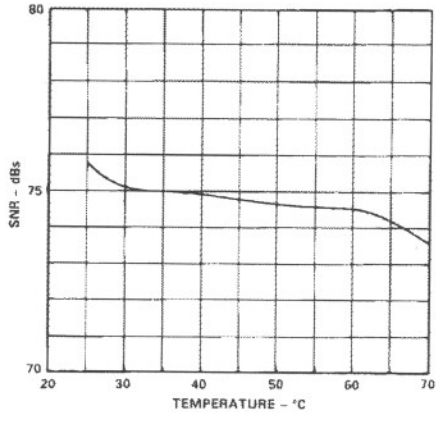


Figure 10. AD7371 SNR vs. Temperature

AD7341 DIP PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
1	TXOUT	Signal output pin from filter.
2	V_{SS}	Negative supply pin for the device. This is −5V ± 5%.
3	$\overline{SYNCOUT}$	This output pulse is derived from the SCF (Switched Capacitor Filter) clock and can be used in system synchronization. The pulse frequency is $f_{SYNCOUT} = f_{CLKIN} / (N1 \times 5 \times N2)$, where f_{CLKIN} is the input frequency at CLKIN, N1 is the value loaded to the input programmable divider and N2 is the value loaded to the output programmable divider. N1 is set by DP0 and DP1 (see Table II). N2 is set by DS0, DS1 and DS2 and varies from 1 to 8. Table I shows the typical $\overline{SYNCOUT}$ frequencies which can be set when f_{CLKIN} is 288kHz and N1 is 1.
4	DS2	Unlatched digital input which is used to set $\overline{SYNCOUT}$ frequency. See Table I.
5	DS1	Unlatched digital input which is used to set $\overline{SYNCOUT}$ frequency. See Table I.
6	DS0	Unlatched digital input which is used to set $\overline{SYNCOUT}$ frequency. See Table I.
7	DGND	Ground point for on chip digital circuitry.
8	V_{CC}	Positive supply pin for the on chip digital circuitry. This is +5V ± 5%.
9	$\overline{SYNCIN}$	This asynchronous digital input resets the internal clock circuitry from which $\overline{SYNCOUT}$ is derived. This allows $\overline{SYNCOUT}$ to be synchronized to an external signal.
10	DP1	Unlatched digital input pin which is used to set divide ratio on the CLKIN input. See Table II.
11	DP0	Unlatched digital input pin which is used to set divide ratio on the CLKIN input. See Table II.
12	CLKIN	Clock input for the device. This is internally divided to produce the SCF clock.
13	$\overline{WR}$	Active low digital input. Data for the on chip programmable attenuation is loaded to the input latch when this signal goes low and is latched when it goes high.
14–19	DB7–DB2	Six-bit data bus which sets the attenuation level on the output. See Table III.
20	NC	No connect.
21	NC	No connect.
22	AGND	Ground point for the on-chip analog circuitry.
23	V_{DD}	Positive supply pin for the on-chip analog circuitry. This is +5V ± 5%.
24	TXIN	Filter input.

Table I. Setting $\overline{SYNCOUT}$ Frequency Using DS2, DS1, DS0

DS2	DS1	DS0	$\overline{SYNCOUT}$ Frequency
0	0	0	7.2kHz
0	0	1	57.6kHz
0	1	0	28.8kHz
0	1	1	19.2kHz
1	0	0	14.4kHz
1	0	1	11.52kHz
1	1	0	9.6kHz
1	1	1	8.22kHz

Table II. Setting CLKIN Divide Ratio Using DP1, DP0

DP1	DP0	CLKIN Divide Ratio, N1
0	0	4
0	1	1
1	0	2
1	1	3

Table III. Output Attenuation vs. Digital Input Code

DB7	DB6	DB5	DB4	DB3	DB2	Attenuation dB
1	1	1	1	1	1	0
0	1	1	1	1	1	−6
0	0	1	1	1	1	−12
0	0	0	1	1	1	−18
0	0	0	0	1	1	−24
0	0	0	0	0	1	−30
0	0	0	0	0	0	−38

AD7341/AD7371

AD7371 DIP PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
1	RXOUT	Signal output pin from filter.
2	V_{SS}	Negative supply pin for the device. This is −5V ± 5%.
3	$\overline{SYNCOUT}$	This output pulse is derived from the SCF (switched capacitor filter) clock and can be used in system synchronization. The pulse frequency is $f_{SYNCOUT} = f_{CLKIN} / (N1 \times 5 \times N2)$, where f_{CLKIN} is the input frequency at CLKIN, N1 is the value loaded to the input programmable divider and N2 is the value loaded to the output programmable divider. N1 is set by DP0 and DP1 (see Table V). N2 is set by DS0, DS1 and DS2 and varies from 1 to 8. Table IV shows the typical $\overline{SYNCOUT}$ frequencies which can be set when f_{CLKIN} is 288kHz and N1 is 1.
4	DS2	Unlatched digital input which is used to set $\overline{SYNCOUT}$ frequency. See Table IV.
5	DS1	Unlatched digital input which is used to set $\overline{SYNCOUT}$ frequency. See Table IV.
6	DS0	Unlatched digital input which is used to set $\overline{SYNCOUT}$ frequency. See Table IV.
7	DGND	Ground point for on chip digital circuitry.
8	V_{CC}	Positive supply pin for the on chip digital circuitry. This is +5V ± 5%.
9	$\overline{SYNCIN}$	This digital input resets the internal clock circuitry from which $\overline{SYNCOUT}$ is derived. This allows $\overline{SYNCOUT}$ to be synchronized to an external signal.
10	DP1	Unlatched digital input pin which is used to set divide ratio on the CLKIN input. See Table V.
11	DP0	Unlatched digital input pin which is used to set divide ratio on the CLKIN input. See Table V.
12	CLKIN	Clock input for the device. This is internally divided to produce the SCF clock.
13	$\overline{WR}$	Active low digital input. Data for the on chip programmable gain is loaded to the input latch when this signal goes low and is latched when it goes high.
14–21	DB7–DB0	Eight-bit data bus which sets the gain level on the input. See Table VI.
22	AGND	Ground point for the on-chip analog circuitry.
23	V_{DD}	Positive supply pin for the on-chip analog circuitry. This is +5V ± 5%.
24	RXIN	Filter input.

Table IV. Setting $\overline{SYNCOUT}$ Frequency Using DS2, DS1, DS0

DS2	DS1	DS0	$\overline{SYNCOUT}$ Frequency
0	0	0	7.2kHz
0	0	1	57.6kHz
0	1	0	28.8kHz
0	1	1	19.2kHz
1	0	0	14.4kHz
1	0	1	11.52kHz
1	1	0	9.6kHz
1	1	1	8.22kHz

Table V. Setting CLKIN Divide Ratio Using DP1, DP0

DP1	DP0	CLKIN Divide Ratio, N1
0	0	4
0	1	1
1	0	2
1	1	3

Table VI. Input Gain vs. Digital Input Code

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Gain dB
0	0	0	0	0	0	0	0	24
0	0	0	0	0	1	1	1	21
0	0	0	1	0	0	0	1	18
0	0	0	1	1	1	1	1	15
0	0	1	1	0	0	1	1	12
0	1	0	1	0	0	0	0	9
0	1	1	1	1	0	0	0	6
1	0	1	1	0	0	0	0	3
1	1	1	1	1	1	1	1	0

CIRCUIT DESCRIPTION

AD7341 Filter

The AD7341 transmit filter performs the reconstruction or smoothing function for the transmit channel D/A converter. Figure 11 is the block diagram for the filter and programmable attenuation section.

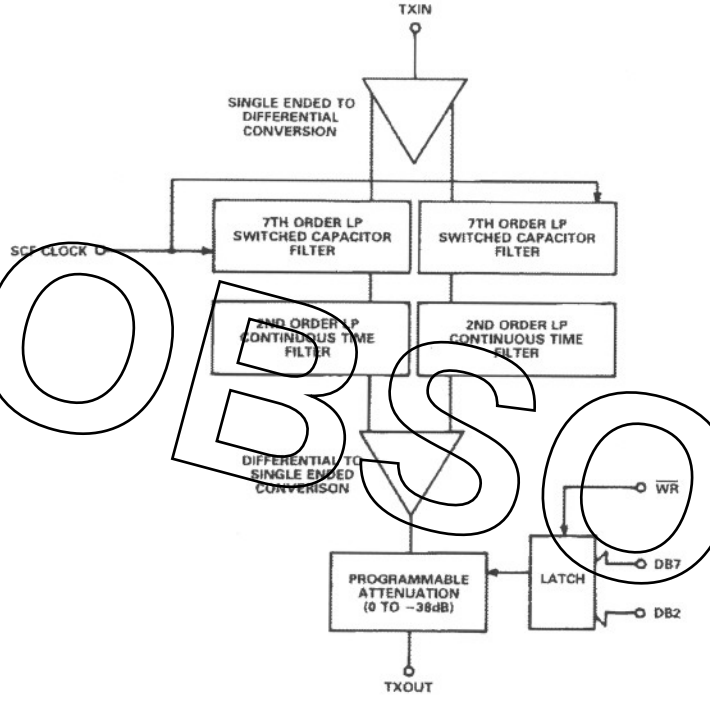


Figure 11. AD7341 Filter Section

The transmit channel signal is applied at TXIN and is converted to a differential signal. It then goes to the fully differential switched capacitor low pass section. This is a seventh order elliptical filter which gives a 3.5kHz cut off frequency and stopband attenuation of greater than 70dB at frequencies above 6.1kHz. The use of the differential filter structure ensures an excellent harmonic distortion figure and also gives improved rejection of common mode noise such as clock feedthrough in the switched capacitor switching transistors. The filter cut off frequency depends directly on the clock driving the switched capacitor section and upon the capacitor matching. Capacitor matching is typically better than 2% and this means that if the clock is constant, cut off frequency variation from device to device will be less than 2%. Since the switched capacitor filters are sampled data systems (analog data) with a sampling frequency of 57.6kHz, they must be followed by a smoothing filter to remove aliased components due to this clock. This smoothing filter is a second order low pass continuous time section. The differential outputs of the two smoothing filters are then recombined to a single ended signal. The level of SCF clock feedthrough at the output is typically −65dB. This can be further reduced by using a simple RC combination at the output (39kΩ and 1000pF reduce the feedthrough to −80dB). The second order filter shown in Figure 22 reduces it to below −90dB. After recombination of the differential signals, a programmable attenuation stage follows. The attenuator circuit diagram is shown in Figure 12. It consists of an 8-bit multiplying DAC with the two LSBs (DB1, DB0) tied high. The transfer function is given by:

$$A = -20 \log \frac{256}{4N+3}$$

where A is the attenuation in dBs and N is the 6-bit binary code loaded to the device. Expressing N in terms of A gives:

$$N = \frac{1}{4}\left[\frac{256}{10^{A/20}} - 3\right]$$

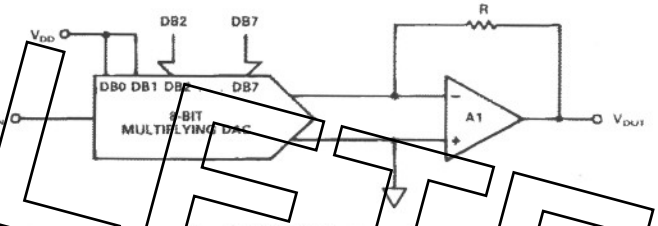


Figure 12. AD7341 Output Attenuator

This allows the calculation of the device input code for a given output attenuation. The attenuation range is 0 to 38dB and allows the user to adapt the output signal for different line specifications. Figure 13 shows how attenuation varies with input code, and Table III gives a selection of attenuations for specific codes.

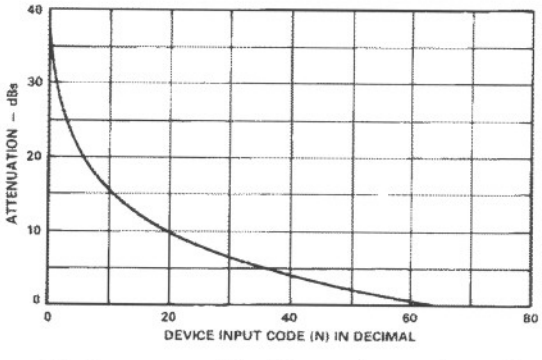


Figure 13. Programmable Attenuation vs. Input Code for the AD7341

AD7341/AD7371

AD7371 Filter

The receive filter performs the antialiasing function for the receive channel A/D converter. It provides rejection of high frequency out-of-band signals, attenuation of low frequency noise at both 50Hz and 60Hz line frequencies and programmable gain for the input signal. Figure 14 is the block diagram for the filter and programmable gain section.

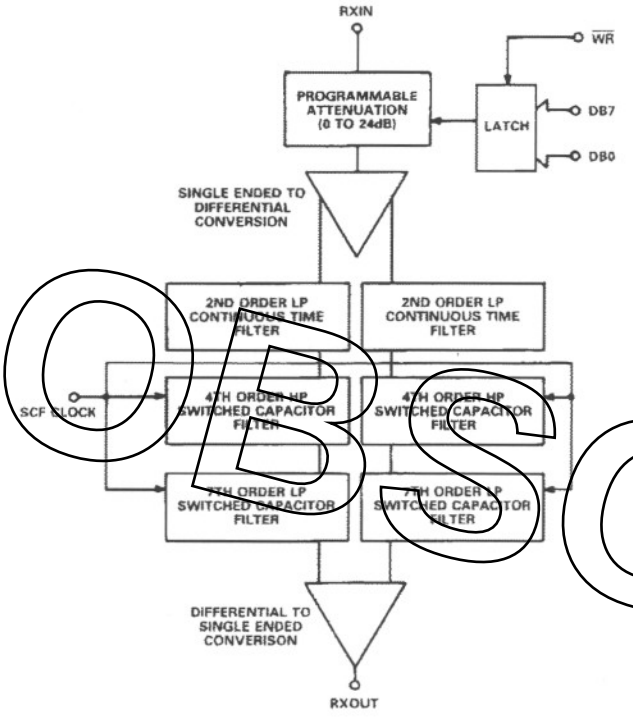


Figure 14. AD7371 Filter Section

The input signal is applied at RXIN and passes through the programmable gain stage. Figure 15 shows the circuit diagram for this. It consists of an 8-bit multiplying DAC and resistor combination in the feedback loop of an operational amplifier. The transfer function is given by:

$$G = 20 \log \frac{272.2}{N+17.2}$$

G is the gain in dBs and N is the 8-bit binary code loaded to the device. Varying this code between 0 and 255 gives a gain range of 24dB to 0dB. Expressing N in terms of G gives:

$$N = \frac{272.2}{10^{G/20}} - 17.2$$

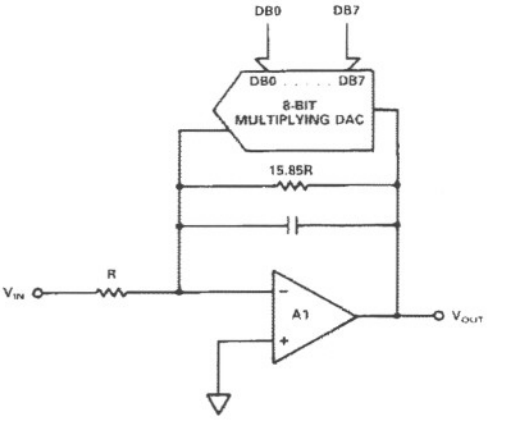


Figure 15. AD7371 Programmable Gain Amplifier

This equation can be used to calculate the code, N, needed to give the desired gain, G. Figure 16 is a graph of gain versus input code, and Table VI gives a selection of gains for specific codes.

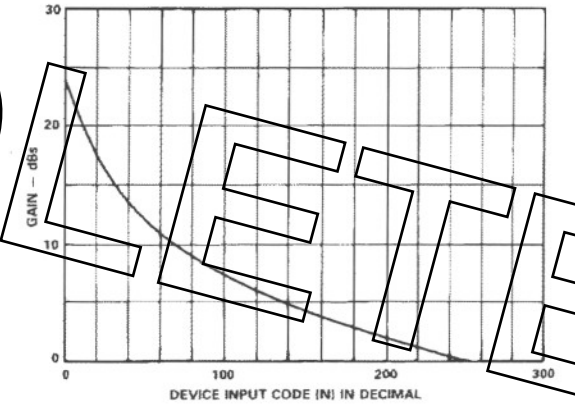


Figure 16. Programmable Gain vs. Input Code for the AD7371

After the PGA stage, the receive signal is converted to a fully differential signal before going to the differential filters. The first differential filter is a second order continuous time section. This is necessary to provide antialiasing for the sampling switched capacitor filter. The continuous time filter eliminates any high frequency components from the input signal which would be aliased back into the passband of the switched capacitor filter and appear as noise. Following the continuous time filter, the fourth order elliptical high pass switched capacitor section has a cutoff frequency of 180Hz, and the seventh order elliptical low pass switched capacitor section has a cutoff frequency of 3.5kHz. As in the reconstruction filter, the cutoff frequency variation from device to device for fixed CLKIN is typically less than 2%. On recombination of the differential signals, the output goes to RXOUT.

SCF Clock and System Synchronization

The clock generation circuitry for both the AD7341 and the AD7371 is identical and is shown in Figure 17. For the specified filter response, the switched capacitor clock must be 57.6kHz. This means that CLKX in Figure 17 must always be 288kHz (57.6kHz×5). The input programmable divider allows the user the option of four CLKIN frequencies (288kHz, 576kHz, 864kHz or 1152kHz). The input divider can then be programmed to ensure that CLKX is 288kHz.

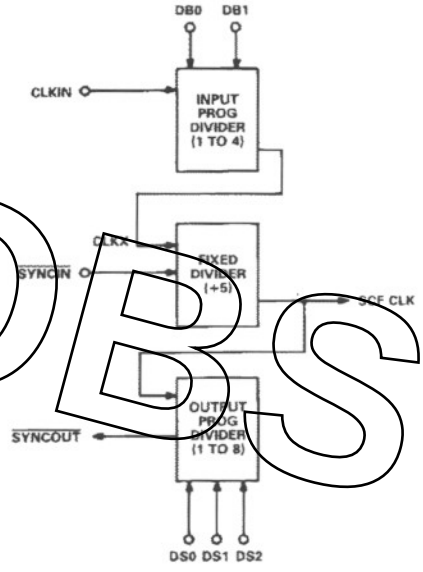


Figure 17. AD7341/AD7371 Clock Generation Circuitry

The AD7341 and the AD7371 are always used with a DAC and ADC respectively. The DAC and ADC update and sample at a certain rate (9.6kHz or 7.2kHz, for example). The filters sample at 57.6kHz. In order to ensure that there is no low frequency aliasing, the DAC/ADC rate must be synchronized with the SCF clock. This means the SCF rate must be an integral multiple of the DAC/ADC rate. The AD7341/AD7371 actually generates this required synchronized clock on chip. The output programmable divider allows division of the SCF clock by 1 to 8. The divide ratio is determined by inputs DS0–DS2. The output of the programmable divider goes to $\overline{\text{SYNCOUT}}$ which is then used to drive either the $\overline{\text{CONVST}}$ input of an ADC or the $\overline{\text{LDAC}}$ input of a DAC. The output programmable divider also has a reset input ($\overline{\text{SYNCIN}}$). This is normally tied high. When it is brought low, the counter is reset. On returning high, the counter is reactivated. By using this $\overline{\text{SYNCIN}}$ facility, it is possible to adjust the point in time at which sampling occurs while maintaining the same rate. This is useful in modem applications and is known as cycle slipping. Figure 18 shows the complete timing waveforms for the AD7341/AD7371.

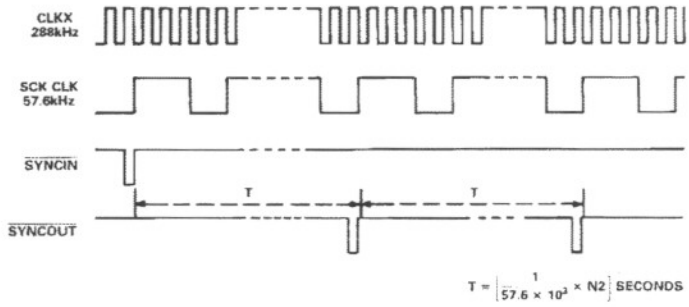


Figure 18. AD7341/AD7371 Timing Waveforms

APPLYING THE AD7341/7371

The prime application for the AD7341/7371 is in the analog front end for echo-cancelling modems. Here, the filters are combined with a high resolution DAC and ADC to provide the interface between the analog and the digital domain. The excellent noise performance of the AD7371 and the high resolution of the AD7871 (14-bit ADC) combine to allow the modem echo-cancelling loop to be implemented totally in the digital domain. This overcomes the disadvantage with lower resolution systems which need to do a digital approximation of the echo and reconstruct in analog form for an analog echo-cancelling loop.

Conversely, in the modem transmitter, the combination of AD7341 and high resolution DAC (14-bit AD7840) allows transmission of the signal with minimum impairments to the line.

Figure 19 shows a typical hardware interface between the analog front end chipset and the ADSP-2101 in an echo-cancelling modem. The ADSP-2101 is the new DSP microcomputer from Analog Devices. It has program memory and data memory on chip

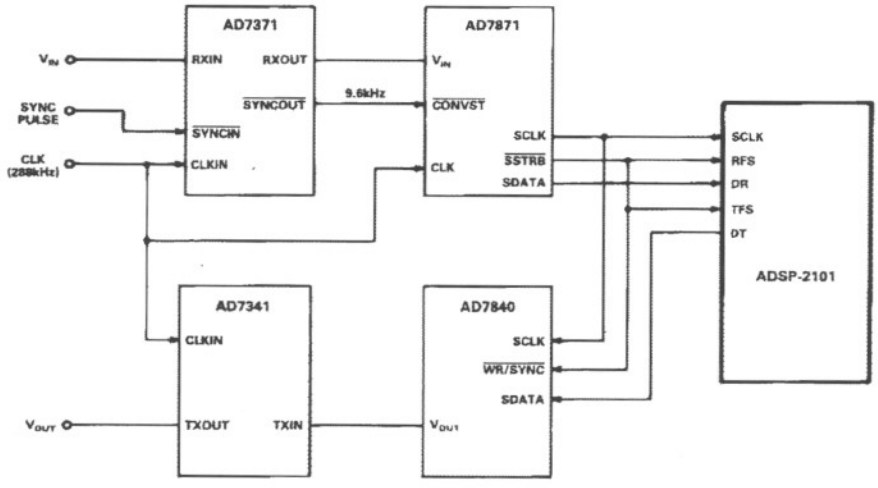


Figure 19. Modem Analog Front End and Interface to ADSP-2101 DSP

AD7341/AD7371

and is code compatible with the ADSP-2100. It also has two serial ports. The particular configuration, shown in Figure 19, uses the serial interface on both the AD7840 and AD7871 to talk to one of the ADSP-2101 serial ports. The system timing diagram is shown on Figure 20. The 288kHz clock drives the two filters and the ADC. The $\overline{\text{SYNCIN}}$ pulse may be used to set the absolute sampling instant. DS0, DS1 and DS2 on the AD7371 are programmed to give a 9.6kHz $\overline{\text{SYNCOUT}}$ signal. This drives the AD7871 $\overline{\text{CONVST}}$ input and is thus the sampling rate. SCLK on the AD7871 clocks out serial data on its rising edge. $\overline{\text{SSTRB}}$ is the framing pulse for the serial data. Within this framing pulse, a 16-bit data stream is output on the SDATA line. Each data bit is valid on the falling edge of SCLK. There are two leading zeros and the 14-bit conversion result appears after these. When RFS on the ADSP-2101 goes low, data appearing on DR is clocked into the receive shift register on each falling edge of SCLK. Once the 16 data bits have been received an internal interrupt is set and the processor can read the data.

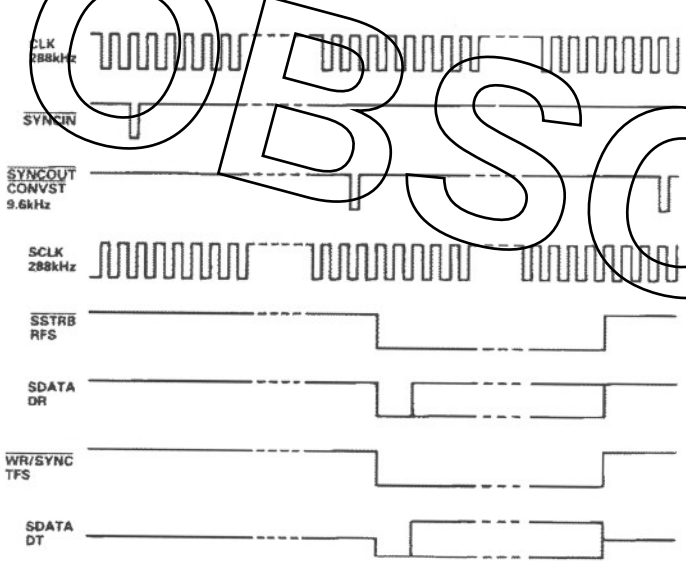


Figure 20. System Timing for Figure 19

The circuit of Figure 19 also uses the $\overline{\text{SSTRB}}$ signal to frame the transmit data from the DSP . Thus, when $\overline{\text{SSTRB}}$ goes low, data contained in the transmit shift register of the DSP is clocked out on each rising edge of SCLK. The AD7840, in turn, loads each data bit into its input register on the SCLK falling edges. The DAC output is updated when 16 data bits have been received.

Using the ADSP-2101 and the chipset, the modem hardware is simplified. The number of lines required to connect the chips is much less than a parallel interface structure would need and no external glue logic is required.

CHIPSET LAYOUT

Figure 23 is the circuit diagram for a modem analog front end based on the Analog Devices chip set. The component overlay is given in Figure 21, while the PCB layout is given in Figures 24 and 25.

The modem analog front end uses the AD7341, AD7371, AD7840 and AD7871. Total channel SNR performance is better than 72dB with a full scale input signal and unity gain on the filter chips. The 14-bit resolution of the converters gives an instantaneous dynamic range of 84dB. If greater dynamic range is required, then the AD7371 PGA can be used to give up to 24dB extra.

The evaluation board makes full use of the flexible interfaces on the AD7840 and the AD7871. J1 is a 96-way VME bus connector which carries the parallel interface for the board. This plugs directly into the connector on the evaluation board for the ADSP-2100, which is another in the Analog Devices family of Digital Signal Processors and is code compatible with the ADSP-2101. Thus, direct interfacing between the boards is possible. All the signals necessary for interfacing to other DSPs are available on J1. The 9-way D-Type connector, J2, carries the serial interface for the board. This allows DSPs with serial ports to interface directly to the chipset.

Power supplies used to operate the board are ±15V analog supplies and a single +5V digital supply. A ±5V analog supply is derived from the ±15V supply by using the 78L05/79L05 regulators. This supply is used for the AD7341, AD7371, AD7840 and AD7871. The supply grounds are tied together on the board so that there is no need to have them connected back at the supply source.

The analog input and output ranges are both ±10V. The analog input is attenuated by IC1 and associated circuitry to give the required ±3V input range for the filter and ADC. Likewise, the analog output from the reconstruction filter (±3V) is gained up by the output amplifier (IC6) to give a ±10V output. This output amplifier also contains a simple second order filter to further attenuate the switched capacitor clock noise at the output.

There are three digital inputs to the board. These are CLKIN, ADC SYNCIN and DAC SYNCIN. CLKIN provides the clock for the ADC and filters. The DIP switches on the board have been set up to accept a nominal clock of 288kHz for the filters. ADC SYNCIN and DAC SYNCIN can be used to resynchronize the filters/converters with an external synchronizing signal. If this is not required, then both of these inputs should be tied high.

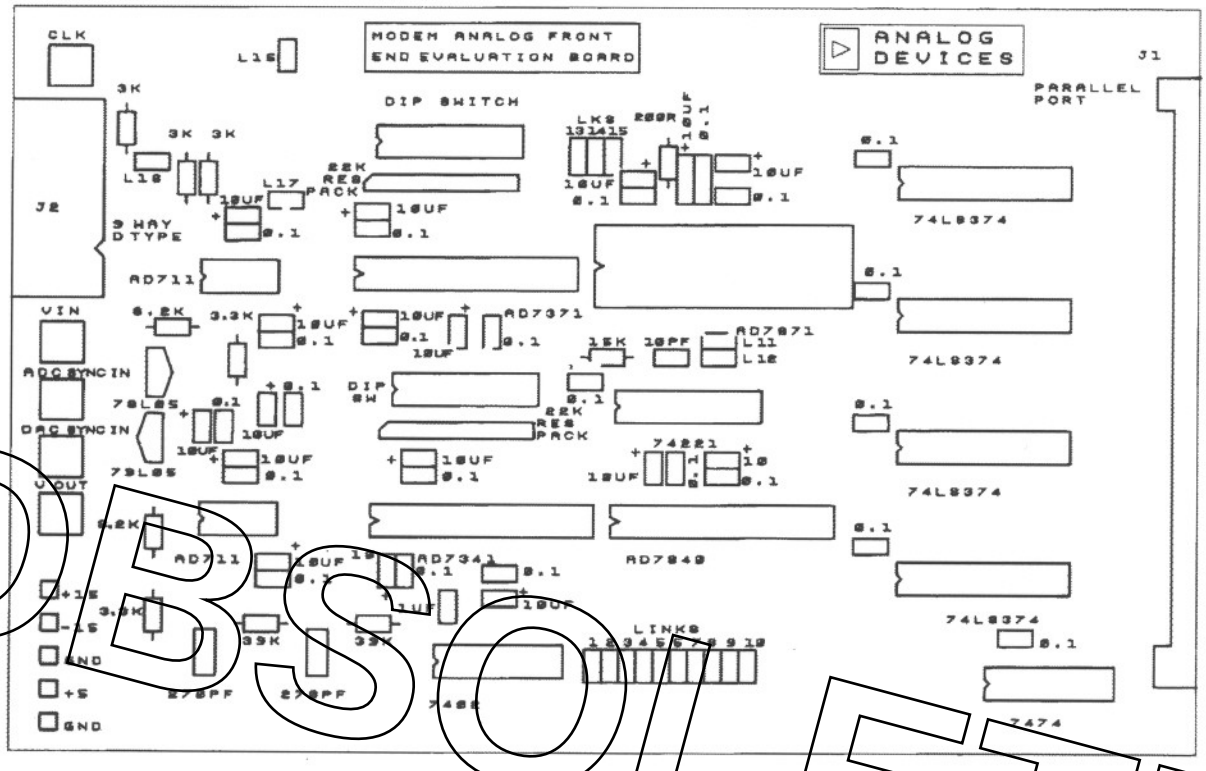


Figure 21. Component Overlay for Circuit of Figure 23

Parallel Interface

If the parallel interface is required, then the four latch chips (IC7 to IC10) should be inserted into the sockets provided. Links L16, L17, L18, L5 and L6 should be omitted. This isolates the serial port from bus activity. Link L15 should be inserted to choose 14-bit parallel operation for the ADC. Omit links L14 and L13. Internal or external clock operation for the ADC may be chosen by L11 and L12. L11 gives external clock operation, while L12 gives internal clock operation. AD7871 conversion is started by $\overline{\text{CONVST}}$ (pin 1) going low. When conversion is complete, $\overline{\text{INT/BUSY}}$ (pin 4) goes low. IC13 extends this pulse. This is then used to read the ADC result into the latches and to interrupt the processor. The processor interrupt service routine then reads the latch contents. Note that the data format is 14 bits with sign extension to 16 bits.

On the AD7840 insert L2 to tie the chip select low and omit L1. Insert L3 to use $\overline{\text{SYNCOUT}}$ of filter to write to the DAC and omit L4. Thus, the processor writes data to the latches and the DAC gets updated on every rising edge of $\overline{\text{WR}}$/$\overline{\text{SYNC}}$. The data format is 14-bit right justified.

Serial Interface

If the serial interface is required, then omit the four latches (74LS374) and use the serial connector (J2). Links L5, L6, L16, L17 and L18 must be inserted. Omit L15 and insert L14. This places the AD7871 in serial mode of operation with continuously running SCLK. As in the parallel mode, conversion is started by $\overline{\text{CONVST}}$ going low. Serial data appears on Pin 9 (SDATA) as conversion is taking place, and it is latched into the processor shift register on each falling edge of SCLK. The frame synchronization pulse for the data is on Pin 7 ($\overline{\text{SSTRB}}$). The data format is 16-bit with the MSB first. The 16 bits of data are made up of two leading zeros and the 14-bit conversion result. For the DAC in the serial mode omit L3 and insert L4. This provides the necessary inversion of the $\overline{\text{SYNCOUT}}$ pulse from the filter so that it can be used as the frame synchronization for the DAC and the processor. When this goes low data in the processor shift register is clocked out on each rising edge of SCLK and latched into the DAC shift register on each falling edge of SCLK. Since $\overline{\text{LDAC}}$ (Pin 24) is tied permanently low, the DAC register is updated automatically when the 16-bit data stream has been received. The format of this data stream is set up by links L7 to L10. Consult Table I on the AD7840 data sheet for the appropriate settings. Figure 22, below, shows the pin designations for J2.

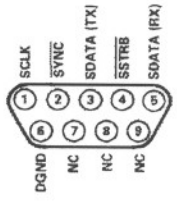


Figure 22. Pin Configuration for J2 (Front View)

AD7341/AD7371

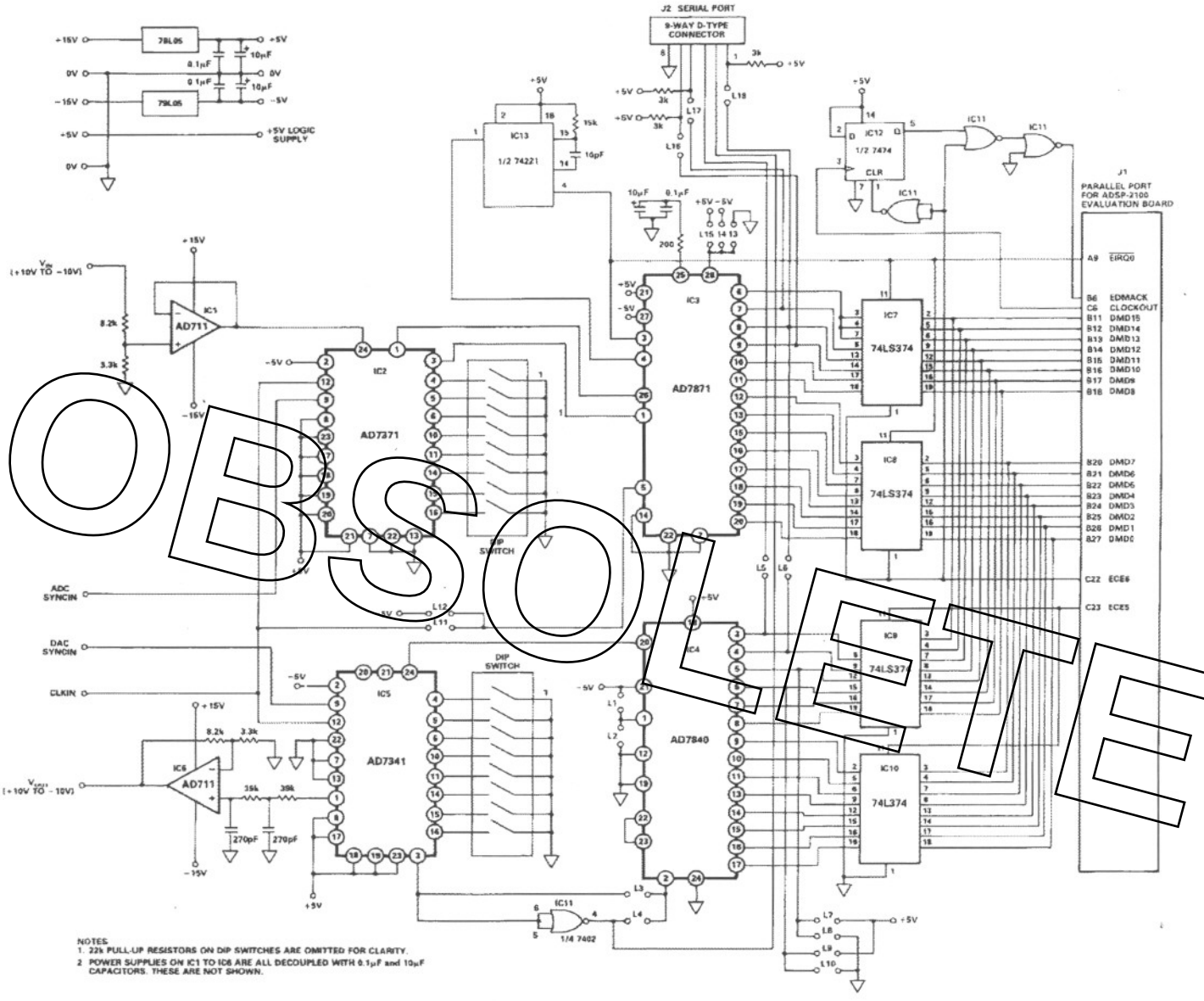


Figure 23. Circuit Diagram for Modem Analog Front End

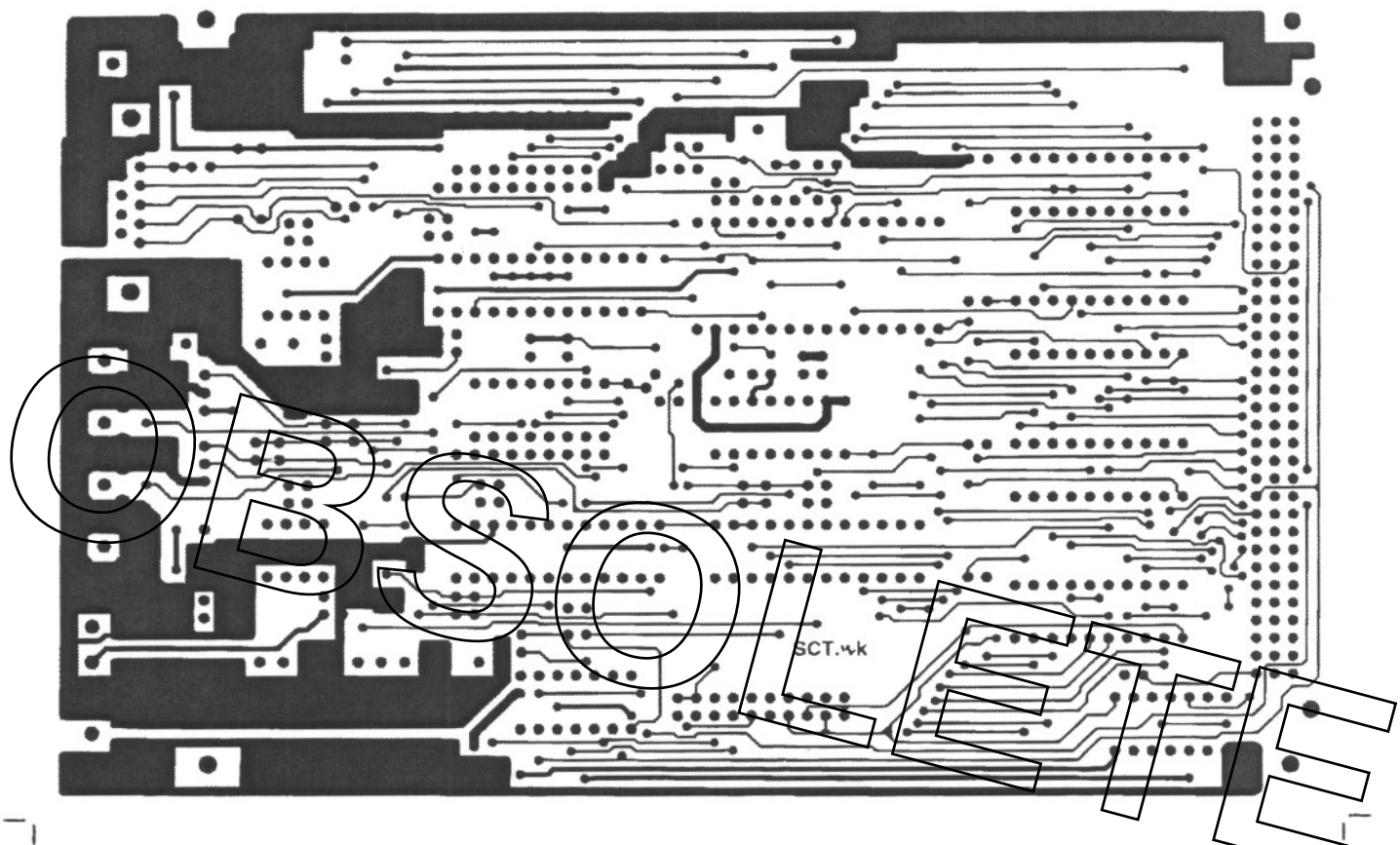


Figure 24. PCB Component Side Layout for Figure 23

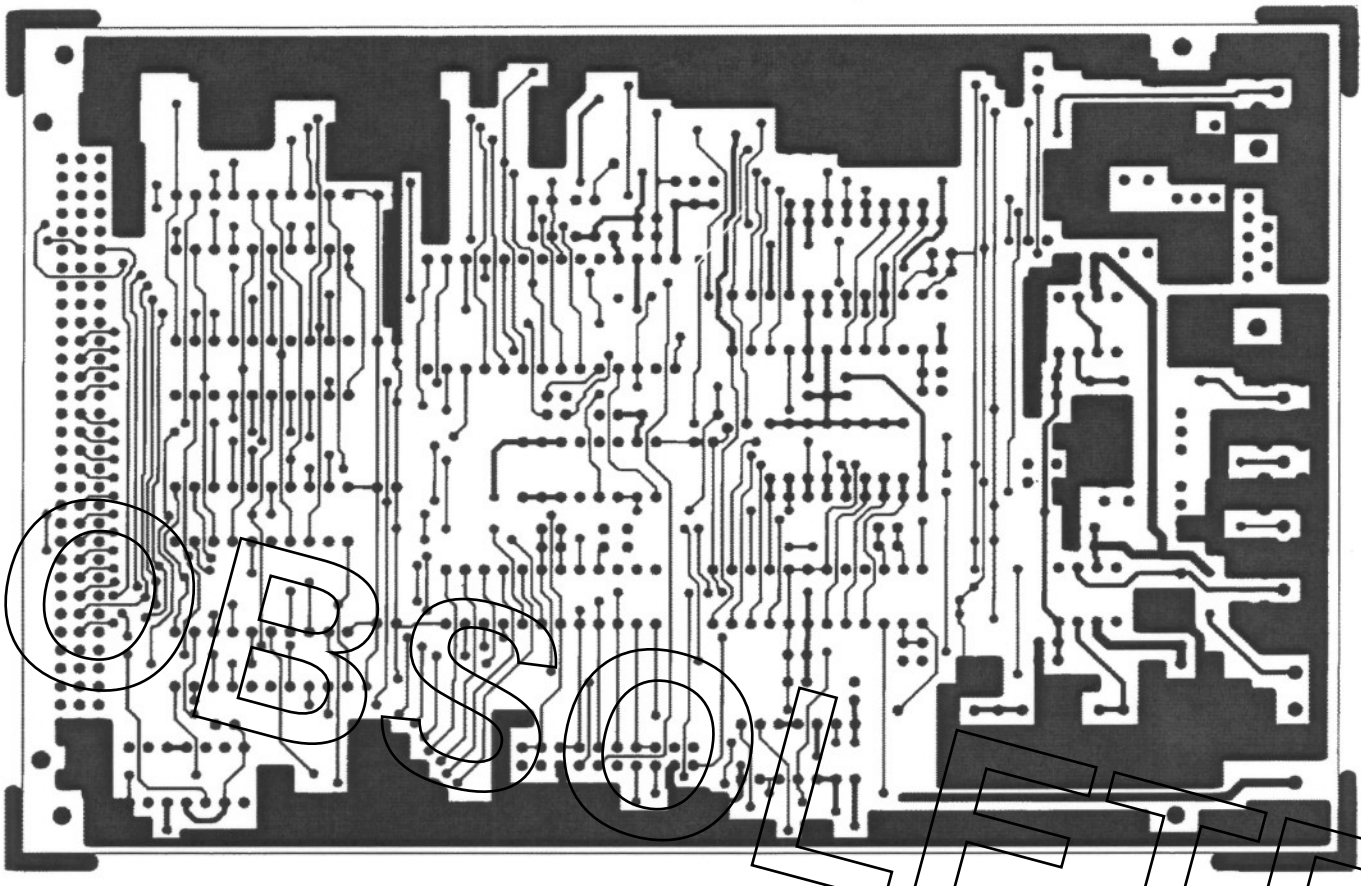


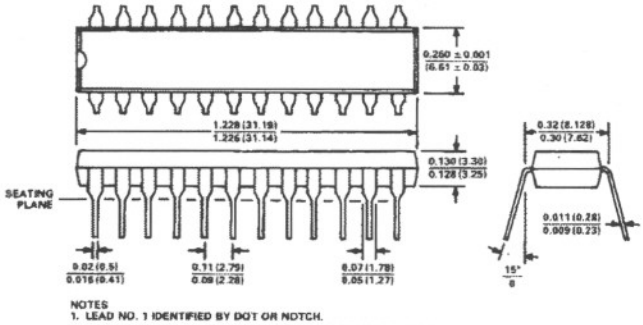
Figure 25. PCB Solder Side Layout for Figure 23

MECHANICAL INFORMATION

OUTLINE DIMENSIONS

Dimensions are shown in inches and (mm).

24-Pin Plastic DIP (N-24)



NOTES
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
2. PLASTIC LEADS WILL BE EITHER SOLDER DIPPED OR TIN LEAD PLATED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

28-Pin Plastic Leaded Chip Carrier (P-28A)