A4993

Automotive Stepper Driver

FEATURES AND BENEFITS

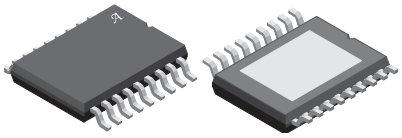
- Peak motor current up to 1.4 A at 28 V
- Low $R_{DS(ON)}$ outputs, 0.5 Ω source and sink typical
- Continuous operation at high ambient temperature
- 3.5 to 50 V supply operation
- Adaptive mixed current decay
- Synchronous rectification for low power dissipation
- Internal overvoltage and undervoltage lockout
- Hot warning and overtemperature shutdown
- Crossover-current protection
- Short-circuit, open-load diagnostics
- Stall-detect features
- Configurable through serial interface

APPLICATIONS

- Automotive stepper motors
- Engine management
- Headlamp positioning
- HVAC flap and valve control

PACKAGE:

20-Pin TSSOP with Exposed Thermal Pad (suffix LP)



Not to scale

DESCRIPTION

The A4993 is a flexible microstepping motor driver with integrated phase current control and a built-in translator for easy operation. It is a single chip solution designed to operate bipolar stepper motors in full-, half-, quarter-, eighth-, and sixteenth-step modes, at up to 28 V. At power-on, the A4993 is configured to drive most small stepper motors with simple step input.

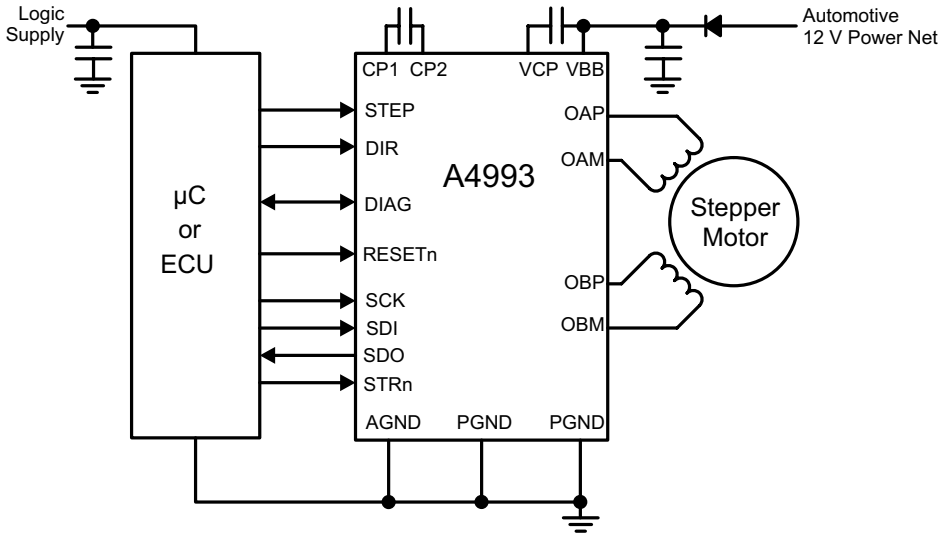
The current regulator operates with fixed frequency PWM and uses adaptive mixed current decay to reduce audible motor noise and increase step accuracy.

The current in each phase of the motor is controlled through a DMOS full-bridge using synchronous rectification to improve power dissipation. Internal circuits and timers prevent cross-conduction and shoot-through when switching between high-side and low-side drives.

The outputs are protected from short circuits, and features for low load current and stalled rotor detection are included. Chip-level protection includes hot thermal warning, overtemperature shutdown, overvoltage and undervoltage lockout.

An SPI-compatible serial interface can be used to switch microstep resolution between step control inputs. It can also be used to configure several motor control parameters and diagnostic thresholds, and to control the motor directly. Detailed diagnostics are available on the serial data output.

The A4993 is supplied in a 20-pin TSSOP power package with an exposed thermal pad (package type LP). This package is lead (Pb) free with 100% matte-tin leadframe plating.



Typical Application Diagram

Selection Guide

Part Number	Packing	Package
A4993KLPTR-T	4000 pieces per 13-inch reel	4.4 mm × 6.5 mm, 1.2 mm nominal height 20-pin TSSOP with exposed thermal pad

Table of Contents

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS [1]

Characteristic	Symbol	Notes	Rating	Unit
Load Supply Voltage	V_{BB}		–0.3 to 50	V
Terminal CP1	V_{CP1}	$V_{CP1} > V_{BB} – 24$ V	–0.3 to V_{BB} + 0.3	V
Terminal CP2	V_{CP2}		–0.3 to V_{BB} + 8	V
Terminal VCP	V_{CP}		–0.3 to V_{BB} + 8	V
Terminals STEP, DIR, SCK, SDI, SDO, STRn			–0.3 to 6	V
Terminal RESETn	V_{RESETn}	Can be pulled to V_{BB} with 33 kΩ	–0.3 to 6	V
Terminal DIAG	V_{DIAG}		–0.3 to 50	V
Terminals OAP, OAM, OBP, OBM			–0.3 to V_{BB}	V
Terminals PGND	V_{PGND}		–0.1 to 0.1	V
Ambient Operating Temperature Range [2]	T_A	Limited by power dissipation	–40 to 150	°C
Maximum Continuous Junction Temperature	T_J(max)		165	°C
Transient Junction Temperature	T_{Jt}	Overtemperature event not exceeding 10 seconds, lifetime duration not exceeding 10 hours, ensured by design and characterization.	175	°C
Storage Temperature Range	T_{stg}		–55 to 150	°C

[1] With respect to GND
[2] Limited by power dissipation

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions [3]	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	4-layer PCB based on JEDEC standard	28	°C/W
		2-layer PCB with 3.8 in^2 copper each side	38	°C/W
	$R_{\theta JP}$		2	°C/W

[3] Additional thermal information available on the Allegro website.

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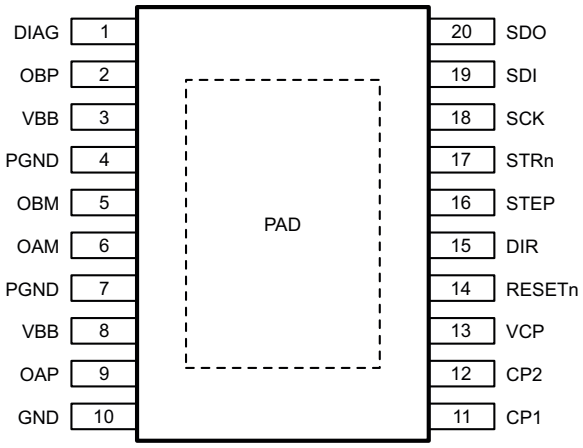

Package LP, 20-Pin eTSSOP Pin-Out Diagram

Terminal List Table

Number	Name	Function
1	DIAG	Diagnostic Output
2	OBP	Bridge B Positive Output
3	VBB	Motor Supply Voltage
4	PGND	Power Ground
5	OBM	Bridge B Negative Output
6	OAM	Bridge A Negative Output
7	PGND	Power Ground
8	VBB	Motor Supply Voltage
9	OAP	Bridge A Positive Output
10	GND	Ground
11	CP1	Charge Pump Capacitor
12	CP2	Charge Pump Capacitor
13	VCP	Pump Storage Capacitor
14	RESETn	Standby Mode Control
15	DIR	Direction Select Input
16	STEP	Step Input
17	STRn	Serial Strobe (chip select) Input
18	SCK	Serial Clock Input
19	SDI	Serial Data Input
20	SDO	Serial Data Output
PAD	–	Exposed Thermal Pad

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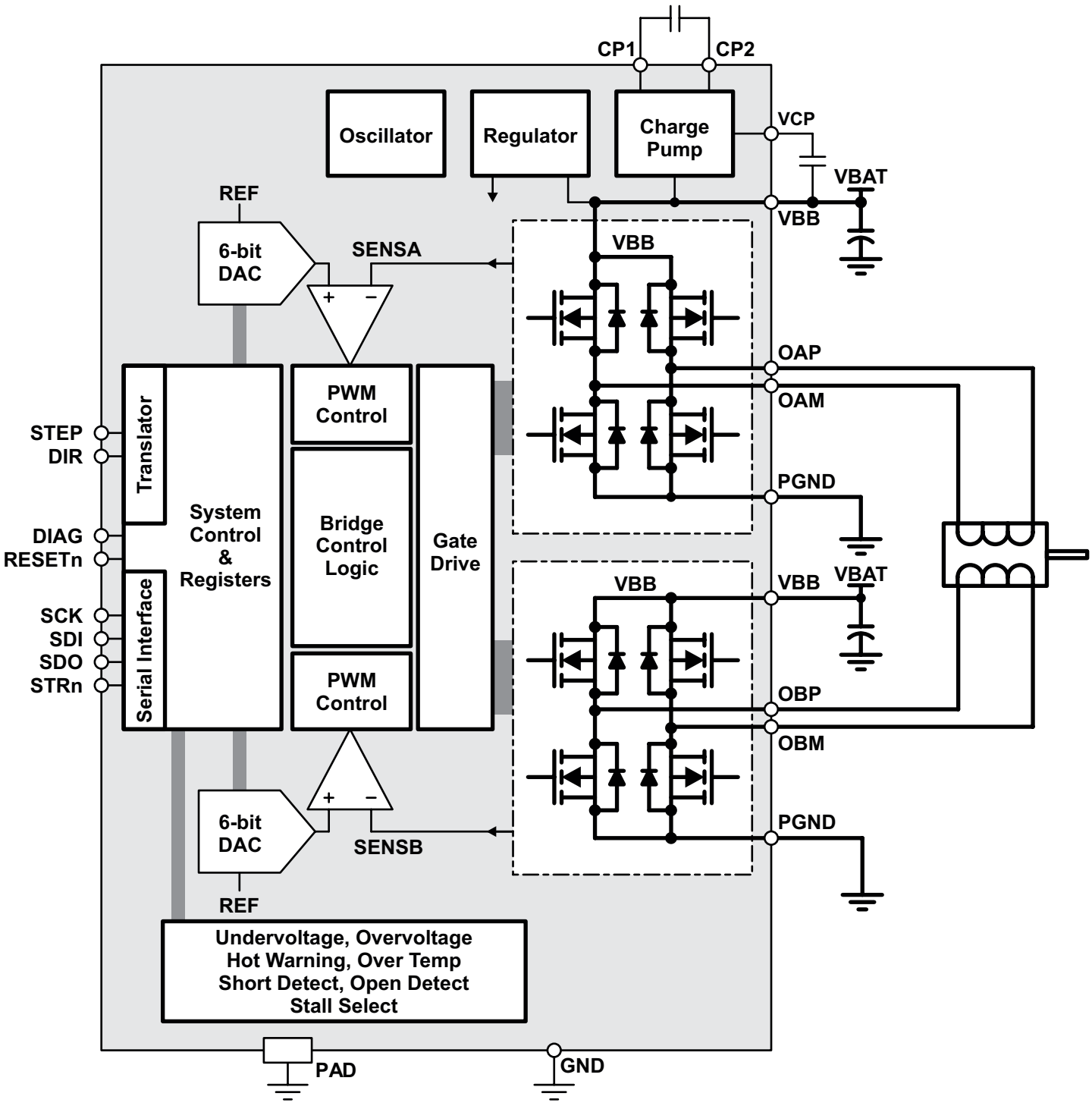

Functional Block Diagram

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ELECTRICAL CHARACTERISTICS: Valid at T_J = –40°C to 150°C, V_{BB} = 3.8 to 28 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
SUPPLIES						
Supply Voltage Range [4]	V_{BB}	No unsafe states	0	–	50	V
		Outputs driving	3.8	–	V_{BBOV}	V
Supply Quiescent Current [1]	I_{BBQ}	DIS = 1	–	–	15	mA
		Sleep Mode, V_{BB} = 12 V, SLP = 1, STRn = 1 or V_{RESETn} < 0.5 V, T_J = 25°C	–	25	35	µA
Charge Pump Voltage	V_{CP}	With respect to V_{BB}, V_{BB} > 7.5 V, DIS = 1, SLP = 0, RESETn = 1	–	7	–	V
MOTOR BRIDGE OUTPUT						
High-Side On-Resistance	R_{ONH}	V_{BB} = 13.5 V, I_{OUT} = –1 A [1], T_J = 25°C	–	500	600	mΩ
		V_{BB} = 13.5 V, I_{OUT} = –1 A [1], T_J = 150°C	–	900	1100	mΩ
		V_{BB} = 7 V, I_{OUT} = –1 A [1], T_J = 25°C	–	625	750	mΩ
High-Side Body Diode Forward Voltage	V_{FH}	I_F = 1 A	–	–	1.4	V
Low-Side On-Resistance	R_{ONL}	V_{BB} = 13.5 V, T_J = 25°C, MXI[3:0] = 13 (1 A)	–	500	600	mΩ
		V_{BB} = 13.5 V, T_J = 150°C, MXI[3:0] = 13 (1 A)	–	900	1100	mΩ
		V_{BB} = 7 V, T_J = 25°C, MXI[3:0] = 13 (1 A)	–	625	750	mΩ
		V_{BB} = 13.5 V, T_J = 25°C, MXI[3:0] = 1 (100 mA)	–	1350	1500	mΩ
		V_{BB} = 13.5 V, T_J = 150°C, MXI[3:0] = 1 (100 mA)	–	2300	2600	mΩ
		V_{BB} = 7 V, T_J = 25°C, MXI[3:0] = 1 (100 mA)	–	1650	1900	mΩ
Low-Side Body Diode Forward Voltage [2]	V_{FL}	I_F = 1 A	–	–	1.4	V
		I_F = 0.1 A	–	–	1	V
Output Current [1]	I_{OUT}	SLP = 0, RESETn = 1, DIS = 1, V_O = V_{BB}	–	65	120	µA
		SLP = 0, RESETn = 1, DIS = 1, V_O = 0 V	–200	–120	–	µA
		SLP = 1, V_{RESETn} < 0.5 V, V_O = V_{BB}	–	1	20	µA
		SLP = 1, V_{RESETn} < 0.5 V, V_O = 0 V	–30	–10	–	µA
Output Slew Rate	dV_O/dt	SLEW = 0, V_{BB} = 13.5 V SLEW = 1, V_{BB} = 13.5 V	–	100 20	–	V/µs
Dither Modulation Depth	D_m	DIT = 1	–	±20	–	% f_{PWM}
Dither Modulation Rate	f_m	DIT = 1	–	10	–	kHz
CURRENT CONTROL						
Internal Oscillator Period	t_{OSC}		45	50	55	ns
Blank Time	t_{BLANK}	Default blank-time	–	3.5	–	µs
PWM Frequency	f_{PWM}	Default frequency	–	21.7	–	kHz
Output Trip Point Error [2]	E_{ITrip}	MXI[3:0] = 0, 1	–	–	±15	%
		MXI[3:0] = 2…13	–	–	±10	%
		MXI[3:0] = 14, 15	–	–	±15	%

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ELECTRICAL CHARACTERISTICS (continued): Valid at T_J = –40°C to 150°C, V_{BB} = 3.8 to 28 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
LOGIC INPUT AND OUTPUT – DC PARAMETERS						
Input Low Voltage	V_{IL}		–	–	0.8	V
Input Low Voltage for Sleep Mode	V_{ILS}	RESETn input only	–	–	0.5	V
Input High Voltage	V_{IH}		2	–	–	V
Input Hysteresis	V_{IHys}		100	300	–	mV
Input Pull-Up Resistor	R_{PU}	STRn	–	80	–	kΩ
Input Pull-Down Resistor	R_{PD}	SDI, STEP, DIR, RESETn	–	80	–	kΩ
Output Low Voltage	V_{OL}	I_{OL} = 2 mA [1]	–	–	0.4	V
Output High Voltage	V_{OH}	I_{OL} = –2 mA [1]	2.4	–	–	V
Output Leakage [1] (SDO)	I_{OSD}	0 V < V_O < 3.3 V, STRn = 1	–1	–	1	µA
Output Leakage [1] (DIAG)	I_{ODI}	0 V < V_O < 9 V	–	–	1	µA
LOGIC INPUT AND OUTPUT – DYNAMIC PARAMETERS						
Reset Pulse Width	t_{RST}		1.5	–	8	µs
Shutdown Time	t_{RSD}	STRn rising or RESETn falling to outputs disabled	–	–	40	µs
Low Power Time	t_{RLP}		–	<200	–	µs
Input Pulse Filter Time (STEP, DIR)	t_{PIN}		–	80	–	ns
STEP High	t_{STPH}		1	–	–	µs
STEP Low	t_{STPL}		1	–	–	µs
Setup Time Control Input Change to STEP	t_{SU}	DIR	200	–	–	ns
Hold Time Control Input Change from STEP	t_H	DIR	200	–	–	ns
Wake Up From Sleep	t_{EN}		–	–	1	ms
Interface Ready From Sleep	t_{IR}		–	–	1.1	ms
SERIAL INTERFACE – DYNAMIC PARAMETERS [3]						
Clock High Time	t_{SCKH}	A [3]	50	–	–	ns
Clock Low Time	t_{SCKL}	B [3]	50	–	–	ns
Strobe Lead Time	t_{STLD}	C [3]	30	–	–	ns
Strobe Lag Time	t_{STLG}	D [3]	30	–	–	ns
Strobe High Time	t_{STRH}	E [3]	300	–	–	ns
Data Out Enable Time	t_{SDOE}	F [3]	–	–	40	ns
Data Out Disable Time	t_{SDOD}	G [3]	–	–	30	ns
Data Out Valid Time from Clock Falling	t_{SDOV}	H [3]	–	–	40	ns
Data Out Hold Time from Clock Falling	t_{SDOH}	I [3]	5	–	–	ns
Data In Setup Time to Clock Rising	t_{SDIS}	J [3]	15	–	–	ns
Data In Hold Time from Clock Rising	t_{SDIH}	K [3]	10	–	–	ns

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
DIAGNOSTICS AND PROTECTION						
VBB Overvoltage Threshold [5]	V_{BBOV}	V_{BB} rising	32	34	36	V
VBB Overvoltage Hysteresis [5]	$V_{BBOVHys}$		2	–	4	V
VBB Low Threshold [5]	V_{BBLO}	V_{BB} falling	5.2	5.5	5.8	V
VBB Low Hysteresis [5]	$V_{BBLOHys}$		500	700	–	mV
VBB Undervoltage Threshold [5]	V_{BBUV}	V_{BB} falling	–	3.3	3.6	V
VBB Undervoltage Hysteresis [5]	$V_{BBUVHys}$		–	50	–	mV
VBB POR	V_{BBPOR}	V_{BB} falling	–	1.9	2.8	V
VCP Undervoltage Threshold – High [5]	V_{CPUVH}	V_{CP} falling	4.5	5	5.5	V
VCP Undervoltage Hysteresis – High [5]	$V_{CPUVHHys}$		300	500	–	mV
VCP Undervoltage Threshold – Low [5]	V_{CPUVL}	V_{CP} falling	2.15	2.5	2.85	V
VCP Undervoltage Hysteresis – Low [5]	$V_{CPUVLHys}$		200	300	–	mV
High-Side Overcurrent Threshold	I_{OCH}		1.4	2.05	2.65	A
High-Side Current Limit	I_{LIMH}	Active during t_{OC}	3	5.5	8	A
Low-Side Overcurrent Threshold	I_{OCL}	MXI[3:0] = 2…15	1.4	2.05	2.65	A
		MXI[3:0] = 0, 1	0.35	0.5	0.65	A
Overcurrent Fault Delay	t_{OC}	Default fault delay	1.5	2	2.7	µs
Open Load Current Threshold	E_{IOC}	OLT = 0 (Default)	8	14	22	mA
		OLT = 1	21	27	35	mA
Hot Temperature Warning Threshold	T_{JWH}	Temperature increasing	125	135	145	°C
Hot Temperature Warning Hysteresis	T_{JWHHys}		–	15	–	°C
Overtemperature Shutdown	T_{JF}	Temperature increasing	170	–	180	°C
Overtemperature Hysteresis	T_{JHys}	Recovery = T_{JF} – T_{JHys}	–	15	–	°C

1 For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device terminal.
2 Current Trip Point Error is the difference between actual current trip point and the target current trip point, referred to maximum full scale (100%) current: $E_{ITrip} = 100 \times (I_{TripActual} – I_{TripTarget}) / IFullScale$ %
3 Timing parameter letters refer to Interface Timing Diagrams.
4 Function is correct but parameters are not guaranteed above or below the general limits (3.8 to 28 V).
5 Outputs disabled if $V_{BB} > V_{BBOV}$ or $V_{BB} < V_{BBUV}$ or $V_{CP} < V_{CPUVH}$ (if $V_{BB} > V_{BBLO}$) or $V_{CP} < V_{CPUVL}$ (if $V_{BB} < V_{BBLO}$)

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INTERFACE TIMING DIAGRAMS

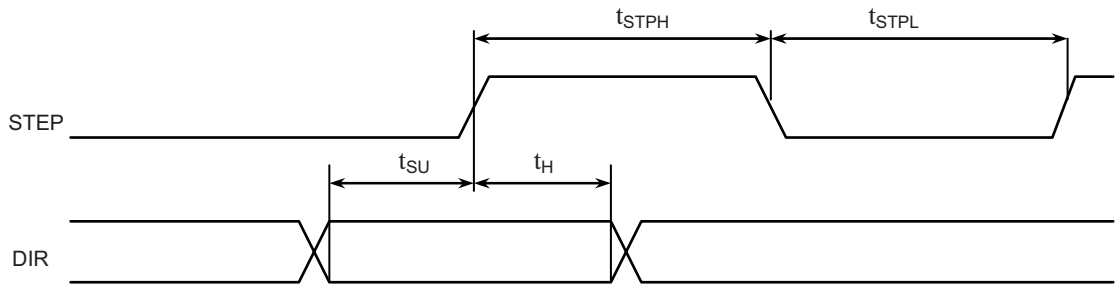

Figure 1: Control Input Timing

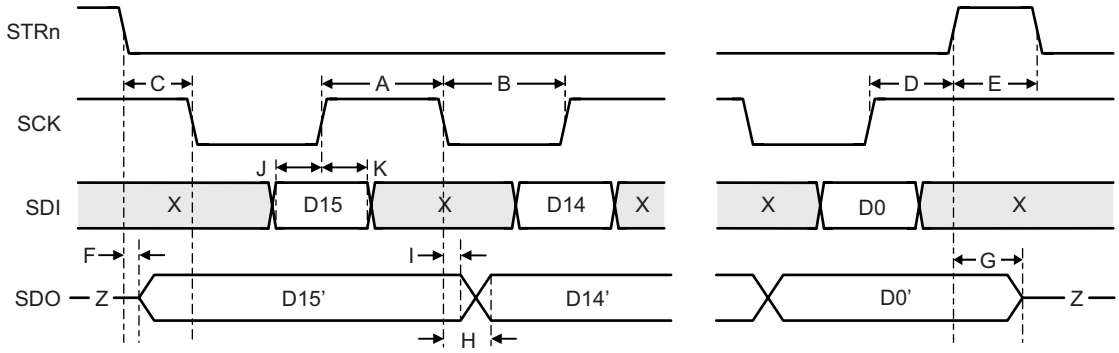

Figure 2: Serial Interface Timing
(X = don't care; Z = high impedance (tri-state)

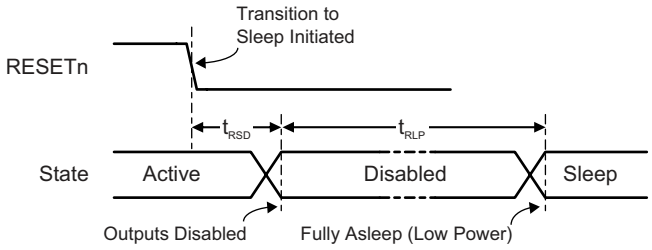

Figure 3a: Transition to Sleep (RESETn)

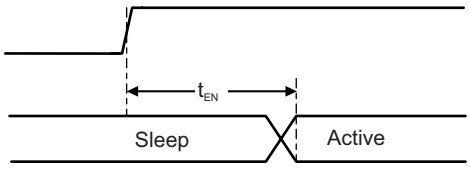

Figure 3b: Transition from Sleep (RESETn)

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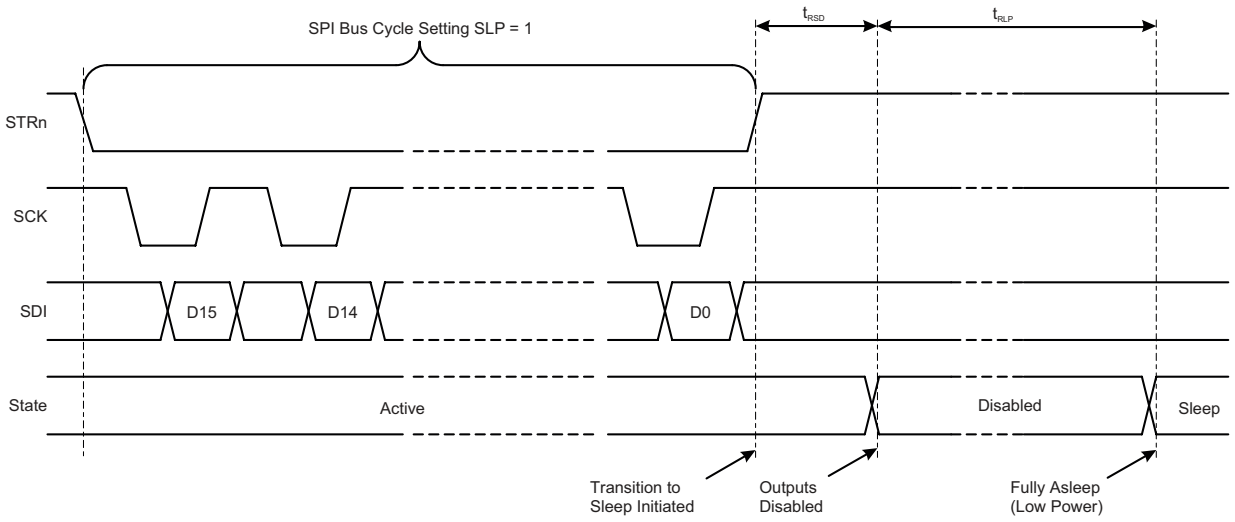

Figure 4a: Transition to Sleep (SPI)

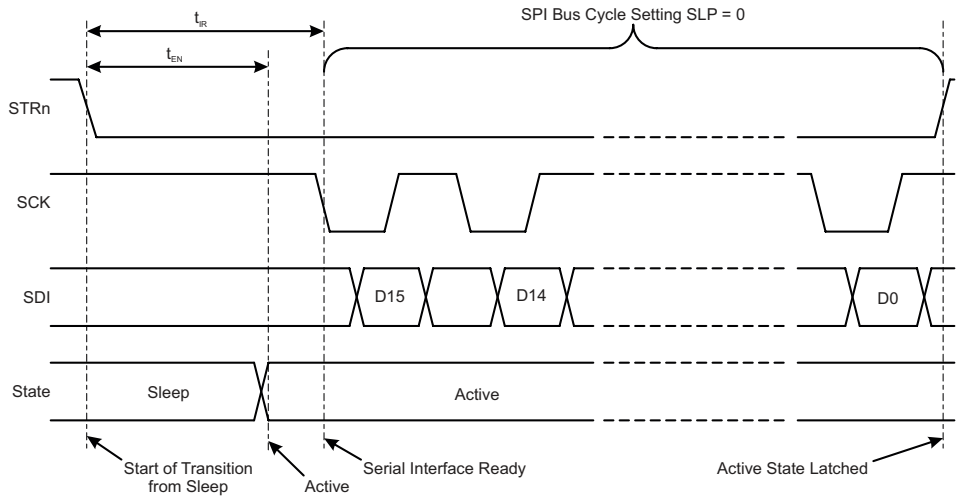

Figure 4b: Transition from Sleep (SPI, Active State Latched)

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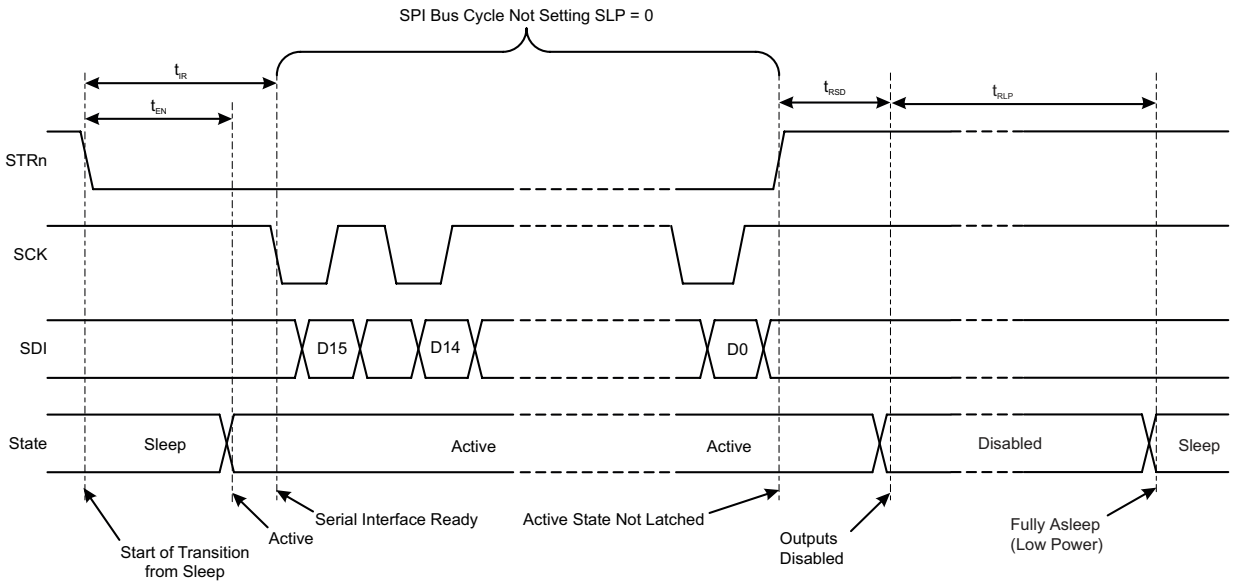

Figure 4c: Transition from Sleep (SPI, Active State Not Latched)

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FUNCTIONAL DESCRIPTION

The A4993 is an automotive stepper motor driver suitable for high-temperature applications such as headlamp bending and leveling, throttle control, and gas recirculation control. It is also suitable for other low-current stepper applications such as air conditioning and venting. It provides a flexible microstepping motor driver controlled by way of simple step and direction inputs or via an SPI-compatible interface.

The SPI-compatible serial interface also allows the selection of step mode, configuration of motor control parameters, and programming of diagnostic thresholds.

A single diagnostic output provides simple indication of a fault condition, and detailed diagnostic information can be read from the serial interface output.

The two DMOS full-bridges are capable of driving bipolar stepper motors in full-, half-, quarter-, eighth- and sixteenth-step modes, at up to 28 V, with phase current up to ±1.4 A but limited by power dissipation and ambient temperature. For most applications typical phase current is up to ±750 mA. The current in each phase of the stepper motor is regulated by a fixed-frequency peak-detect PWM current-control scheme operating in an adaptive mixed decay mode. This provides reduced audible motor noise and increased step accuracy for a wide range of motors and operating conditions.

The outputs are protected from short circuits and features for open load and stalled rotor detection are included. Chip-level protection includes hot thermal warning, overtemperature shutdown, overvoltage lockout, and undervoltage lockout.

Pin Functions

VBB: Main motor supply and chip supply for internal regulators and charge pump. Both VBB pins should be connected together and each decoupled to ground with a low ESR electrolytic capacitor and a good ceramic capacitor.

CP1, CP2: Pump capacitor connection for charge pump. Connect a 100 nF (50 V) ceramic capacitor, between CP1 and CP2.

VCP: Above supply voltage for high-side drive. A 100 nF (16 V) ceramic capacitor should be connected between VCP and VBB to provide the pump storage reservoir.

GND: Power and reference ground. Connect to PGND pins—see layout recommendations.

PGND: Bridge power grounds. Connect to GND—see layout recommendations.

OAP, OAM: Motor connection for phase A. Positive motor phase current direction is defined as flowing from OAP to OAM.

OBP, OBM: Motor connection for phase B. Positive motor phase current direction is defined as flowing from OBP to OBM.

STEP: Step logic input with internal pull-down. Motor advances on rising edge.

DIR: Direction logic input. Direction changes on next STEP rising edge. When low (and the DIR bit in the Control register is in its default low state) the phase angle number is incremented on rising edge of STEP.

SDI: Serial data input. 16-bit serial word, input MSB first.

SDO: Serial data output. High impedance when the STRn input is high. Outputs bit 15 of the Status register, the fault flag, as soon as the STRn input goes low.

SCK: Serial clock. Data is latched in from SDI on the rising edge of SCK. There must be 16-rising edges per write and SCK must be held high when the STRn input changes.

STRn: Serial data strobe and serial access enable. When STRn is high, any activity on SCK or SDI is ignored and SDO is high impedance, allowing multiple SDI slaves to have common SDI, SCK, and SDO connections.

DIAG: Diagnostic output. Function selected through serial interface. Default is fault output.

RESETn: Resets faults when pulsed low for a duration compliant with the Reset Pulse Width (t_{RST}). Forces low-power shutdown (sleep) when held low for more than the Reset Shutdown Width (t_{RSD}). Can be pulled to VBB with a 33 kΩ resistor

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Driving a Stepper Motor

A two-phase stepper motor is made to rotate by sequencing the relative currents in each phase. In its simplest form, each phase is fully energized in turn by applying a voltage to the winding. For more precise control of the motor torque across temperature and voltage ranges, current control is required. For efficiency, this is usually accomplished using PWM techniques. In addition, current control also allows the relative current in each phase to be controlled, providing more precise control over the motor movement and hence improvements in torque ripple and mechanical noise.

For bipolar stepper motors, the current direction is significant, so the voltage applied to each phase must be reversible. This requires the use of a full-bridge (also known as an H-bridge), which can switch each phase connection to supply or ground.

Phase Current Control

In the A4993, current to each phase of the two-phase bipolar stepper motor is controlled through a low-impedance n-channel DMOS full-bridge. This allows efficient and precise control of the phase current using fixed-frequency pulse-width-modulation (PWM) switching. The full-bridge configuration provides full control over the current direction during the PWM on-time and the current decay mode during the PWM off-time. The A4993 automatically controls the bridge decay mode to provide the optimum current control completely transparent to the user.

Each leg (high-side, low-side pair) of each bridge is protected from shoot-through by a fixed dead-time. This is the time between switching off one MOSFET and switching on the complementary MOSFET. Cross-conduction is prevented by lockout logic in each driver pair.

Except for the half-step uncompensated mode, the phase currents and, in particular, the relative phase currents are defined by the phase current table. This table defines the two phase currents at each microstep position. For each of the two phases, the currents are measured in the bridge transistors on the A4993. The target current level is defined by the output from the digital-to-analog converter (DAC) for that phase.

The actual current delivered to each phase at each step angle is determined by the value of the Config 0 register MXI[3:0] bits and the contents of the phase table. For each phase, the value in the phase table is passed to the DAC, which uses MXI[3:0] as the reference 100% level (code 63) and reduces the current target depending on the DAC code. The output from the DAC is used as the input to the current comparators.

The one exception is the uncompensated half-step mode. In this mode, the current in each phase at the half-step positions (8, 24, 40, and 56), with both phases active, will be the same level as at the full-step detent positions (0, 16, 32, and 48), with one phase active.

Low-side on-resistance (R_{ONL}) is automatically modified at maximum phase current settings of 100 mA or less (MXI[3:0] = 0,1) to maintain current-sense accuracy. High-side on-resistance (R_{ONH}) remains constant across all maximum phase current settings.

The current comparison is ignored at the start of the PWM on-time for a duration referred to as the blank time. The blank time is necessary to prevent any capacitive switching currents from causing a peak current detection.

The PWM on-time starts at the beginning of each PWM period. The current rises in the phase winding until it reaches the required peak current level. At this point, the PWM off-time starts and the bridge is switched into fast decay. The current continues to be monitored. When the current drops below the peak current level, the bridge is switched into slow decay for the remainder of the PWM period. This mixed decay technique automatically adapts the current control to a wide range of motors and operating conditions in order to minimize motor torque ripple and motor noise. It also provides the lowest motor dissipation and highest motor efficiency over a wide range of voltage and temperature conditions.

PWM frequency may be set to one of four preset values by writing to the FRQ[1:0] bits in the Config 0 register. If the DIT bit in the Config 0 register is set to 1, the PWM frequency is dithered with a modulation depth D_m at a rate of f_m per the Electrical Characteristics table. FRQ and DIT value changes take effect at the start of the PWM cycle following completion of the SPI write to Config 0 (STRn transition low to high).

Phase Current Table

Except for the uncompensated half-step mode, the relative phase currents are defined by the phase current table. This table contains 64 lines and is addressed by the step angle number, where step angle 0 corresponds to 0° or 360°. The step angle number is generated internally by the step sequencer, which is controlled

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by either the STEP input or by the step change value from the serial input. The step angle number determines the motor position within the 360° electrical cycle, and a sequence of step angles determines the motor movement. Note that there are four full mechanical steps per 360° electrical cycle.

Each line of the phase current table has a 6-bit value per phase to set the DAC level for each phase, plus an additional bit per phase to determine the current direction in each phase. The step angle number sets the electrical angle of the stepper motor in sixteenth microsteps, approximately equivalent to electrical steps of 5.625°.

On first power-up, after a power-on reset, or after sleep, the step angle number is set to 8, equivalent to the electrical 45° position, except for full-step single-phase drive where the step angle number is set to 0. This position is defined as the "home" position.

When using the STEP and DIR inputs to control the stepper motor, the A4993 automatically increments or decrements the step angle according to the step sequence associated with the selected step mode. The default step mode, reset at power-up or after a power-on reset, is compensated half step. Full single-phase-, full two-phase-, uncompensated half-, quarter-, eighth-, and sixteenth-step sequences are also available when using the STEP and DIR inputs, and are selected using the MS[2:0] bits in the control register. When changing microstep resolution and using the STEP input mode, the step angle will change to the next valid step angle for the microstep resolution selected on the next rising edge of STEP. The DIR pin and the DIR bit in the Control register operate as detailed in Table 1. For example, if the DIR pin is held at logic 0, setting the DIR bit to 0 (the default condition) results in the motor rotating in the forward direction, and setting the DIR bit to 1 results in it rotating in reverse. Alternatively, if the DIR bit in the Control register is set to 0, driving the DIR pin to 0 results in the motor rotating in the forward direction, and driving the DIR pin to 1 results in the motor rotating in reverse.

Table 1: DIR Logic

DIR PIn	DIR Bit	Rotation*
0	0	Forward
0	1	Reverse
1	0	Reverse
1	1	Reverse

*Forward = Phase angle count incremented
*Reverse = Phase angle count decremented

When using the serial interface to control the stepper motor, a 6-bit step change value is written to SC[5:0] to increment or decrement the step angle. The step change value is a two's-complement (2'sC) number, where a positive value increments the step angle and a negative value decrements the step angle. A single step change in the step angle is equivalent to a single 1/16th microstep. Therefore, for correct motor movement, the step change value should be restricted to no greater than 16 steps positive or negative.

This facility enables full control of the stepper motor at any microstep resolution up to 16th step, plus the ability to change microstep resolution "on-the-fly" from one microstep to the next. The only restriction is that serial control mode cannot operate in uncompensated half-step mode without reprogramming the phase table.

In both control input cases, the resulting step angle number is used to determine the phase current value and current direction for each phase based on the phase current table.

Low-Power Sleep Mode

The A4993 can be commanded to drop into a low-power sleep mode by taking the RESETn pin low or setting the SLP bit in the Control register to 1. If the RESETn pin is used, the motor drive outputs are disabled and the transition to low power begins within a Shutdown Time, t_{RSD}, of the applied logic low (Figure 3a). If the Control register is used, the motor drive outputs are disabled and the transition to low power begins within a Shutdown Time of the rising edge of STRn at the end of the SPI write cycle (Figure 4a). In combination, the two means of initiating sleep behave as detailed in Table 2.

Table 2: Sleep Mode Logic

RESETn	SLP Bit	Mode
0	0	Sleep
0	1	Sleep
1	0	Normal
1	1	Sleep

In sleep mode, the outputs are disabled and the internal regulators are switched off to minimize current drain from the battery supply. If the initiation of sleep mode is successful, the DIAG output is set high; if unsuccessful, it is set low. This behavior occurs regardless of the value of DG[1:0] in the Config 2 register, and may be used to confirm that a command to enter or exit sleep mode has been successful. The DIAG output state is not defined, and should not be read during the Shutdown Time (t_{RSD}) or Wake Up From Sleep (t_{EN}) periods.

Operation in sleep mode should be avoided if V_{BB} is lower than 4.5 V (for example, during cold cranking). Below 4.5 V, the low power sleep regulator may introduce transients to the logic supply resulting in a power-on-reset and the loss of configuration data.

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If sleep mode is initiated by taking RESETn low, it will be exited on the following rising edge on RESETn per Figure 3b. If sleep mode is initiated by setting SLP to 1, the part will start to wake up on the first falling edge on STRn as detailed in Figure 4b. The SPI serial transfer associated with the STRn falling transition initiating wake up must set SLP to 0, otherwise active mode will not be latched and the device will revert to sleep at the end of the cycle per Figure 4c.

Unlike other bus cycles, the first transfer after sleep must satisfy the constraint that the first falling edge on SCK occurs at least an Interface Ready period (t_{IR}) after the falling edge on STRn. This allows the internal regulators to power up and the interface logic to become active.

If sleep mode is initiated by setting SLP to 1 and then RESETn is taken low, exit from sleep requires that RESETn is taken high prior to setting SLP to 1.

Diagnostics

The A4993 integrates a number of diagnostic features to protect the driver and load as far as possible from fault conditions and extreme operating environments. When a fault condition is detected or confirmed, then a fault state exists, and the fault is captured by the Diag 1 and/or Status register(s). There are two types of fault conditions: dynamic and static.

Dynamic fault conditions are those that only exist for a short duration, either due to some action being taken by the A4993 that removes the fault condition, or the fault is only detectable at specific instants. Fault states generated in response to Dynamic faults are latched to ensure that such faults are reported through the diagnostic output terminal (DIAG), and to ensure that dangerous conditions cannot return or persist to damage the A4993 or the load.

Bridge overcurrent (bridge short condition), bridge open, and stall detect faults are categorized as Dynamic.

Static faults states are those that only exist when the fault condition is present. When such a fault condition is removed, the fault state is no longer present.

In both cases, the fault is always captured independently by the Diag 1 or Status register. The contents of these registers are not reset when the fault state clears and provide a record of all faults that have occurred since the last reset of the register in question. Any fault bits set to 1 in the Diag 1 or Status registers are only reset to 0 by a power-on reset, a reset pulse on RESETn, a transition to sleep mode and back (RESETn or the SLP bit in the Control register) or completion of a successful read of the appropriate register. If any faults persist beyond a reset action, the relevant fault states and register bits will reflect this immediately after completion of the reset.

A number of these features automatically disable the current drive to protect the outputs and the load. Others only provide an indication of the likely fault status. Fault states and associated actions are listed in Table 3.

Table 3: Fault State Table

Diagnostic	Action	Latched
VBB Overvoltage	Disable outputs	No
VBB Low	Flag fault only	No
VBB Undervoltage	Disable outputs	No
VCP Undervoltage	Disable outputs	No
Temperature Warning	Flag fault only	No
Overtemperature	Disable outputs	No
Bridge Short	Disable output	Yes
Bridge Open	Flag fault only	Yes
Stall Detect	Flag fault only	Yes
Serial Interface Fault	Flag fault only	No

A single open-drain diagnostic output (DIAG) can be programmed through the serial interface to provide four different fault signals.

At power-up or after a power-on reset, the DIAG terminal outputs a general fault flag, which goes low when a fault state is present. It indicates that a static fault condition is present or a dynamic fault condition has been detected and latched.

In addition to the general fault flag, the DIAG output can be programmed via the serial interface to output any of three optional fault indicators:

- A stall-detect error signal, which is low when a stall-detected state is present. A motor stall is only confirmed or cleared when the operating quadrant changes.
- A supply voltage error signal, which is low when a VBB overvoltage, VBB low or VCP undervoltage fault state is present.
- An open-load error signal, which is low when an open-load fault state is present.

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The DIAG pin will survive a maximum applied voltage of 50 V per the Absolute Maximum Ratings table, but switches into a high-impedance state when the applied voltage exceeds approximately 16 V (regardless of programmed pin function or device status). On-state drive capability and off-state leakage current limits are defined in the Electrical Characteristics table by the V_{OL} and I_{ODI} parameters respectively and may be used to calculate a suitable pull-up resistance. In the majority of applications, a resistor in the range 10 to 20 kΩ is suitable.

System Diagnostics

At the system level, the supply voltages and chip temperature are monitored.

SUPPLY VOLTAGE MONITORS

The main supply VBB, the charge pump voltage VCP, and the internal supply voltages (derived from VBB but not externally accessible) are monitored—the main supply for overvoltage and undervoltage, the others for undervoltage only.

- If the main supply voltage (V_{BB}) rises above its overvoltage threshold (V_{BBOV}), the A4993 disables the outputs, drives the general fault flag (DIAG) low and sets the OV bit in the Status register to 1. When the main supply voltage falls below its overvoltage threshold (V_{BBOV} - $V_{BBOVHys}$), the outputs are re-enabled, the general fault flag goes high, and the OV bit is cleared by the next Status register read operation.
- If the main supply voltage (V_{BB}) falls below the VBB low threshold, the A4993 drives the general fault flag (DIAG) low, sets the VL bit in the Status register to 1, and reduces the VCP undervoltage threshold to its lower level (V_{CPUVL}). When the main supply voltage rises above the VBB low threshold plus hysteresis, the VCP threshold rises to its higher level (V_{CPUVH}), the general fault flag goes high, and the VL bit is cleared by the next Status register read operation. The motor drive outputs remain active when VBB is below the VBB undervoltage threshold.
- If the main supply voltage (V_{BB}) falls below the VBB undervoltage threshold (V_{BBUV}), the A4993 disables the outputs, drives the general fault flag (DIAG) low, and sets the UV bit in the Status register to 1. The serial interface may be disabled, but all register states (including step angle and phase table settings) are retained. When VBB rises above the undervoltage threshold (V_{BBUV} + $V_{BBUVHys}$), the serial interface is enabled. The outputs are guaranteed to be enabled and the general fault flag is guaranteed to be high after VBB rises above V_{BBLO} + $V_{BBLOHys}$ and VCP rises above V_{CPUVH} + $V_{CPUVHHys}$ (its higher threshold level). After this, the UV bit may be cleared by reading the Status register.
- If the output of the charge pump (VCP) falls below its undervoltage threshold (V_{CPUVH} or V_{CPUVL}, depending upon the state of VBB Low), the A4993 disables the outputs, drives the general fault flag (DIAG) low, and sets the UV bit in the Status register to 1. When the charge pump output rises above its threshold (V_{CPUVH} + $V_{CPUVHHys}$ or V_{CPUVL} + $_{VCPUVLHys}$, depending upon the state of VBB Low), the outputs are re-enabled, the general fault flag goes high, and the UV bit is cleared by the next Status register read operation.
- If VBB falls below the VBB power-on reset (POR) level and the internal supply voltages derived from VBB drop below acceptable levels, the A4993 is completely disabled. DIAG is set low and held in this state for as long as the supply voltage permits. When the internal supply voltages rise to acceptable levels, a power-on reset takes place, the POR and FF bits are set to 1, and all other register bits are set to their default state.

If any of these supply fault states are present, and either the general fault flag or the supply fault flag is selected for output on DIAG, then DIAG will be low.

The VCP undervoltage threshold level is determined by the state of the VBB low monitor. If VBB falls causing a VBB low fault, then the VCP threshold is reduced to the low level (V_{CPUVL}). When VBB is above the VBB low threshold plus hysteresis, the VCP undervoltage threshold is set to the high level (V_{CPUVH}). This allows the A4993 to continue to drive a stepper motor with a motor supply (VBB) voltage down to the VBB undervoltage threshold of 3.3 V(typ), 3.6 V(max), subject to parametric performance not being guaranteed below a VBB of 3.8 V.

Figures 5 and 6 show how the undervoltage thresholds change when a typical cold-crank transient occurs.

The A4993 meets the requirements of ISO 16750 Starting Profile, Levels I (Class A), II (Class B) and IV (Class A). The illustrative VBB transient is lower than the standard ISO pulse due to the forward voltage of a reverse polarity protection diode and switching transients. ISO 16750 Starting Profile, Level II for 12 V (nominal) systems is also shown on Figure 5 for reference.

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Figure 6 provides more detail around the time that the VBB low is detected, and shows the VCP voltage falling as a result of the downward change in VBB.

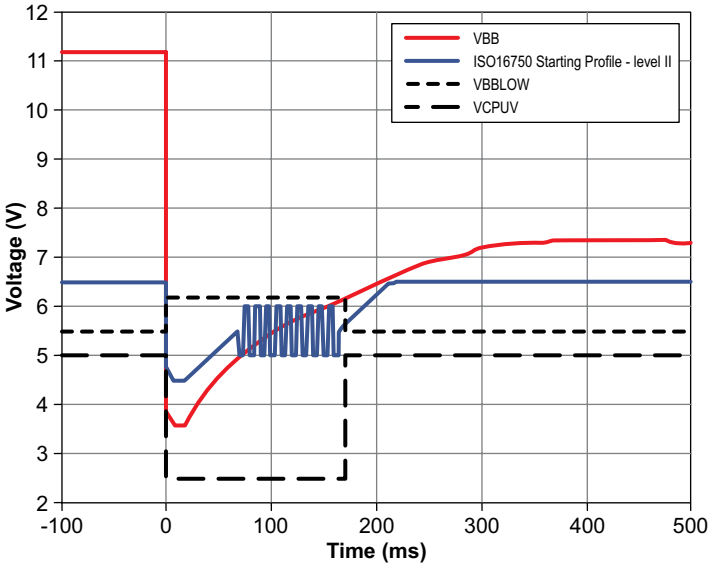

Figure 5: Response to an Undervoltage Transient

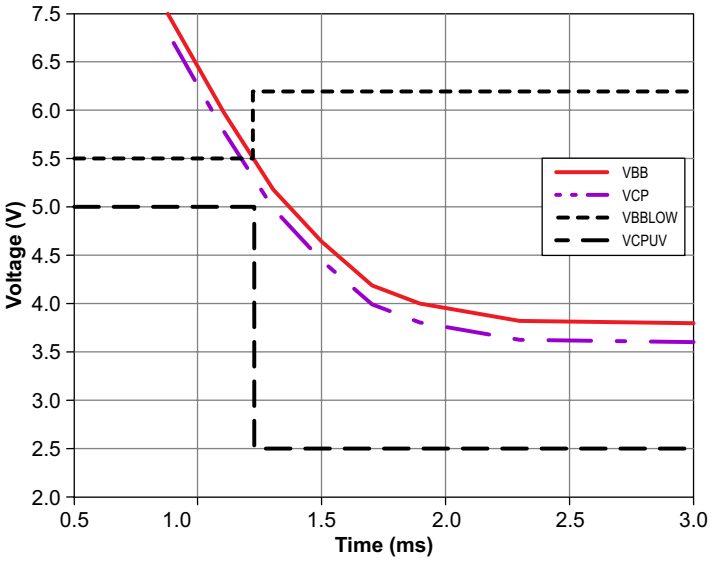

Figure 6: Expanded View of an Undervoltage Transient Response

When VBB drops below the falling VBB low threshold (at 1.2 ms and 5.5 V in Figure 6), the VCP undervoltage threshold drops from typically 5 V to typically 2.5 V. At the same time, the VBB low threshold increases by the threshold hysteresis, typically 700 mV, and the fault flag is active.

This state remains until VBB increases above the rising VBB low threshold (at 170 ms and 6.2 V in Figure 5). At this point, the VCP undervoltage threshold is increased back to the high threshold value of typically 5 V, and the reverse hysteresis is applied to the VBB low threshold, causing it to drop back to the falling level of typically 5.5 V. The fault flag goes inactive, but the UV fault bit remains set in the fault register until cleared.

When a power-on reset occurs, or the A4993 is activated from sleep mode, then the VCP undervoltage threshold is initially set to the high level (V_{CPUVH}). (A power-on reset occurs when power is first applied or the internal logic supply drops below its operational limit.) The threshold will remain at the high level, irrespective of the state of VBB, until the VBB voltage has exceeded the VBB low threshold for the first time. When this happens, the VCP undervoltage threshold is then determined by the state of the VBB low monitor output. When applying power or when activating from sleep mode, the outputs should remain inactive for at least the Wake Up From Sleep time (t_{EN}) to allow the internal charge pump and regulator to reach their full operating state.

The VBB low and VCP undervoltage monitor system is designed to allow the A4993 to continue operating safely during the extreme motor supply voltage drop caused by cold cranking with a weak battery when a reverse-battery protection diode is also present. During low-voltage transients, the A4993 will continue to step a motor; however, current control will not achieve the same accuracy as specified with a motor supply voltage greater than 7 V. In fact, a low motor supply voltage may not provide sufficient drive to allow the motor current to reach its normal operating level, especially if the motor is rotating and a back-EMF is present. It is therefore recommended that when a VBB-low condition is indicated, the motor is held stationary. This will help ensure that the motor does not slip and that the system retains some degree of control over the motor position, thus avoiding the need to recalibrate the motor position.

The output drive MOSFETs of the A4993 remain protected from short circuits down to the VBB undervoltage level; however, the overcurrent thresholds cannot be guaranteed to meet the precision

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specified at higher supply voltage. In addition, the open-load detection may indicate a fault.

TEMPERATURE MONITORS

Two temperature thresholds are provided: a hot warning and an overtemperature shutdown.

- If the chip temperature rises above the hot temperature warning threshold (T_{JW}), the hot warning bit (TW) is set to 1 in the Status register. No action is taken by the A4993. When the temperature drops below T_{JW} by more than the hysteresis value (T_{JWHys}), the fault state is cleared, but the TW bit remains at1 in the Status register until reset.
- If the chip temperature rises above the overtemperature threshold (T_{JF}), the overtemperature bit (OT) is set to 1 in the Status register, and the A4993 disables the outputs to try to prevent a further increase in the chip temperature. When the temperature drops below T_{JF} by more than the hysteresis value (T_{JFHys}), the fault state is cleared, and the outputs re-enabled. The OT bit remains at 1 in the Status register until reset.

If either of these supply fault states is present and the general fault flag is selected for output on DIAG, then DIAG will be low.

Bridge and Output Diagnostics

The A4993 includes monitors that can detect a short to supply or a short to ground at the motor phase connections. These conditions are detected by monitoring the current from the motor phase connections through the bridge to the motor supply and to ground.

Low-current comparators and timers are provided to help detect possible open-load conditions.

LOW-SIDE OVERCURRENT (SHORT TO SUPPLY)

A short from any of the motor connections to the motor supply VBB is detected by monitoring the current through each of the low-side MOSFETs in each bridge.

An overcurrent condition is detected when the current through the active low-side MOSFET exceeds the low-side overcurrent threshold (I_{OCL}) per the Electrical Characteristics table. If the maximum phase current is set to a value of 280 mA or higher (MXI[3:0]=2...15), a threshold value of 2.05 V (typical) applies; if the maximum phase current is set to a value of 100 mA or lower (MXI[3:0]=0,1), the threshold is reduced to 0.5 A (typical).

The overcurrent condition must be present for at least the overcurrent fault delay time (t_{OC}) before the overcurrent fault state is confirmed by setting the overcurrent fault bit to 1 for the associated MOSFET in the Diag 1 register.

If overcurrent fault states are present and the general fault flag is selected for output on DIAG, then DIAG will be taken low. The affected bridge (A or B) is switched off and remains off until an overcurrent fault reset occurs.

HIGH-SIDE OVERCURRENT (SHORT TO GROUND)

A short from any of the motor connections to ground is detected by monitoring the current through each of the high-side MOSFETs in each bridge.

An overcurrent condition is detected when the current through the active high-side MOSFET exceeds the high-side overcurrent threshold (I_{OCH}) per the Electrical Characteristics table. The high-side overcurrent threshold value of 2.05 A (typical) applies for all maximum phase current settings (MXI[3:0]=0...15).

The overcurrent condition must be present for at least the overcurrent fault delay time (t_{OC}) before the overcurrent fault state is confirmed by setting the overcurrent fault bit to 1 for the associated MOSFET in the Diag 1 register.

If overcurrent fault states are present and the general fault flag is selected for output on DIAG, then DIAG will be low. The affected bridge (A or B) is switched off and remains off until an overcurrent fault reset occurs.

Note that when a high-side overcurrent condition is detected, the current through the high-side MOSFET is limited to the high-side current limit (I_{LIMH}) during the overcurrent fault delay time. This prevents large negative transients at the phase output terminals when the outputs are switched off.

SHORTED LOAD

If the supply voltage is high enough to drive the bridge current above the overcurrent thresholds, a short across the load may be indicated by concurrent overcurrent fault states on both high-side and low-side MOSFETs.

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OVERCURRENT FAULT BLANKING

All overcurrent conditions are ignored for the duration of the overcurrent detection delay time (t_{OC}) set between 1 and 4 µs by the contents of the TOC[1:0] variable. The overcurrent detection delay timer is started when an overcurrent condition is first detected. If the overcurrent condition is still present at the end of the overcurrent detection delay time, then an overcurrent fault state will be detected and latched. If the overcurrent condition is removed before the overcurrent detection delay time is complete, then the timer is reset and no fault is detected.

This prevents false overcurrent detection caused by supply and load transients. It also prevents false overcurrent detection from the current transients generated by the motor or wiring capacitance when a MOSFET is first switched on

OVERCURRENT FAULT RESET AND RETRY

Once an overcurrent fault state has been detected, all outputs for the phase where the fault state is present are disabled until the fault state is reset. Overcurrent fault states are reset as a result of a successful read of the Diag 1 register, or a reset pulse on RESETn, or a transition to sleep mode and back via RESETn, or the SLP bit in the Control register. Additionally, if the Overcurrent Fault Action bit (OFA) is set to 0, any overcurrent fault states are reset on every rising edge on the STEP input. When the fault state is reset, the outputs are re-enabled and, if the general fault flag is selected for output on DIAG and there are no other faults, then DIAG will be allowed to go high.

Resetting Overcurrent fault states on STEP rising edges allows automatic restart when the cause of the overcurrent is removed. If the cause of the overcurrent persists, the part will repeatedly cycle between overcurrent and attempted restart. In this condition, the device will not suffer damage, but if step demands are being applied at a high rate, it may eventually shut down due to overtemperature.

If the OFA bit is set to 1, rising edges on STEP do not reset overcurrent fault states, and the automatic restart capability is disabled.

OPEN-LOAD DETECTION

Open-load detection is carried out on both phases, and if either phase current drops below the open-load current threshold (I_{OL}), an open-load state is flagged. (I_{OL} is set to either 13 mA or 26 mA according to the state of the OLT bit in the Config 1 register.)

Unfortunately, simple current monitoring is only viable for stationary motors where the current rises quickly. When motors are running at high speed, phase current rise time is severely affected by motor back-EMF, and the current may not reach its peak until late in the step period. Consequently, if open-load current comparisons were to run continuously, false open-load states would be flagged for at least part of the step period in many instances. To avoid such false states, the open-load comparator outputs are only checked after the expiry of the open-load detect time. This lockout period starts on each step command and has a duration of 10 to 40 ms per the contents of the TOL[1:0] variable. Additionally, the comparator output for each phase is only checked if the target current for that phase is greater than twice the open-load threshold current.

The A4993 continues to drive the bridge outputs under an open-load condition. The associated fault state is cleared as soon as (i) a step command is received, or (ii) the phase current reaches the PWM threshold level, or (iii) the open-load detect time expires and the phase current is detected to have risen above the open-load current threshold.

Device Reset

Various mechanisms may be used to reset or partially reset the A4993.

RESET PULSE

Pulsing the RESETn input low for a duration compliant with the Reset Pulse Width (t_{RST}) clears all fault states (with the exception of POR and, if set by POR, FF) and the General Fault Flag (DIAG pin). Additionally, the Diag 1 and Status registers (with the exception of the POR bit and, if set by POR, FF) are both cleared. The Diag 0 register (step angle number) is not reset to its home value.

SLEEP

Entering and then exiting sleep mode (via RESETn or the SLP bit in the Control register) clears all fault states (with the exception of POR and, if set by POR, FF) and the General Fault Flag (DIAG pin). Additionally, the Diag 1 and Status registers (with the exception of the POR bit and, if set by POR, FF) are cleared, and the step angle number in the Diag 0 register is reset to its home value (step 0 for single phase full step, step 8 for all other modes).

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DIAG 0 REGISTER READ

Reading Diag 0 via the SPI bus does not clear any fault states, nor the General Fault Flag (DIAG pin), nor any registers.

DIAG 1 REGISTER READ

Reading Diag 1 via the SPI bus clears all overcurrent fault states and the General Fault Flag (if exclusively set as a result of an overcurrent fault). Additionally, the BML, BMH, BPL, BPH, AML, AMH, APL, APH bits in the Diag 1 register are cleared, as are the OCA and OCB bits in the Status register. All other bits in the Status register are not cleared, and the contents of the Diag 0 register are not altered.

STATUS REGISTER READ

Implicitly reading the Status register via the SPI bus (by completing a valid serial write) clears all fault states other than those generated by overcurrent faults. If no other faults are present, this action also clears the General Fault Flag. Additionally, the FF, POR, SE, UV, TW, OT, ST, OV, VL, OLB, and OLA bits in the Status register are cleared. The Diag 0 register (step angle number) is left unchanged.

STEP INPUT

If the Overcurrent Fault Action (OFA) bit in the Config 1 register is set to its default value of 0, all overcurrent fault states and any associated fault indication on the General Fault Flag are cleared on every rising edge on the STEP input. This provides a means of automatically attempting a restart. No bits in the Diag 0, Diag 1 or Status registers are cleared, thereby allowing suspected faults to be investigated via the SPI bus.

If the Overcurrent Fault Action (OFA) bit in the Config 1 register is set to 1, rising edges on the STEP input do not clear any fault states or register bits. Automatic attempts at restart are disabled.

Step Angle Reset

The step angle number may be set to its home value by a power-on reset, using RESETn to enter and then exit sleep mode, or by writing a logic 1 to the SAR bit in the Control register. If using the SAR bit, the reset takes place on the rising edge on STRn at the end of the write cycle. Repeatedly overwriting the value 1 to the SAR bit repeatedly resets the step angle. The SAR bit may be cleared by a writing 0 via the SPI interface. Maintaining SAR at 1 does not lock the step angle in the home condition, and any step commands received via the STEP input or Control register are obeyed.

Stall Detection

For all motors, it is possible to determine the mechanical state of the motor by monitoring the back-EMF (BEMF) generated in the motor phase winding. For most stepper motors, this can be used to detect a motor stall condition. A stalled motor is defined as one in which the phase currents are being sequenced to cause rotation but no movement occurs. This can be due to a mechanical blockage, such as an end stop, or it can be due to the step sequence exceeding the motor capability for the attached load.

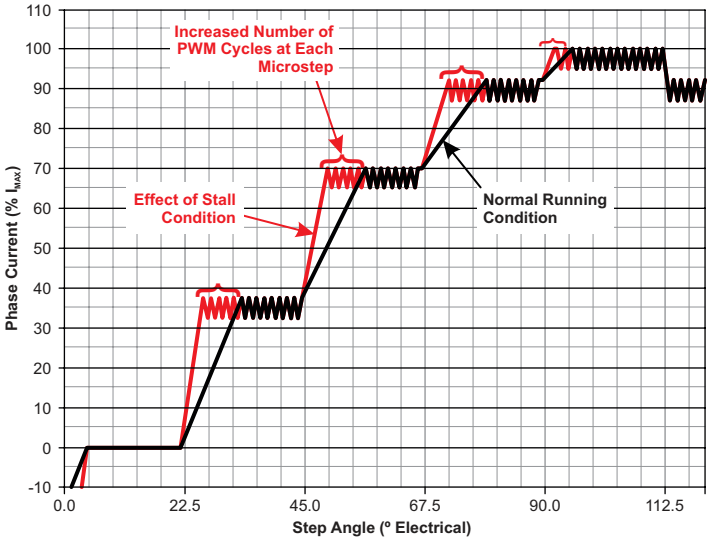

Figure 7: Effect of Stall Condition on Current Rise

The stall detect in the A4993 uses the indirect effect of the BEMF on the current rise time by comparing the PWM count during successive current rise quadrants to determine the point at which a stall occurs.

When a motor is running normally, at speed, the back-EMF generated by the magnetic poles in the motor passing the phase windings acts against the supply voltage and reduces the rise rate of the phase current, as shown in Figure 7. The PWM current control does not activate until the current reaches the set trip level for the microstep position. When a motor is stopped, as in a stall condition, the back-EMF is reduced. This allows the current to rise to the limit faster and the PWM current control to activate sooner. Assuming a constant step rate and motor load, this results in an increase in the number of PWM cycles for each step of the motor.

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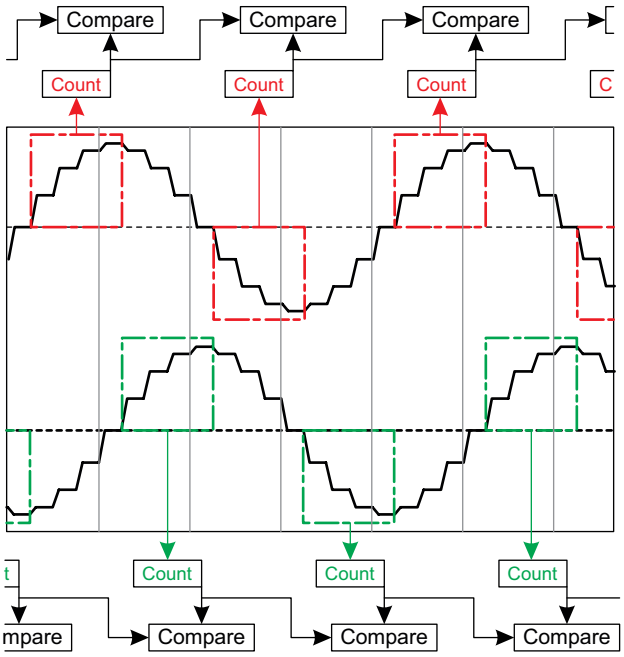

Figure 8: Stall Detect by PWM Count Compare

The A4993 uses this difference to detect a motor changing from continuous stepping to stalled. Two PWM counters, one for each phase, accumulate the number of PWM cycles when the phase current is stepped from zero to full current as shown in Figure 8. At the end of each phase current rise, the counter for that phase is compared to the count result for the previous current rise in the same phase. If the difference is greater than the number in the PWM compare register (CD[5:0]), then a stall condition will be detected and indicated.

This stall detection scheme requires that the motor is stepping fast enough for the back-EMF to reduce the phase current slew rate. Stall detection reliability improves as the current slew rate reduces.

Although stall detection cannot be guaranteed using this detection method, good stall detection reliability can be achieved by careful selection of motor-winding resistance and inductance, motor speed, count difference, and by conforming to the above factors.

Braking

The A4993 can be used to perform dynamic braking by setting the BRK = 1 in the Control register. If BRK is set to 1 and HLR = 0 in the Config 2 register, all high-side MOSFETs are turned on and all low-side MOSFETs are turned off, effectively short-circuiting any back-EMF generated by the motor and creating a breaking torque. If BRK is set to 1 and HLR=1, all low-side MOSFETs are turned on and all high-side MOSFETs are turned off, producing a similar effect at the motor. During braking, motor current (I_{BREAK}) can be approximated by:

$$I_{BRAKE} = \frac{V_{BEMF}}{R_L}$$

where V_{BEMF} is the voltage generated by the motor and R_L is the resistance of the phase winding. Care must be taken during braking to ensure that the power MOSFET maximum ratings are not exceeded. When dynamic braking is commanded, open-load conditions cannot be detected because of the bridge configuration that is enforced (both ends of each motor winding held in the same state).

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SERIAL INTERFACE

Serial Registers Definition*

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Config 0 (Current)	0	0	0	WR	NSR	TBK1	TBK0	FRQ1	FRQ0	DIT	SLEW	MXI3	MXI2	MXI1	MXI0	P
					0	1	1	0	1	0	0	1	0	0	0	
Config 1 (Protection)	0	0	1	WR	OLT		OFA	TOC1	TOC0	CD5	CD4	CD3	CD2	CD1	CD0	P
					0	0	0	0	1	0	0	0	0	0	0	
Config 2 (Operating)	0	1	0	WR	DG1	DG0	HLR	TOL1	TOL0				MS2	MS1	MS0	P
					0	0	0	1	0	0	0	0	0	1	0	
Table Load	0	1	1	WR						PT5	PT4	PT3	PT2	PT1	PT0	P
					0	0	0	0	0	0	0	0	1	0	1	
Diag 0	1	0	0	0						SA5	SA4	SA3	SA2	SA1	SA0	P
					0	0	0	0	0	0	0	1	0	0	0	
Diag 1	1	0	1	0				BML	BMH	BPL	BPH	AML	AMH	APL	APH	P
					0	0	0	0	0	0	0	0	0	0	0	
Mask	1	1	0	WR	TW	OT	ST	OV	VL			OLB	OLA	OCB	OCA	P
					0	0	0	0	0	0	0	0	0	0	0	
Control	1	1	1	WR	SLP	DIR	BRK	DIS	SAR	SC5	SC4	SC3	SC2	SC1	SC0	P
					0	0	0	0	0	0	0	0	0	0	0	

Status	FF	POR	SE	UV	TW	OT	ST	OV	VL			OLB	OLA	OCB	OCA	P
	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	

*Power-on reset value shown below each input register bit.

A three-wire synchronous serial interface, compatible with SPI, can be used to control all features of the A4993. A fourth wire can be used during a serial transfer to provide diagnostic feedback and read-back of the register contents.

The A4993 can be operated without the serial interface using the default settings and the STEP and DIR input terminals. Application specific configurations are only possible by setting the appropriate register bits through the serial interface. In addition to setting the configuration bits, the serial interface can also be used to control the motor directly.

The serial interface timing requirements are specified in the Electrical Characteristics table and illustrated in the Serial Interface Timing diagram (see Figure 2). Data is received on the SDI terminal and clocked through a shift register on the rising edge of the clock signal input on the SCK terminal. A serial transfer is initiated by pulling the STRn terminal low.

STRn is normally high and is only brought low to initiate a serial transfer. No data is clocked through the shift register when STRn is high, allowing multiple slave units to use common SDI and SCK connections. Each slave then requires an independent STRn connection. The SDO output assumes a high-impedance state when STRn is high, allowing a common data read-back connection. When driving devices running from a 5 V logic supply, it may be necessary to add a 2 kΩ pull-up resistor from SDO to that supply to ensure an adequate logic high output voltage level is achieved.

When 16 data bits have been clocked into the shift register, STRn must be taken high to latch the data into the selected register. When this occurs, the internal control circuits act on the new data.

If there are more than 16 rising edges on SCK, or if STRn goes high and there are fewer than 16 rising edges on SCK, the write will be cancelled without writing data to the registers. In addition, the Diag 1 and Status registers will not be reset, and the SE bit will be set to indicate a data transfer error. This fault condition can be cleared by a subsequent valid serial write, a reset pulse on RESETn, a transition to sleep mode and back (RESETn or the SLP bit in the Control register), or a power-on reset.

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The first three bits (D[15:13]) in a serial word are the register address bits giving the possibility of 8 register addresses. The fourth bit (WR D[12]) is the write/read bit. Except for the read-only registers, when WR is 1, the following 11 bits (D[11:1]) clocked in from the SDI terminal are written to the addressed register. When WR is 0, no data is written to the serial registers, and the contents of the addressed register are clocked out on the SDO terminal.

The last bit in any serial transfer (D[0]) is a parity bit that is set to ensure odd parity in the complete 16-bit word. Odd parity means that the total number of 1s in any transfer should always be an odd number. This ensures that there is always at least one bit set to 1 and one bit set to 0 and allows detection of stuck-at faults on the serial input and output data connections. The parity bit is not stored but generated on each transfer.

If the A4993 detects a parity error during a serial transfer, the data in question will not be written to the selected device register.

Register data is output on the SDO terminal MSB first while STRn is low and changes to the next bit on each falling edge of SCK. The first bit, which is always the FF bit from the Status register, is output as soon as STRn goes low.

Registers 4 and 5 (Diag 0, Diag 1) contain detailed diagnostic indicators and are read-only. If D[12] is set to 0, the content of the addressed register is clocked out on SDO D[11:1]. If D[12] is set to 1, no data is written to the addressed register, and the content of the Status register is clocked out on SDO D[11:1].

In addition to the addressable registers, a read-only Status register is output on SDO for all register addresses when WR is set to 1. For all serial transfers, the first four bits output on SDO will always be the first four bits from the Status register.

Configuration Registers

Three registers are used to configure the parameters of the A4993.

CONFIG 0: CURRENT CONTROL PARAMETERS

NSR: Disables synchronous rectification

TBK: 2 bits select the blank time, t_{BL}

FRQ: 2 bits select the PWM clock frequency

DIT: Enables PWM frequency jitter

SLEW: Selects output voltage slew rate

MXI: 4 bits select the maximum output current

CONFIG 1: PROTECTION AND DIAGNOSTIC PARAMETERS:

OLT: Selects the open-load threshold current

OFA: Selects action taken on an overcurrent fault

TOC: 2 bits select the overcurrent fault delay time t_{OC}

CD: 6-bit integer to set the PWM count difference for stall detection

CONFIG 2: OPERATING PARAMETERS:

DG: 2 bits selects the output on the DIAG terminal

HLR: Selects the slow decay recirculation path

TOL: 2 bits selects the open-load detect timeout

MS: 3 bits select the microstep resolution

Table Load Register

This register provides an access port to write or read an array of 16 phase table values, PT(0) to PT(15), sequentially to or from the phase current table in the A4993. This allows the current at each Step Angle Number to be tailored to suit the microstep current profile requirements of a specific motor. In most cases, this feature will not be required and the default sinusoidal profile will suffice; however, for some motor/load combinations, altering the current profile can improve torque ripple, resulting in lower mechanical vibration and noise. Although the phase current table contains 64 entries for each of two phases, only 16 distinct values are required. These 16 values correspond to one quadrant of the table for a single phase, and they are repeated for the other three quadrants and again for the four quadrants of the other phase. So each of the 16 values written to the Table Load register are written to 8 locations in the phase current table. The mapping of the phase table values to the step angle number entries is shown in Table 4.

The 16 phase table values must be entered by sequential uninterrupted writes to the Table Load register. A reset, read of any register (including the Table Load register), or write to any register other than the Table Load register will reset the table load pointer back to 0, as will any event that sets the SE bit in the Status register. The first write to the table load register after the

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table load pointer has been reset to 0 will write the 6-bit value in the PT[5:0] variable into the first phase table address, a 6-bit field defined as PT(0). Subsequent writes put values into successive addresses: PT(1), PT(2), and so forth, up to PT(15). After the sixteenth value has been written, no more values are accepted and any writes to the Table Load register are ignored. As each value is received, it is effectively distributed to all eight required locations in the phase current table.

Table 4: Table Load Register Mapping

	Step Angle Numbers							
	Phase A				Phase B			
0%	0		32			16		48
PT(0)	1	31	33	63	15	17	47	49
PT(1)	2	30	34	62	14	18	46	50
PT(2)	3	29	35	61	13	19	45	51
PT(3)	4	28	36	60	12	20	44	52
PT(4)	5	27	37	59	11	21	43	53
PT(5)	6	26	38	58	10	22	42	54
PT(6)	7	25	39	57	9	23	41	55
PT(7)	8	24	40	56	8	24	40	56
PT(8)	9	23	41	55	7	25	39	57
PT(9)	10	22	42	54	6	26	38	58
PT(10)	11	21	43	53	5	27	37	59
PT(11)	12	20	44	52	4	28	36	60
PT(12)	13	19	45	51	3	29	35	61
PT(13)	14	18	46	50	2	30	34	62
PT(14)	15	17	47	49	1	31	33	63
PT(15)		16		48	0		32	

The 16 phase table values can be read from the A4993 by sequential uninterrupted reads from the Table Load register. A reset, write to any register (including the Table Load register), or read from any register other than the Table Load register will reset the table load pointer back to 0, as will any event that sets the SE bit in the Status register. The first read from the table load register after the table load pointer has been reset to 0 will output the 6-bit value from the PT[5:0] variable stored in the first phase table address, PT(0). Subsequent reads output values from successive addresses: PT(1), PT(2), and so forth, up to PT(15). After the sixteenth value has been read, any reads from the Table Load register will output 1s in bits 11 through 1. In all reads, the parity bit will be set to ensure odd parity.

Control Register

A single register used to control the motion of the motor and the operating status of the A4993.

CONTROL:

SLP: Allows low-power sleep mode

DIR: Sets the direction for the STEP input

BRK: Puts the both bridges into permanent slow decay

DIS: Disables the motor drive outputs

SAR: Step angle reset. Resets the step angle number to the home position on STRn rising at the end of any write cycle setting the SAR bit to 1

SC: 6-bit integer step change number. Two's-complement number to increase or decrease the step angle number

Diagnostic Registers

In addition to the read-only Status register, three registers provide detailed diagnostic management and reporting.

DIAG 0 (READ-ONLY):

Returns the current step angle number. The contents of this register have no effect on the operation and can only be changed by the internal step angle controller in the A4993. A transition to sleep mode and back to operation (RESETn or the SLP bit in the Control register) resets the step angle number to its home value (step 0 for single phase full step, step 8 for all other modes).

Diag 0 is read-only. If an attempt is made to write to it by setting D[12] to 1, no data is transferred to the register, and Status register bits 1 to 11 are clocked out on SDO D[11:1] rather than Diag 0 bits 1 to 11.

DIAG 1 (READ-ONLY):

Individual bits indicating overcurrent faults detected in each bridge MOSFET. Any bits set to 1 in the Diag 1 register are reset to 0 as a result of a successful read of the Diag 1 register, or a reset pulse on RESETn, or a transition to sleep mode and back (via RESETn or the SLP bit in the Control register).

Diag 1 is read-only. If an attempt is made to write to it by setting D[12] to 1, no data is transferred to the register, and Status register bits 1 to 11 are clocked out on SDO D[11:1] rather than Diag 1 bits 1 to 11.

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MASK:

Contains a fault mask bit for each of the 11 least significant fault bits in the Status register. If a bit is set to 1 in the mask register, then the corresponding diagnostic will be completely disabled. No fault states for the disabled diagnostic will be generated, and no fault flags or diagnostic bits will be set.

Status Register

There is one Status register in addition to the 8 addressable registers. When any register transfer takes place, the first four bits output on SDO are always the most significant four bits of the Status register, irrespective of whether the addressed register is being read or written (see serial timing diagram). The content of the remaining twelve bits will depend on the state of the WR bit input on SDI. When WR is 1, the addressed register will be written, and the remaining twelve bits output on SDO will be the least significant eleven bits of the Status register and a parity bit. When WR is 0, the addressed register will be read, and the remaining twelve bits will be the contents of the addressed register and a parity bit.

If an attempt is made to write to either of the read-only registers (Diag 0 or Diag 1), no data will be written, and the remaining twelve bits output on SDO will be the least significant eleven bits of the Status register and a parity bit.

The read-only Status register provides a summary of the chip status by indicating whether any diagnostic monitors have detected a fault. The most significant four bits of the Status register indicate critical system faults. Bits 11 to 7, 4, and 3 provide indicators for specific individual monitors, and bits 2 and 1 are derived from the contents of the Diag 1 register.

The first and most significant bit in the register is the diagnostic status flag (FF). If any other bits in the Status register are set, this bit is high. When STRn goes low, to start a serial transfer, SDO outputs the diagnostic status flag. This allows the main controller to poll the A4993 through the serial interface to determine if a fault has been detected. If no faults have been detected, then the serial transfer may be terminated without generating a serial read fault by ensuring that SCK remains high while STRn is low. When STRn goes high, the transfer will be terminated and SDO will go into its high-impedance state.

The second most significant bit is the POR bit. At power-up or after a power-on reset, the FF bit and the POR bit are set, indicating to the external controller that a power-on reset has taken place. All other diagnostic bits are reset, and all other registers are returned to their default state. Note that a power-on reset only occurs when the outputs of the internal supply regulators (derived from VBB) rise to acceptable levels. Power-on reset is not directly affected by the state of the VBB supply or the charge pump output (VCP). In general, the UV bit will also be set following a power-on reset, as the charge pump will not have reached its rising undervoltage threshold until after the register reset is completed.

The third bit in the Status register is the SE bit, which indicates that the previous serial transfer (read or write) was not completed successfully.

Bits 12 to 3 contain fault bits for the eight individual monitors (UV, TW, OT, ST, OV, VL, OLB, and OLA). If one or more of these faults are no longer present, then the corresponding fault bits will be reset as a result of a successful read of the Status register, or a reset pulse on RESETn or a transition to sleep mode and back (via RESETn or the SLP bit in the Control register). Resetting only affects latched fault bits for faults that are no longer present. For any static faults that are still present (e.g., overtemperature), the fault flag will remain set after the reset.

The remaining bits (OCB and OCA) are derived from the contents of the Diag 1 register. If any of the phase B overcurrent fault bits (BML, BMH, BPL, BPH) are set, OLB is set. If any of the phase A overcurrent fault bits (AML, AMH, APL, APH) are set, OLA is set. OCB and OCA are only cleared when the corresponding contents of the Diag 1 register are cleared as a result of a successful read of the Diag 1 register, or a reset pulse on RESETn, or a transition to sleep mode and back (via RESETn or the SLP bit in the Control register). OCB and OCA cannot be cleared by reading the Status register. If, upon reading the Status register, OCA or OCB is found to be set to 1, the Diag 1 register may be read to locate the source of the fault and clear the fault state.

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	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Config 0 (Current)	0	0	0	WR	NSR	TBK1	TBK0	FRQ1	FRQ0	DIT	SLEW	MXI3	MXI2	MXI1	MXI0	P
					0	1	1	0	1	0	0	1	0	0	0	

Config 0

NSR – Non-synchronous Rectification

NSR	Synchronous rectification	Default
0	Enabled	D
1	Disabled - Diode recirculation	

TBK[1:0] – Blank Time

TBK1	TBK0	Period / Frequency	Default
0	0	1.0 µs	
0	1	1.5 µs	
1	0	2.5 µs	
1	1	3.5 µs	D

FRQ[1:0] – Frequency

FRQ 1	FRQ 0	Period / Frequency	Default
0	0	62 µs / 16.1 kHz	
0	1	46 µs / 21.7 kHz	D
1	0	39 µs / 25.6 kHz	
1	1	32 µs / 31.3 kHz	

DIT – Dither Control

DIT	Dither	Default
0	Inactive	D
1	Active	

SLEW – Slew Rate Control

SLEW	Slew Rate	Default
0	Fast	D
1	Slow	

MIX[3:0] – Max Phase Current (mA)

MXI3	MXI2	MXI1	MXI0	Maxi-mum Current	Default
0	0	0	0	60 mA	
0	0	0	1	100 mA	
0	0	1	0	280 mA	
0	0	1	1	500 mA	
0	1	0	0	550 mA	
0	1	0	1	600 mA	
0	1	1	0	650 mA	
0	1	1	1	700 mA	
1	0	0	0	750 mA	D
1	0	0	1	800 mA	
1	0	1	0	850 mA	
1	0	1	1	900 mA	
1	1	0	0	950 mA	
1	1	0	1	1000 mA	
1	1	1	0	1200 mA	
1	1	1	1	1400 mA	

P – Parity Bit

Ensures an odd number of 1s in any serial transfer.

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	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Config 1 (Protection)	0	0	1	WR	OLT		OFA	TOC1	TOC0	CD5	CD4	CD3	CD2	CD1	CD0	P
					0	0	0	0	1	0	0	0	0	0	0	
Config 2 (Operating)	0	1	0	WR	DG1	DG0	HLR	TOL1	TOL0				MS2	MS1	MS0	P
					0	0	0	1	0	0	0	0	0	1	0	

Config 1

OLT – Open-Load Threshold

OLT	Open-Load Threshold	Default
0	13 mA	D
1	26 mA	

OFA – Overcurrent Fault Action

OFA	Overcurrent Fault Action	Default
0	Retry	D
1	Disable outputs	

TOC[1:0] – Overcurrent Fault Delay

TOC1	TOC0	Detect delay time	Default
0	0	1 µs	
0	1	2 µs	D
1	0	3 µs	
1	1	4 µs	

CD[5:0] – PWM Count Difference for ST Detection

0 = Stall detect disabled

Default to 0.

P – Parity Bit

Ensures an odd number of 1s in any serial transfer.

Config 2

DG[1:0] – DIAG Output Select

DG1	DG0	DIAG output	Default
0	0	General fault, active low	D
0	1	Supply fault, active low	
1	0	Open load, active low	
1	1	Stall detect, active low	

HLR – Selects Slow Decay Recirculation Path

HLR	Recirculation Path	Default
0	High Side	D
1	Low Side	

TOL[1:0] – Open-Load Detect Time

TOL1	TOL0	OL Detect Time	Default
0	0	10 ms	
0	1	20 ms	
1	0	30 ms	D
1	1	40 ms	

MS[2:0] – Microstep Resolution

MS2	MS1	MS0	Microstep Resolution	Default
0	0	0	Full Two Phase	
0	0	1	Full One Phase Detent	
0	1	0	1/2 Compensated	D
0	1	1	1/2 Uncompensated	
1	0	0	1/4	
1	0	1	1/8	
1	1	0	1/16	
1	1	1	1/16	

P – Parity Bit

Ensures an odd number of 1s in any serial transfer.

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	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Table Load	0	1	1	WR						PT5	PT4	PT3	PT2	PT1	PT0	P
					0	0	0	0	0	0	0	0	1	0	1	

Table Load

PT(0..15)[5:0] – Phase Table Value

Sequential write to or read from the 16 values in the phase table value array, PT(0..15). Values in the phase table value array are mapped to the step angle number entries according to the following table:

Table Load Register Mapping

	Step Angle Number							
	Phase A				Phase B			
0%	0		32			16		48
PT(0)	1	31	33	63	15	17	47	49
PT(1)	2	30	34	62	14	18	46	50
PT(2)	3	29	35	61	13	19	45	51
PT(3)	4	28	36	60	12	20	44	52
PT(4)	5	27	37	59	11	21	43	53
PT(5)	6	26	38	58	10	22	42	54
PT(6)	7	25	39	57	9	23	41	55
PT(7)	8	24	40	56	8	24	40	56
PT(8)	9	23	41	55	7	25	39	57
PT(9)	10	22	42	54	6	26	38	58
PT(10)	11	21	43	53	5	27	37	59
PT(11)	12	20	44	52	4	28	36	60
PT(12)	13	19	45	51	3	29	35	61
PT(13)	14	18	46	50	2	30	34	62
PT(14)	15	17	47	49	1	31	33	63
PT(15)		16		48	0		32	

P – Parity Bit

Ensures an odd number of 1s in any serial transfer.

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	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Diag 0	1	0	0	0						SA5	SA4	SA3	SA2	SA1	SA0	P
					0	0	0	0	0	0	0	1	0	0	0	
Diag 1	1	0	1	0				BML	BMH	BPL	BPH	AML	AMH	APL	APH	P
					0	0	0	0	0	0	0	0	0	0	0	

Diag 0 (Read-Only)

SA[5:0] – Current Step Angle Number

6-bit integer from 0 to 63 indicating the step angle number currently in the internal step angle counter.

SA[5:0] can only be changed by the internal step angle counter. The contents of this register have no effect on the operation.

P – Parity Bit

Ensures an odd number of 1s in any serial transfer.

Diag 1 (Read-Only)

BML – Overcurrent on BM Output Low-Side

BMH – Overcurrent on BM Output High-Side

BPL – Overcurrent on BP Output Low-Side

BPH – Overcurrent on BP Output High-Side

AML – Overcurrent on AM Output Low-Side

AMH – Overcurrent on AM Output High-Side

APL – Overcurrent on AP Output Low-Side

APH – Overcurrent on AP Output High-Side

P – Parity Bit

Ensures an odd number of 1s in any serial transfer.

xx	Fault
0	No fault detected
1	Fault detected

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	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mask	1	1	0	WR	TW	OT	ST	OV	VL			OLB	OLA	OCB	OCA	P
					0	0	0	0	0	0	0	0	0	0	0	
Control	1	1	1	WR	SLP	DIR	BRK	DIS	SAR	SC5	SC4	SC3	SC2	SC1	SC0	P
					0	0	0	0	0	0	0	0	0	0	0	

MASK

TW – Temperature Warning

OT – Overtemperature

ST – Stall

OV – VBB Overvoltage

VL – VBB Low Voltage

OLB – Phase B Open Load

OLA – Phase A Open Load

OCB – Phase B Overcurrent

OCA – Phase A Overcurrent

P – Parity Bit

Ensures an odd number of 1s in any serial transfer.

xx	Fault mask	Default
0	Fault detection permitted	D
1	Fault detection disabled	

Control

SLP – Sleep Mode Enable

SLP	Sleep	Default
0	Sleep mode disabled	D
1	Sleep mode enabled	

DIR – Motor Stepping Direction

DIR	Step Direction	Default
0	Forward	D
1	Reverse	

BRK – Brake Enable

BRK	Brake	Default
0	Normal Operation	D
1	Brake Active	

DIS – Phase Current Disable

DIS	Phase Outputs	Default
0	Output bridges enabled	D
1	Output bridges disabled	

SAR: Step Angle Reset

SAR	Phase Outputs	Default
0	Normal operation	D
1	Reset to home position on STRn high	

SC[5:0] – Step Change Number

2’s-complement format

Positive value increases step angle number

Negative value decreases step angle number

P – Parity Bit

Ensures an odd number of 1s in any serial transfer.

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Status	FF	POR	SE	UV	TW	OT	ST	OV	VL			OLB	OLA	OCB	OCA	P
	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	

Status (Read-Only)

FF – Fault Register Flag

POR – Power-On Reset

SE – Serial Error

UV – Undervoltage on VBB or VCP

TW – Temperature Warning

OT – Overtemperature

ST – Stall

OV – Overvoltage on VBB

VL – Low Voltage on VBB

OLB – Open Load on Phase B

OLA – Open Load on Phase A

OCB – Overcurrent on Phase B

OCA – Overcurrent on Phase A

Status Register Bit Mapping

Status Register Bit	Related Diag 1 Register Bits
OCB	BML, BMH, BPL, BPH
OCA	AML, AMH, APL, APH

P – Parity Bit

Ensures an odd number of 1s in any serial transfer.

xx	Fault
0	No fault detected
1	Fault detected

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Table 5: Phase Current Table[1,2] (default, power-on content)

Step Number					Phase Current [%I_{SMAX}]		Step Angle	Phase		DAC	
Full	1/2	1/4	1/8	1/16	A	B		A	B	A	B
	0	0	0	0	0.00%	100.00%	0.0	0	0	0	63
				1	9.38%	100.00%	5.4	0	0	5	63
			1	2	18.75%	98.44%	10.8	0	0	11	62
				3	29.69%	95.31%	17.3	0	0	18	60
		1	2	4	37.50%	92.19%	22.1	0	0	23	58
				5	46.88%	87.50%	28.2	0	0	29	55
			3	6	56.25%	82.81%	34.2	0	0	35	52
				7	64.06%	76.56%	39.9	0	0	40	48
0	1	2	4	8	70.31%	70.31%	45.0	0	0	44	44
				9	76.56%	64.06%	50.1	0	0	48	40
			5	10	82.81%	56.25%	55.8	0	0	52	35
				11	87.50%	46.88%	61.8	0	0	55	29
		3	6	12	92.19%	37.50%	67.9	0	0	58	23
				13	95.31%	29.69%	72.7	0	0	60	18
			7	14	98.44%	18.75%	79.2	0	0	62	11
				15	100.00%	9.38%	84.6	0	0	63	5
	2	4	8	16	100.00%	0.00%	90.0	0	0	63	0
				17	100.00%	-9.38%	95.4	0	1	63	5
			9	18	98.44%	-18.75%	100.8	0	1	62	11
				19	95.31%	-29.69%	107.3	0	1	60	18
		5	10	20	92.19%	-37.50%	112.1	0	1	58	23
				21	87.50%	-46.88%	118.2	0	1	55	29
			11	22	82.81%	-56.25%	124.2	0	1	52	35
				23	76.56%	-64.06%	129.9	0	1	48	40
1	3	6	12	24	70.31%	-70.31%	135.0	0	1	44	44
				25	64.06%	-76.56%	140.1	0	1	40	48
			13	26	56.25%	-82.81%	145.8	0	1	35	52
				27	46.88%	-87.50%	151.8	0	1	29	55
		7	14	28	37.50%	-92.19%	157.9	0	1	23	58
				29	29.69%	-95.31%	162.7	0	1	18	60
			15	30	18.75%	-98.44%	169.2	0	1	11	62
				31	9.38%	-100.00%	174.6	0	1	5	63
	4	8	16	32	0.00%	-100.00%	180.0	0	1	0	63

Step Number					Phase Current [%I_{SMAX}]		Step Angle	Phase		DAC	
Full	1/2	1/4	1/8	1/16	A	B		A	B	A	B
	4	8	16	32	0.00%	-100.00%	180.0	0	1	0	63
				33	-9.38%	-100.00%	185.4	1	1	5	63
			17	34	-18.75%	-98.44%	190.8	1	1	11	62
				35	-29.69%	-95.31%	197.3	1	1	18	60
		9	18	36	-37.50%	-92.19%	202.1	1	1	23	58
				37	-46.88%	-87.50%	208.2	1	1	29	55
			19	38	-56.25%	-82.81%	214.2	1	1	35	52
				39	-64.06%	-76.56%	219.9	1	1	40	48
2	5	10	20	40	-70.31%	-70.31%	225.0	1	1	44	44
				41	-76.56%	-64.06%	230.1	1	1	48	40
			21	42	-82.81%	-56.25%	235.8	1	1	52	35
				43	-87.50%	-46.88%	241.8	1	1	55	29
		11	22	44	-92.19%	-37.50%	247.9	1	1	58	23
				45	-95.31%	-29.69%	252.7	1	1	60	18
			23	46	-98.44%	-18.75%	259.2	1	1	62	11
				47	-100.00%	-9.38%	264.6	1	1	63	5
	6	12	24	48	-100.00%	0.00%	270.0	1	1	63	0
				49	-100.00%	9.38%	275.4	1	0	63	5
			25	50	-98.44%	18.75%	280.8	1	0	62	11
				51	-95.31%	29.69%	287.3	1	0	60	18
		13	26	52	-92.19%	37.50%	292.1	1	0	58	23
				53	-87.50%	46.88%	298.2	1	0	55	29
			27	54	-82.81%	56.25%	304.2	1	0	52	35
				55	-76.56%	64.06%	309.9	1	0	48	40
3	7	14	28	56	-70.31%	70.31%	315.0	1	0	44	44
				57	-64.06%	76.56%	320.1	1	0	40	48
			29	58	-56.25%	82.81%	325.8	1	0	35	52
				59	-46.88%	87.50%	331.8	1	0	29	55
		15	30	60	-37.50%	92.19%	337.9	1	0	23	58
				61	-29.69%	95.31%	342.7	1	0	18	60
			31	62	-18.75%	98.44%	349.2	1	0	11	62
				63	-9.38%	100.00%	354.6	1	0	5	63
	0	0	0	0	0.00%	100.00%	0.0	0	0	0	63

[1] To be read in conjunction with Table 6: Step Angle Allocation
[2] The home position is defined as step number 8 for all modes of operation except 1-phase full step in which home is defined as step 0

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APPLICATIONS INFORMATION

Motor Movement Control

The A4993 provides two independent methods to control the movement of a stepper motor. The simplest is the step and direction method, which only requires two control signals to control the stepper motor in either direction. The other is through the serial interface, which provides more flexible control capability. Although it is not common, both methods can be used together provided the timing restrictions of the STEP input in relation to the STRn input are preserved.

PHASE TABLE AND PHASE DIAGRAM

The key to understanding both of the available control methods lies in understanding the phase current table. This table contains the relative phase current magnitude and direction for each of the two motor phases at each microstep position. The maximum resolution of the A4993 is 1/16th microstep. That is 16 microsteps per full step. There are 4 full steps per electrical cycle so the phase current table has 64 microstep entries. The entries are numbered from 0 to 63. This number represents the phase angle within the full 360° electrical cycle and is called the step angle number. This is illustrated in Figure 10.

Figure 10 shows the contents of the phase current table as a phase diagram. The phase B current (I_B) from the phase current table is plotted on horizontal axis, and the phase A current (I_A) is plotted on the vertical axis. The resultant motor current at each microstep is shown as numbered radial arrows. The number shown corresponds to the 1/16th microstep step angle number in the phase current table.

Figure 9 shows an example of calculating the resultant motor current magnitude and angle for step number 28. The target is to have the magnitude of the resultant motor current to be 100% at all microstep positions. The relative phase currents from the phase current table are:

$$I_A = 37.50\%$$

$$I_B = -92.19\%$$

Assuming a full-scale (100%) current of 1 A means that the two phase currents are:

$$I_A = 0.3750\ A$$

$$I_B = -0.9219\ A$$

The magnitude of the resultant will be the square root of the sum of the squares of these two currents:

$$|I_{28}| = \sqrt{I^2_A + I^2_B} = \sqrt{0.1406 + 0.8499} = 0.9953 \qquad (A)$$

So the resultant current magnitude is 99.53% of full scale. This is within 0.5% of the target 100% and is well within the ±10% accuracy of the A4993.

The reference angle, that is zero degrees (0°), within the full electrical cycle (360°), is defined as the angle where I_B is at +100% and I_A is zero. Each full step is represented by 90° in the electrical cycle, so each 1/16th microstep is (90°/16 steps =) 5.625°. The target angle of each microstep position with the electrical cycle is determined by product of the step angle number and the angle for a single microstep. So for the example of Figure 9:

$$\alpha_{28(TARGET)} = 28 \times 5.625^o = 157.5^o$$

The actual angle is calculated using basic trigonometry as:

$$\alpha_{28(ACTUAL)} = 180 + tan\text{-}1\left(\frac{I_{A28}}{I_{B28}}\right) = 180 + (-22.1) = 157.9^o$$

So the angle error is only 0.4°. Equivalent to about 0.1% error in 360° and well within the current accuracy of the A4993.

Note that each phase current in the A4993 is defined by a 6-bit DAC. This means that the smallest resolution of the DAC is 100 / 64 = 1.56% of the full scale, so the A4993 cannot produce a resultant motor current of exactly 100% at each microstep, nor can it produce an exact microstep angle. However, as can be seen from the calculations above, the results for both are well within the specified accuracy of the A4993 current control. The resultant motor current angle and magnitude are also more than precise enough for all but the highest precision stepper motors.

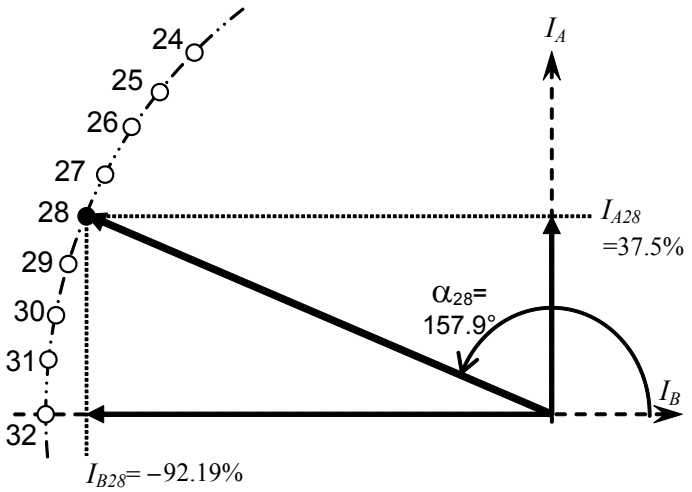

Figure 9: Calculating the Resultant Motor Current

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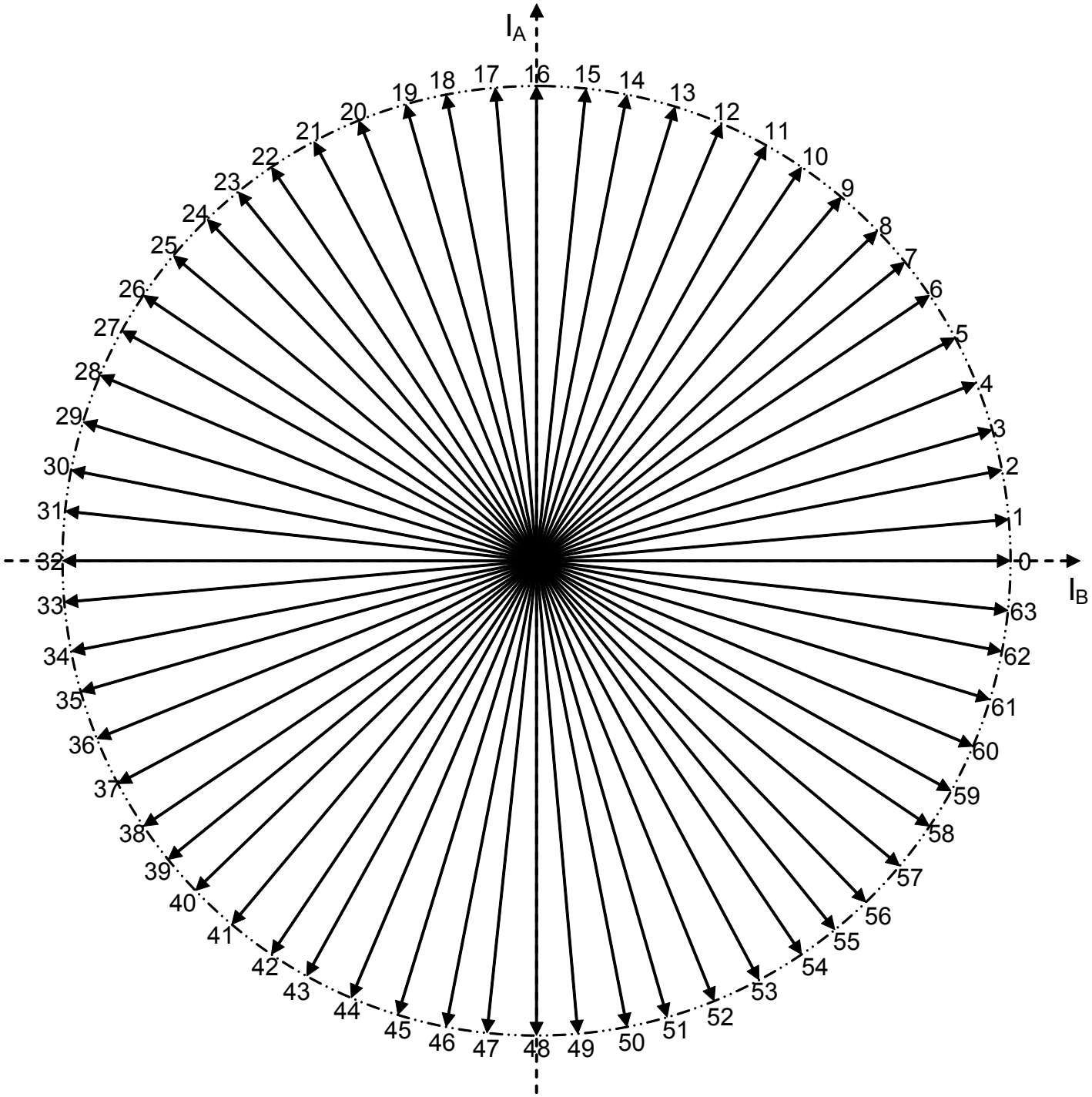

Figure 10: A4993 Phase Current Table as a Phase Diagram

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With the phase current table, control of a stepper motor is simply a matter of increasing or decreasing the Step angle number to move around the phase diagram of Figure 10. This can be in predefined multiples using the STEP input, or it can be variable using the serial interface.

USING STEP AND DIRECTION CONTROL

The STEP input moves the motor at the microstep resolution defined by the MS[2:0] bits. The DIR input defines the motor direction. These inputs define the output of a step angle counter which determines the required step angle number in the phase current table. Table 5 summarizes the step angle numbers used for the resolutions available when using the STEP input to control the output of the A4993.

Note that the MS[2:0] microstep resolution bits and the DIR bit are only relevant when controlling the motor with the STEP input. They have no effect when the motor is fully controlled over the serial interface by writing to the SC[5:0] bits.

In sixteenth-step mode, the step angle counter simply increments or decrements the step angle number by one on each rising edge of the STEP input depending on the logic state of the DIR input. In the other microstep resolution modes, the step angle counter outputs specific step angle numbers as defined in Table 5: Phase Current Table and summarized in Table 6: Step Angle Allocation.

Table 6: Step Angle Allocation

Mode	Step angle numbers used
Full 1 phase	0, 16, 32, 48
Full 2 phase	8, 24, 40, 56
Half Compensated.	0, 8, 16, 24, 32, 40, 48,56
Half Uncompensated	0, 0/16, 16, 16/32, 32, 32/48, 48, 48/0
Quarter	0, 4, 8, 12, 16, 20, 24, 28, 32, 36, 40, 44, 48, 52, 56, 60
Eighth	0, 2, 4, 6, 8, 10, 12, 14, 16 18, 20, 22, 24, 26, 28, 30, 32, 34, 36, 38, 40, 42, 44, 46, 48, 50, 52, 54, 56, 58, 60, 62
Sixteenth	All

There are two full-step modes available: 1-phase and 2-phase. In both cases, four of the entries in the phase current table are used. 1-phase full-step mode uses step angles 0, 16, 32, and 48, as shown in Figure 11, and only one phase is active at any time. These step angles place the motor at the detent points, the positions where the motor naturally settles to minimize the internal magnetic path reluctance. This mode has the advantage that once the motor movement has stopped, the current can be reduced to a very low level to hold the motor. The magnetic fields will be acting with any hold current to prevent motor movement.

2-phase mode uses step angles 8, 24, 40, and 56, as shown in Figure 12. In this case, two phases are always active at each step position. There are two advantages in using these positions rather than the single full current positions. With both phases active, the power dissipation is shared between two drivers. This slightly improves the ability to dissipate the heat generated and reduces the stress on each driver. The second advantage is that the holding torque is slightly improved because the forces holding the motor are mainly rotational rather than mainly radial.

Two half-step modes are available: compensated and uncompensated. Compensated mode uses eight of the entries in the phase current table. These are 0, 8, 16, 24, 32, 40, 48, and 56, as shown in Figure 13. In this mode, the current in each phase is compensated for the step angle to ensure that the average torque is the same at all step positions.

Uncompensated half-step mode does not reduce the current based on the step angle. Instead, each phase is driven to the current target defined by the 100% current value at steps 0, 16, 32, or 48, in the phase angle table. This is the value stored in the PT(15) variable. The current polarity is the same at each half-step angle, as defined in the phase angle table. The resulting phase diagram is shown in Figure 14.

Quarter-step uses sixteen of the entries in the phase current table. These are the multiples of 4, namely 0, 4, 8, 12, 16, 20, 24, 28, 32, 36, 40, 44, 48, 52, 56, and 60, as shown in Figure 15. Eighth-step mode uses the 32 even-numbered entries in the phase current table including 0, namely 0, 2, 4, and so on up to 58, 60, and 62, as shown in Figure 16.

In quarter-step, eighth-step and sixteenth-step modes, the current in each phase is compensated for the step angle to ensure that the average torque is the same at all step positions.

The microstep selection can be changed between each rising edge of the STEP input. When the microstep resolution changes, the A4993 moves to the next available step angle number at the new resolution on the next rising edge of the STEP input. For example, if the microstep mode is sixteenth and the present step angle is 57, then with the direction forwards (increasing step angle), changing to quarter-step mode will cause the phase number to go to 60 on the next rising edge of the STEP input, and changing to half-step mode will cause the phase number to go to 0 on the next rising edge of the STEP input.

On first power-up, after a power-on reset or after sleep, the step angle number is set to 8, equivalent to the electrical 45° position, except for full-step single-phase drive where the step angle number is set to 0. This position is defined as the “home” position.

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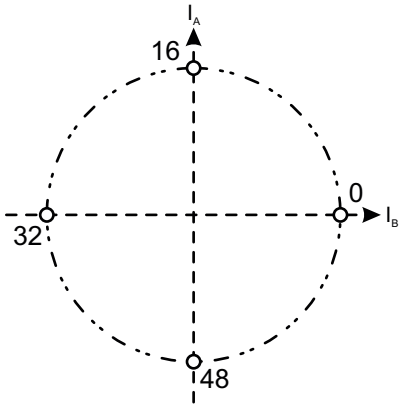

Figure 11: Full-Step 1-Phase Drive Phase Diagram

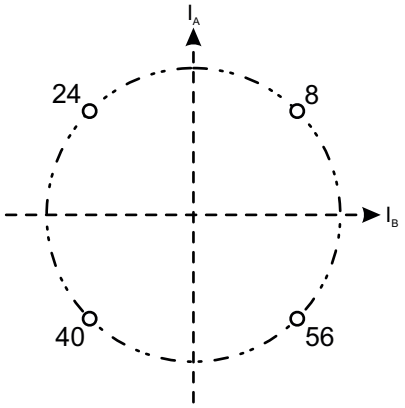

Figure 12: Full-Step 2-Phase Drive Phase Diagram

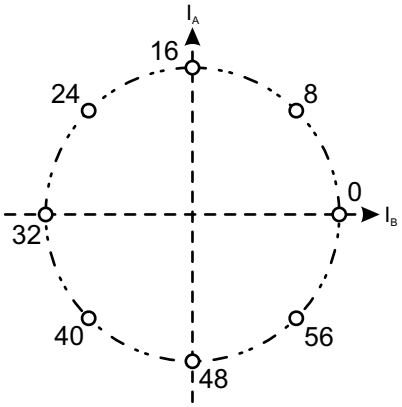

Figure 13: Compensated Half-Step Phase Diagram

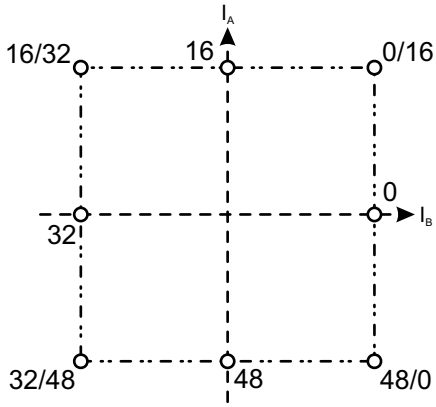

Figure 14: Uncompensated Half-Step Phase Diagram

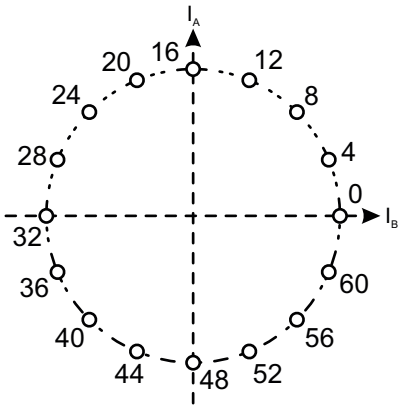

Figure 15: Quarter-Step Phase Diagram

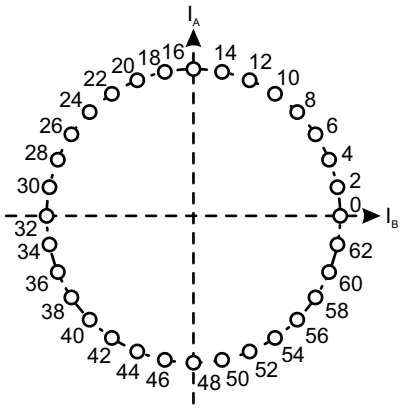

Figure 16: Eighth-Step Phase Diagram

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CONTROL THROUGH THE SERIAL INTERFACE

The A4993 provides the ability to directly control the motor movement using only the serial interface by directly increasing or decreasing the step angle number. Note that the maximum value of the step angle number is 63 and the minimum number is 0. Therefore, any increase or reduction in the microstep number is performed using modulo 64 arithmetic. This means that increasing a step angle number of 63 by 1 will produce a step angle number of 0, increasing by two from 63 will produce 1, and so on. Similarly, in the reverse direction, reducing a step angle number of 0 by 1 will produce a step angle number of 63, decreasing by two from 0 will produce 62, and so on.

The step angle is changed by writing a value to the SC[5:0] variable in the control register. This number is a two's-complement number that is added to the step angle number causing it to increase or decrease. Two's complement is the natural integer number system for most microcontrollers. This allows standard arithmetic operators to be used, within the microcontroller, to determine the size of the next step increment. Table 6 shows the binary equivalent of each decimal number between –16 and +16.

Each increase in the step angle number represents a forward movement of one eighth microstep. Each decrease in the step angle number represents a reverse movement of one eighth microstep.

To move the motor one full step, the step angle number must be increased or decreased by 16. To move the motor one half step, the step angle number must be increased or decreased by 8. For quarter step, the increment or decrement is 4, and for eighth step, the increment or decrement is 2.

So, for example, to continuously move the motor forwards in quarter-step increments, the number 4 (000100) is repeatedly written to SC[5..0] through the serial interface Run register (see Figure 17). To move the motor backwards in quarter step increments, the number –4 (111100) is repeatedly written to SC[5..0] (see Figure 18). Figures 19 and 20 show half-step forward and eighth-step backward sequences respectively. The remaining bits in the Run register should be set for the required configuration and sent with the step change number each time.

Table 6: Two's Complements

Decimals	2's Comp.	Decimals	2's Comp.
0	00 0000		
1	00 0001	-1	11 1111
2	00 0010	-2	11 1110
3	00 0011	-3	11 1101
4	00 0100	-4	11 1100
5	00 0101	-5	11 1011
6	00 0110	-6	11 1010
7	00 0111	-7	11 1001
8	00 1000	-8	11 1000
9	00 1001	-9	11 0111
10	00 1010	-10	11 0110
11	00 1011	-11	11 0101
12	00 1100	-12	11 0100
13	00 1101	-13	11 0011
14	00 1110	-14	11 0010
15	00 1111	-15	11 0001
16	01 0000	-16	11 0000

The step rate is controlled by the timing of the serial interface. It is the inverse of the step time (t_{STEP}) shown in Figure 17. The motor step only takes place when the STRn goes from low to high when writing to the Run register. The motor step rate is therefore determined by the timing of the rising edge of the STRn input. The clock rate of the serial interface, defined by the frequency of the SCK input, has no effect on the step rate.

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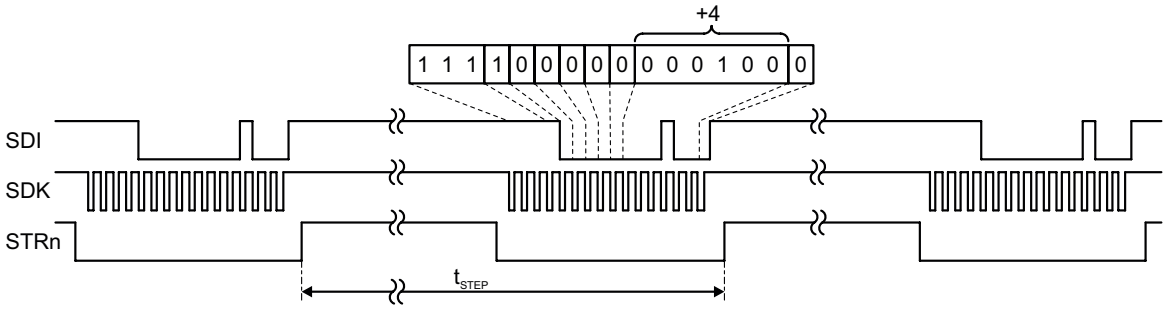

Figure 17: Serial Interface Sequence for Quarter Step in Forward Direction

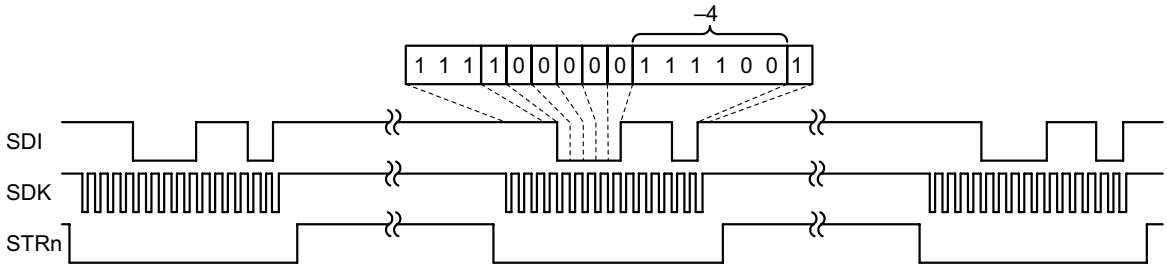

Figure 18: Serial Interface Sequence for Quarter Step in Reverse Direction

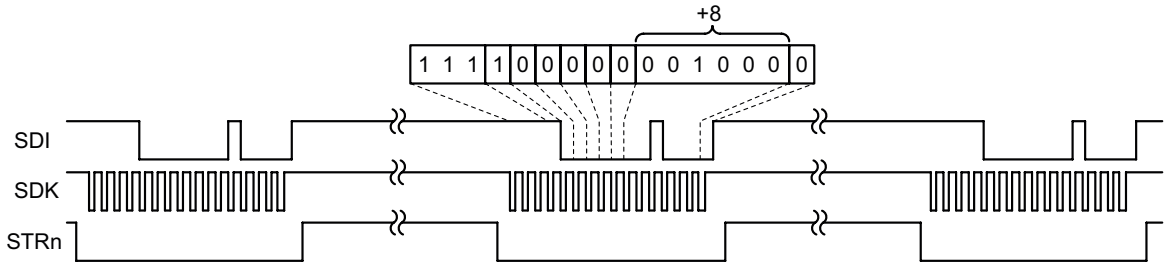

Figure 19: Serial Interface Sequence for Half Step in Forward Direction

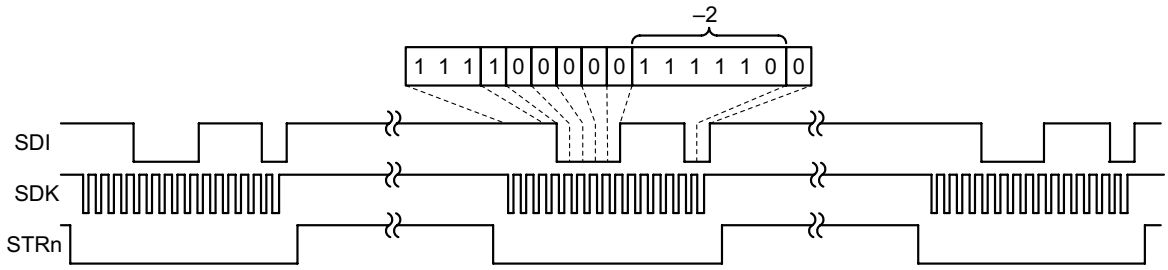

Figure 20: Serial Interface Sequence for Eighth Step in Reverse Direction

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Layout

The printed circuit board (PCB) should use a higher weight copper thickness than a standard small signal or digital board. This helps to reduce the impedance of the copper traces when conducting high currents. PCB traces carrying switching currents should be as wide and short as possible to reduce the inductance of the trace. This will help reduce any voltage transients caused by current switching during PWM current control.

For optimum thermal performance, the exposed thermal pad on the underside of the A4993 should be soldered directly onto the board. A solid ground plane should be added to the opposite side of the board and multiple vias through the board placed in the area under the thermal pad.

DECOUPLING

The ceramic capacitor should have a value of 100 nF and be placed as close as possible to the VBB and ground pins of the A4993. The electrolytic capacitor should be rated to at least 1.5 times the maximum system operating voltage and selected to support the maximum motor ripple current over the applicable temperature range. In many instances, capacitance value will be of secondary importance and device selection will be principally dictated by ripple current rating and ESR.

The pump capacitor between CP1 and CP2 and the charge storage capacitor between VCP and VBB should be connected as close to the terminals of the A4993 as possible.

GROUNDING

The GND pin and the two PGND pins must be connected together. A star ground arrangement with the common point located close to the A4993 is recommended. Typically, the ground plane located under the exposed thermal pad is used as the star ground.

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INPUT/OUTPUT STRUCTURES

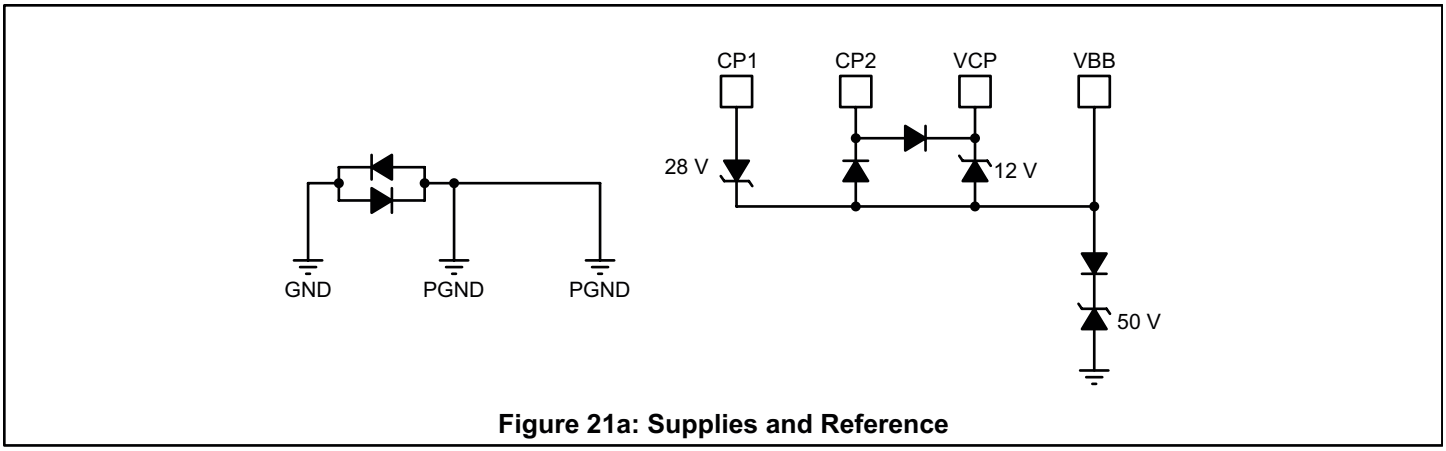

Figure 21a: Supplies and Reference

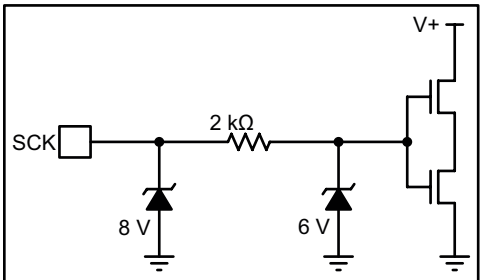

Figure 21b: SCK Input

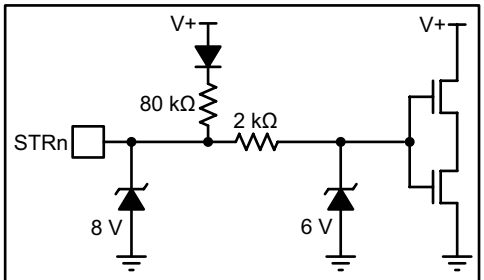

Figure 21c: STRn Input

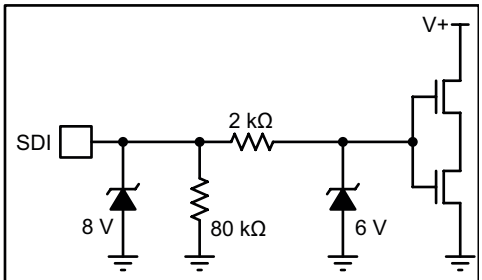

Figure 21d: SDI Input

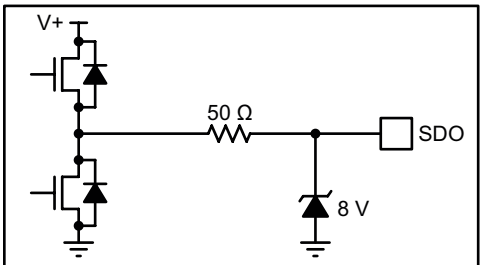

Figure 21e: SDO Output

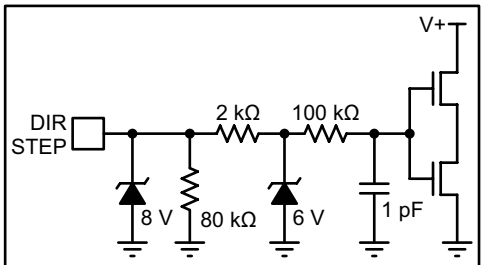

Figure 21f: DIR, STEP Inputs

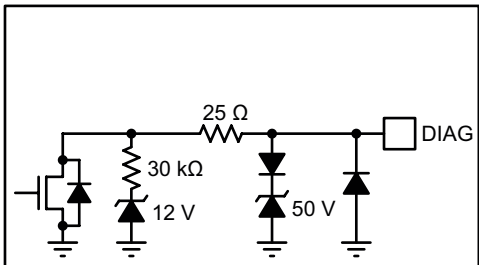

Figure 21g: DIAG Output

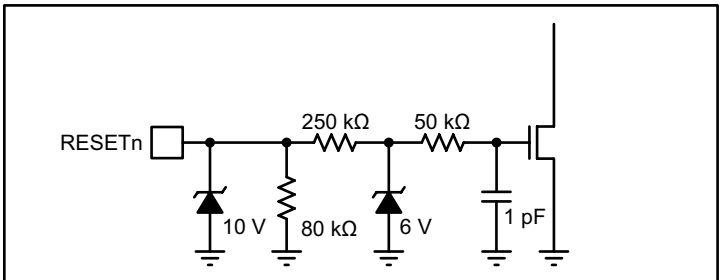

Figure 21h: RESETn Input

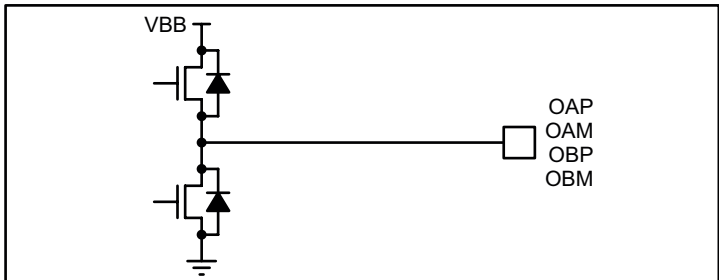

Figure 21i: PHASE Outputs

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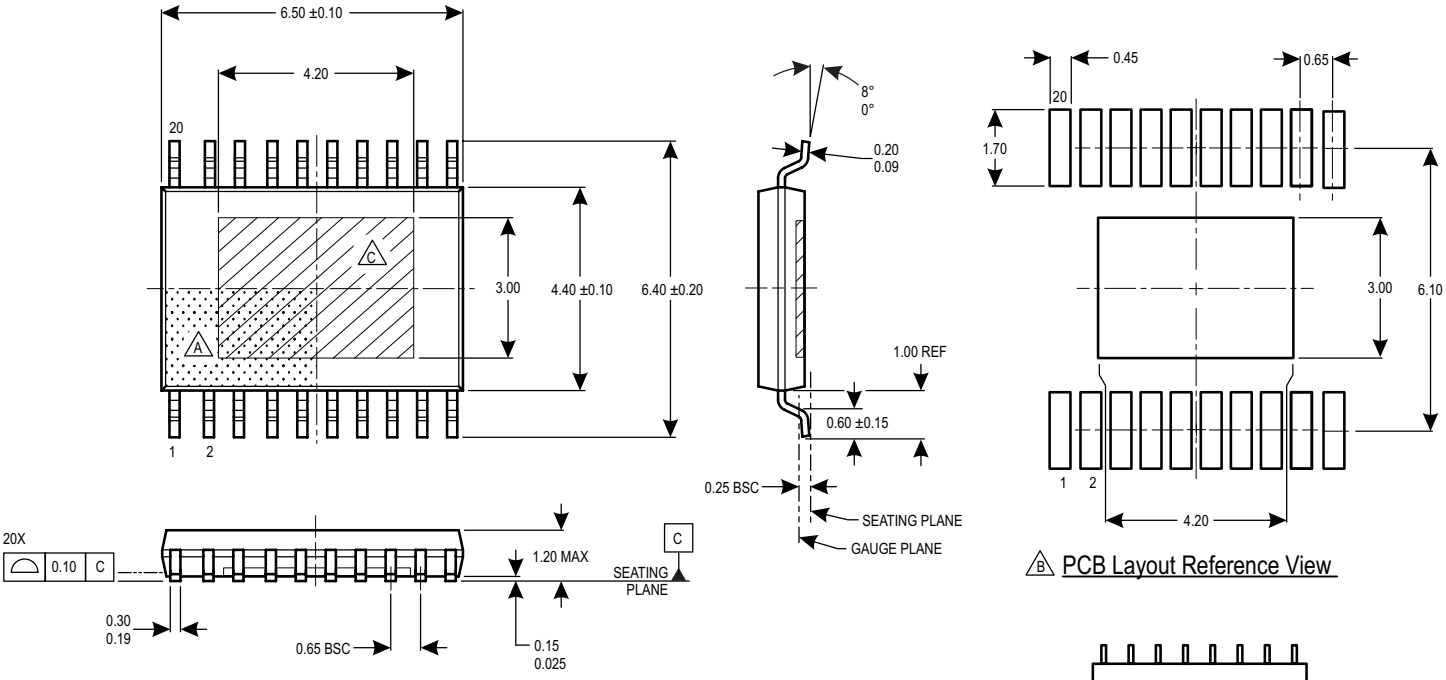
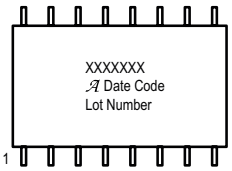
PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference JEDEC MO-153ACT; Allegro DWG-0000379, Rev. 3)
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown





A Terminal #1 mark area

B Reference land pattern layout (reference IPC7351 SOP65P640X110-21M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

C Exposed thermal pad (bottom surface)

D Branding scale and appearance at supplier discretion

D Standard Branding Reference View

Line 1, 2, 3 = 8 characters

Line 1: Part Number
Line 2: Logo A, 4 digit Date Code
Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

Figure 22: Package LP, 20-Pin TSSOP with Exposed Thermal Pad

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Revision History

Number	Date	Description
–	October 27, 2016	Initial Release
1	April 25, 2019	Minor editorial updates
2	April 21, 2022	Updated package drawing (page 41)

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