File Number **15.94**

MJH13090, MJH13091

T-33-13

High-Speed Silicon N-P-N Power Transistors

Features:

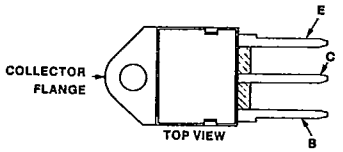
100° C Performance Specified for:

- *Reverse-Biased SOA with inductive loads*
- *Switching times with inductive loads*
- *Saturation voltages*
- *Leakage currents*

The MJH13090 and MJH13091 silicon n-p-n power transistors are designed for high-voltage, high-speed switching applications in inductive circuits where fall time is critical. They are particularly suited for off-line power supplies, converter circuits, and pulse-width-modulated regulators. These transistors are tested for parameters that are essential to the design of high-power switching circuits. Resistive and inductive switching times, leakage current, and saturation voltages are specified at 25° C and 100° C to provide information necessary for worst-case design.

These devices are supplied in the JEDEC TO-218AC plastic package.

TERMINAL DESIGNATION



92CS-40257

JEDEC TO-218AC

MAXIMUM RATINGS (T_A = 25°C) (unless otherwise specified)

RATING	SYMBOL	MJH13090	MJH13091	UNITS
Collector-Emitter Voltage	V_{CEO}	400	450	Volts
Collector-Emitter Voltage	V_{CEV}	650	750	Volts
Emitter Base Voltage	V_{EBO}	6	6	Volts
Collector Current — Continuous Peak (Repetitive)(1)	I_C I_{CM}	15 20	15 20	A
Base Current — Continuous Peak (Non-Repetitive)(1)	I_B I_{BM}	5 10	5 10	A
Total Power Dissipation @ Tc = 25°C @ Tc = 100°C Derate above 25°C	P_D	125 50 1	125 50 1	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	°C

THERMAL CHARACTERISTICS

Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	1.0	°C/W
Maximum Lead Temperature for Soldering Purpose: ⅛" from Case for 5 Seconds	T_L	275	275	°C

(1) Pulse Test: Pulse Width = 5ms. Duty Cycle ≤ 10%.

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ELECTRICAL CHARACTERISTICS (T_C = 25°C) (unless otherwise specified)

CHARACTERISTIC		SYMBOL	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS(1)						
Collector-Emitter Sustaining Voltage (I_C = 100mA, I_B = 0)	MJH13090 MJH13091	$V_{CEO(sus)}$	400 450	— —	— —	Volts
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(OFF)}$ = -1.5V) (V_{CEV} = Rated Value, $V_{BE(OFF)}$) = -1.5V, T_C = 100°C)		I_{CEV}	— —	— —	0.5 2.5	mA
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50Ω, T_C = 100°C)		I_{CER}	—	—	3	mA
Emitter Cutoff Current (V_{EB} = 6V, I_C = 0)		I_{EBO}	—	—	1	mA
SECOND BREAKDOWN						
Second Breakdown with Base Forward Biased		FBSOA	SEE FIGURE 12			
Clamped Inductive SOA with Base Reversed Bias		RBSOA	SEE FIGURE 13			
ON CHARACTERISTICS(1)						
DC Current Gain (I_C = 10A, V_{CE} = 3V)		h_{FE}	8	—	—	—
Collector-Emitter Saturation Voltage (I_C = 10A, I_B = 2A) (I_C = 15A, I_B = 3A) (I_C = 10A, I_B = 2A, T_C = 100°C)		$V_{CE(sat)}$	— — —	— — —	1 3 2	V
Base-Emitter Saturation Voltage (I_C = 10A, I_B = 2A) (I_C = 10A, I_B = 2A, T_C = 100°C)		$V_{BE(sat)}$	— —	— —	1.5 1.5	V
SWITCHING CHARACTERISTICS						
Resistive Load						
Delay Time	V_{CC} = 250V, I_C = 10A	t_d	—	0.03	0.05	μs
Rise Time	I_{B1} = -I_{B2} = 1.25A,	t_r	—	0.13	0.5	
Storage Time	t_p = 30 μsec	t_s	—	0.55	2.5	
Fall Time		t_f	—	0.1	0.5	
Inductive Load, Clamped						
Storage Time	$I_{CC(PK)}$ = 10A	t_{sv}	—	0.8	3	μs
Crossover Time	I_{B1} = 1.25A (at T_J = 100°C)	t_c	—	0.175	0.4	
Fall Time	$V_{BE(OFF)}$ = -5V	t_{fi}	—	0.15	0.3	
Storage Time	$V_{CE(PK)}$ = 250V	t_{sv}	—	0.5	—	
Crossover Time	(at T_J = 25°C)	t_c	—	0.15	—	
Fall Time		t_{fi}	—	0.1	—	

(1) Pulse Test: Pulse Width - 300μs Duty Cycle ≤ 2.%

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TYPICAL ELECTRICAL CHARACTERISTICS

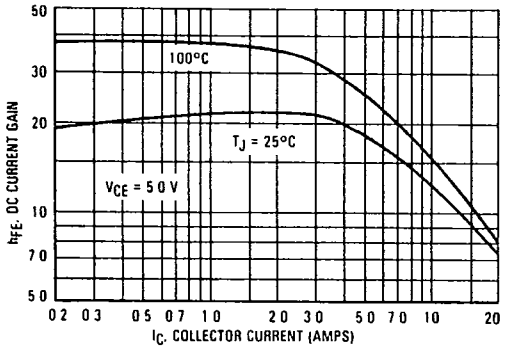

FIGURE 1 — DC CURRENT GAIN

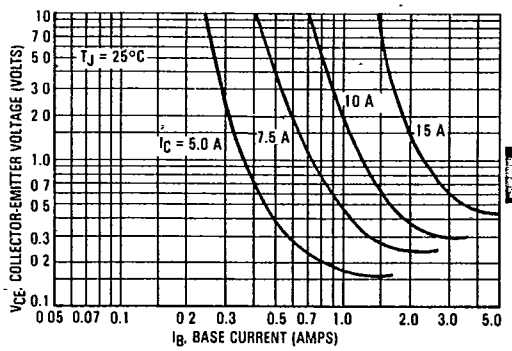

FIGURE 2 — COLLECTOR SATURATION REGION

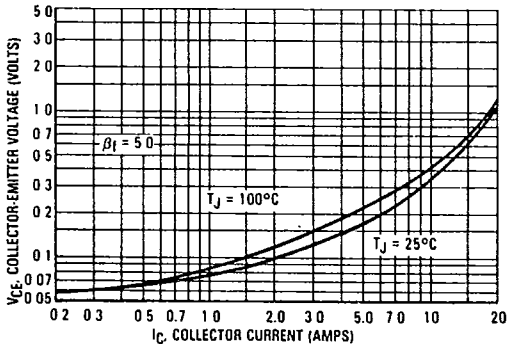

FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

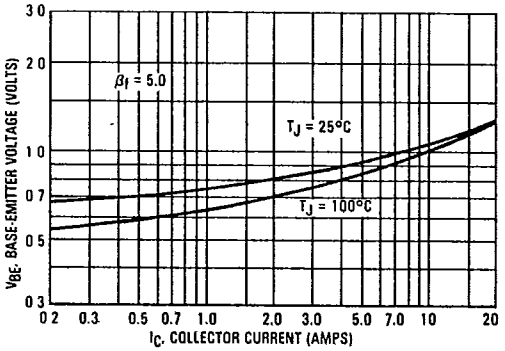

FIGURE 4 — BASE-EMITTER VOLTAGE

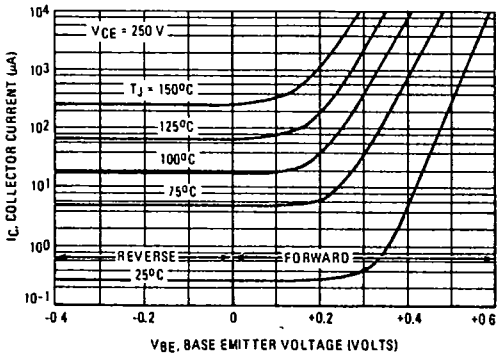

FIGURE 5 — COLLECTOR CUTOFF REGION

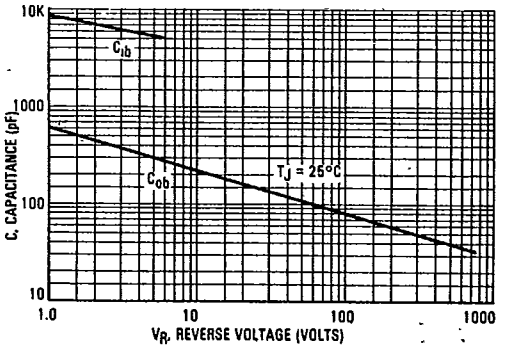

FIGURE 6 — CAPACITANCE

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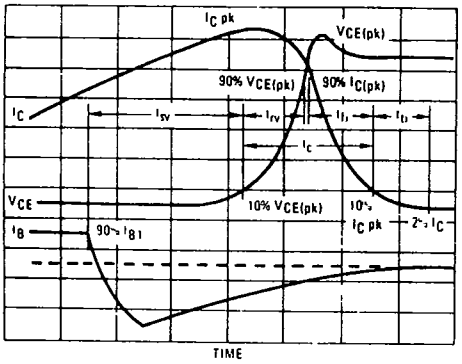

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

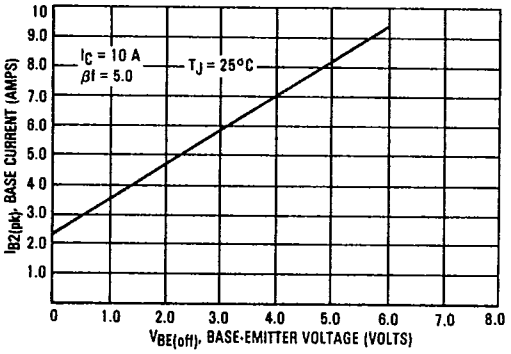

FIGURE 8 — PEAK REVERSE CURRENT

INDUCTIVE SWITCHING

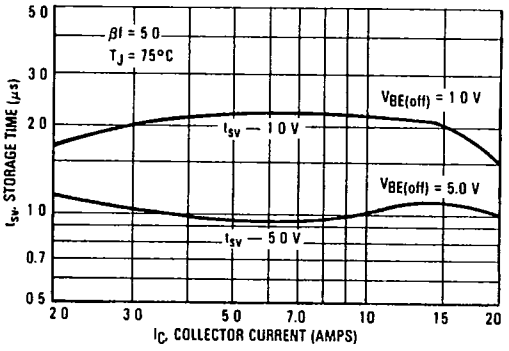

FIGURE 9 — STORAGE TIME

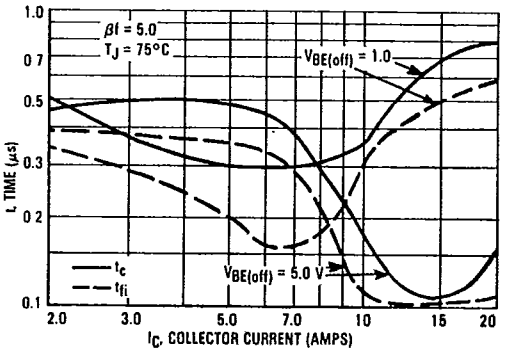

FIGURE 10 — CROSSOVER AND FALL TIMES

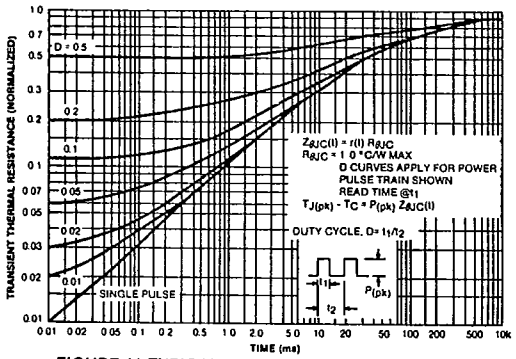

FIGURE 11 TYPICAL THERMAL RESPONSE [($Z_{\theta JC}(t)$)]

The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

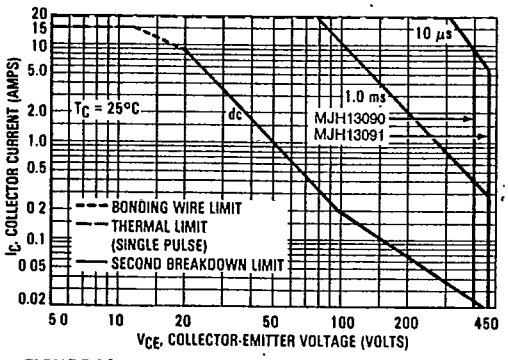

FIGURE 12 — FORWARD BIAS SAFE OPERATING AREA

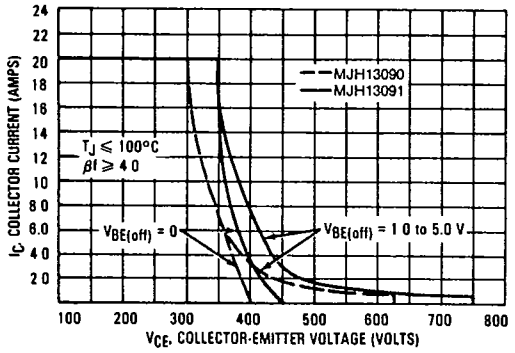

FIGURE 13 — REVERSE BIAS SAFE OPERATING AREA

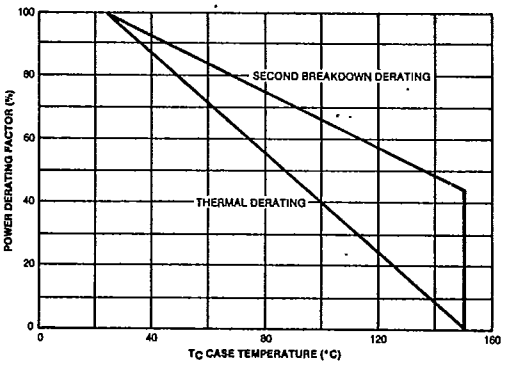

FIGURE 14 — POWER DERATING