

1. General description

Planar passivated high commutation three quadrant triac in a SOT186A (TO-220F) "full pack" plastic package intended for use in circuits where high static and dynamic dV/dt and high dI/dt can occur. This "series B0" triac will commute the full rated RMS current at the maximum rated junction temperature without the aid of a snubber.

2. Features and benefits

- 3Q technology for improved noise immunity
- High immunity to false turn-on by dV/dt
- High minimum I_{GT} for guaranteed immunity to gate noise
- High voltage capability
- Isolated mounting base package
- Least sensitive gate for highest noise immunity
- Planar passivated for voltage ruggedness and reliability
- Triggering in three quadrants only
- Very high commutation capability with maximum false trigger immunity

3. Applications

- Electronic thermostats
- High power motor controls - e.g. washing machines and vacuum cleaners
- Rectifier-fed DC inductive loads e.g. DC motors and solenoids
- Refrigeration and air conditioning compressors

4. Quick reference data

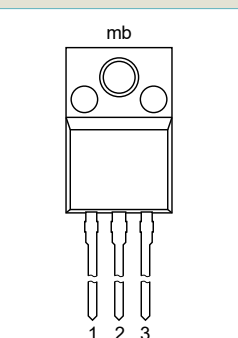
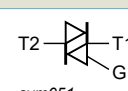
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	-	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_h \leq 45\text{ °C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	-	16	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(\text{init})} = 25\text{ °C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5	-	-	140	A
		full sine wave; $T_{j(\text{init})} = 25\text{ °C}$; $t_p = 16.7\text{ ms}$	-	-	150	A
T_j	junction temperature		-	-	125	°C
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ °C}$; Fig. 7	10	-	50	mA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T2+ \text{ G-}; T_j = 25\text{ }^\circ\text{C}; \text{Fig. 7}$	10	-	50	mA
		$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T2- \text{ G-}; T_j = 25\text{ }^\circ\text{C}; \text{Fig. 7}$	10	-	50	mA
I_H	holding current	$V_D = 12\text{ V}; T_j = 25\text{ }^\circ\text{C}; \text{Fig. 9}$	-	-	60	mA
V_T	on-state voltage	$I_T = 18\text{ A}; T_j = 25\text{ }^\circ\text{C}; \text{Fig. 10}$	-	1.3	1.5	V
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 536\text{ V}; T_j = 125\text{ }^\circ\text{C}; (V_{DM} = 67\% \text{ of } V_{DRM}); \text{exponential waveform; gate open circuit}$	2500	-	-	V/ μ s
dI_{com}/dt	rate of change of commutating current	$V_D = 400\text{ V}; T_j = 125\text{ }^\circ\text{C}; I_{T(RMS)} = 16\text{ A}; dV_{com}/dt = 20\text{ V}/\mu\text{s}; (\text{snubberless condition}); \text{gate open circuit}$	20	-	-	A/ms

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1	 <p>TO-220F (SOT186A)</p>	 <p>sym051</p>
2	T2	main terminal 2		
3	G	gate		
mb	n.c.	mounting base; isolated		

6. Ordering information

Table 3. Ordering information

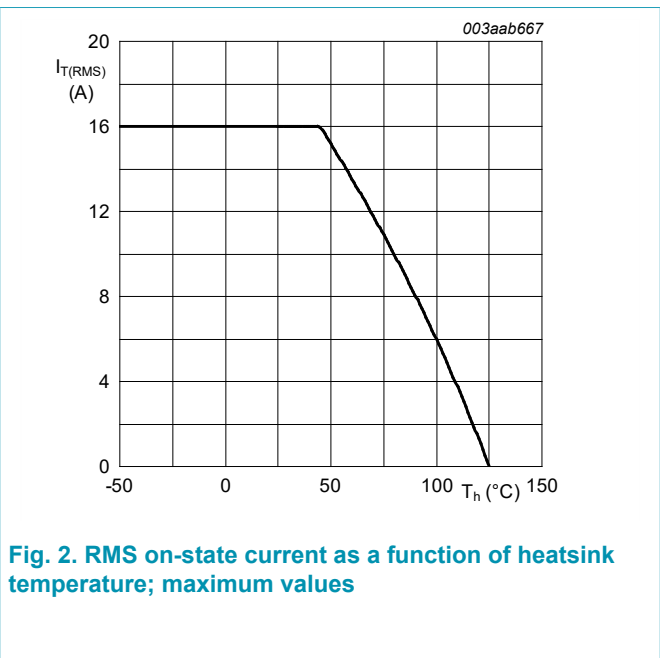
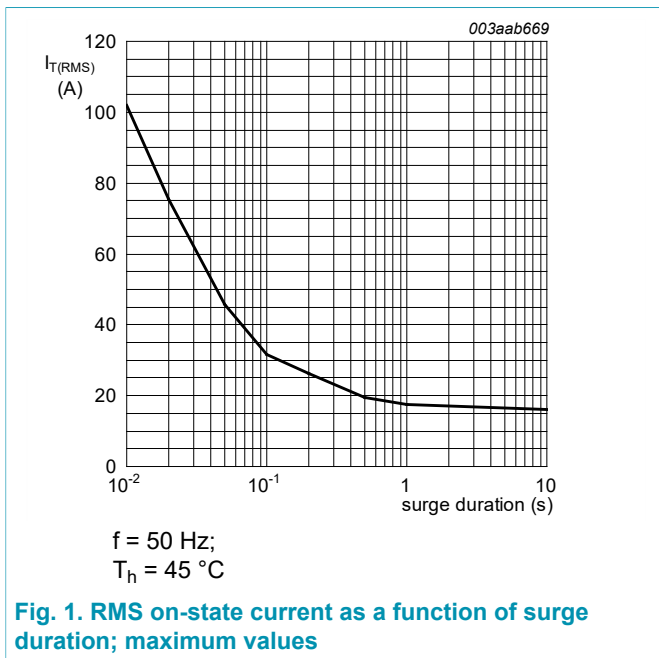
Type number	Package		
	Name	Description	Version
BTA316X-800B0	TO-220F	plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack"	SOT186A

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_h \leq 45\text{ }^\circ\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	16	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5	-	140	A
		full sine wave; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$; $t_p = 16.7\text{ ms}$	-	150	A
I^2t	I^2t for fusing	$t_p = 10\text{ ms}$; SIN	-	98	A^2s
di_T/dt	rate of rise of on-state current	$I_G = 0.2\text{ A}$	-	100	$\text{A}/\mu\text{s}$
I_{GM}	peak gate current		-	2	A
P_{GM}	peak gate power		-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.5	W
T_{stg}	storage temperature		-40	150	$^\circ\text{C}$
T_j	junction temperature		-	125	$^\circ\text{C}$



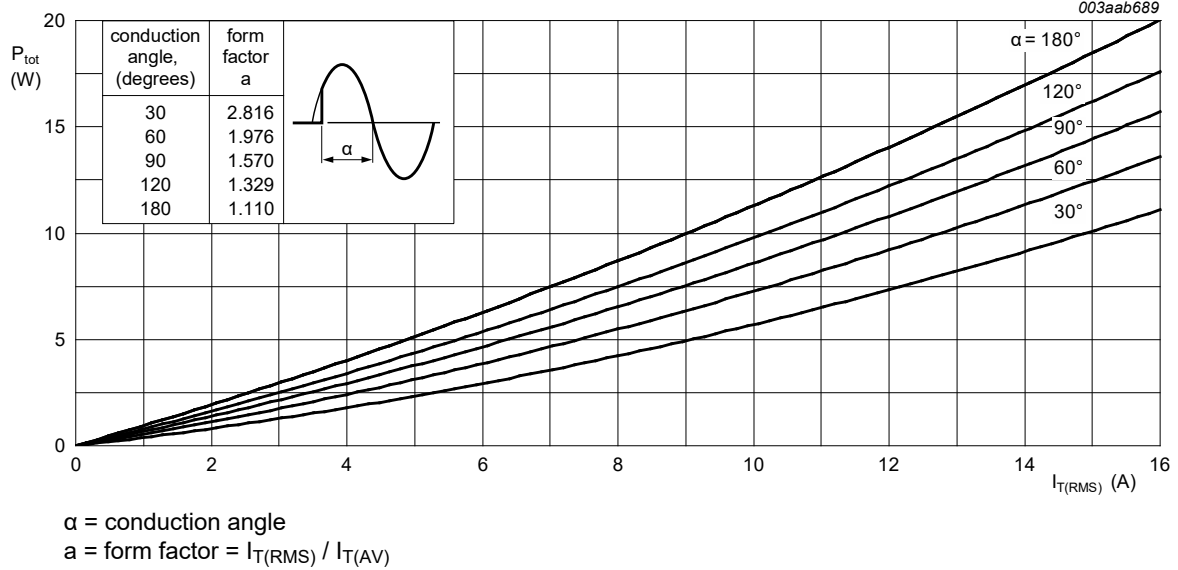


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

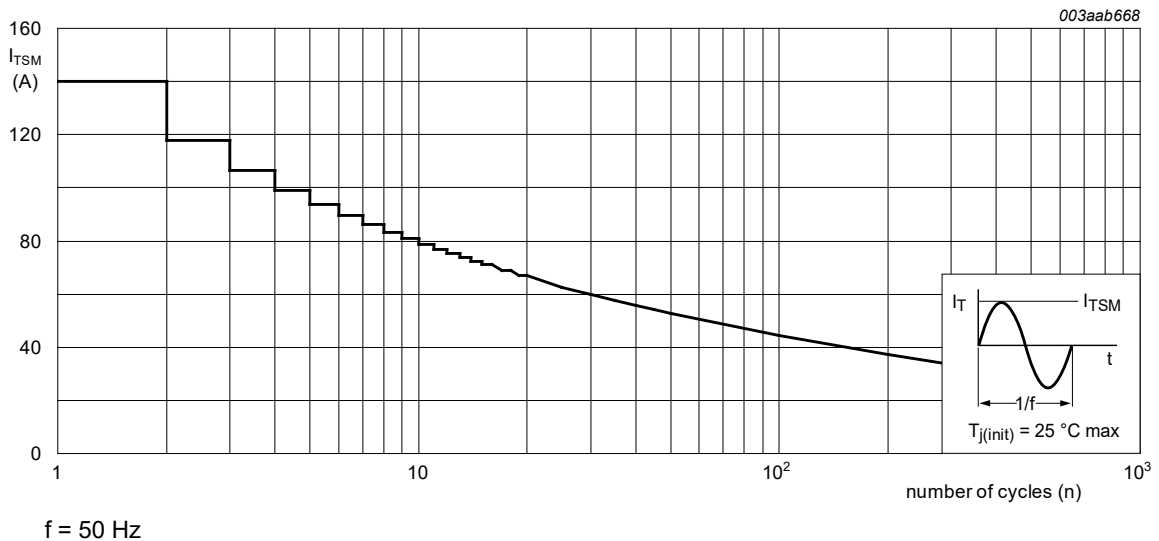


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

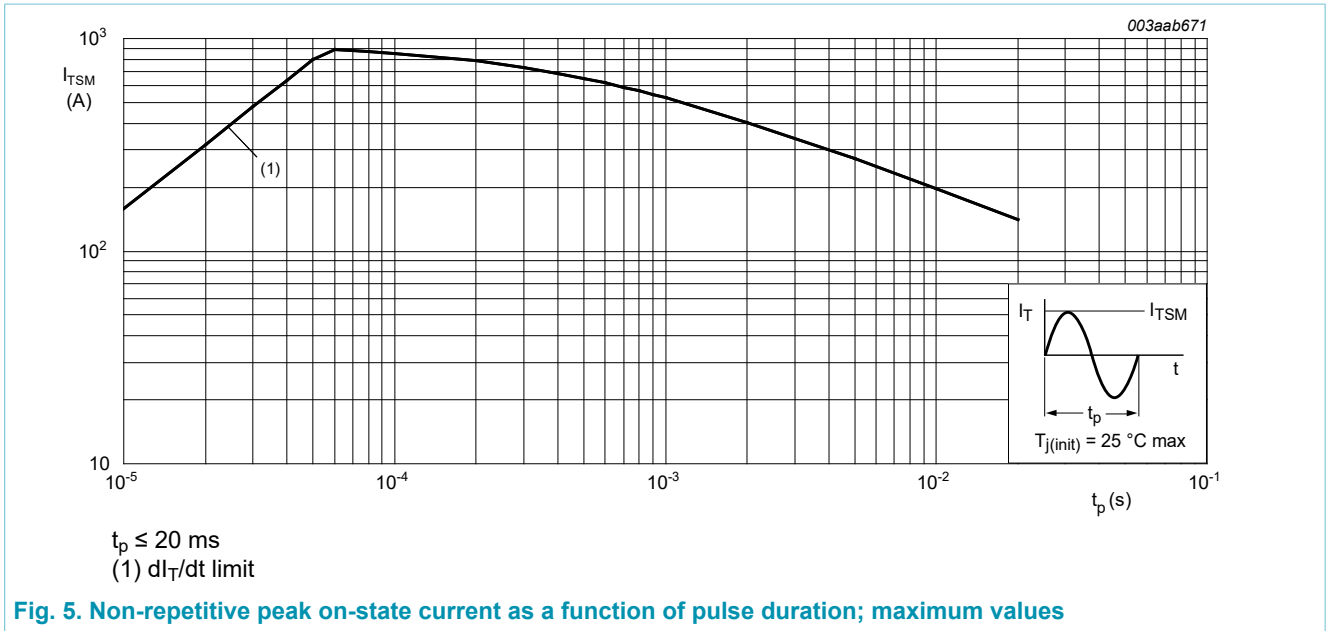
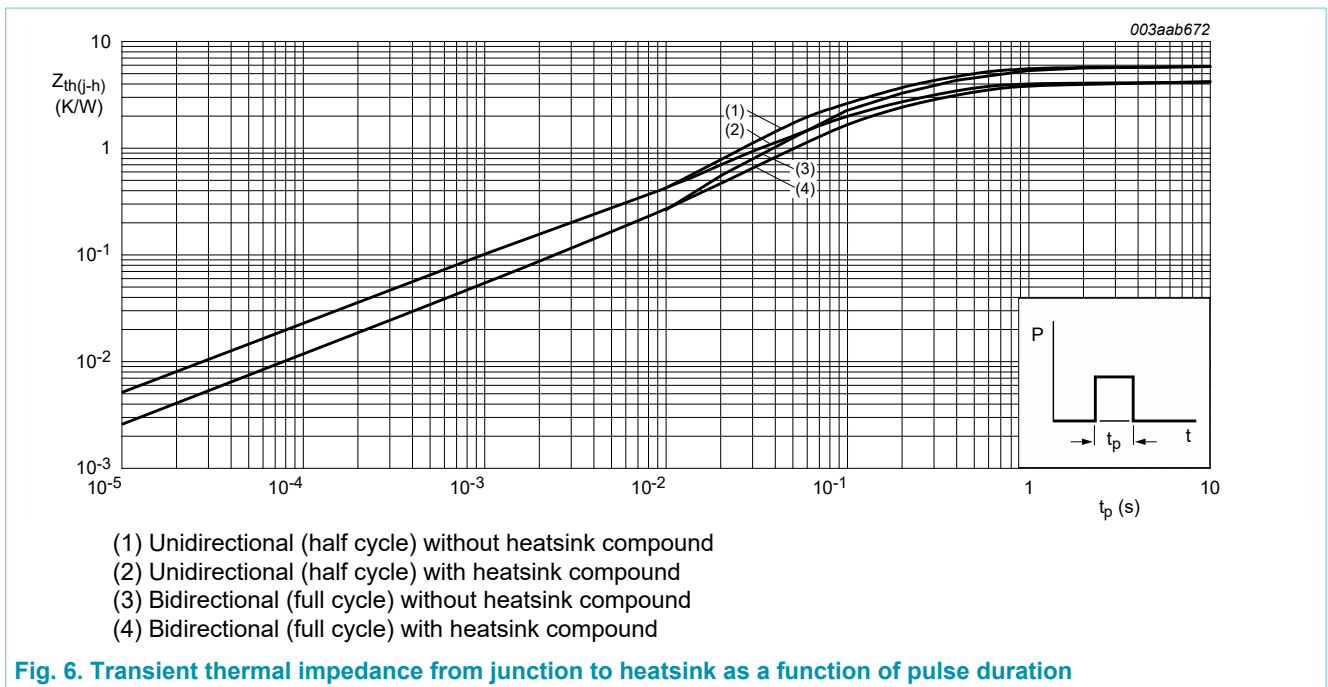


Fig. 5. Non-repetitive peak on-state current as a function of pulse duration; maximum values

8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-h)}$	thermal resistance from junction to heatsink	full cycle or half cycle; with heatsink compound; Fig. 6	-	-	4	K/W
		full cycle or half cycle; without heatsink compound; Fig. 6	-	-	5.5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	in free air	-	55	-	K/W



9. Isolation characteristics

Table 6. Isolation characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{isol(RMS)}$	RMS isolation voltage	from all three terminals to external heatsink; sinusoidal waveform; clean and dust free; $50\text{ Hz} \leq f \leq 60\text{ Hz}$; $RH \leq 65\%$; $T_h = 25\text{ }^\circ\text{C}$	-	-	2500	V
C_{isol}	isolation capacitance	from main terminal 2 to external heatsink; $f = 1\text{ MHz}$; $T_h = 25\text{ }^\circ\text{C}$	-	10	-	pF

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ °C}$; Fig. 7	10	-	50	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ °C}$; Fig. 7	10	-	50	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ °C}$; Fig. 7	10	-	50	mA
I_L	latching current	$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ °C}$; Fig. 8	-	-	60	mA
		$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ °C}$; Fig. 8	-	-	90	mA
		$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ °C}$; Fig. 8	-	-	60	mA
I_H	holding current	$V_D = 12\text{ V}$; $T_j = 25\text{ °C}$; Fig. 9	-	-	60	mA
V_T	on-state voltage	$I_T = 18\text{ A}$; $T_j = 25\text{ °C}$; Fig. 10	-	1.3	1.5	V
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 25\text{ °C}$; Fig. 11	-	0.8	1.5	V
		$V_D = 400\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 125\text{ °C}$; Fig. 11	0.25	0.4	-	V
I_D	off-state current	$V_D = 800\text{ V}$; $T_j = 125\text{ °C}$	-	0.1	0.5	mA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 536\text{ V}$; $T_j = 125\text{ °C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit	2500	-	-	V/ μ s
dI_{com}/dt	rate of change of commutating current	$V_D = 400\text{ V}$; $T_j = 125\text{ °C}$; $I_{T(RMS)} = 16\text{ A}$; $dV_{com}/dt = 20\text{ V}/\mu\text{s}$; (snubberless condition); gate open circuit	20	-	-	A/ms

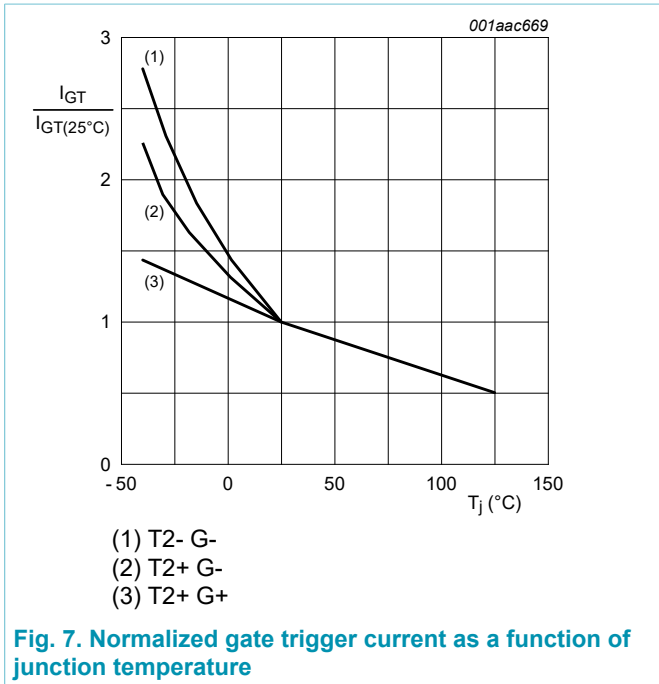


Fig. 7. Normalized gate trigger current as a function of junction temperature

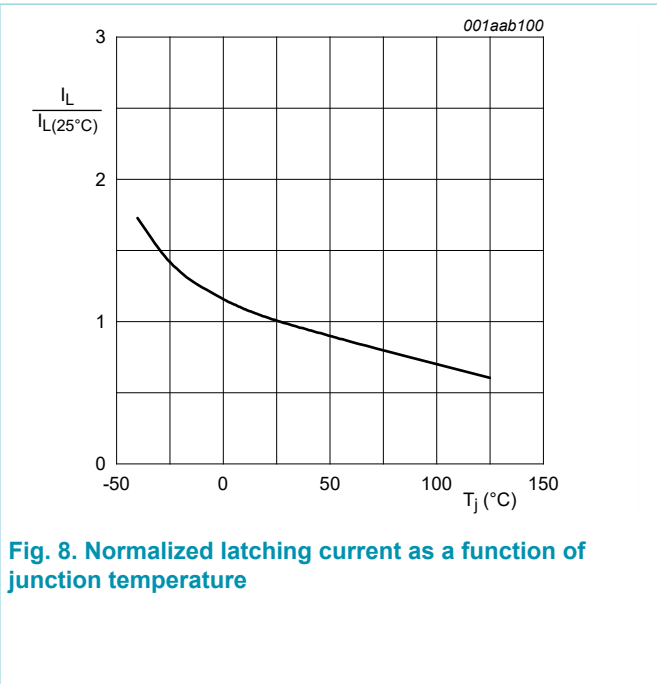


Fig. 8. Normalized latching current as a function of junction temperature

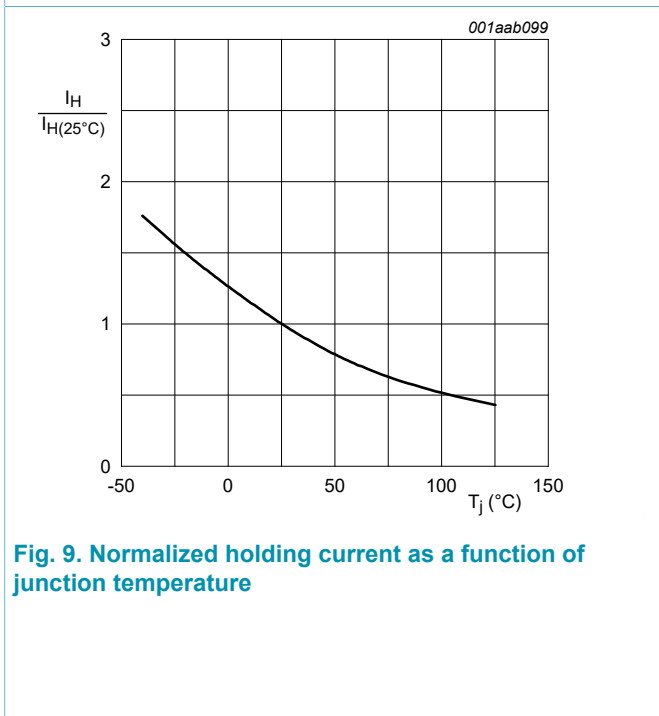


Fig. 9. Normalized holding current as a function of junction temperature

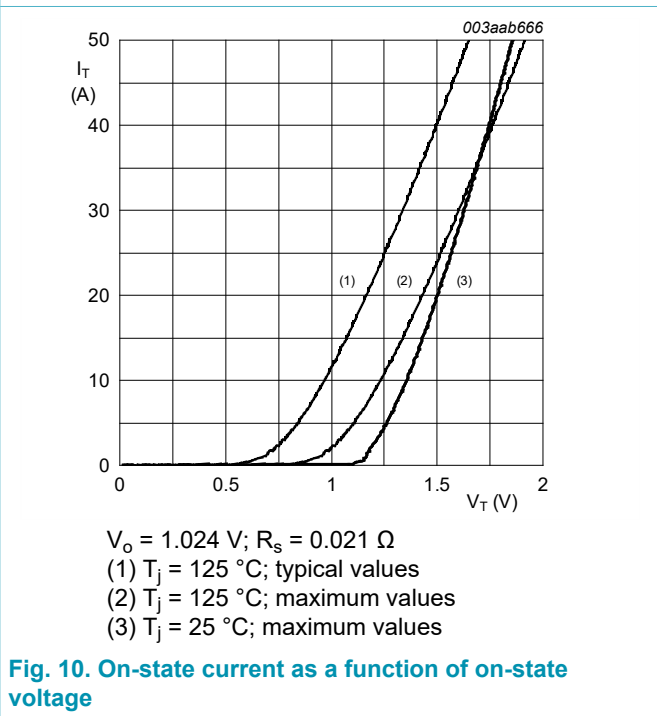


Fig. 10. On-state current as a function of on-state voltage

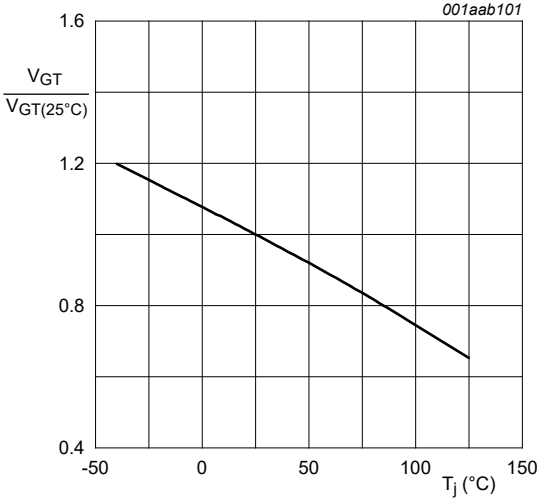


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

11. Package outline

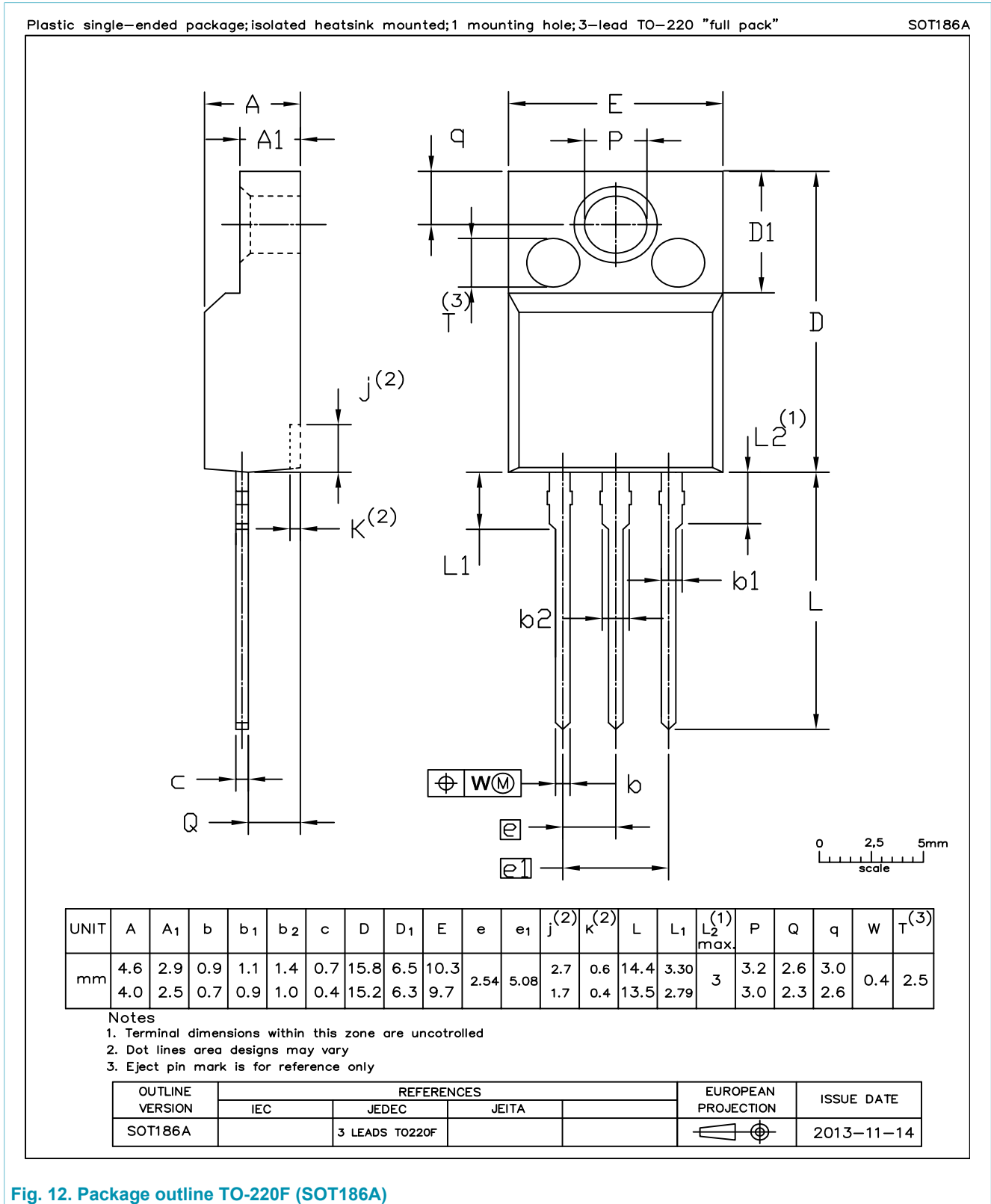


Fig. 12. Package outline TO-220F (SOT186A)

12. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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