National Semiconductor

CGS2534V Commercial/CGS2534TV Industrial Quad 1 to 4 Clock Drivers

General Description

These Clock Generation and Support clock drivers are specifically designed for driving memory arrays requiring large fanouts while operating at high speeds,

CGS2534 is a 4 to 16 inverting driver with TTL compatible I/Os. This device has skew specifications of 350 ps pin-to-pin as well as a 650 ps specification for part-to-part propagation delay variation.

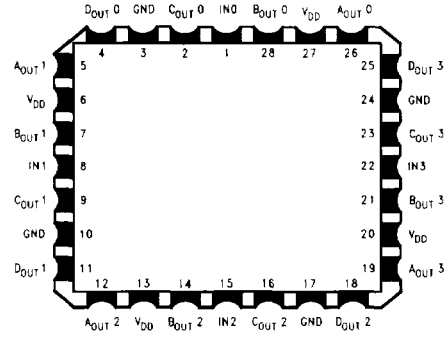
Features

- Guaranteed and tested:
  350 ps pin-to-pin skew (t_{OSHL} and t_{OSLH})
- 650 ps part-to-part variation on positive or negative transition
- Implemented on National's ABT family process
- Symmetric output current drive: −36/36 mA $I_{OH/IOL}$
- Industrial temperature of −40°C to +85°C
- 28-pin PLCC for optimum skew performance
- Symmetric package orientation
- Large fanout for memory driving applications
- Guaranteed 2 kV ESD protection

Ordering Code: See Section 10

Connection Diagrams

Pin Assignment for 28-Pin PLCC

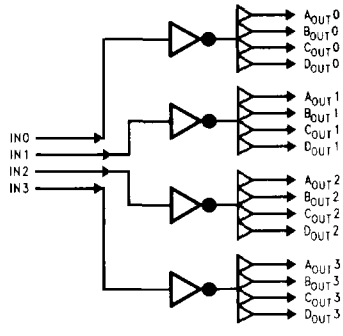


TL/F/11921-5

Truth Table

Input	Output
In(0–3)	$\overline{ABCD}$ Out (0–3)

CGS2534



TL/F/11921-1

8

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	7.0V
Input Voltage (V_I)	7.0V
Input Current	−30 mA
Current Applied to Output (High/Low)	twice the rated I_{OH}/I_{OL} mA
Operating Temperature	
Industrial Grade	−40°C to +85°C
Commercial Grade	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Airflow	Typical θ_{JA}
0 LFM	62°C/W
225 LFM	43°C/W
500 LFM	34°C/W
900 LFM	27°C/W

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.5V to 5.5V
Maximum Input Rise/Fall Time (0.8V to 2.0V)	5 ns
Free Air Operating Temperature (T_A)	
Industrial	−40°C to +85°C
Commercial	0°C to +70°C

Note: *The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the DC and AC Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The Recommended Operating Conditions will define the conditions for actual device operation.*

DC Electrical Characteristics

Over recommended operating conditions unless otherwise specified. All typical values are measured at V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input Low Level Voltage				0.8	V
V_{IH}	Input High Level Voltage		2.0			V
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA			−1.2	V
V_{OH}	High Level Output Voltage (Note 5)	I_{OH} = −3 mA, V_{CC} = 4.5V	2.4			V
		I_{OH} = −36 mA, V_{CC} = 4.5V	2.0			
V_{OL}	Low Level Output Voltage (Note 5)	V_{CC} = 4.5V, I_{OL} = 36 mA		0.4	0.5	V
		V_{CC} = 4.5V, I_{OL} = 50 μA		0.1	0.1	
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V			7	μA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V			5	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V	−5			μA
I_{OS}	Output Drive Current	V_{CC} = 5.5V, V_O = 0V	−100		275	mA
I_{OLD}	Minimum Dynamic Output Current (Note 1)	V_{CC} = 5.5V, V_{OLD} = 0.8V	70			mA
I_{OHD}	Minimum Dynamic Output Current (Note 1)	V_{CC} = 5.5V, V_{OHD} = 2.0V	−90			mA
I_{CCT}	Maximum I_{CC}/Input	V_{CC} = 5.5V			3.6	mA
I_{CC}	Supply Current '2534 (Quiescent)	V_{CC} = 5.5V			235	μA
C_{IN}	Input Capacitance	V_{CC} = 5V		5		pF

Note 1: Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics

Over recommended operating conditions unless otherwise specified. All typical values are measured at V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	CGS2534						Unit
		T_A = +25°C, C_L = 50 pF, R_L = 500Ω			T_A = −40°C to +85°C, C_L = 50 pF, R_L = 500Ω			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Frequency Maximum					125		MHz
t_{PLH}	Low-to-High Propagation Delay IN_n to OUT_n			3.5			3.5	ns
t_{PHL}	High-to-Low Propagation Delay IN_n to OUT_n			3.5			3.5	ns
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation (Note 2)		150	350		300	350	ps
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation (Note 2)		150	350		300	350	ps
t_{RISE}, t_{FALL}	Rise/Fall Time (from 0.8V/2.0V to 2.0V/0.8V)			1.5			1.5	ns
t_{HIGH} t_{LOW}	Pulse Width Duration High Pulse Width Duration Low (Note 4)	4 4			4 4			ns
t_{PVLH}	Part-to-Part Variation of Low-to-High Transitions (Note 3)			650			650	ps
t_{PVHL}	Part-to-Part Variation of High-to-Low Transitions (Note 3)			650			650	ps

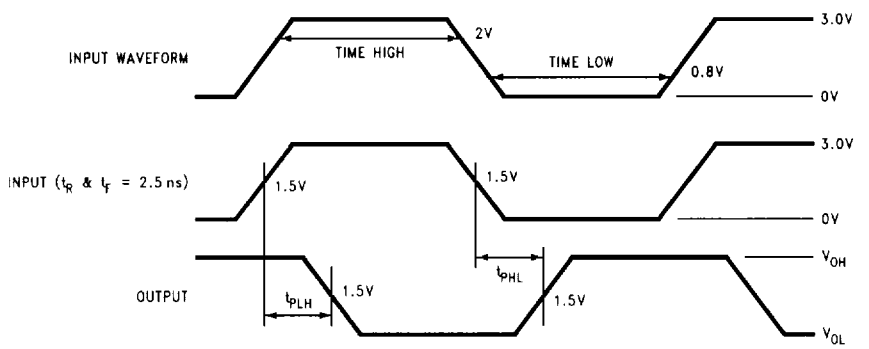
Note 2: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Limits are guaranteed by design.

Note 3: Part to Part transition variation is defined as the absolute difference between the propagation delay of any output on one device to any output on another device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{PVHL}) or LOW to HIGH (t_{PVLH}). Limits are guaranteed by design.

Note 4: Time high is measured at 2.0V, time low is measured at 0.8V.

Note 5: For increased drive, output pins may be connected together when the corresponding input pins are connected together.

Timing Information



TL/F/11921–2

Memory Array Driving

In order to minimize the total load on the address bus, quite often memory arrays are being driven by buffers while having the inputs of the buffers tied together. Although this practice was feasible in the conventional memory designs, in today's high speed, large buswidth designs which require address fetching at higher speeds, this technique produces many undesired results such as cross-talk and over/undershoot.

CGS2534/35/36/37 Quad 1 to 4 Clock Drivers were designed specifically to address these application issues on high speed, large memory arrays systems.

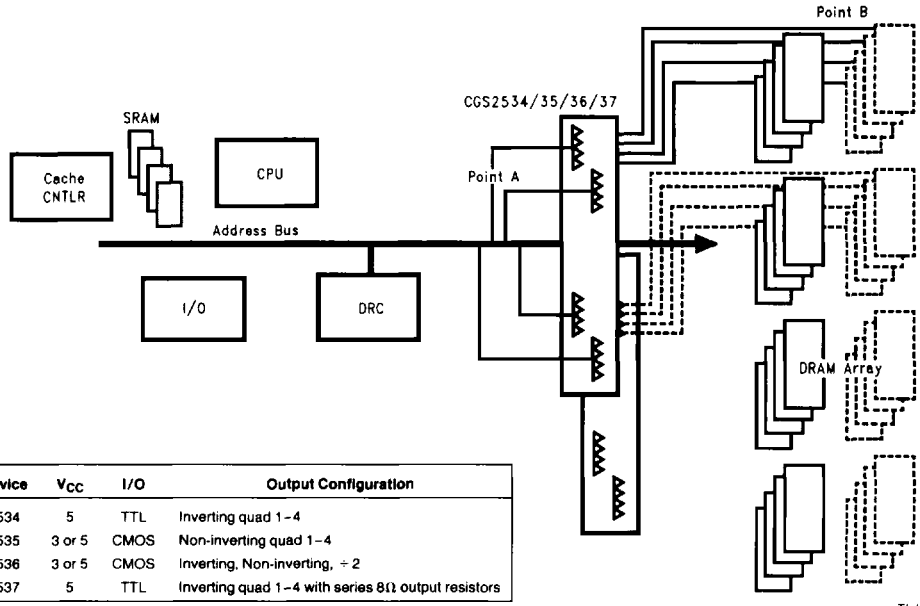
These drivers are optimized to driver large loads, with 3.5 ns propagation delays. These drivers produce less noise while reducing the total capacitive loading on the address bus by having only four inputs tied together (see the diagram below, point A). This helps to minimize the overshoot and undershoot by having only four outputs being switched simultaneously.

Also this larger fan-out helps to save board space since for every one of these drivers, two conventional buffers were typically being used.

Another feature associated with these clock drivers is a 350 ps pin-to-pin skew specification. The minimum skew specification allows high speed memory system designers to optimize the performance of their memory sub-system by operating at higher frequencies without having concerns about output-to-output (bank-to-bank) synchronization problem which are associated with driving high capacitive loads (Point B).

The diagram below depicts a "2534/35/36/37" a memory subsystem operating at high speed with large memory capacity. The address bus is common to both the memory and the CPU and I/Os.

These drivers can operate beyond 125 MHz, and are also available in 3V–5V TTL/CMOS versions with large current drive .



Device	V_{CC}	I/O	Output Configuration
2534	5	TTL	Inverting quad 1–4
2535	3 or 5	CMOS	Non-inverting quad 1–4
2536	3 or 5	CMOS	Inverting, Non-inverting, ÷2
2537	5	TTL	Inverting quad 1–4 with series 8Ω output resistors

TL/F/11921–7