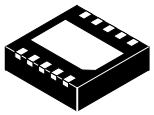
130 V, 2.0 A / 3.0 A High and Low Side Drivers with Dead Time & Interlock

NCP51513

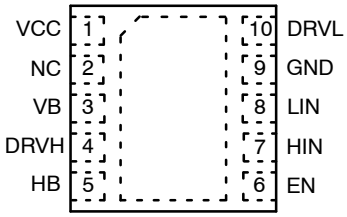


DFN10 (3x3)
CASE 506CL

MARKING DIAGRAM

x = A or B (Input Noise Filter)
y = Internal Dead Time 80 ns
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PIN CONNECTION



Top View

ORDERING INFORMATION

Device	Package	Shipping†
NCP51513ABMNTWG	DFN10 (Pb−free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Description

NCP51513 is 130 V half bridge driver with high drive current capabilities and options for DC−DC power supplies and inverters. NCP51513 offers best in class propagation delay, low quiescent current and low switching current at high frequencies of operation.

This device is tailored for highly efficient power supplies operating at high frequencies. NCP51513 is offered in two versions for propagation delays. With filter version, it has a typical 50 ns propagation delay, while without filter version it has a typical propagation delay of 20 ns. Internal 80 ns dead time and interlock function protect the output MOSFETs against cross conduction events. Enable functionality provides additional system flexibility and helps reducing power consumption.

Features

- High Voltage Range: Up to 130 V
- dV/dt Immunity Up to 50 V/ns
- Output Source / Sink Current Capability 2.0 A / 3.0 A
- Rise / Fall Time 9 ns / 7 ns for 1 nF Load
- Independent Logic Inputs 3.3 V and 5 V Compatible
- Enable Input
- Propagation Delay 50 ns A Version, 20 ns B Version
- Input Filter Time 30 ns for A Version and No Filter for B Version
- Internal Fixed 80 ns Dead Time
- Input Cross−Conduction Prevention
- Extended Allowable Negative Bridge Pin Voltage Swing to −10 V @ Vcc = 10 V
- Matched Propagation Delays Between Both Channels Max 11 ns
- Independent Under Voltage Lock Out (UVLO) for Both Channels
- This is a Pb−Free Device

Typical Applications

- Half and Full Bridge Converters
- DC−to−AC Inverters
- Motor Drivers
- Synchronous Buck

QUICK SELECTION TABLE

OPN	Package	Drive Current [A]		Dead Time [ns]	Filter [ns]	UVLO Levels Max [V]		t_r and t_f at 1 nF [ns]		Prop Delay [ns]		Delay Match [ns]
		Source	Sink			Vcc/Vb ON	Vcc/Vb OFF	Rise	Fall	ON	OFF	
NCP51513ABMNTWG	DFN10	2.0	3.0	80	30	7.1	6.6	9	7	50	50	11

OPTION TABLE

Suffix	Value	Description
x	A	Input filter time 30 ns
x	B	No input filter (on demand)
y	A	0 ns fixed dead time (on demand)
y	B	80 ns fixed dead time
y	C	200 ns fixed dead time (on demand)

Table 1. PIN DESCRIPTION

Pin Out	Name	Function
1	VCC	Power Ground
2	NC	Not Connected
3	VB	High Side Supply
4	DRVH	High Side Output
5	HB	High Side Supply Return, Half Bridge Pin
6	EN	Enable Input
7	HIN	High Side Input
8	LIN	Low Side Input
9	GND	Low Side and Logic Supply
10	DRVL	Low Side Output
EP	EP	Connect the EP Flag to GND

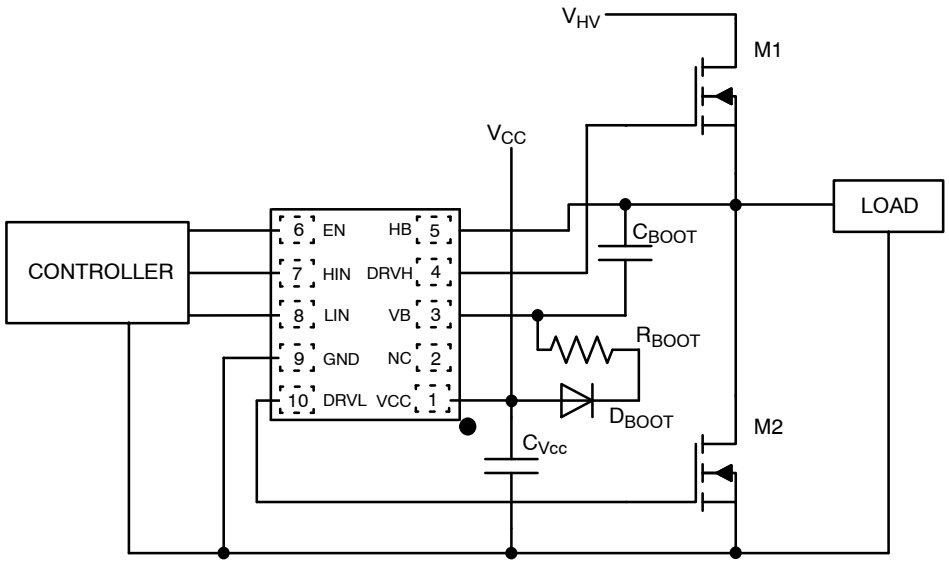


Figure 1. Typical Application Schematic

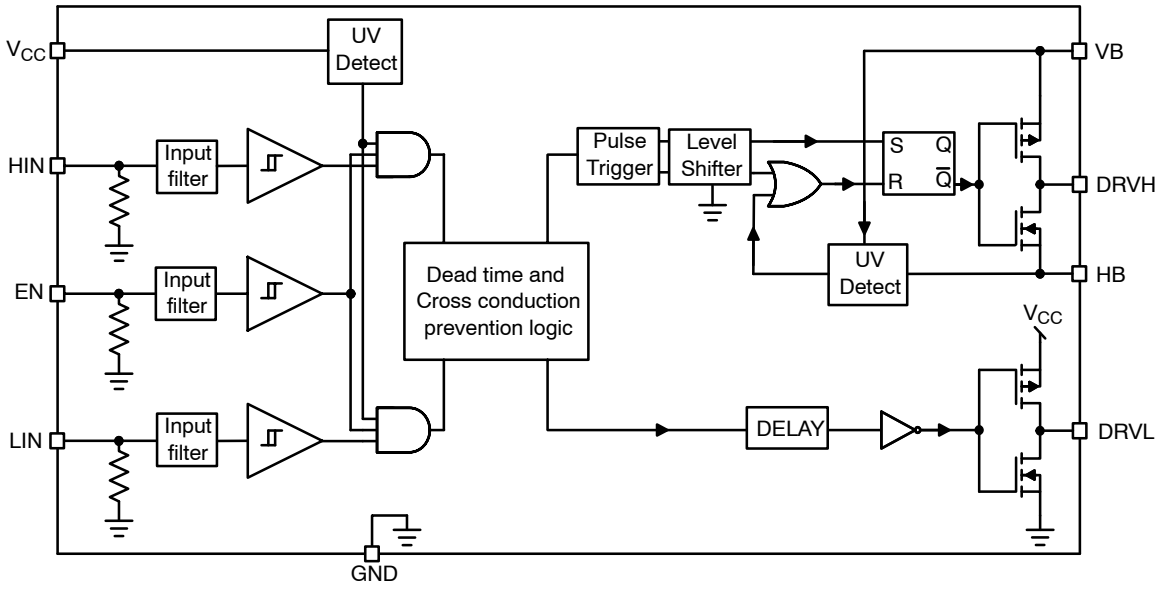


Figure 2. NCP51513A Version

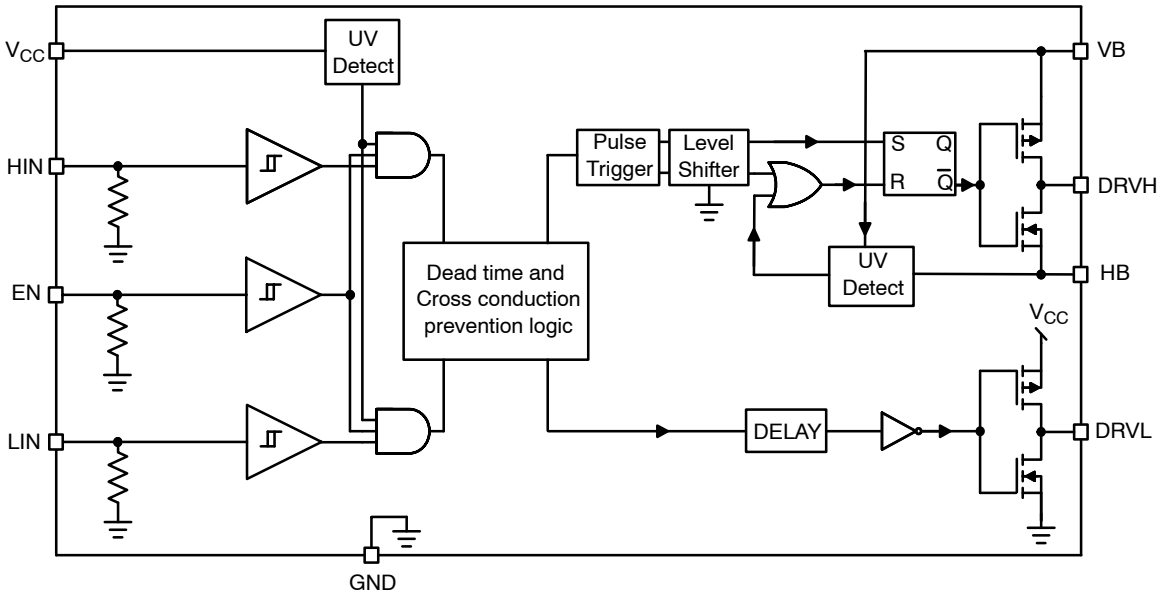


Figure 3. NCP51513B Version

MAXIMUM RATINGS

Rating	Symbol	Value	Units
Supply Voltage Range	V_{CC}	−0.3 to 20	V
High Side Boot Pin Voltage	V_B	−0.3 to 150	V
High Side Floating Voltage	V_B−V_{HB}	−0.3 to 20	V
High Side Bridge Pin Voltage	V_{HB}	V_B −20 to V_B + 0.3	V
High Side Drive Output Voltage	V_{DRVH}	V_{HB} −0.3 to V_B + 0.3	V
Low Side Output Voltage	V_{DRVL}	−0.3 to V_{CC} + 0.3	V
Allowable Output Slew Rate	dV_{HB}/dt	50	V/ns
Inputs HIN, LIN	V_{LIN}, V_{HIN}	−5 to V_{CC} + 0.3	V
Input EN	V_{EN}	−0.3 to V_{CC} + 0.3	V
Junction Temperature	T_{J_max}	+150	°C
Storage Temperature Range	T_{ST}	−55 to +150	°C
ESD Capability (Note 1): − HBM Model − CDM Model		 2000 1000	 V V
Lead Temperature Soldering Reflow (SMD Styles ONLY), Pb−Free Versions (Note 2)		260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series incorporates ESD protection and is tested by the following methods. ESD Human Body Model tested perAEC−Q100−002(EIA/JESD22−A114)
   ESD Charged Device Model tested per AEC−Q100−11(EIA/JESD22−C101E)
   Latchup Current Maximum Rating: ≤100 mA per JEDEC standard: JESD78E.
2. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Units
Thermal Resistance Junction to Air (Note 3)	$R_{\theta JA}$	157	°C/W
Junction to Top Characterization Parameter	Ψ_{J-T}	8.5	°C/W
Junction to Bottom Characterization Parameter	Ψ_{J-B}	0.12	°C/W

3. Values based on copper area of 100 mm^2 1 oz copper thickness and FR4 PCB substrate

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Min	Max	Unit
Supply Voltage Range	V_{CC}	8	19	V
Floating Supply Voltage Range	V_B−V_{HB}	8	19	V
Bridge Pin Voltage Range @ Vcc = 10 V	V_{HB}	−2	110	V
High Side Driver Voltage	V_{DRVH}	V_{HB}	V_B	V
Low Side Driver Voltage	V_{DRVL}	GND	V_{CC}	V
Input Signal Voltage	V_{HIN}, V_{LIN}	−3	V_{CC}	V
Input Signal Voltage	V_{EN}	GND	V_{CC}	V
Operating Junction Temperature Range	T_J	−40	+125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS

(VCC = VB = 12 V, VGND = VHB, −40°C < Tj < 125°C, Outputs loaded with 1 nF, typical values are valid for 25°C. All voltages are referred to GND pin)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SUPPLY SECTION						
V_{CC} Current Consumption in Active Mode	I_{CC1}	f_{SW} = 100 kHz	–	1.8	2.3	mA
V_B Current Consumption in Active Mode	I_{B1}	f_{SW} = 100 kHz	–	1.8	2.3	mA
V_{CC} Current Consumption in Active Mode	I_{CC1_noload}	f_{SW} = 100 kHz, C_{LOAD} = 0	–	0.6	1.2	mA
V_B Current Consumption in Active Mode	$I_{B1-noload}$	f_{SW} = 100 kHz, C_{LOAD} = 0	–	0.3	0.5	mA
Vcc Current Consumption in Active Mode	$I_{CC2\_EN\_H}$	f_{SW} = 0 Hz, V_{EN} = 3 V	–	150	250	μA
V_B Current Consumption in Active Mode	$I_{B2\_EN\_H}$	f_{SW} = 0 Hz, V_{EN} = 3 V	–	100	150	μA
V_{CC} Current Consumption in Inhibition Mode	I_{CC2}	V_{EN} = 0 V	–	150	250	μA
V_B Current Consumption in Inhibition Mode	I_{B2}	V_{EN} = 0 V	–	100	150	μA
Leakage Current on High Voltage Pins to GND	I_{HV_LEAK}	V_B = HB = DRVH = 130 V	–	2	5	μA
INPUT SECTION						
Low Level Input Voltage Threshold	V_{xINL}, V_{ENL}		–	–	0.8	V
Input Pull−Down Resistor	R_{xIN}	V_{xIN} = 5 V, V_{EN} = 0 V	100	175	250	kΩ
High Level Input Voltage Threshold	V_{xINH}, V_{ENH}		2.3	–	–	V
Enable Pin Pull−Down Resistor	R_{EN}	V_{EN} = 5 V	60	95	135	kΩ
Logic “1” Input Bias Current	I_{xIN+}	V_{xIN} = 5 V, V_{EN} = 5 V	–	30	50	μA
Logic “0” Input Bias Current	I_{xIN-}	V_{xIN} = 0 V, V_{EN} = 0 V	–	–	2.0	μA
Logic “1” Input Bias Current	I_{EN+}	V_{EN} = 5 V	–	50	85	μA
Logic “0” Input Bias Current	I_{EN-}	V_{EN} = 0 V	–	–	2.0	μA
UVLO SECTION						
V_{CC} UV Start−Up Voltage Threshold	V_{CCon}		5.8	6.4	7.0	V
V_{CC} UV Shut−Down Voltage Threshold	V_{CCoff}		5.3	5.9	6.5	V
Hysteresis on V_{CC}	V_{CChyst}		0.2	0.5	–	V
Vboot Start−Up Voltage Threshold Reference to Bridge Pin	V_{Bon}	V_{Bon} = V_B − HB	5.8	6.4	7.0	V
Vboot UV Shut−Down Voltage Threshold	V_{Boff}		5.3	5.9	6.5	V
Hysteresis on Vboot	V_{Bhyst}		0.2	0.5	–	V
Time between Vboot > V_{Bon} & 1st DRVH Pulse	$t_{startup}$		–	–	10	μs
OUTPUT SECTION						
Output High Short Circuit Pulsed Current (Note 4)	$I_{DRVxsource}$	V_{DRVx} = 0 V, PW = 300 ns	–	2.0	–	A
Output Low Short Circuit Pulsed Current (Note 4)	$I_{DRVxsink}$	V_{DRVx} = V_{CC} (V_B), PW = 300 ns	–	3.0	–	A
Output Resistance Source	R_{OH}	I_{DRVx} = 30 mA	–	2.5	7	Ω
Output Resistance Sink	R_{OL}	I_{DRVx} = 30 mA	–	1.5	5	Ω
High Level Output Voltage	$V_{DRVx\,H}$	V_{BIAS} − V_{DRVx} @ I_{DRVL} = 20 mA	–	0.06	0.25	V
Low Level Output Voltage	$V_{DRVx\,L}$	V_{DRVx} @ I_{DRVx} = 20 mA	–	0.04	0.15	V
OUTPUT RISE AND FALL TIME						
Output Voltage Rise Time (from 10% to 90%)	t_r	V_{xIN} = 3 V	–	9	30	ns
Output Voltage Fall Time (from 90% to 10%)	t_f	V_{xIN} = 0 V	–	7	25	ns

ELECTRICAL CHARACTERISTICS (continued)
(VCC = VB = 12 V, VGND = VHB, −40°C < Tj < 125°C, Outputs loaded with 1 nF, typical values are valid for 25°C. All voltages are referred to GND pin)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
PROPAGATION DELAY NCP51513A						
Turn−On Propagation Delay	t_{ON}	HB = 0 V, 50 V or 130 V, Cload = 0 pF, V_{xIN} = 3 V	–	50	100	ns
Turn−Off Propagation Delay	t_{OFF}	HB = 0 V, 50 V or 130 V, Cload = 0 pF	–	50	100	ns
Enable High Signal Propagation Delay	t_{EN}	HB = 0 V, 50 V or 130 V, Cload = 0 pF, V_{xIN} = 3 V	–	50	100	ns
Enable Low Signal Propagation Delay	t_{ENoff}	HB = 0 V, 50 V or 130 V, Cload = 0 pF, V_{xIN} = 3 V	–	50	100	ns
Minimum Input Filter Time	t_{FLT}	V_{xIN} = 3 V	20	30	–	ns
PROPAGATION DELAY NCP51513B						
Turn−On Propagation Delay	t_{ON}	HB = 0 V, 50 V or 130 V, Cload = 0 pF, V_{xIN} = 3 V	–	20	40	ns
Turn−Off Propagation Delay	t_{OFF}	HB = 0 V, 50 V or 130 V, Cload = 0 pF	–	20	40	ns
Enable High Signal Propagation Delay	t_{EN}	HB = 0 V, 50 V or 130 V, Cload = 0 pF, V_{xIN} = 3 V	–	20	40	ns
Enable Low Signal Propagation Delay	t_{ENoff}	HB = 0 V, 50 V or 130 V, Cload = 0 pF, V_{xIN} = 3 V	–	20	40	ns
DELAY MATCHING						
Propagation Delay Matching between the High Side and the Low Side	Δt	V_{xIN} = 3 V	–	0	11	ns
TIMING						
Minimum Input Width that Changes the Output	t_{PW}	V_{xIN} = 3 V (B Version Only)	–	–	10	ns
Internal Dead Time	t_{DT}	V_{xIN} = 3 V	60	80	100	ns
Dead Time Matching	Δt_{DT}		–	–	20	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
4. Parameter guaranteed by design.

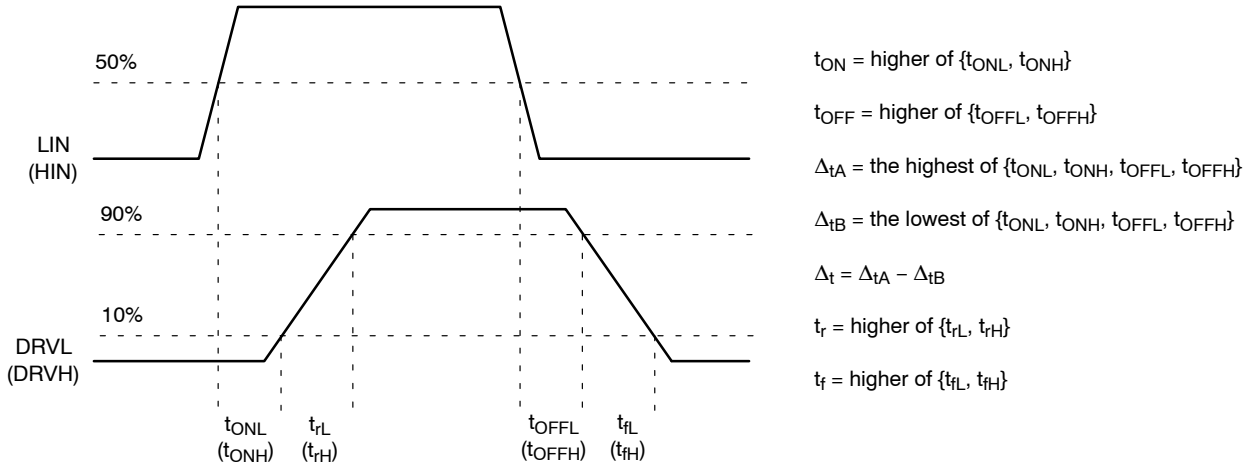


Figure 4. Propagation Delay, Propagation Delay Matching, Rise Time and Fall Time Testing

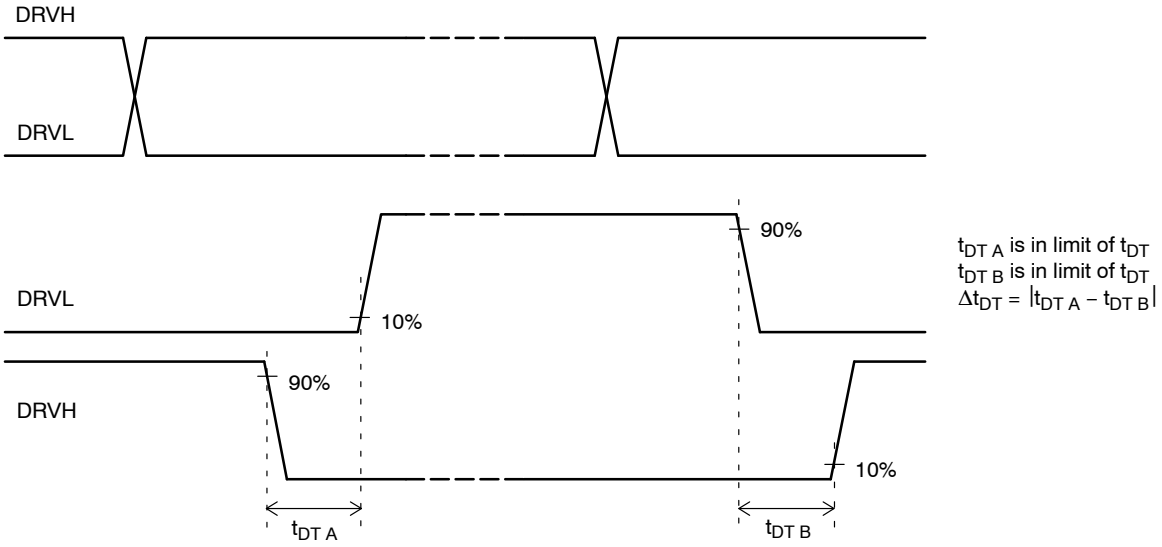


Figure 5. Dead Time and Dead Time Matching Measurement

TYPICAL ELECTRICAL CHARACTERISTICS

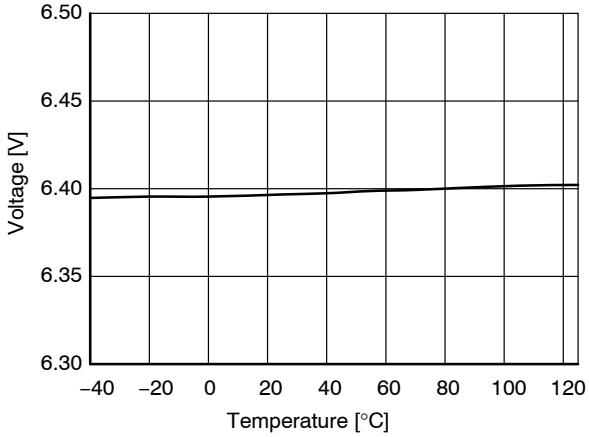


Figure 6. V_{CCon} vs. Temperature

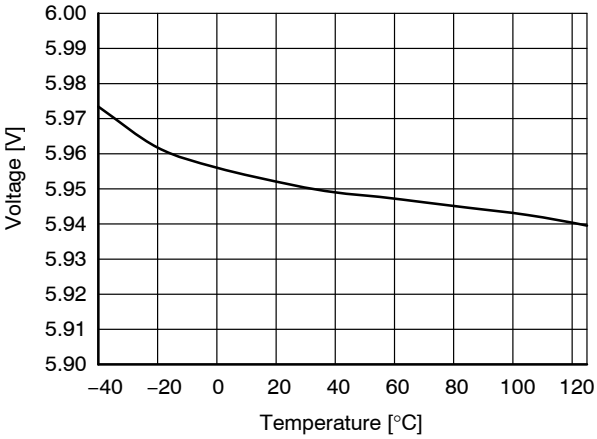


Figure 7. V_{CCoff} vs. Temperature

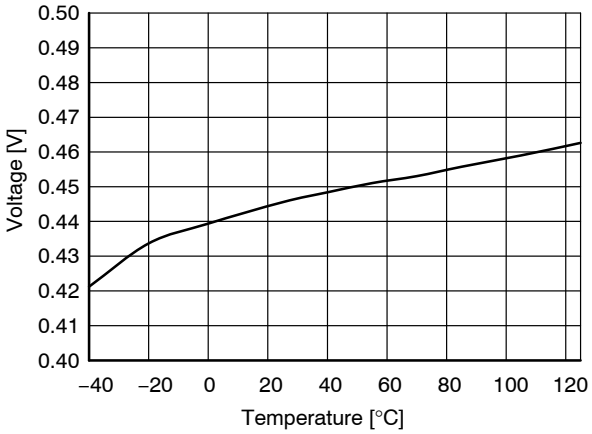


Figure 8. V_{CChyst} vs. Temperature

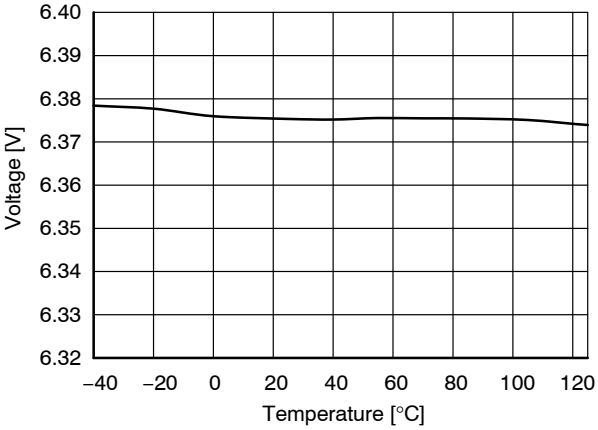


Figure 9. V_{Bon} vs. Temperature

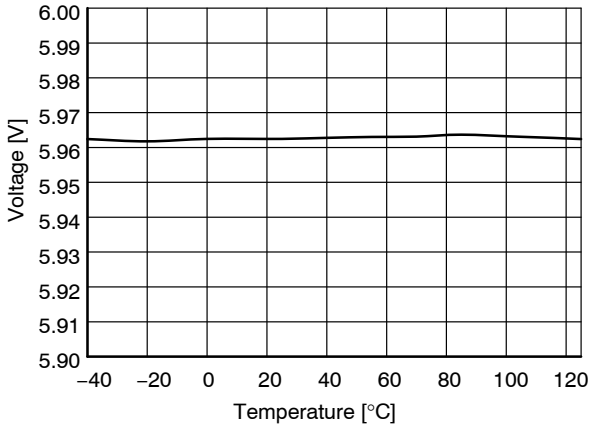


Figure 10. V_{Boff} vs. Temperature

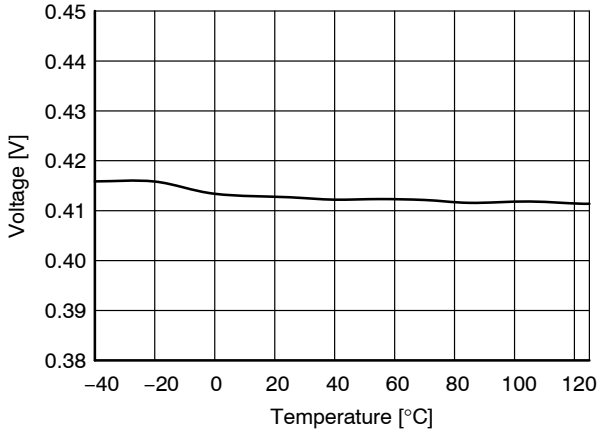


Figure 11. V_{Bhyst} vs. Temperature

TYPICAL ELECTRICAL CHARACTERISTICS (continued)

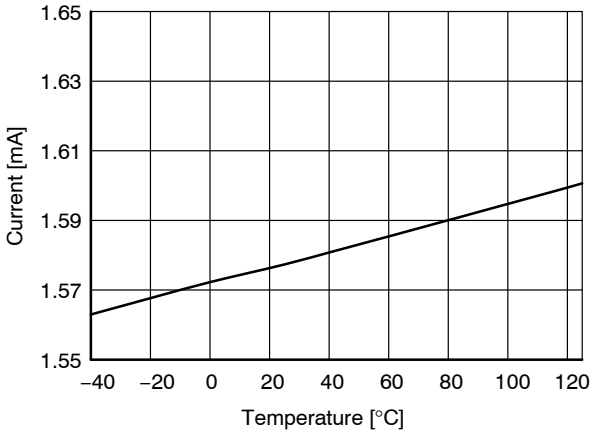


Figure 12. I_{CC1} vs. Temperature

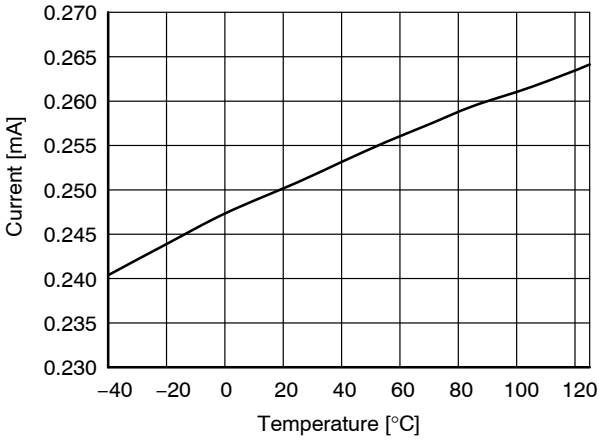


Figure 13. $I_{CC1\ noload}$ vs. Temperature

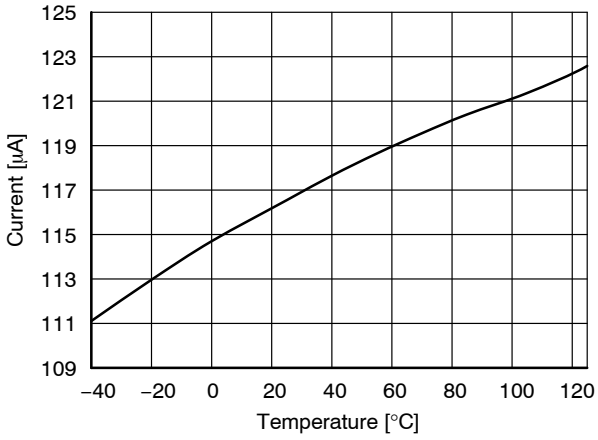


Figure 14. $I_{CC2\ EN\ H}$ vs. Temperature

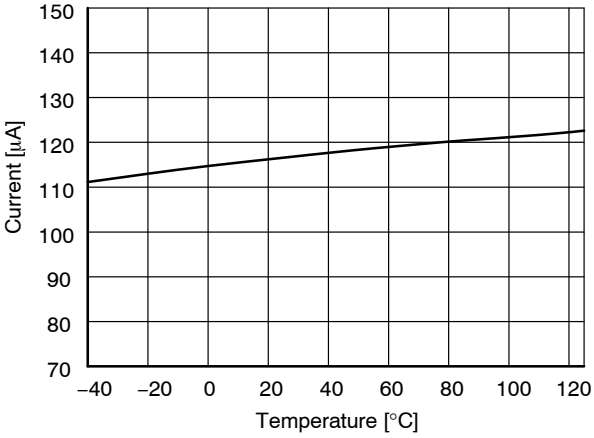


Figure 15. I_{CC2} vs. Temperature

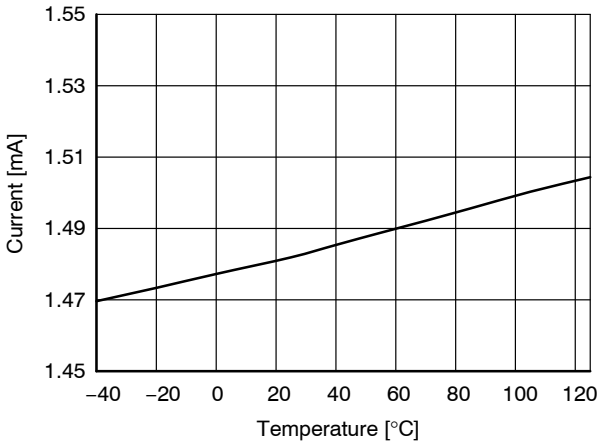


Figure 16. I_{B1} vs. Temperature

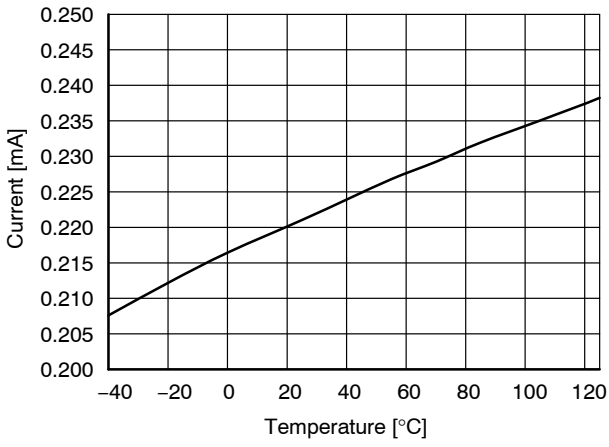


Figure 17. $I_{B1\ noload}$ vs. Temperature

TYPICAL ELECTRICAL CHARACTERISTICS (continued)

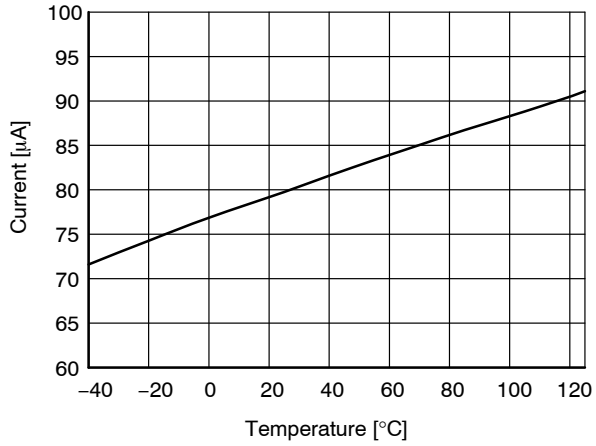


Figure 18. $I_{B2\ EN\ H}$ vs. Temperature

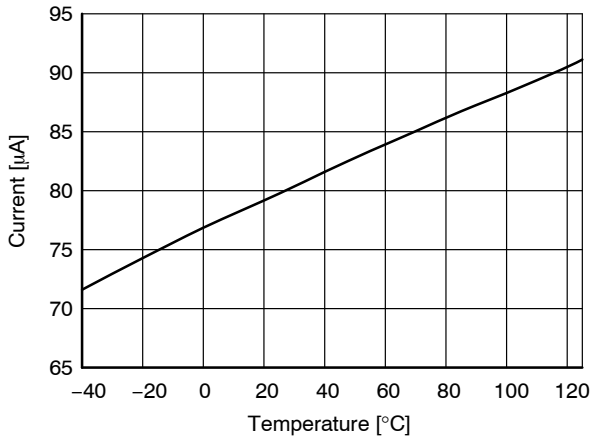


Figure 19. I_{B2} vs. Temperature

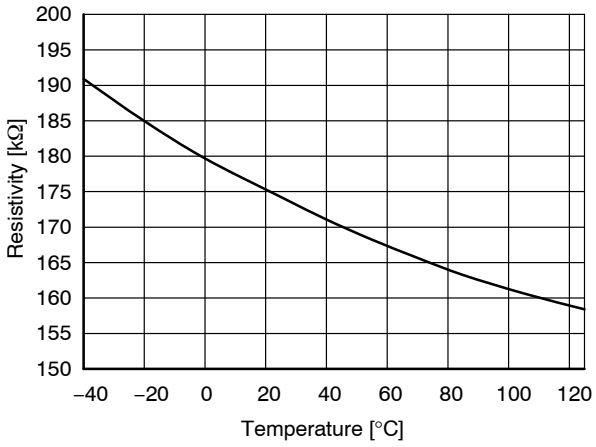


Figure 20. R_{xIH} vs. Temperature

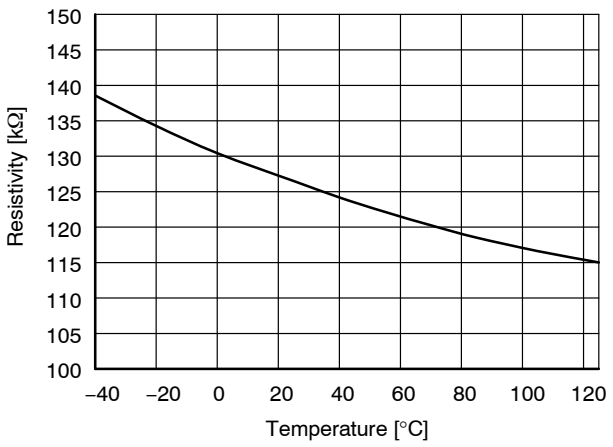


Figure 21. R_{EN} vs. Temperature

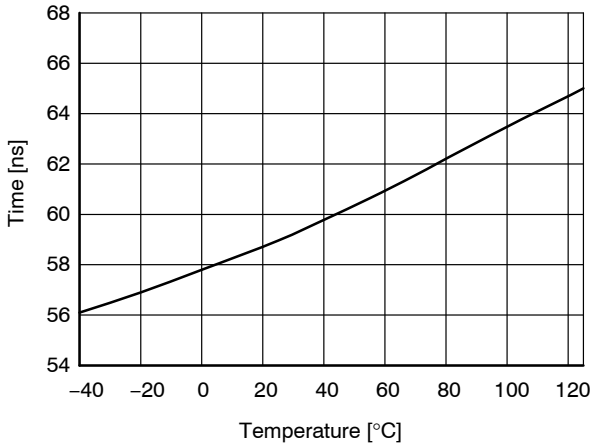


Figure 22. t_{ON} vs. Temperature

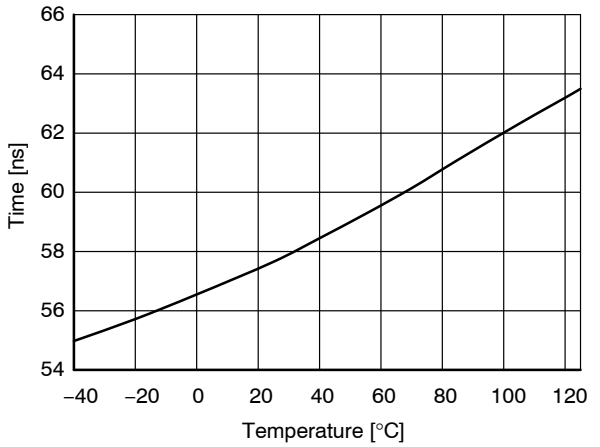


Figure 23. t_{OFF} vs. Temperature

TYPICAL ELECTRICAL CHARACTERISTICS (continued)

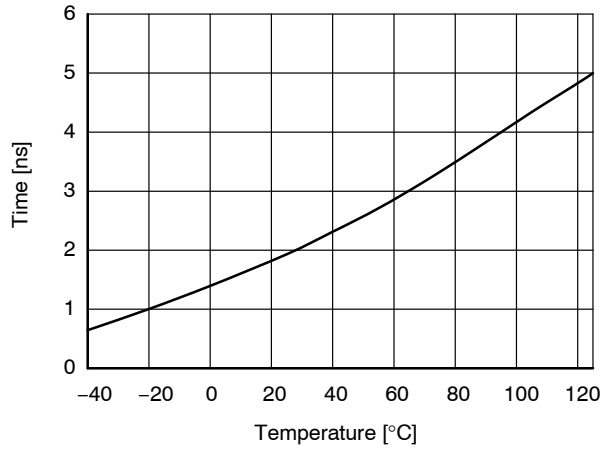


Figure 24. Δt vs. Temperature

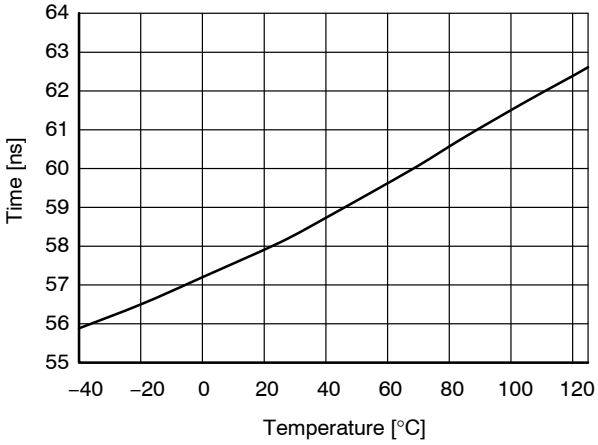


Figure 25. t_{EN} vs. Temperature

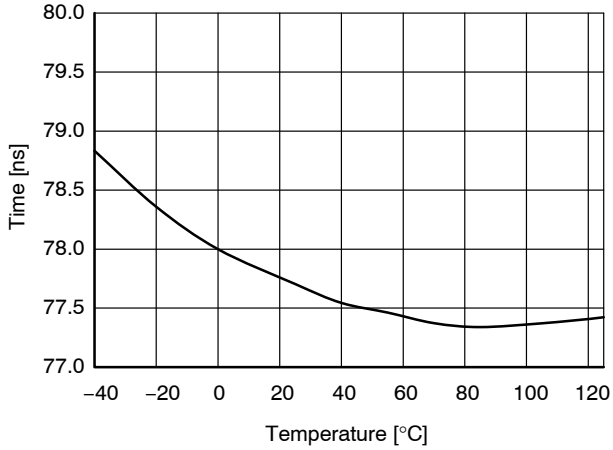


Figure 26. t_{DT} vs. Temperature

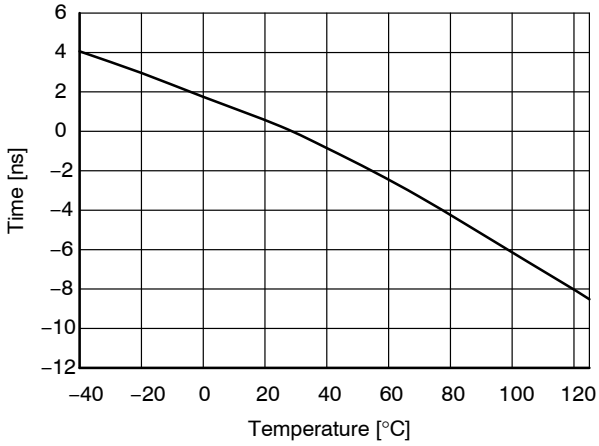


Figure 27. Δt_{DT} vs. Temperature

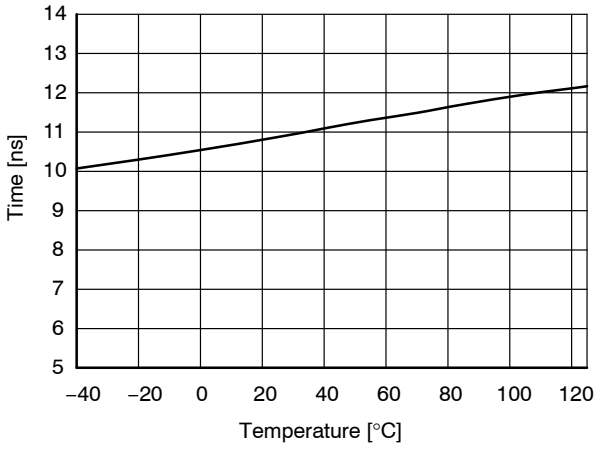


Figure 28. t_r vs. Temperature

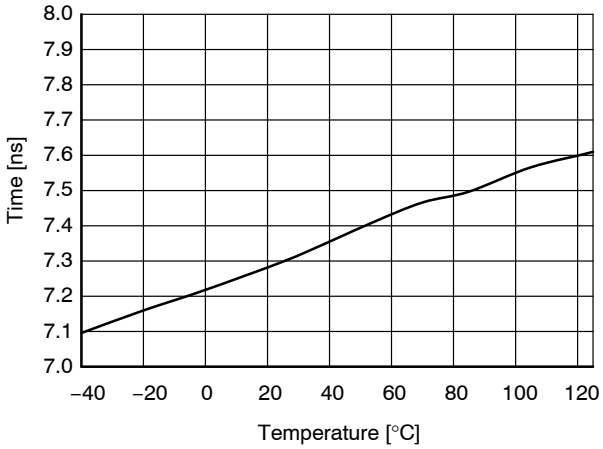


Figure 29. t_f vs. Temperature

TYPICAL ELECTRICAL CHARACTERISTICS (continued)

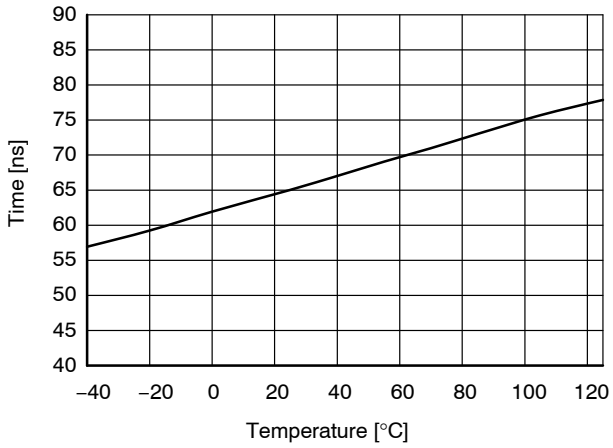


Figure 30. t_r 10 nF vs. Temperature

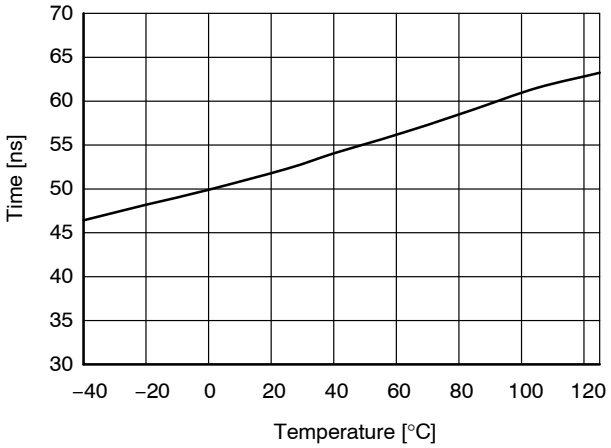


Figure 31. t_f 10 nF vs. Temperature

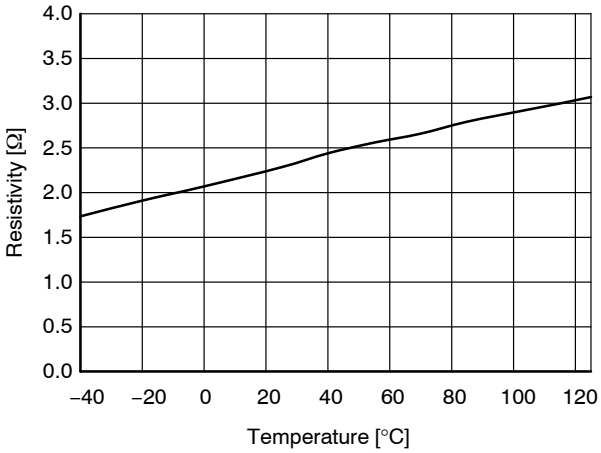


Figure 32. R_{OH} vs. Temperature

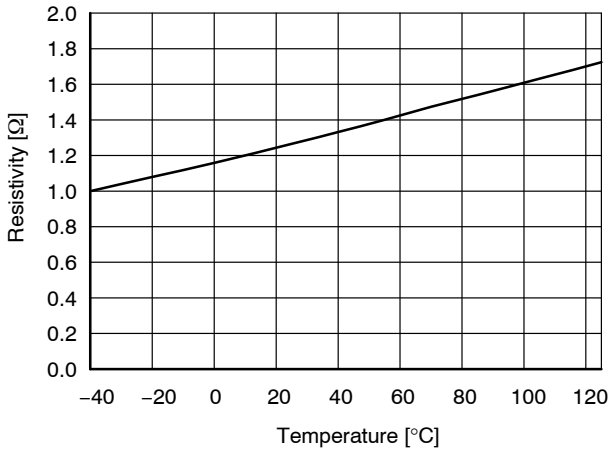


Figure 33. R_{OL} vs. Temperature

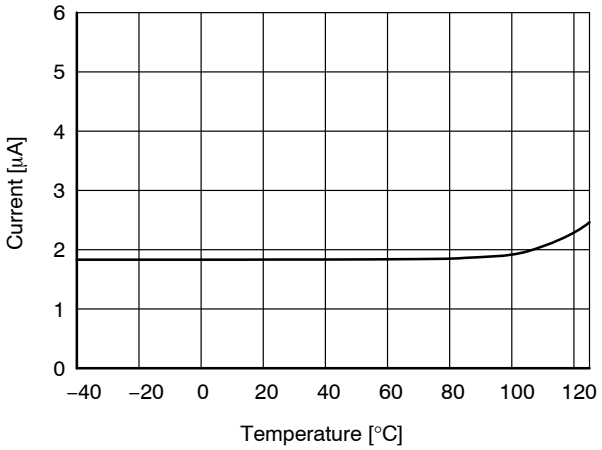


Figure 34. I_{HV_leak} vs. Temperature

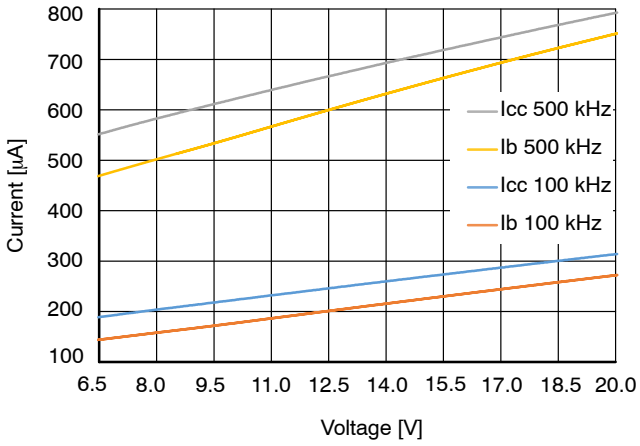


Figure 35. Current Consumption vs. Voltage. Cload = 0 nF

TYPICAL ELECTRICAL CHARACTERISTICS (continued)

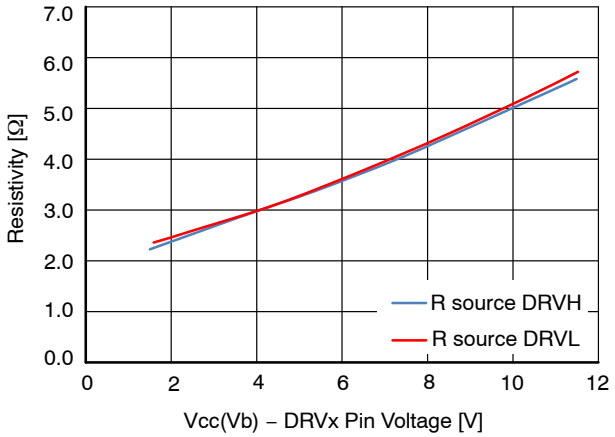


Figure 36. DRVx Source Resistance. 25°C. GBD

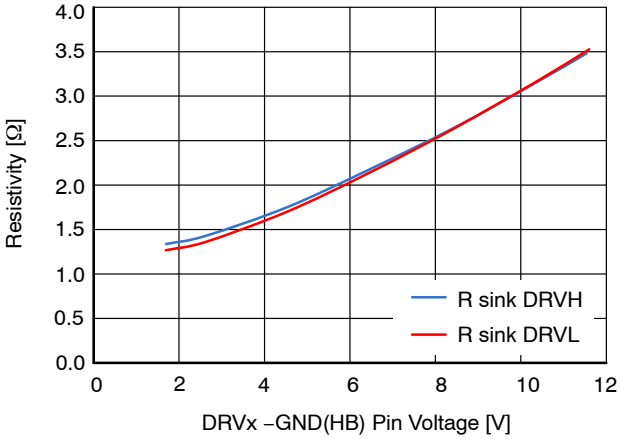


Figure 37. DRVx Sink Resistance. 25°C. GBD

General Description

For popular topologies like LLC, half bridge full brige converters, synchronous buck converters, etc. low−side and high−side drivers are needed which perform the function of both buffer and level shifter. These devices can drive the gate of the topside MOSFETs whose source node is a dynamically changing node. The bias for the high side driver in these devices is usually provided through a bootstrap circuit.

In a bid to make modern power supplies more compact and efficient, power supply designers are increasingly opting for high frequency operations. High frequency operation causes higher losses in the drivers, hence reducing the efficiency of the power supply.

NCP51513x are 130 V high side−low side drivers for DC−DC power supplies and inverters. NCP51513x offer best in class propagation delay, low quiescent current and low switching current at high frequencies of operation. This device thus enables highly efficient power supplies operating at high frequencies.

NCP51513x are available in two versions, NCP51513A or B. The A version includes a 30 ns input filter time, so propagation delay is 50 ns, the B version is without any filter, the propagation delay is reduced to 20 ns.

Internal 80 ns dead time eliminates cross conduction of the output MOSFETs.

NCP51513x have three input pins HIN, LIN and EN, allowing it to be used in a variety of applications. This device also includes features where in case of floating input, the logic is still defined. Driver inputs are compatible with both CMOS and TTL logic hence it provides easy interface with analog and digital controllers. NCP51513x has under voltage lock out feature for both high and low side drivers which ensures operation at correct V_{CC} and V_B voltage levels.

The output stage of NCP51513x has 2.0/3.0 A source/sink capability which can effectively charge and discharge a 1nF load in 9/7 ns.

Features

Input Stages

NCP51513x driver have three input pins HIN, LIN and EN, allowing it to be used in a variety of applications. The input stages of NCP51513x are TTL and CMOS compatible. This ensures that the inputs of NCP51513x can be driven with 3.3 V or 5 V logic signals from analog or digital PWM controllers or logic gates.

The input pins have Schmitt triggers to avoid noise induced logic errors.

NCP51513x come with an important feature wherein outputs (DRVH, DRVL) stays low in case any of the input pin is floating. At all the input pins there is an internal pull down resistor to define its logic value in case the pin is left open or NCP51513x are driven by open drain signal.

NCP51513A features a noise rejection function to ensure that any pulse glitch shorter than 30 ns will not produce any output change. This feature is well illustrated in the Figure 39.

NCP51513B have no such filter in the input stages. The timing diagram NCP51513B is depicted in Figure 39.

Enable pin in L state sets both outputs to L state. Enable pin in H state lets outputs to switch according to input signals. See Figure 40 for more details.

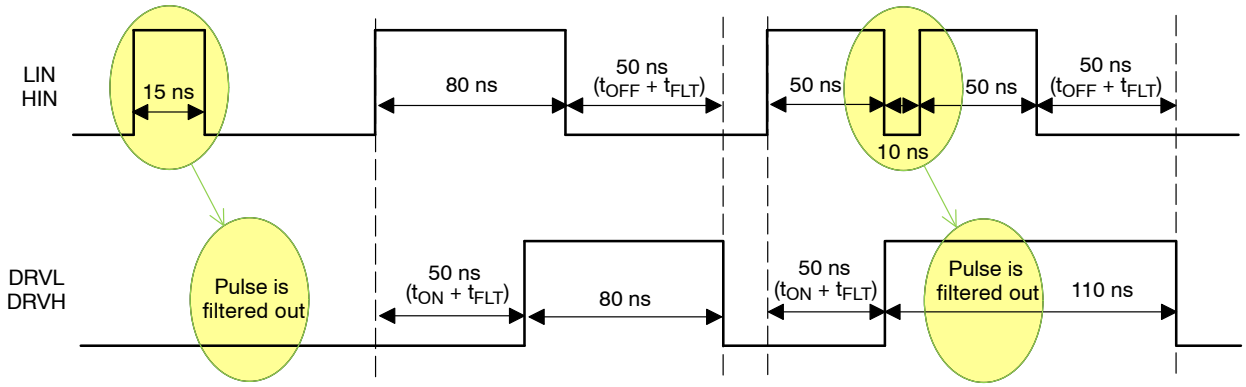


Figure 38. Version with Input Filter (NCP51513A)

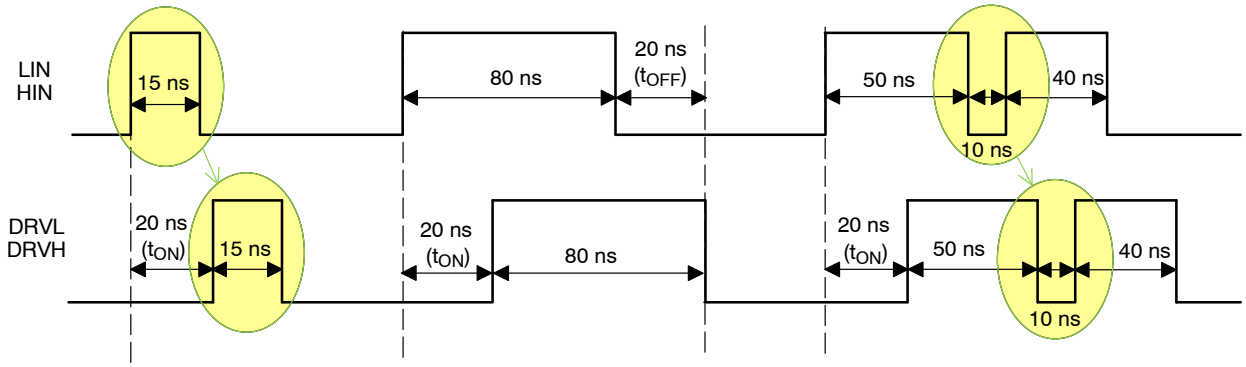


Figure 39. Version without Input Filter (NCP51513B)

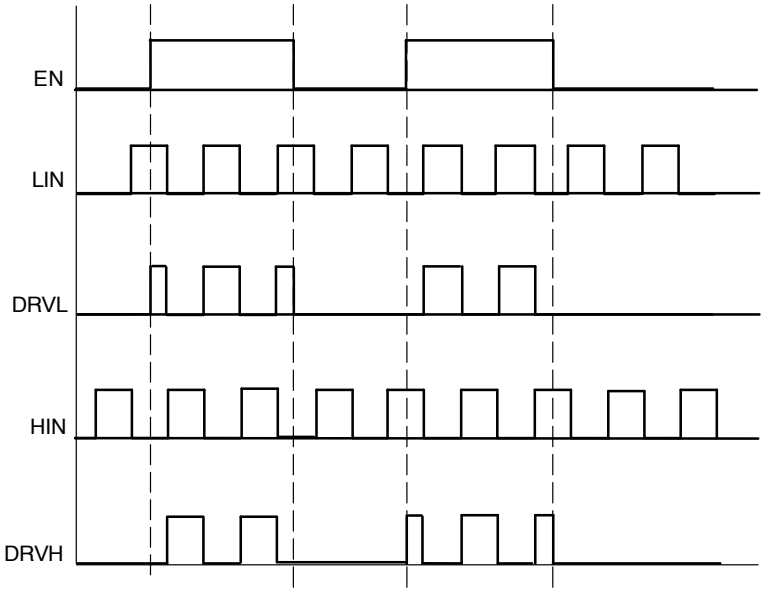
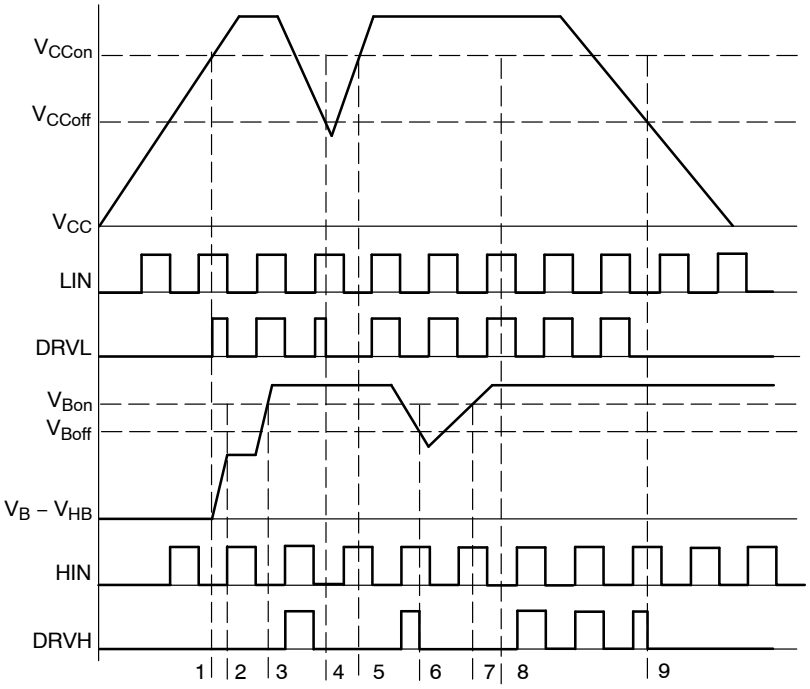


Figure 40. Enable Pin Function

Under Voltage Lock−Out

NCP51513x has under voltage lockout protection on both the high side and the low side driver. The function of the UVLO circuits is to ensure that there is enough supply voltages (V_{CC} and V_B) to correctly bias high side and low side circuits. This also ensures that the gate of external MOSFETs are driven at an optimum voltage. If the V_{CC} is below the V_{CC} UVLO voltage, the low side driver output (DRVL) and high side driver output (DRVH) both remain low. If V_B is below V_{Boff} UVLO voltage the high side driver output (DRVH) remains low. However if the V_{CC} is above V_{CCon} UVLO voltage level, the low side driver output (DRVL) can still turn on and off based on the low side driver input (LIN) and is not affected by the V_B status. This ensures proper charging of the bootstrap capacitor to bring the high side bias supply V_B above UVLO voltage. Both the V_{CC} and V_B UVLO circuits are provided with hysteresis feature. This hysteresis feature avoids errors due to ground noise in the power supply. The hysteresis also ensures continuous operation in case of a small drop in the bias voltage. This drop in the bias can happen when device starts switching MOSFET and the operating current of the device increases. The UVLO feature of the device is explained in the Figure 41.



Legend:
1. Vcc crossed Vcc ON level, LIN is set to H. The DRVH is set to H immediately. Current starts to flow from Vcc to Cboot via bootstrap diode.
2. Cboot is not fully charged in first pulse.
3. Vb cross Vbon level. HIN is in L, output stays in L. Both UVLOs are activated, pulses Can pass the driver.
4. Vccoff level is activated, DRVL is set to L, DRVH had been in L, it stayes in L
5. Vccon level crossed, HS UVLO had been activated earlier, the pulse is ignored.
6. Vboff level crossed while DRVH is H. DRVH is set to L immediately.
7. Vbon level crossed. Current (ongoing) HIN pulse is ignored.
8. Both UVLOs are activated, all pulses passes the driver. Steady state conditions.
9. Vccoff level is croosed while DRVH is in H. Both drivers are inhibited, DRVH is set to L immediately. From now on, no pulse will pass the driver (LS nor HS).

Figure 41. UVLO Timing Diagram

Dead Time Control & Interlock

NCP51513x features inbuild 80 ns dead control logic. The logic inserts the 80 ns delay after any driver turn off to postpone turn on of the opposite one. The delay helps to minimize cross conduction current through the MOSFETs when one is switched off and simultaneously other one is switched on. The dead time section also includes cross conduction prevention logic (interlock), which does not let to set both drivers to High simultaneously. See detail function in Figure 42.

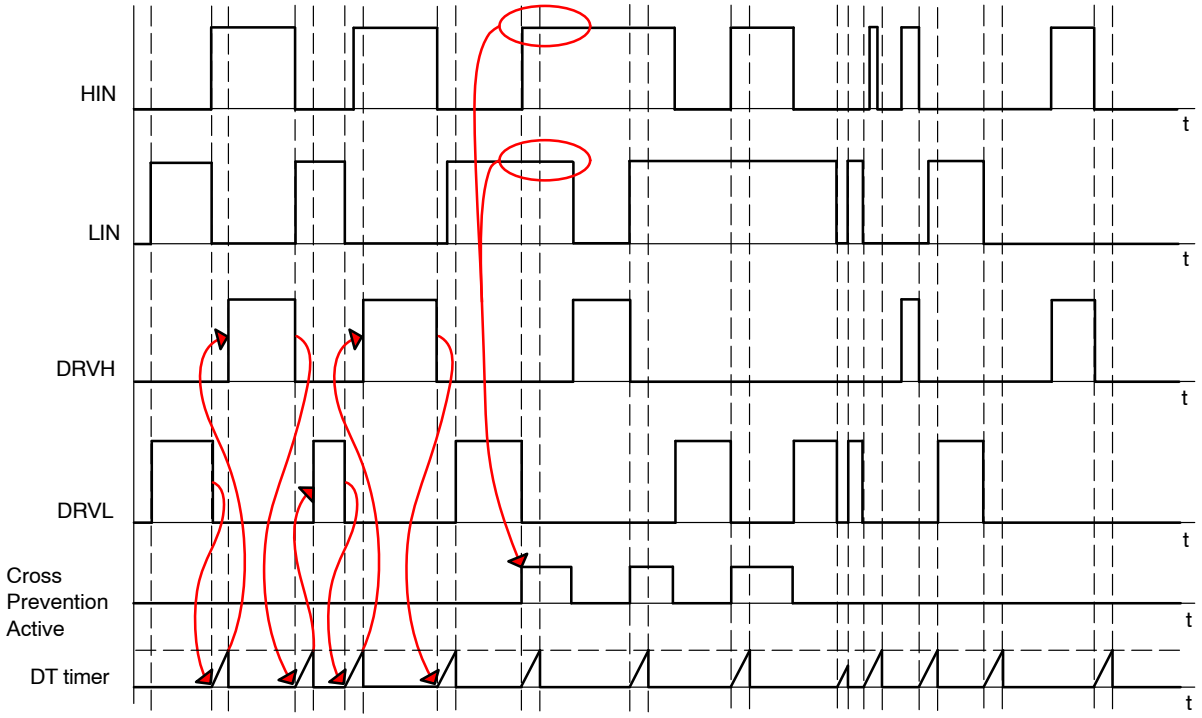


Figure 42. Dead Time Timing Diagram

Table 2. TRUE TABLE

#	Vcc Supply	Vb Supply	EN	LIN	HIN	DRVL	DRVH
1	Vcc < Vccoff	Vb = x	x	x	x	L (Note 7)	L (Note 7)
2	Vcc > Vccon (Note 5)	Vb = x	L	x	x	L	L (Note 7)
3	Vcc > Vccon (Note 5)	Vb < Vboff	H	L	x	L	L
4	Vcc > Vccon (Note 5)	Vb < Vboff	H	H	L	H	L
5	Vcc > Vccon (Note 5)	Vb > Vbon (Note 5)	H	L	L	L	L
6	Vcc > Vccon (Note 5)	Vb > Vbon (Note 5)	H	H	L	H	L
7	Vcc > Vccon (Note 5)	Vb > Vbon (Note 5)	H	L	H	L	H
8	Vcc > Vccon (Note 5)	Vb > Vbon (Note 5)	H	H	H	L	L
9	Vcc ↑ Vccon (Note 6)	Vb < Vboff	H	L	x	L	L
10	Vcc ↑ Vccon (Note 6)	Vb < Vboff	H	H	L	L ↑ H	L
11	Vcc ↑ Vccon (Note 6)	Vb > Vbon (Note 5)	H	L	L	L	L
12	Vcc ↑ Vccon (Note 6)	Vb > Vbon (Note 5)	H	L	H	L	L
13	Vcc > Vccon (Note 6)	Vb ↑ Vbon (Note 6)	H	L	H	L	L
14	Vcc ↓ Vccoff	Vb > Vbon (Note 5)	H	H	L	H ↓ L	L
15	Vcc ↓ Vccoff	Vb > Vbon (Note 5)	H	L	H	L	H ↓ L
16	Vcc > Vccon (Note 5)	Vb ↓ Vboff	H	H	L	H	L
17	Vcc > Vccon (Note 5)	Vb ↓ Vboff	H	L	H	L	H ↓ L

5. The voltage has crossed Vcc/Vb on level and it is higher than Vcc/Vb off level.
6. The voltage is rising from 0 V.
7. If the Vcc/Vb is lower than 3 V, the driver is pulled down via 150 kΩ.

NOTE: x – Any value

Output Stages

NCP51513x are equipped with two independent drivers with typical source/sink current is 2.0/3.0 A. The driver can effectively charge/discharge a 1 nF load in 9/7 ns. NCP51513x output drivers can not be turned on at the same time. Internal dead time generator inserts 80 ns dead time to eliminate short through current through the MOSFETs. See Figure 42.

The Figure 43 shows the output stage structure and the charging and discharging path of the external power MOSFET. The bias supply V_{CC} or V_B supplies energy to charge the gate capacitance C_{gs} of the low side or the high side external MOSFETs respectively. When a logic high is received from input stage, Qsource turns on and V_{CC}/V_B starts charging C_{gs} through R_g. Once the C_{gs} is charged to the drive voltage level, the external power MOSFET turns on and connects HB pin either to GND node (low side switch) or to HV line (high side switch).

When a logic low signal is received from the input stage, Qsource turns off and Qsink turns on providing a path for gate terminal discharging.

As seen in the Figure 43, there are parasitic inductances in charging and discharging path of the C_{gs}. This can result in a little dip in the bias voltages V_{CC}/V_B. If the V_{CC}/V_B drops below UVLO level, the power supply can shut down the device.

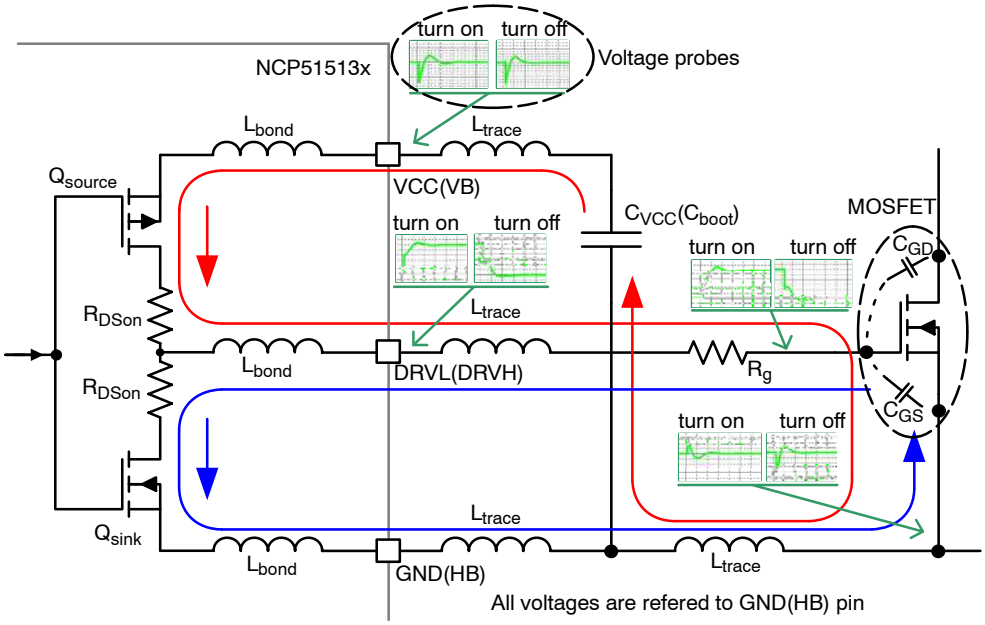


Figure 43. NCP51513x Turn ON−OFF Paths

Short Propagation Delay

NCP51513x boast short propagation delay between input and output. NCP51513A have a typical of 50 ns propagation delay. The best in class propagation delay in NCP51513x makes it suitable for high frequency operation.

Since NCP51513B doesn't have the input filter included, the propagation delays are even faster. NCP51513B offers 20 ns propagation delay between input and output.

The device allows 100 % duty cycle operation. The DRVH or DRVL can be continuously in H or L state. It is necessary to have a floating source to supply DRVH driver when using the driver under this 100% DC.

Negative Transient Immunity (NTI) Operating Conditions

In any HB switching applications the HB node is often pulled under the ground during the switching operation because of parasitic inductances and inductive load. These negative spikes may lead to malfunction or damage of the circuit.

Below schematics depicts parasitic and current circulation during switching operations that could create the negative deep of the HB node.

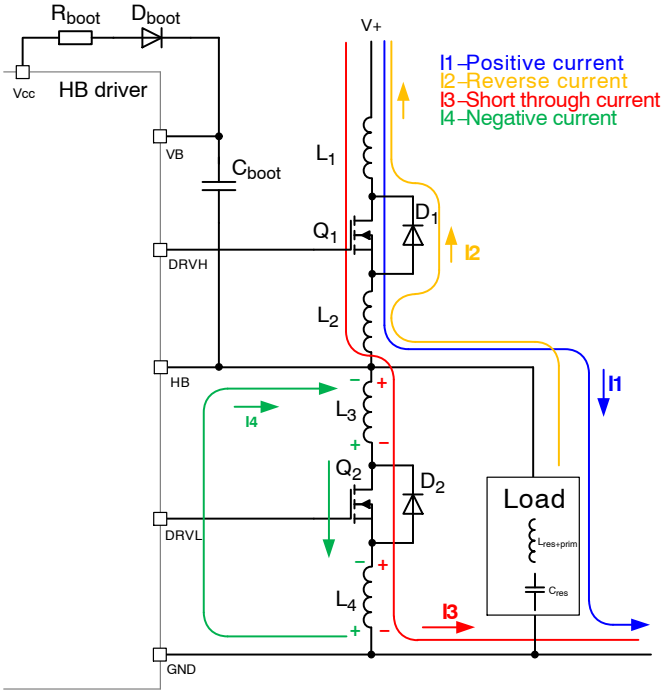


Figure 44. HB Negative Voltage in an LLC Configuration

NTI Robustness Measurement

The capability of NCP51513 to operate under negative voltage conditions is reported in NTI graph using below test set up.

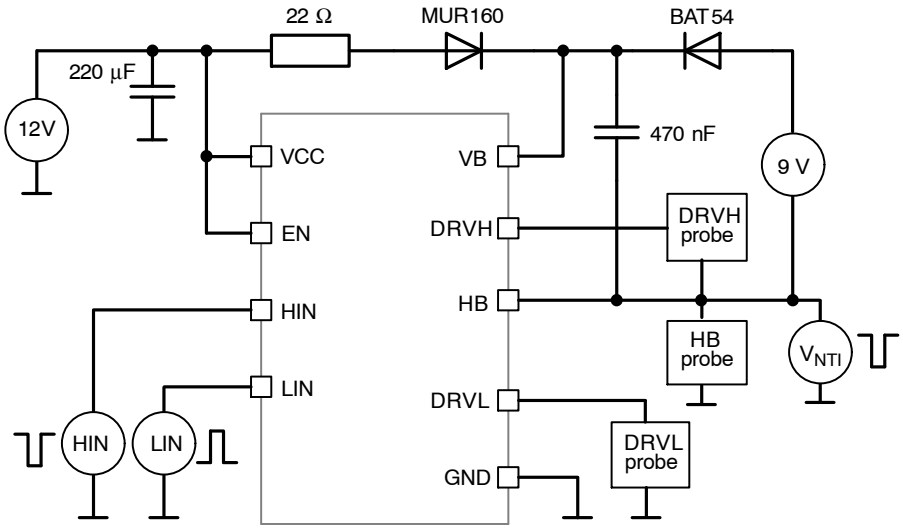


Figure 45. NTI Test Set Up

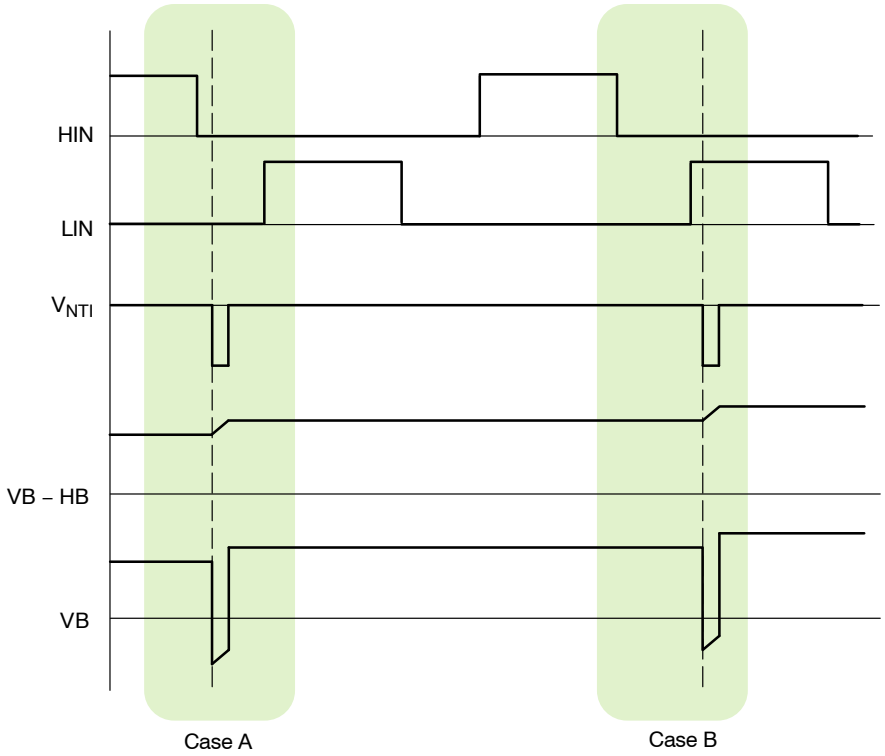


Figure 46. Timing Diagram

NCP51513 robustness against negative spikes is shown in Figure 47. The result is a curve which shows negative voltage level for specific pulse width under which driver could still operate properly.

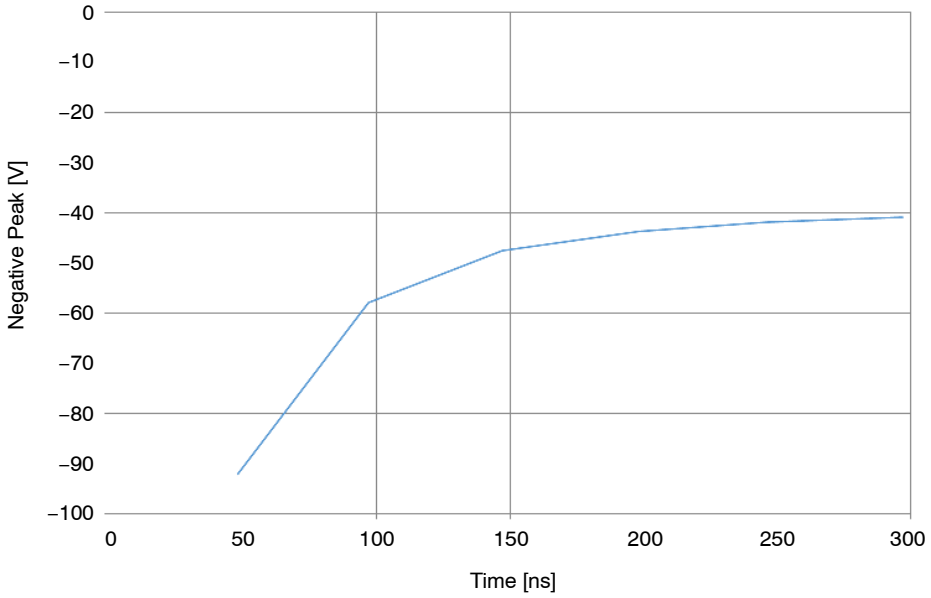


Figure 47. Indicative Negative Transient Immunity

Important note:
Even though above figure shows that NCP51513 is able to handle negative transient voltage conditions, it is highly recommended that the application circuit design is such that it removes or at least always limit the negative transient voltage on VB pin as much as possible via careful PCB layout and proper component selection.

Applications information & Component Selection

This section outlines the key design steps and components selection to get full benefit of NCP51513 performances. It includes as well some power dissipation considerations and layout recommendations.

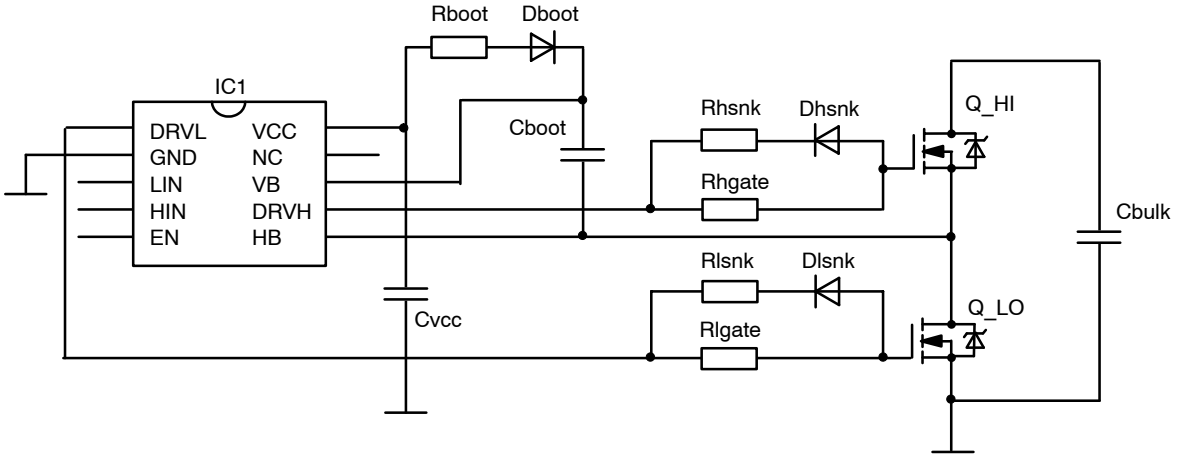


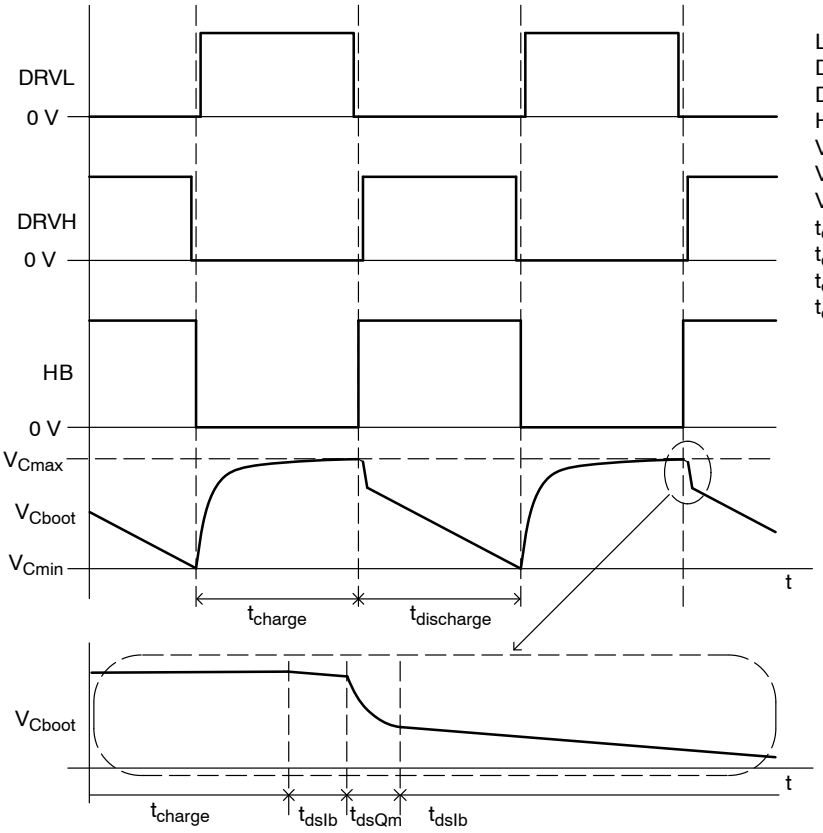
Figure 48. Recommended Schematic

C_{boot} Capacitor Value Calculation

The device features two independent drivers. The low side driver (DRVL) supplies a MOSFET whose source is connected to ground. The driver is powered from V_{CC} line. The high side driver (DRVH) supplies a MOSFET whose source is floating from GND to bulk voltage. The floating driver is powered from C_{boot} capacitor. The capacitor is charged only when HB pin is pulled to GND (by inductance or the low side MOSFET when turned on). If too small C_{boot} capacitor is used the high side UVLO protection can disable the high side driver which leads to improper switching.

Expected voltage on Cboot is pictured in Figure 49. The curves are valid for ZVS (Zero Voltage Switching) observed in LLC applications. For hard switch the curves are slightly different, but from charge on C_{boot} point of view more favorable. Under the hard switch conditions the energy to charge Q_g (from zero voltage to V_{th} of the MOSFET) is taken from V_{CC} capacitor (through an external boot strap diode) so the voltage drop on C_{boot} is smaller. For the calculation of C_{boot} value the ZVS conditions are taken account.

The switching cycle is divided into two parts, the charging (t_{charge}) and the discharging ($t_{discharge}$) of the C_{boot} capacitor. The discharging can be divided even more to discharging by floating driver current consumption I_{B2} (t_{dsIb}), and to discharging by transfering energy from C_{boot} to gate terminal of the MOSFET (t_{dsQm}) and discharging by leakage current of the bootstrap diode (not taken account). Discharging by I_{CC4} becoming more dominant when driver runs at lower frequencies and/or during skip mode operation. To calculate C_{boot} value, follow these steps:



Legend:

DRVL	low side driver
DRVH	high side driver
HB	bridge pin
V_{Cboot}	boot strap capacitor voltage
V_{Cmax}	maximum C_{boot} voltage
V_{Cmin}	minimum C_{boot} voltage
t_{charge}	charging period
$t_{discharge}$	discharging period
t_{dslb}	discharging by I_B current
t_{dsQm}	discharging by transcer a charge to a MOSFET

Figure 49. Boot Strap Capacitor Charging

1. For example, let's have a MOSFET with Q_g = 49 nC, V_{DD} = 10 V.
2. Charge stored in C_{boot} necessary to cover the period the C_{boot} is not supplied from V_{CC} line (which is basically the period the high side MOSFET is turned on). Let's say the application is switching at 100 kHz, 50% duty cycle, which means the upper MOSFET is conductive for 5 μs. It means the C_{boot} is discharged by I_{B2} current (100 μA typ) for 5 μs, so the charge consumed by floating driver is:

$$Q_b = I_{B2} \cdot t_{discharge} = 100\,\mu \cdot 5\,\mu = 500\,pC \quad \text{(eq. 1)}$$

3. Total charge loss during one switching cycle is sum of charge to supply the high side driver and MOSFET's gate charge:

$$Q_{tot} = Q_g + Q_b = 49\,n + 500\,p = 49.5\,nC \quad \text{(eq. 2)}$$

4. Let's determine acceptable voltage ripple on C_{boot} to 1% of nominal value, which is 100 mV. To cover charge losses from Eq. 2.

$$C_{boot} = \frac{Q_{tot}}{V_{ripple}} = \frac{49.5\,n}{0.1} = 495\,nF \quad \text{(eq. 3)}$$

R_{boot} Resistor Value Calculation

To keep the application running properly, it is necessary to charge the C_{boot} again. This is done by external diode from V_{CC} line to VB pin. In serial with the diode a resistor is placed to reduce the current peaks from V_{CC} line. The resistor value selection is critical for proper function of the high side driver. If too small high current peaks are drown from V_{CC} line, if too high the capacitor will not be charged to appropriate level and the high side driver can be disabled by internal UVLO protection.

First of all keep in mind the capacitor is charged through the external bootstrap diode, so it can be charged to a maximum voltage level of $V_{CC} - V_f$. The resistor value is calculated using this equation:

$$R_{boot} = \frac{t_{charge}}{C_{boot} \cdot \ln\left(\frac{V_{max} - V_{Cmin}}{V_{max} - V_{Cmax}}\right)} = \frac{5\,\mu}{1\,\mu \cdot \ln\left(\frac{9.4 - 9.25}{9.4 - 9.35}\right)} \cong 4.6\,\Omega \quad \text{(eq. 4)}$$

Where:

t_{charge}	time period the Cboot is being charged, usually the period the low side MOSFET is turned on,
C_{boot}	boot strap capacitor value,
V_{max}	maximum voltage the C_{boot} capacitor can be theoretically charged to. Usually the $V_{CC} - V_f$. The V_f is forward voltage of used diode,

V_{Cmin} the voltage level the capacitor is charge from,

V_{Cmax} the voltage level the capacitor is charged to. It is necessary to determine the target voltage for charging, because in theory, when a capacitor is charged from a voltage source through a resistor, the capacitor can never reach the voltage of the source. In this particular case a 50 mV difference (between the voltage behind the diode and V_{Cmax}) is used.

The resistor value obtained from Eq. 4 does not count with the quiescent current I_{B2} of the high side driver. This current will create another voltage drop of:

$$V_{IB2\_drop} = R_{boot} \cdot I_{B2} = 4.6 \cdot 100\ \mu \cong 460\ \mu V \quad \text{(eq. 5)}$$

The current consumed by high side driver will be higher, because the I_{B2} is valid when the device is not switching. While switching, losses by charging and discharging internal transistors as well as the level shifters will be added. This current will increase with frequency.

The additional 460 μV drop will be added to V_{Cmax} value. The additional 460 μV drop can be either accepted or the R_{boot} value can be recalculated to eliminate this additional drop.

The resistor R_{boot} calculated in Eq. 4 is valid under steady state conditions. During start and/or skip operation the starting point voltage value is different (lower) and it takes more time to charge the boot strap capacitor. More over it is not counted with temperature and voltage variability during normal operation or the dynamic resistance of the boot strap diode (approximately 0.34 Ω for MURA160). From these reasons the resistor value should be decreased especially with respect to skip operation.

Boot strap resistor loss calculation.

$$P_{Rboot} \cong Q_{tot} \cdot V_{max} \cdot f = 49.5\ n \cdot 9.4 \cdot 100\ k \cong 46.3\ mW \quad \text{(eq. 6)}$$

Boot strap diode loss calculation.

$$P_{Dboot} \cong Q_{tot} \cdot V_f \cdot f = 49.5\ n \cdot 0.6 \cdot 100\ k \cong 3\ mW \quad \text{(eq. 7)}$$

Please keep in mind the value is temperature and voltage dependent. Especially C_{boot} voltage can be higher than calculated value. See “Layout recommendation” section for more details. Also keep in mind, the Boot strap resistor power dissipation calculated in Eq. 6 is valid for steady state conditions. For first C_{boot} charging, the power loss (the current) is much higher.

$$I_{Rboot} = \frac{C_{Vcc} - V_{Dboot} - V_{Cboot}}{R_{boot}} = \frac{10 - 0.6 - 0}{4.6} \cong 2\ A \quad \text{(eq. 8)}$$

$$P_{Rboot} = (C_{Vcc} - V_{Dboot} - V_{Cboot}) \cdot I_{Rboot} = (10 - 0.6 - 0) \cdot 2 \cong 18.8\ W \quad \text{(eq. 9)}$$

The Boot strap resistor must be designed to accept the current from Eq. 8 and power loss from Eq. 9 for a while.

V_{CC} Capacitor Selection

V_{CC} capacitor value should be selected at least ten times the value of C_{boot} . In this case thus $C_{Vcc} > 10\ \mu F$.

Very close to the driver should be placed a ceramic capacitor at least the same value of C_{boot}, to cover current peaks for low side MOSFET gate charging.

R_{gate} Selection

The R_{gate} are selected to limit the peak gate current during charging and discharging of the gate capacitance. This resistance also helps to damp the ringing due to the parasitic inductances, reduce dV/dt on HB pin to safe level and attenuate EMI radiation. If high dV/dt (during rise/fall edge and/or ringing after switching) is applied on HB pin, it can cause unexpected behavior of the driver.

On the other hand, too high resistor will increase power loss on MOSFETs, which leads to lower efficiency. It is recommended to start evaluation with a high resistor value and decrease the value if behavior is safe under all conditions. We recommend to have at least a 4.7 Ω resistor between NCP51513 outputs and MOSFET’s gate.

The resistors also help to decrease power dissipation of the driver, because part of the energy from charging and discharging C_{gs} is radiated on the resistors R_{xgate} (and on R_{xsnk} if they are used) outside the driver see Figure 48. The gate resistor selection is tricky task. It depends on application, topology, on used MOSFETs, layout etc.

For example for an R_{xgate} value of 4.7 Ω, the peak source and sink currents would be limited to the following values. R_{gate} = 4.7 Ω

$$I_{DRVL\_Source} = \frac{V_{cc}}{R_{Lgate} + R_{LOL} + R_g} = \frac{10\ V}{12.7\ \Omega} = 787\ mA \quad \text{(eq. 10)}$$

$$I_{DRVL\_Sink} = \frac{V_{cc}}{R_{Lgate} + R_{LOL} + R_g} = \frac{10\ V}{10.7\ \Omega} = 935\ mA \quad \text{(eq. 11)}$$

Where:

R_{LOH} R_{DSon} of internal source MOSFET (see parametric table R_{OH} parameter),

R_{LOL} R_{DSon} of internal sink MOSFET (see parametric table R_{OL} parameter),

Rg internal gate resistance of external MOSFET (see appropriate DS), in this case 1 Ω.

In some applications it is desired/advantageous to use separated current paths for charging and discharging the gate capacitance. For this purpose external MOSFET gate connection must be extended (see Figure 48). Two components Rxsnk and Dxsnk can be added in parallel to Rxgate resistor. The charging path is now only through

Rxgate resistor, while discharging path is through Rxsnk and Rxgate in parallel combination. Consider both resistors are the same value 10 Ω. The source current is calculated using Eq. 10. The current is 556 mA.

R_{lgate} = 10 Ω

$$I_{DRVL_{Sink}} = \frac{V_{cc}}{R_{lgate} + (R_{LOL} + R_g) \cdot 2} + \frac{V_{cc} - V_{Dlsnk}}{R_{lsnk} + (R_{LOL} + R_g) \cdot 2}$$

$$= \frac{10\ V}{22\ \Omega} + \frac{9.4\ V}{22\ \Omega} = 882\ mA \quad \text{(eq. 12)}$$

For high side driver current calculation use the same method. Use Eq. 10 to Eq. 12, but use V_{Cboot} voltage (usually diminished by V_f of used bootstrap diode).

Total Power Dissipation

Total power dissipation of NCP51513x is sum of partial dissipations which can be calculated as follows. For more details, please refer to AND90004.

1. Power loss of device (except drivers) while switching at appropriate frequency is calculated from current consumption at given voltage for specific frequency. The current can be estimated from Figure 35, or it could be calculated using these formulas:

$$Icc = 21.1\ \mu \cdot f \cdot V + 7.01\ m \cdot V + 783\ \mu \cdot f + 53.6\ m \quad \text{(eq. 13)}$$

$$Ib = 28.6\ \mu \cdot f \cdot V + 6.75\ m \cdot V + 633\ \mu \cdot f + 17.6\ m \quad \text{(eq. 14)}$$

Where:

f is frequency in kHz,

V is voltage in V,

Calculated current will be in mA.

The power dissipation of device (without drivers) is equal to.

$$P_{logic} = P_{HS} + P_{LS} = \left(V_{boot} \cdot I_{B1_{noload}}\right) + \left(V_{CC} \cdot I_{CC1_{noload}}\right)$$

$$= (9.4 \cdot 0.171\ m) + (10 \cdot 0.223\ m) \cong 3.8\ mW \quad \text{(eq. 15)}$$

2. Power loss of drivers

$$P_{drivers} = \left(\left(Q_g \cdot V_{boot}\right) + \left(Q_g \cdot V_{CC}\right)\right) \cdot f$$

$$= \left((49\ n \cdot 9.4) + (49\ n \cdot 10)\right) \cdot 100\ k$$

$$\cong 95.1\ mW \quad \text{(eq. 16)}$$

3. Level shifter power loss

$$P_{lvlshft} = (V_{HV} + V_B) \cdot f_{SW} \cdot (Q_S + Q_R)$$

$$= (100 + 9.4) \cdot 100\ k \cdot (190\ p + 190\ p)$$

$$\cong 4.2\ mW \quad \text{(eq. 17)}$$

Where:

V_{HV} is DC link voltage, here 100 V,

V_B is boot strap voltage, here 9.6 V,

f_{SW} is duty frequency, here 100 kHz,

Q_S, Q_R is energy needed to transfer information from LS part to HS part of the driver. The worst case is ZVS mode. In hard switch mode is Q_S very small, as the set pulse come when HB pin is on low voltage.

4. HS leakage power loss

$$P_{leak} = I_{HV_{LEAK}} \cdot (V_{HV} + V_B) \cdot DC$$

$$= 1.8\ \mu \cdot (100 + 9.4) \cdot 0.5 \cong 0.1\ mW \quad \text{(eq. 18)}$$

Where:

V_{HV} is DC link voltage, here 100 V,

V_B is boot strap voltage, here 9.4 V,

DC is duty cycle, here 50%.

5. Total power losses

$$P_{total} = P_{logic} + P_{drivers} + P_{lvlshft} + P_{leak}$$

$$= 3.8\ m + 95.1\ m + 4.2\ m + 0.1\ m$$

$$\cong 103\ mW \quad \text{(eq. 19)}$$

6. Junction temperature rises for calculated power loss

$$t_J = R_{tJa} \cdot P_{total} = 157 \cdot 0.103 \cong 16\ K \quad \text{(eq. 20)}$$

The temperature calculated in Eq. 15 is the value which has to be added to ambient temperature. In case the ambient temperature is 30°C, the junction temperature will be 46°C.

Layout Recommendations

The NCP51513x are high speed drivers suitable for mid−high power application. To avoid any damage and/or malfunction during switching (and/or during transients, overloads, shorts etc.) it is very important to avoid a high parasitic inductances in high current paths (see “MOSFET turn on and turn off current path” section). It is recommended to fulfill some rules in layout. One of a possible layout for the IC is depictured in Figure 50.

- Keep loop HB_pin – GND_pin – Q_LO as small as possible. This loop (parasitic inductance) has potential to increase negative spike on HB pin which can cause malfunction or damage of HB driver. The negative voltage presented on HB pin is added to V_{CC}−V_f voltage so V_{Cboot} is increased. In extreme case the C_{boot} voltage can be so high it will cross maximum rating value which can lead to device damage.
- Keep loop VCC_pin – GND_pin – C_{VCC} as small as possible (locate C_{VDD} as close to the IC as possible). The IC features high current capability driver. Any parasitic inductance in this path will result in slow Q_LO turn on and voltage drop on VCC pin which can result in UVLO activation.
- To avoid switching current (a noise) from the driver to disturb the Vcc line a small resistance in serie with C_{VCC} and V_{CC} supply line is good to add.
- Keep loop VB_pin – HB_pin – C_{boot} as small as possible (locate C_{boot} as close to the IC as possible). The IC featured high current capability driver. Any parasitic inductance in this path will result in slow Q_HI turn on and voltage drop on VB pin which can result in UVLO activation.
- To limit bootstap switching current from the C_{VCC} it is recommended to add a resistor in serial with bootstrap diode. The resistor also protect HS driver against overvoltage on V_B – HB pins in case of negative spikes on HB pin.
- Do not let high current flow through trace between GND_pin and C_{VCC}.Even a small parasitic inductance here will create high voltage drop if high current flows through this path. This voltage is added or subtracted from HIN, LIN and EN signal, which results in incorrect thresholds or device damaging.
- Keep loops DRVL_pin – Q_LO – GND_pin and DRVH_pin – Q_HI – HB_pin as small as possible. A high parasitic inductance in these paths will result in slow MOSFET switching and undesired resonance on gate terminal.
- The high side driver is jumping up and down with high dV/dt at high frequency. The generated noise can influence devices and traces around. Do not place low voltage and sensitive traces into the vicinity of this HV node.

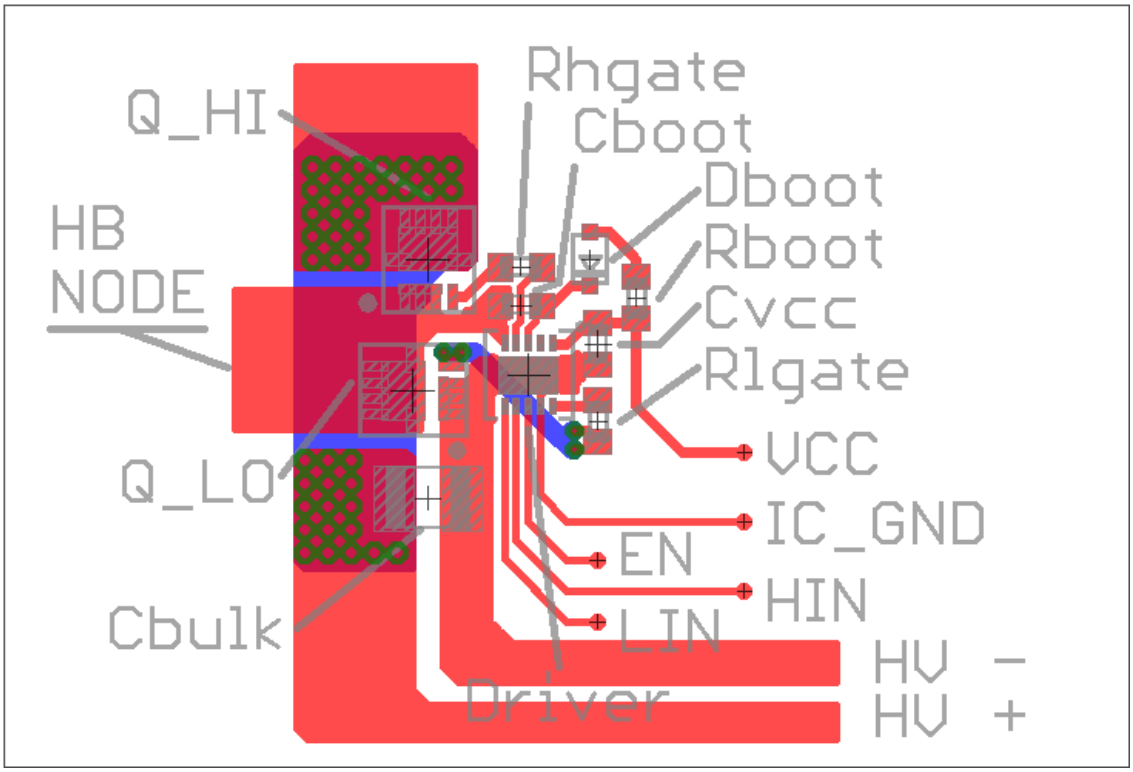
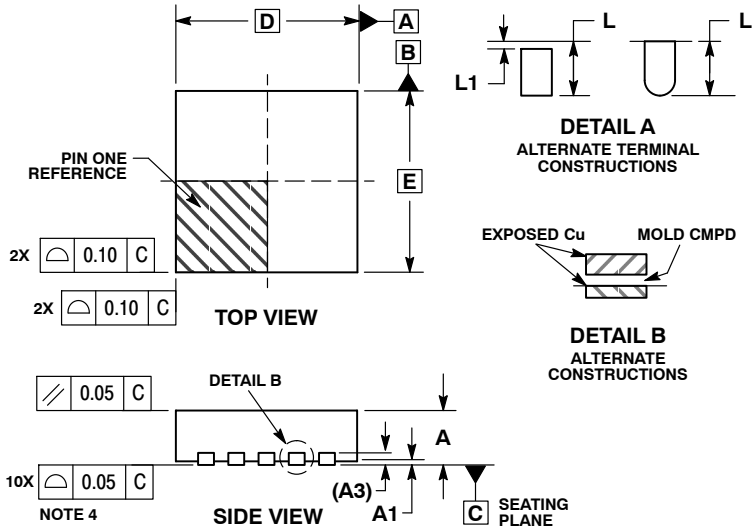


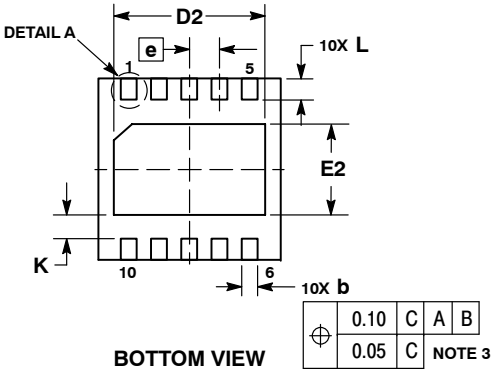
Figure 50. Recommended Layout

DFN10, 3x3, 0.5P
CASE 506CL
ISSUE O

DATE 02 APR 2013

SCALE 2:1





NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. TERMINAL b MAY HAVE MOLD COMPOUND MATERIAL ALONG SIDE EDGE. MOLD FLASHING MAY NOT EXCEED 30 MICRONS ONTO BOTTOM SURFACE OF TERMINAL b.
6. FOR DEVICE OPN CONTAINING W OPTION, DETAIL B ALTERNATE CONSTRUCTION IS NOT APPLICABLE.

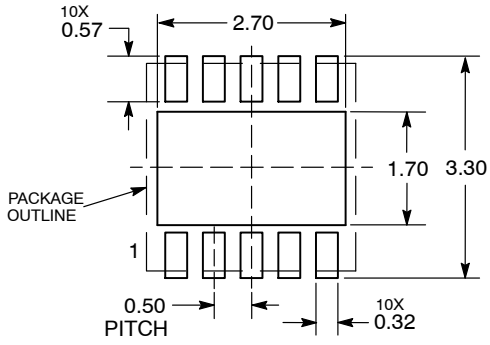
	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	3.00 BSC	
D2	2.40	2.60
E	3.00 BSC	
E2	1.40	1.60
e	0.50 BSC	
K	0.25	---
L	0.25	0.45
L1	0.00	0.03

GENERIC MARKING DIAGRAM*

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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