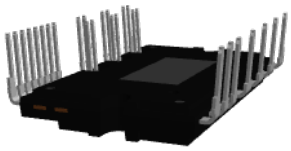
ASPM 27 Series

3−Phase 650 V, 40 A Automotive Smart Power Module

NFVA34065L32



3D Package Drawing
(Click to Activate 3D Content)

ASPM27−CCA
CASE MODCB

General Description

NFVA34065L32 is an advanced Automotive SPM® module providing a fully−featured, high−performance inverter output stage for hybrid and electric vehicles. These modules integrate optimized gate drive of the built−in IGBTs to minimize EMI and losses, while also providing multiple on−module protection features including under−voltage lockouts, over−current shutdown, thermal monitoring of drive IC, and fault reporting. The built−in, high−speed HVIC requires only a single supply voltage and translates the incoming logic−level gate inputs to the high−voltage, high−current drive signals required to properly drive the module's internal IGBTs. Separate negative IGBT terminals are available for each phase to support the widest variety of control algorithms.

Features

- Automotive SPM in 27 Pin DIP Package
- AEC & AQG324 Qualified and PPAP Capable
- 650 V/40 A 3−Phase IGBT Inverter with Integral Gate Drivers and Protections
- 175°C Guaranteed Short−Circuit Rated FS Trench IGBTs with Low Vce(sat) and Fast Switching
- Outstanding Thermal Resistance Using AI_2O_3 DBC Substrate
- Separated Open−Emitter Pins from Low−Side IGBTs for Three−Phase Current Sensing
- Single−Grounded Power Supply
- LVIC Temperature−Sensing Built−In for Temperature Monitoring
- Isolation Rating: 2500 V_{rms}/1 min.
- Pb−Free and RoHS Compliant
- UI1557 Certified (File No. E209204) and UL94V−0 Compliant

Applications

- Automotive high voltage auxiliary motors
  - Climate e−Compressors
  - Oil/Water Pumps
  - Super/Turbo Chargers
  - Variety Fans

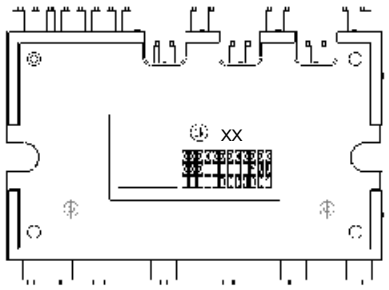
Related Resources

- AND9800 − Automotive Smart Power Module, 650 V ASPM27 Series
- AN−9086 − SPM 3 Package Mounting Guidance

Integrated Power Functions

- 650 V−40 A IGBT inverter for three−phase DC/AC power conversion (Refer to Figure 2)

MARKING DIAGRAM



ON	= **onsemi** Logo
XX	= Version and Current Rate
XXXXXXXXXXXX	= Specific Device Code
XXX	= Lot Number
Y	= Year
WW	= Work Week
0000001	= Serial Number

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

Integrated Drive, Protection and System Control Functions

- For inverter high−side IGBTs: gate drive circuit, high−voltage isolated high−speed level shifting control circuit, Under−Voltage Lock−Out (UVLO) protection
- For inverter low−side IGBTs: gate drive circuit, Short−Circuit Protection (SCP) control circuit, Under−Voltage Lock−Out Protection (UVLO)
- Fault signaling: corresponding to UVLO (low−side supply) and SC faults
- Input interface: active−HIGH interface, works with 3.3/5 V logic, Schmitt−trigger input

PIN CONFIGURATION

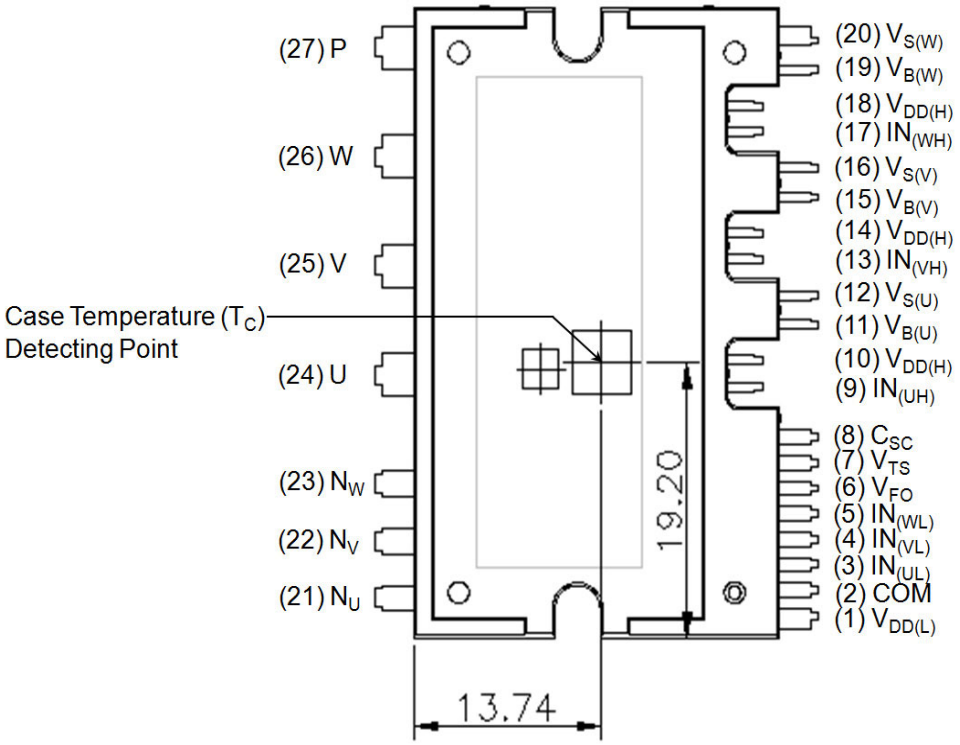
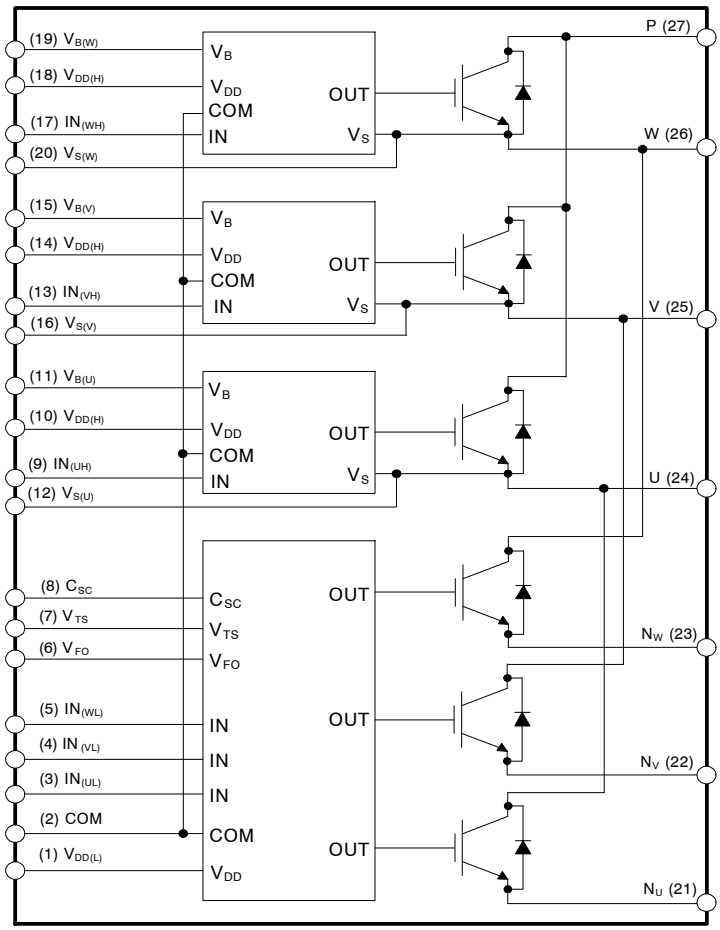


Figure 1. Top View

PIN DESCRIPTIONS

Pin Number	Pin Name	Pin Description
1	$V_{DD(L)}$	Low−Side Common Bias Voltage for IC and IGBTs Driving
2	COM	Common Supply Ground
3	$IN_{(UL)}$	Signal Input for Low−Side U−Phase
4	$IN_{(VL)}$	Signal Input for Low−Side V−Phase
5	$IN_{(WL)}$	Signal Input for Low−Side W−Phase
6	V_{FO}	Fault Output
7	V_{TS}	Output for LVIC Temperature Sensing Voltage Output
8	C_{SC}	Shut Down Input for Short−Circuit Current Detection Input
9	$IN_{(UH)}$	Signal Input for High−Side U−Phase
10	$V_{DD(H)}$	High−Side Common Bias Voltage for IC and IGBTs Driving
11	$V_{B(U)}$	High−Side Bias Voltage for U−Phase IGBT Driving
12	$V_{S(U)}$	High−Side Bias Voltage Ground for U−Phase IGBT Driving
13	$IN_{(VH)}$	Signal Input for High−Side V−Phase
14	$V_{DD(H)}$	High−Side Common Bias Voltage for IC and IGBTs Driving
15	$V_{B(V)}$	High−Side Bias Voltage for V−Phase IGBT Driving
16	$V_{S(V)}$	High−Side Bias Voltage Ground for V−Phase IGBT Driving
17	$IN_{(WH)}$	Signal Input for High−Side W−Phase
18	$V_{DD(H)}$	High−Side Common Bias Voltage for IC and IGBTs Driving
19	$V_{B(W)}$	High−Side Bias Voltage for W−Phase IGBT Driving
20	$V_{S(W)}$	High−Side Bias Voltage Ground for W−Phase IGBT Driving
21	N_U	Negative DC−Link Input for U−Phase
22	N_V	Negative DC−Link Input for V−Phase
23	N_W	Negative DC−Link Input for W−Phase
24	U	Output for U−Phase
25	V	Output for V−Phase
26	W	Output for W−Phase
27	P	Positive DC−Link Input

INTERNAL EQUIVALENT CIRCUIT AND INPUT/OUTPUT PINS



NOTES:
1. Inverter low−side is composed of three IGBTs, freewheeling diodes for each IGBT, and one control IC. It has gate drive and protection functions.
2. Inverter power side is composed of four inverter DC−link input terminals and three inverter output terminals.
3. Inverter high−side is composed of three IGBTs, freewheeling diodes, and three drive ICs for each IGBT.

Figure 2. Internal Block Diagram

ABSOLUTE MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Rating	Unit
INVERTER PART				
V_{PN}	Supply Voltage	Applied between P–N_U, N_V, N_W	500	V
$V_{PN(Surge)}$	Supply Voltage (Surge)	Applied between P–N_U, N_V, N_W	550	V
V_{CES}	Collector–Emitter Voltage		650	V
$\pm I_C$	Each IGBT Collector Current	T_C = 100°C, $V_{DD} \geq$ 15 V, $T_J \leq$ 175°C (Note 4)	40	A
$\pm I_{CP}$	Each IGBT Collector Current (Peak)	T_C = 25°C, $T_J \leq$175°C, Under 1 ms Pulse Width (Note 4)	80	A
P_C	Collector Dissipation	T_C = 25°C per One Chip (Note 4)	107	W
T_J	Operating Junction Temperature	IGBT and Diode	–40~175	°C
		Driver IC	–40~150	
CONTROL PART				
V_{DD}	Control Supply Voltage	Applied between $V_{DD(H)}$, $V_{DD(L)}$ –COM	20	V
V_{BS}	High–Side Control Bias Voltage	Applied between $V_{B(U)}$–$V_{S(U)}$, $V_{B(V)}$–$V_{S(V)}$, $V_{B(W)}$–$V_{S(W)}$	20	V
V_{IN}	Input Signal Voltage	Applied between $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$, $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$ –COM	–0.3~V_{DD}+0.3	V
V_{FO}	Fault Output Supply Voltage	Applied between V_{FO} –COM	–0.3~V_{DD}+0.3	V
I_{FO}	Fault Output Current	Sink Current at V_{FO} pin	2	mA
V_{SC}	Current Sensing Input Voltage	Applied between C_{SC} –COM	–0.3~V_{DD}+0.3	V
TOTAL SYSTEM				
t_{SC}	Short Circuit Withstand Time	V_{DD} = $V_{BS} \leq$ 16.5 V, $V_{PN} \leq$ 400 V, T_J = 150°C Non–repetitive	3	μs
T_{STG}	Storage Temperature		–55~175	°C
V_{ISO}	Isolation Voltage	60 Hz, Sinusoidal, AC 1 minute, Connection Pins to Heat Sink Plate	2500	V_{rms}

THERMAL RESISTANCE

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$R_{th(j-c)Q}$	Junction to Case Thermal Resistance (Note 5)	Inverter IGBT part (per 1/6 module)	–	–	1.40	°C/W
$R_{th(j-c)F}$		Inverter FWD part (per 1/6 module)	–	–	2.20	°C/W
L_σ	Package Stray Inductance	P to N_U, N_V, N_W (Note 5)	–	24	–	nH

4. These values had been made an acquisition by the calculation considered to design factor.
5. For the measurement point of case temperature (T_C), please refer to Figure 1. DBC discoloration and Picker Circle Printing allowed, please refer to application note AN–9190 (Impact of DBC Oxidation on SPM® Module Performance).
6. Stray inductance per phase measured per IEC 60747–15.

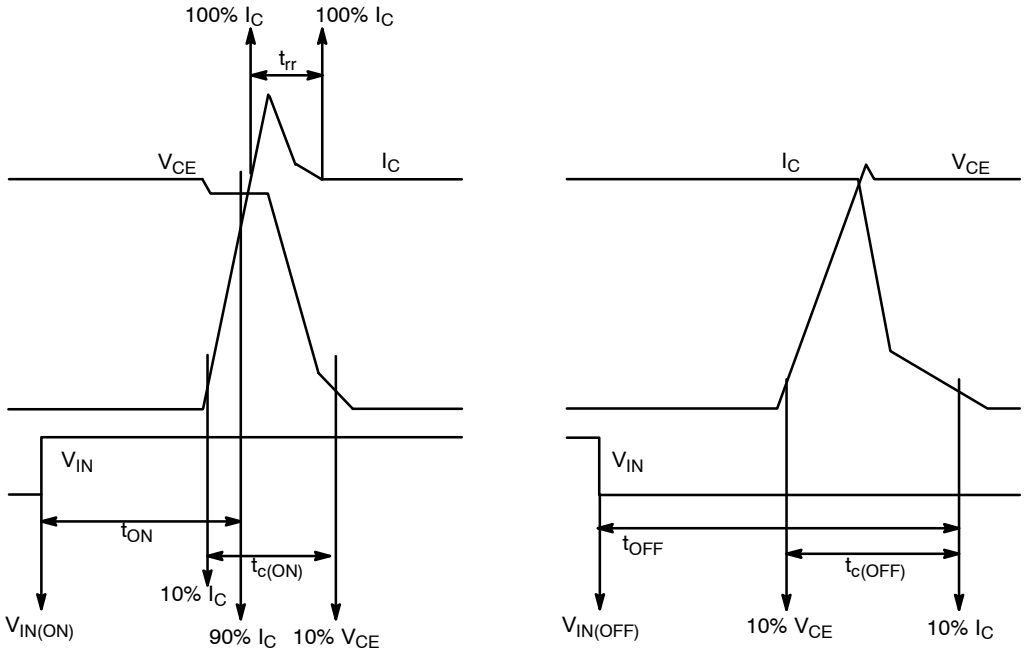
ELECTRICAL CHARACTERISTICS – INVERTER PART (T_J as specified)

Symbol		Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{CE(SAT)}$		Collector – Emitter Saturation Voltage	$V_{DD} = V_{BS}$ = 15 V, V_{IN} = 5 V, I_C = 40 A, T_J = 25°C	–	1.50	2.05	V
			$V_{DD} = V_{BS}$ = 15 V, V_{IN} = 5 V, I_C = 40 A, T_J = 175°C		1.90	2.50	V
V_F		FWDi Forward Voltage	V_{IN} = 0 V, I_F = 40 A, T_J = 25°C	–	1.75	2.35	V
			V_{IN} = 0 V, I_F = 40 A, T_J = 175°C		1.70	2.30	V
HS	t_{ON}	High Side Switching Times	V_{PN} = 300 V, V_{DD} = 15 V, I_C = 40 A, T_J = 25°C V_{IN} = 0 V ⇔ 5 V, Inductive Load See Figure 5 (Note 7)	0.75	1.15	1.75	μs
	$t_{C(ON)}$			–	0.25	0.75	μs
	t_{OFF}			–	1.20	1.70	μs
	$t_{C(OFF)}$			–	0.15	0.50	μs
	t_{rr}			–	0.14	–	μs
LS	t_{ON}	Low Side Switching Times	V_{PN} = 300 V, V_{DD} = 15 V, I_C = 40 A, T_J = 25°C V_{IN} = 0 V ⇔ 5 V, Inductive Load See Figure 5 (Note 7)	0.60	1.00	1.60	μs
	$t_{C(ON)}$			–	0.25	0.70	μs
	t_{OFF}			–	1.25	1.75	μs
	$t_{C(OFF)}$			–	0.20	0.55	μs
	t_{rr}			–	0.14	–	μs
I_{CES}		Collector–Emitter Leakage Current	T_J = 25°C, V_{CE} = V_{CES}	–	–	3	mA

7. t_{ON} and t_{OFF} include the propagation delay time of the internal drive IC. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching time of IGBT itself under the given gate driving condition internally. For the detailed information see Figure 3.

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Shipping
NFVA34065L32	NFVA34065L32	ASPM27−CCA	10 Units/Tube



(a) turn – on **(b) turn – off**

Figure 3. Switching Time Definition

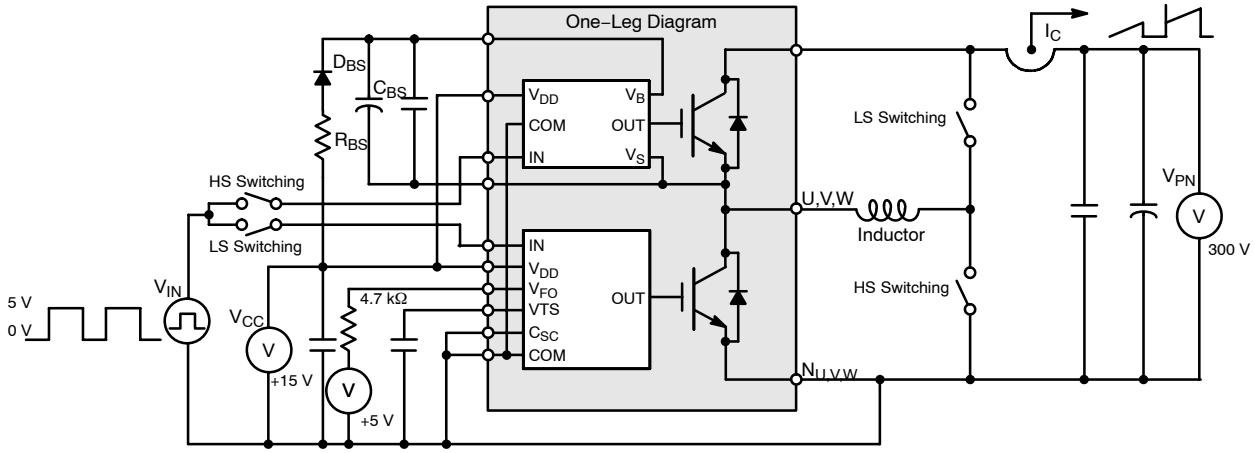


Figure 4. Example Circuit for Switching Test

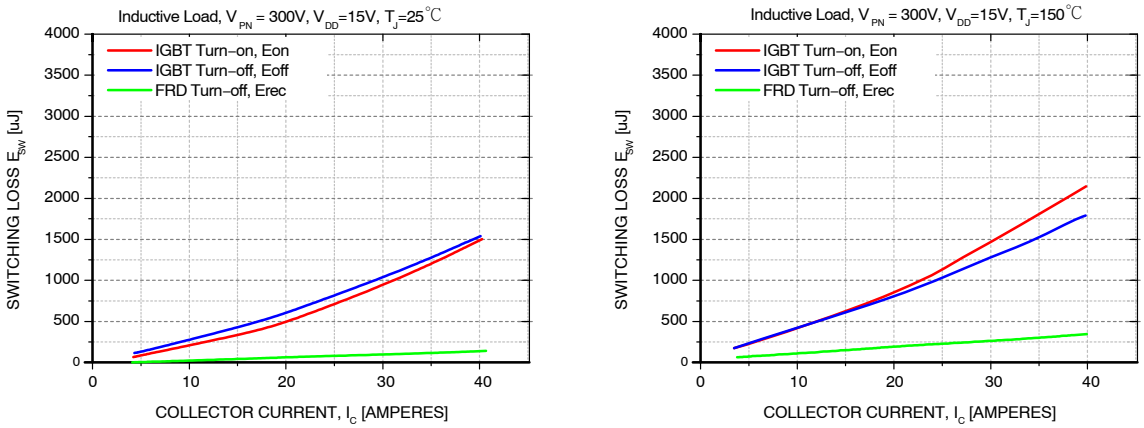


Figure 5. Switching Loss Characteristics

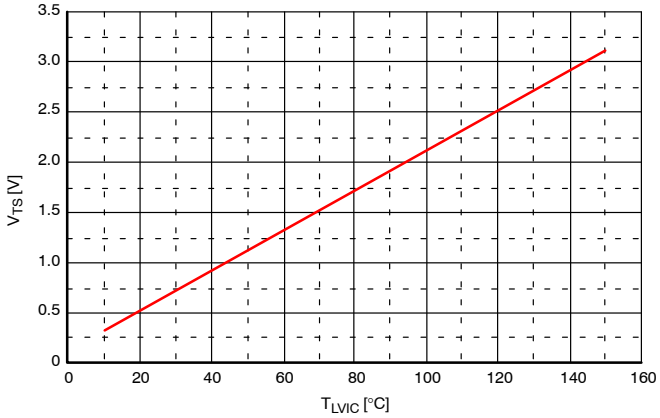


Figure 6. Temperature Profile of V_{TS} (Typical)

CONTROL PART (T_J = 25°C)

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
I_{QDDH}	Quiescent V_{DD} Supply Current	$V_{DD(H)}$ = 15 V, $IN_{(UH,VH.WH)}$ = 0 V	$V_{DD(H)}$ – COM	–	–	0.40	mA
I_{QDDL}		$V_{DD(L)}$ = 15 V, $IN_{(UL,VL.WL)}$ = 0 V	$V_{DD(L)}$ – COM	–	–	4.80	mA
I_{PDDH}	Operating V_{DD} Supply Current	$V_{DD(H)}$ = 15 V, f_{PWM} = 20 kHz, duty = 50%, applied to one PWM signal input for High–Side	$V_{DD(H)}$ – COM	–	–	0.48	mA
I_{PDDL}		$V_{DD(L)}$ = 15 V, f_{PWM} = 20 kHz, duty = 50%, applied to one PWM signal input for Low–Side	$V_{DD(L)}$ – COM	–	–	8.80	mA
I_{QBS}	Quiescent V_{BS} Supply Current	V_{BS} = 15 V, $IN_{(UH,VH.WH)}$ = 0 V	$V_{B(U)} - V_{S(U)}$, $V_{B(V)} - V_{S(V)}$, $V_{B(W)} - V_{S(W)}$,	–	–	0.24	mA
I_{PBS}	Operating V_{BS} Supply Current	V_{DD} = V_{BS} = 15 V, f_{PWM} = 20 kHz, duty = 50%, applied to one PWM signal input for High–Side	$V_{B(U)} - V_{S(U)}$, $V_{B(V)} - V_{S(V)}$, $V_{B(W)} - V_{S(W)}$,	–	–	4.40	mA
V_{FOH}	Fault Output Voltage	V_{DD} = 15 V, V_{SC} = 0 V, V_{FO} Circuit: 4.7 kΩ to 5 V Pull–up		4.5	–	–	V
V_{FOL}		V_{DD} = 15 V, V_{SC} = 1 V, V_{FO} Circuit: 4.7 kΩ to 5 V Pull–up		–	–	0.50	V
$V_{SC(ref)}$	Short Circuit Trip Level	V_{DD} = 15 V (Note 8)	C_{SC} – $COM_{(L)}$	0.45	0.50	0.55	V
UV_{DDD}	Supply Circuit Under–Voltage Protection	Detection Level		9.80	–	13.3	V
UV_{DDR}		Reset Level		10.3	–	13.8	V
UV_{BSD}		Detection Level		9.00	–	12.5	V
UV_{BSR}		Reset Level		9.50	–	13.0	V
t_{FOD}	Fault–Out Pulse Width			50	–	–	μs
V_{TS}	LVIC Temperature Sensing Voltage Output	$V_{DD(L)}$ = 15 V, T_{LVIC} = 25°C (Note 9) See Figure 6		540	640	740	mV
$V_{IN(ON)}$	ON Threshold Voltage	Applied between $IN_{(UH,VH.WH)}$ – COM $IN_{(UL,VL.WL)}$ – COM		–	–	2.60	V
$V_{IN(OFF)}$	OFF Threshold Voltage			0.80	–	–	V

8. Short–circuit current protection os functioning only at the low–sides.
9. T_{LVIC} is the temperature of LVIC itself. V_{TS} is only for sensing temperature of LVIC and can not shutdown IGBTs automatically.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{PN}	Supply Voltage	Applied between P – N_U, N_V, N_W	–	300	400	V
V_{DD}	Control Supply Voltage	Applied between $V_{DD(H)}$ – COM, $V_{DD(L)}$ – COM	14.0	15	16.5	V
V_{BS}	High–Side Bias Voltage	Applied between $V_{B(U)} - V_{S(U)}$, $V_{B(V)} - V_{S(V)}$, $V_{B(W)} - V_{S(W)}$	13.0	15	18.5	V
dV_{DD}/dt, dV_{BS}/dt,	Control Supply Variation		–1	–	1	V/μs
t_{dead}	Blanking Time for Preventing Arm–Short	For Each Input Signal	2.0	–	–	μs
f_{PWM}	PWM Input Signal	–40°C ≤ T_C ≤ 125°C, –40°C ≤ T_J ≤ 150°C	–	–	20	kHz
V_{SEN}	Voltage for Current Sensing	Applied between N_U, N_V, N_W – COM (Including Surge Voltage)	–5	–	5	V

RECOMMENDED OPERATING CONDITIONS (continued)

$PW_{IN(ON)}$	Minimum Input Pulse Width	$V_{DD} = V_{BS}$ = 15 V, $I_C \le 40$ A, Wiring Inductance between $N_{U,V,W}$ and DC Link N < 10 nH (Note 10)	2.0	–	–	μs
$PW_{IN(OFF)}$			2.0	–	–	
$PW_{IN(ON)}$		$V_{DD} = V_{BS}$ = 15 V, 40 A $\le I_C \le$ 80 A, Wiring Inductance between $N_{U,V,W}$ and DC Link N < 10 nH (Note 10)	2.5	–	–	μs
$PW_{IN(OFF)}$			2.5	–	–	
T_J	Junction Temperature		−40	–	150	°C

10. This product might not make response if input pulse width is less than the recommended value.

MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Conditions		Value			Unit
			Min.	Typ.	Max.	
Device Flatness	See Figure 7		0	–	+150	μm
Mounting Torque	Mounting Screw: M3 See Figure 8	Recommended 0.7 N•m	0.6	0.7	0.8	N•m
		Recommended 7.1 kg•cm	6.2	7.1	8.1	kg•cm
Terminal Pulling Strength	Load 19.8 N		10	–	–	s
Terminal Bending Strength	Load 9.8 N 90 deg. bend		2	–	–	times
Weight			–	15	–	g

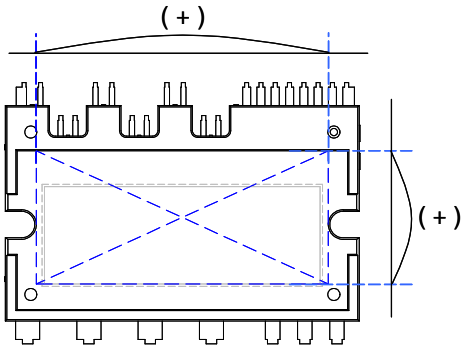
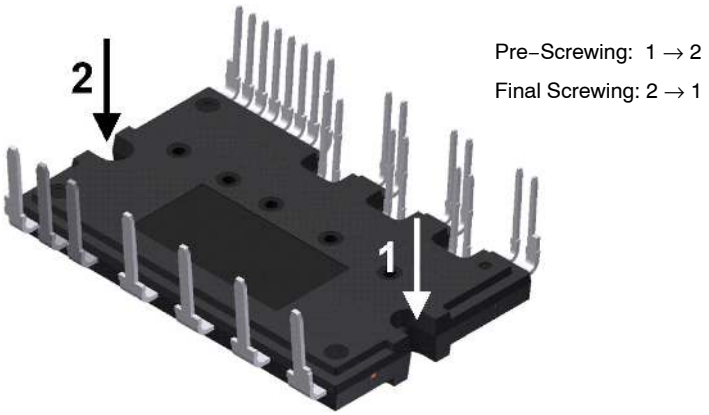


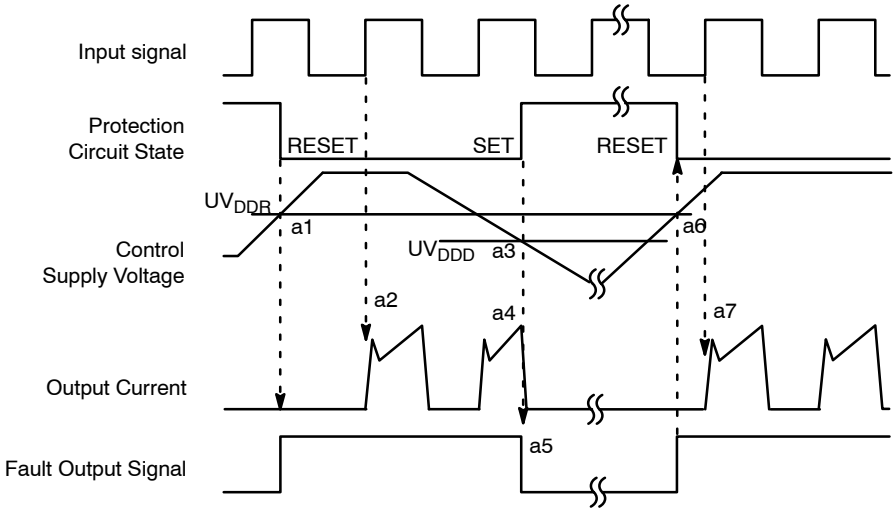
Figure 7. Flatness Measurement Position



NOTES:

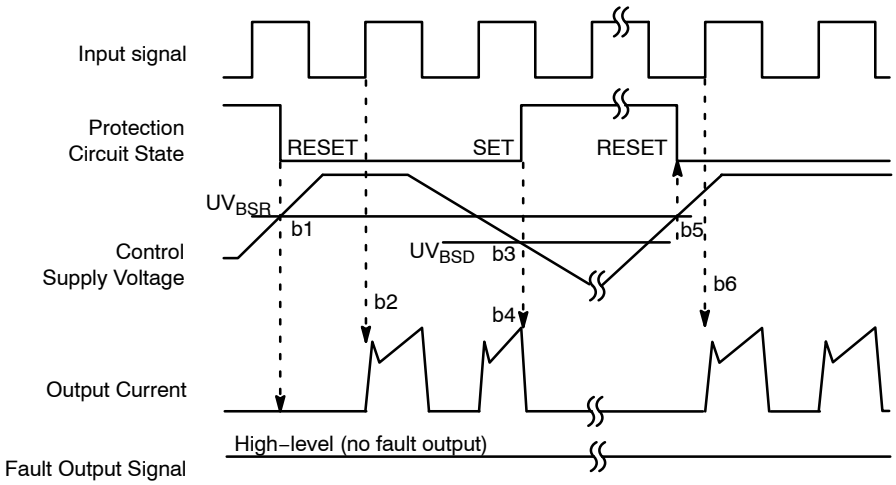
11. Do not make over torque when mounting screws. Much mounting torque may cause DBC cracks, as well as bolts and Al heat−sink destruction
12. Avoid one−sided tightening stress. Figure 8 shows the recommended torque order for mounting screws. Uneven mounting can cause the DBC substrate of package to be damaged. The pre−screwing torque is set to 20 ~ 30% of maximum torque rating.

Figure 8. Mounting Screws Torque Order



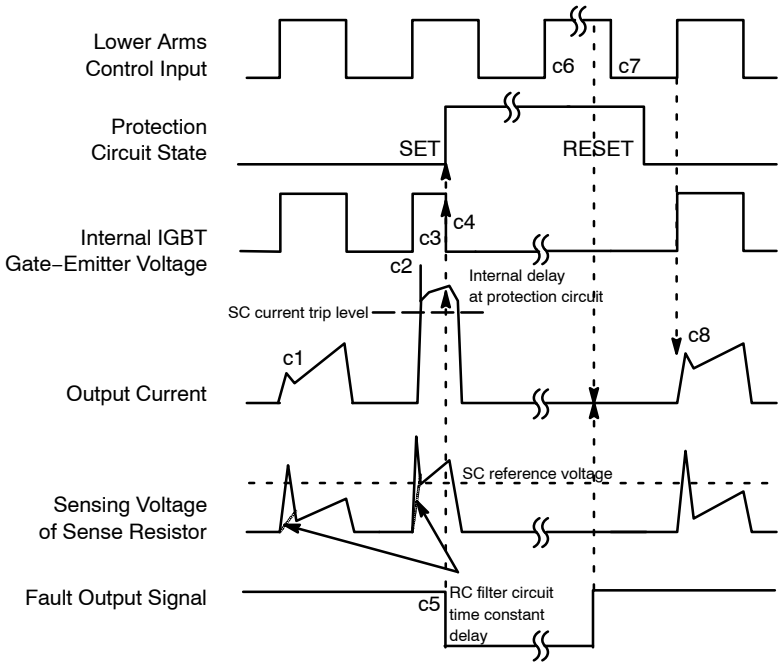
a1: Control supply voltage rises: After the voltage rises UV_{DDR}, the circuits start to operate when next input is applied.
a2: Normal operation: IGBT ON and carrying current.
a3: Under voltage detection (UV_{DDD}).
a4: IGBT OFF in spite of control input condition.
a5: Fault output operation starts with a fixed pulse width.
a6: Under voltage reset (UV_{DDR}).
a7: Normal operation: IGBT ON and carrying current by triggering next signal from LOW to HIGH.

Figure 9. Under−Voltage Protection (Low−Side)



b1: Control supply voltage rises: After the voltage rises UV_{BSR}, the circuits start to operate when next input is applied.
b2: Normal operation: IGBT ON and carrying current.
b3: Under voltage detection (UV_{BSD}).
b4: IGBT OFF in spite of control input condition, but there is no fault output signal.
b5: Under voltage reset (UV_{BSR}).
b6: Normal operation: IGBT ON and carrying current by triggering next signal from LOW to HIGH.

Figure 10. Under−Voltage Protection (High−Side)



(with the external sense resistance and RC filter connection)

c1: Normal operation: IGBT ON and carrying current.

c2: Short circuit current detection (SC trigger).

c3: All low−side IGBT's gate are hard interrupted.

c4: All low−side IGBTs turn OFF.

c5: Fault output operation starts with a fixed pulse width.

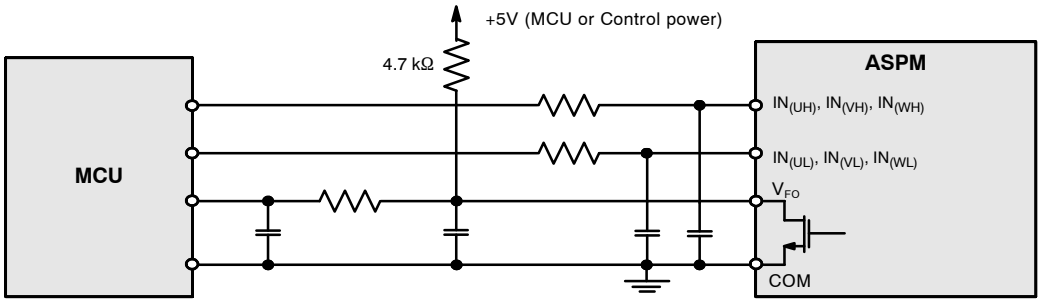
c6: Input HIGH: IGBT ON state, but during the active period of fault output the IGBT doesn't turn ON.

c7: Fault output operation finishes, but IGBT doesn't turn on until triggering next signal from LOW to HIGH.

c8: Normal operation: IGBT ON and carrying current.

Figure 11. Short−Circuit Current Protection (Low−Side Operation Only)

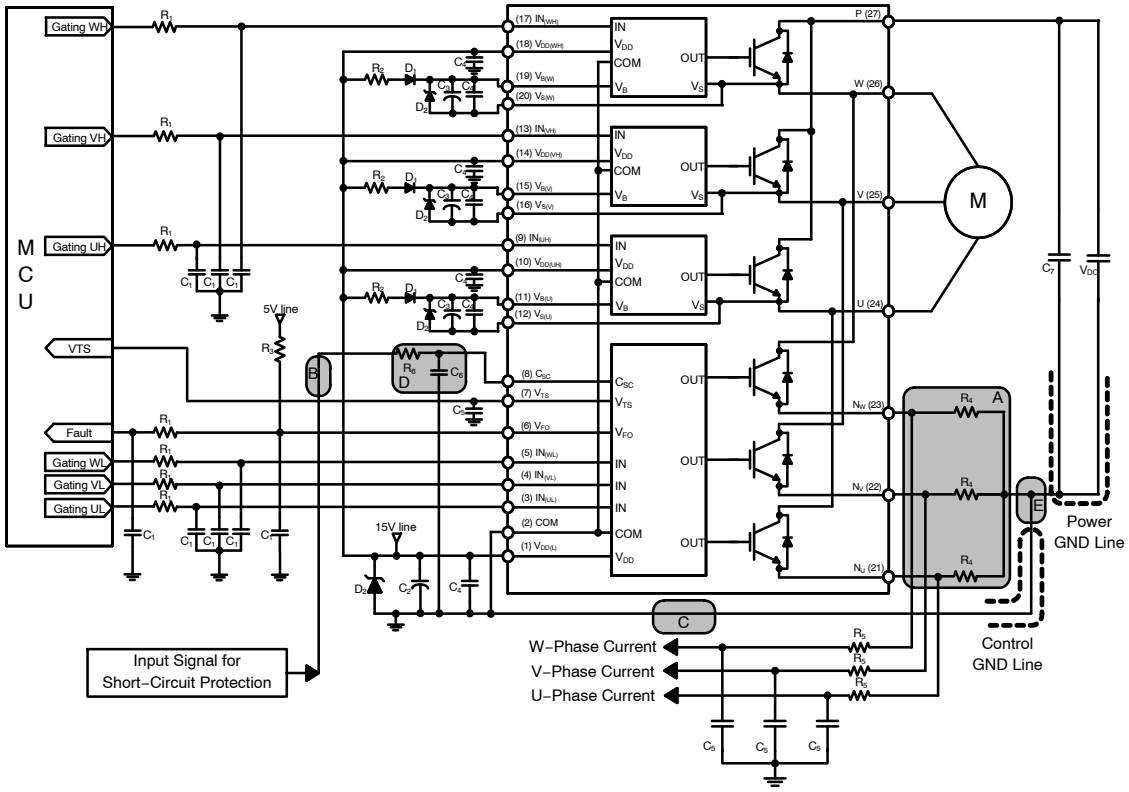
INPUT/OUTPUT INTERFACE CIRCUIT



NOTE:

13. RC coupling at each input might change depending on the PWM control scheme used in the application and the wiring impedance of the application's printed circuit board. The input signal section of the ASPM27 product integrates 5kΩ (typ.) pull−down resistor. Therefore, when using an external filtering resistor, please pay attention to the signal voltage drop at input terminal.

Figure 12. Recommended CPU I/O Interface Circuit



NOTES:

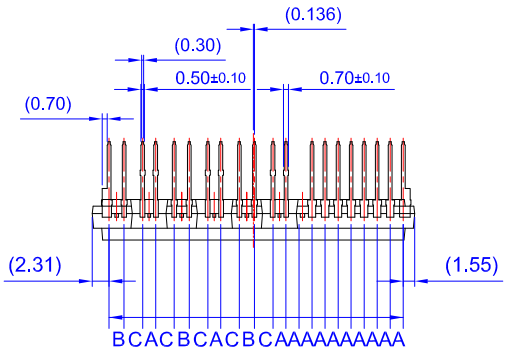
14. To avoid malfunction, the wiring of each input should be as short as possible. (less than 2−3 cm)
15. V_{FO} output is open−drain type. The signal line should be pulled up to the positive side of the MCU or control power supply with a resistor that makes I_{FO} up to 2mA. Refer to Figure 12.
16. Input signal is active−HIGH type. There is a 5 kΩ resistor inside the IC to pull−down each input signal line to GND. RC coupling circuits should be adopted for the prevention of input signal oscillation. R_1C_1 time constant should be selected in the range 50~150 ns. (Recommended R_1 = 100 Ω, C_1 = 1 nF)
17. Each wiring pattern inductance of A point should be minimized (Recommended less than 10 nH). Use the shunt resistor R_4 of surface mounted (SMD) type to reduce wiring inductance. To prevent malfunction, wiring of point E should be connected to the terminal of the shunt resistor R_4 as close as possible.
18. To prevent errors of the protection function, the wiring of B, C and D point should be as short as possible.
19. In the short−circuit protection circuit, please select the R_6C_6 time constant in the range 1.5~2 μs.
20. Each capacitor should be mounted as close to the pins of the ASPM27 product as possible.
21. To prevent surge destruction, the wiring between the smoothing capacitor C_7 and the P & GND pins should be as short as possible. The use of a high−frequency non−inductive capacitor between the P & GND pins is recommended.
22. Relays are used at almost every systems of electrical equipment at industrial application. In these cases, there should be sufficient distance between the CPU and the relays.
23. The zener diode or transient voltage suppressor should be adopted for the protection of ICs from the surge destruction between each pair of control supply terminals (Recommended zener diode is 22 V/1 W. which has the lower zener impedance characteristic than about 15 Ω).
24. C_2 of around 7 times larger than bootstrap capacitor C_3 is recommended.
25. Choose the electrolytic capacitor with good temperature characteristic in C_3. Also choose 0.1~0.2 μF R−category ceramic capacitors with good temperature and frequency characteristics in C_4.

Figure 13. Typical Application Circuit

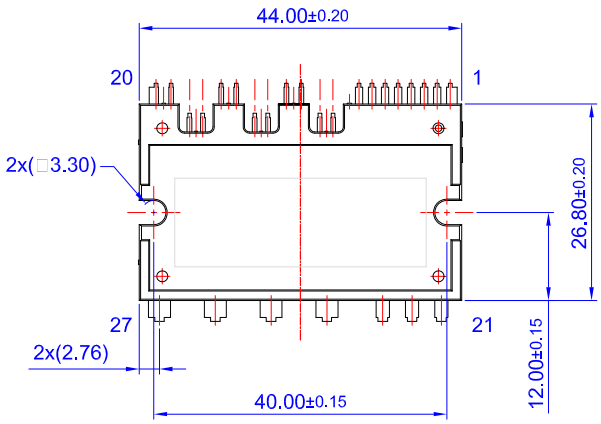
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

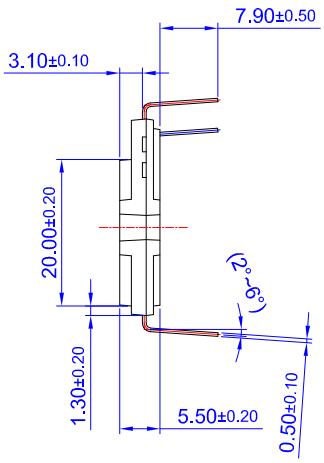
27LD MODULE PDD STD
CASE MODCB
ISSUE A

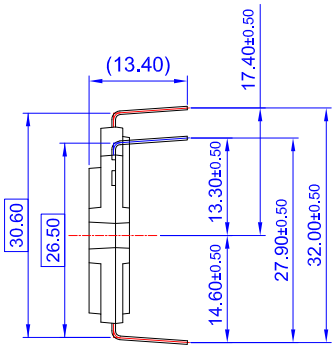
DATE 30 JAN 2023

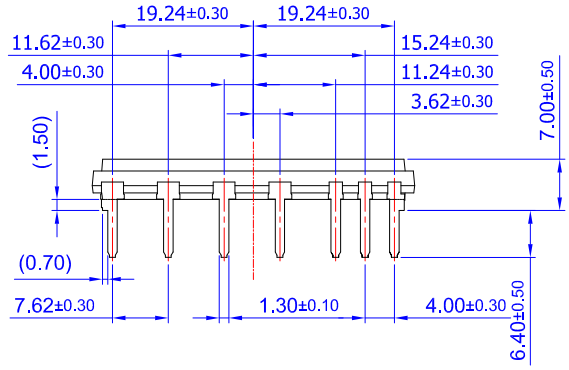


LEAD PITCH (TOLERANCE : ±0.30)
A : 1.778
B : 2.050
C : 2.531









NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE DOES NOT COMPLY TO ANY CURRENT PACKAGING STANDARD
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
D) ( ) IS REFERENCE

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