CY7C1364C

9-Mbit (256 K × 32) Pipelined Sync SRAM

Features

- Registered inputs and outputs for pipelined operation
- 256 K × 32 common I/O architecture
- 3.3 V core power supply (V_{DD})
- 2.5 V/3.3 V I/O power supply (V_{DDQ})
- Fast clock-to-output times
  - 3.5 ns (for 166-MHz device)
- Provide high-performance 3-1-1-1 access rate
- User-selectable burst counter supporting Intel® Pentium® interleaved or linear burst sequences
- Separate processor and controller address strobes
- Synchronous self-timed writes
- Asynchronous output enable
- Available in 165-ball FBGA package
- “ZZ” Sleep Mode Option
- IEEE 1149.1 JTAG-compatible boundary scan

Functional Description

The CY7C1364C SRAM integrates 256 K × 32 SRAM cells with advanced synchronous peripheral circuitry and a two-bit counter for internal burst operation. All synchronous inputs are gated by registers controlled by a positive-edge-triggered Clock Input (CLK). The synchronous inputs include all addresses, all data inputs, address-pipelining Chip Enable ($\overline{CE_1}$), depth-expansion Chip Enables (CE_2 and $\overline{CE_3}$), Burst Control inputs ($\overline{ADSC}$, $\overline{ADSP}$, and $\overline{ADV}$), Write Enables ($\overline{BW}_{[A:D]}$, and $\overline{BWE}$), and Global Write ($\overline{GW}$). Asynchronous inputs include the Output Enable ($\overline{OE}$) and the ZZ pin.

Addresses and chip enables are registered at rising edge of clock when either Address Strobe Processor ($\overline{ADSP}$) or Address Strobe Controller ($\overline{ADSC}$) are active. Subsequent burst addresses can be internally generated as controlled by the Advance pin ($\overline{ADV}$).

Address, data inputs, and write controls are registered on-chip to initiate a self-timed Write cycle.This part supports Byte Write operations (see Pin Descriptions and Truth Table for further details). Write cycles can be one to four bytes wide as controlled by the Byte Write control inputs. $\overline{GW}$ when active LOW causes all bytes to be written.

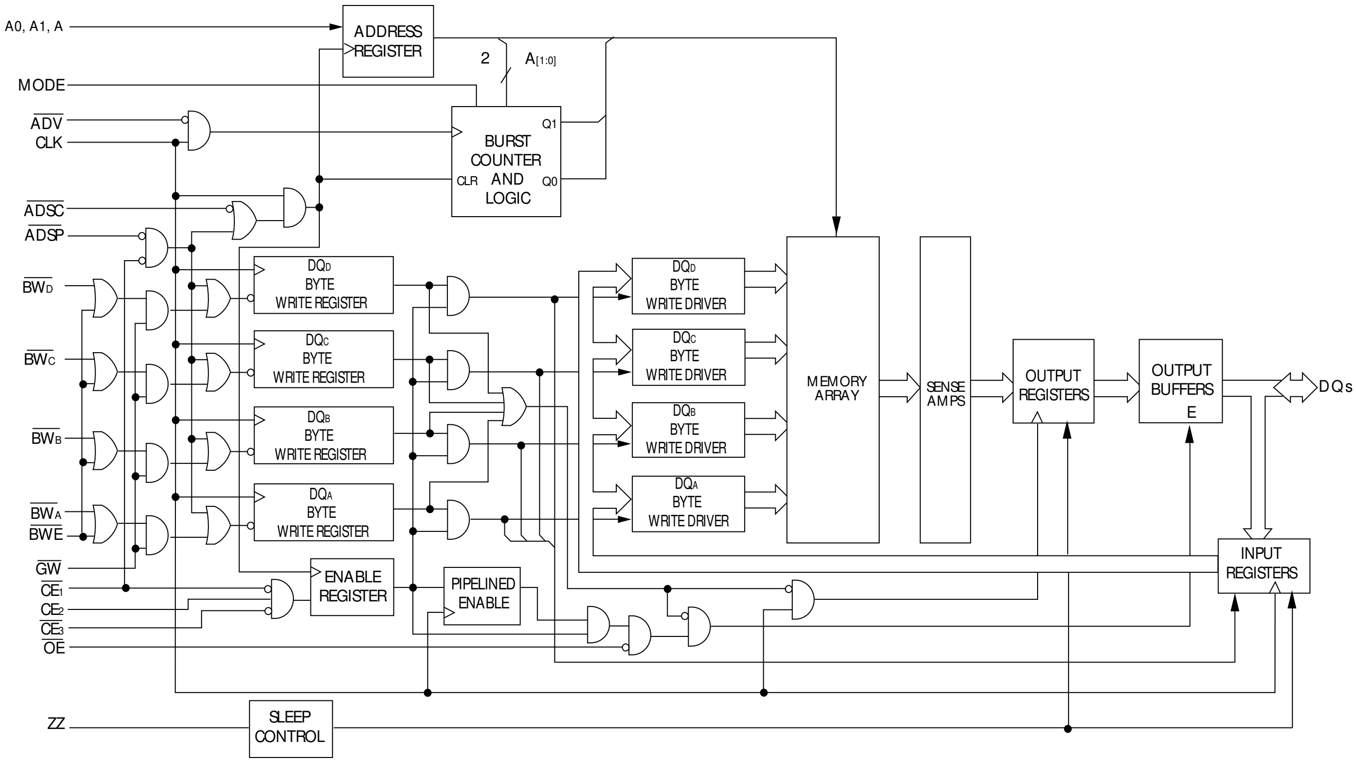
The CY7C1364C operates from a +3.3 V core power supply while all outputs may operate with either a +2.5 or +3.3 V supply. All inputs and outputs are JEDEC-standard JESD8-5-compatible.

For a complete list of related documentation, click here.

Selection Guide

Description	166 MHz	Unit
Maximum Access Time	3.5	ns
Maximum Operating Current	180	mA
Maximum CMOS Standby Current	40	mA

Logic Block Diagram – CY7C1364C



Contents

Pin Configurations

Figure 1. 165-ball FBGA (15 × 17 × 1.40 mm) pinout

CY7C1364C (256 K × 32)

	1	2	3	4	5	6	7	8	9	10	11
A	NC/288M	A	$\overline{CE_1}$	$\overline{BW_C}$	$\overline{BW_B}$	$\overline{CE_3}$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A	NC
B	NC/144M	A	CE2	$\overline{BW_D}$	$\overline{BW_A}$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A	NC/576M
C	NC	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC/1G	NC
D	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
E	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
F	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
G	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
H	NC	V_{SS}	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
K	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
L	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
M	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
N	NC	NC	V_{DDQ}	V_{SS}	NC	NC/18M	NC	V_{SS}	V_{DDQ}	NC	NC
P	NC	NC/72M	A	A	TDI	A1	TDO	A	A	A	A
R	MODE	NC/36M	A	A	TMS	A0	TCK	A	A	A	A

Pin Definitions

Name	I/O	Description
A_0, A_1, A	Input-Synchronous	**Address Inputs used to select one of the 256K address locations**. Sampled at the rising edge of the CLK if ADSP or ADSC is active LOW, and $\overline{CE}_1$, CE_2, and $\overline{CE}_3$ are sampled active. $A_{[1:0]}$ feed the 2-bit counter.
$\overline{BW}_A$, $\overline{BW}_B$, $\overline{BW}_C$, $\overline{BW}_D$	Input-Synchronous	**Byte Write Select Inputs, active LOW**. Qualified with $\overline{BWE}$ to conduct byte writes to the SRAM. Sampled on the rising edge of CLK.
$\overline{GW}$	Input-Synchronous	**Global Write Enable Input, active LOW**. When asserted LOW on the rising edge of CLK, a global Write is conducted (ALL bytes are written, regardless of the values on $\overline{BW}_{[A:D]}$ and $\overline{BWE}$).
$\overline{BWE}$	Input-Synchronous	**Byte Write Enable Input, active LOW**. Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a Byte Write.
CLK	Input-Clock	**Clock Input**. Used to capture all synchronous inputs to the device. Also used to increment the burst counter when $\overline{ADV}$ is asserted LOW, during a burst operation.
$\overline{CE}_1$	Input-Synchronous	**Chip Enable 1 Input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE}_3$ to select/deselect the device. $\overline{ADSP}$ is ignored if $\overline{CE}_1$ is HIGH. $\overline{CE}_1$ is sampled only when a new external address is loaded.
CE_2	Input-Synchronous	**Chip Enable 2 Input, active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ to select/deselect the device. CE_2 is sampled only when a new external address is loaded.
$\overline{CE}_3$	Input-Synchronous	**Chip Enable 3 Input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and CE_2 to select/deselect the device.$\overline{CE}_3$ is assumed active throughout this document for BGA. $\overline{CE}_3$ is sampled only when a new external address is loaded.
$\overline{OE}$	Input-Asynchronous	**Output Enable, asynchronous input, active LOW**. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins. $\overline{OE}$ is masked during the first clock of a Read cycle when emerging from a deselected state.
$\overline{ADV}$	Input-Synchronous	**Advance Input signal, sampled on the rising edge of CLK**, **active LOW**. When asserted, it automatically increments the address in a burst cycle.
$\overline{ADSP}$	Input-Synchronous	**Address Strobe from Processor, sampled on the rising edge of CLK, active LOW**. When asserted LOW, A is captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized. $\overline{ASDP}$ is ignored when $\overline{CE}_1$ is deasserted HIGH.
$\overline{ADSC}$	Input-Synchronous	**Address Strobe from Controller, sampled on the rising edge of CLK, active LOW**. When asserted LOW, A is captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized.
ZZ	Input-Asynchronous	**ZZ "sleep" Input, active HIGH**. This input, when High places the device in a non-time-critical "sleep" condition with data integrity preserved. For normal operation, this pin has to be LOW or left floating. ZZ pin has an internal pull-down.
DQs	I/O-Synchronous	**Bidirectional Data I/O lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by "A" during the previous clock rise of the Read cycle. The direction of the pins is controlled by $\overline{OE}$. When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, DQ are placed in a tri-state condition.
V_{DD}	Power Supply	**Power supply inputs to the core of the device**.
V_{SS}	Ground	**Ground for the core of the device**.
V_{DDQ}	I/O Power Supply	**Power supply for the I/O circuitry**.
V_{SSQ}	I/O Ground	**Ground for the I/O circuitry**.
MODE	Input-Static	**Selects Burst Order**. When tied to GND selects linear burst sequence. When tied to V_{DD} or left floating selects interleaved burst sequence. This is a strap pin and should remain static during device operation. Mode pin has an internal pull-up.
TDO	JTAG serial output synchronous	**Serial data-out to the JTAG circuit**. Delivers data on the negative edge of TCK. If the JTAG feature is not being used, this pin should be disconnected.

Pin Definitions (continued)

Name	I/O	Description
TDI	JTAG serial input synchronous	**Serial data-in to the JTAG circuit**. Sampled on the rising edge of TCK. If the JTAG feature is not being used, this pin can be disconnected or connected to V_{DD}.
TMS	JTAG serial input synchronous	**Serial data-in to the JTAG circuit**. Sampled on the rising edge of TCK. If the JTAG feature is not being used, this pin can be disconnected or connected to V_{DD}.
TCK	JTAG-clock	**Clock input to the JTAG circuitry**. If the JTAG feature is not being used, this pin must be connected to V_{SS}.
NC	–	**No Connects**. Not internally connected to the die.

Functional Overview

All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock.

The CY7C1364C supports secondary cache in systems utilizing either a linear or interleaved burst sequence. The interleaved burst order supports Pentium and i486™ processors. The linear burst sequence is suited for processors that utilize a linear burst sequence. The burst order is user selectable, and is determined by sampling the MODE input. Accesses can be initiated with either the Processor Address Strobe (ADSP) or the Controller Address Strobe (ADSC). Address advancement through the burst sequence is controlled by the ADV input. A two-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte Write operations are qualified with the Byte Write Enable (BWE) and Byte Write Select ($BW_{[A:D]}$) inputs. A Global Write Enable (GW) overrides all Byte Write inputs and writes data to all four bytes. All writes are simplified with on-chip synchronous self-timed Write circuitry.

Three synchronous Chip Selects (CE_1, CE_2, CE_3) and an asynchronous Output Enable (OE) provide for easy bank selection and output tri-state control. ADSP is ignored if CE_1 is HIGH.

Single Read Accesses

This access is initiated when the following conditions are satisfied at clock rise: (1) ADSP or ADSC is asserted LOW, (2) CE_1, CE_2, CE_3 are all asserted active, and (3) the Write signals (GW, BWE) are all deasserted HIGH. ADSP is ignored if CE_1 is HIGH. The address presented to the address inputs (A) is stored into the address advancement logic and the address register while being presented to the memory array. The corresponding data is allowed to propagate to the input of the output registers. At the rising edge of the next clock the data is allowed to propagate through the output register and onto the data bus within t_{CO} if OE is active LOW. The only exception occurs when the SRAM is emerging from a deselected state to a selected state, its outputs are always tri-stated during the first cycle of the access. After the first cycle of the access, the outputs are controlled by the OE signal. Consecutive single Read cycles are supported. Once the SRAM is deselected at clock rise by the chip select and either ADSP or ADSC signals, its output will tri-state immediately.

Single Write Accesses Initiated by ADSP

This access is initiated when both of the following conditions are satisfied at clock rise: (1) ADSP is asserted LOW, and (2) CE_1, CE_2, CE_3 are all asserted active. The address presented to A is loaded into the address register and the address advancement logic while being delivered to the RAM array. The Write signals (GW, BWE, and $BW_{[A:D]}$) and ADV inputs are ignored during this first cycle.

ADSP-triggered Write accesses require two clock cycles to complete. If GW is asserted LOW on the second clock rise, the data presented to the DQ inputs is written into the corresponding address location in the memory array. If GW is HIGH, then the Write operation is controlled by BWE and $BW_{[A:D]}$ signals. The CY7C1364C provides Byte Write capability that is described in the Write Cycle Descriptions table. Asserting the Byte Write Enable input (BWE) with the selected Byte Write ($BW_{[A:D]}$) input, will selectively write to only the desired bytes. Bytes not selected during a Byte Write operation will remain unaltered. A synchronous self-timed Write mechanism has been provided to simplify the Write operations.

Because the CY7C1364C is a common I/O device, the Output Enable (OE) must be deasserted HIGH before presenting data to the DQ inputs. Doing so will tri-state the output drivers. As a safety precaution, DQ are automatically tri-stated whenever a Write cycle is detected, regardless of the state of OE.

Single Write Accesses Initiated by ADSC

ADSC Write accesses are initiated when the following conditions are satisfied: (1) ADSC is asserted LOW, (2) ADSP is deasserted HIGH, (3) CE_1, CE_2, CE_3 are all asserted active, and (4) the appropriate combination of the Write inputs (GW, BWE, and $BW_{[A:D]}$) are asserted active to conduct a Write to the desired byte(s). ADSC-triggered Write accesses require a single clock cycle to complete. The address presented to A is loaded into the address register and the address advancement logic while being delivered to the memory array. The ADV input is ignored during this cycle. If a global Write is conducted, the data presented to the DQ is written into the corresponding address location in the memory core. If a Byte Write is conducted, only the selected bytes are written. Bytes not selected during a Byte Write operation will remain unaltered. A synchronous self-timed Write mechanism has been provided to simplify the Write operations.

Because the CY7C1364C is a common I/O device, the Output Enable (OE) must be deasserted HIGH before presenting data to the DQ inputs. Doing so will tri-state the output drivers. As a safety precaution, DQs are automatically tri-stated whenever a Write cycle is detected, regardless of the state of $\overline{OE}$.

Burst Sequences

The CY7C1364C provides a two-bit wraparound counter, fed by $A_{[1:0]}$, that implements either an interleaved or linear burst sequence. The interleaved burst sequence is designed specifically to support Intel Pentium applications. The linear burst sequence is designed to support processors that follow a linear burst sequence. The burst sequence is user selectable through the MODE input.

Asserting $\overline{ADV}$ LOW at clock rise will automatically increment the burst counter to the next address in the burst sequence. Both Read and Write burst operations are supported.

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation “sleep” mode. Two clock cycles are required to enter into or exit from this “sleep” mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the “sleep” mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the “sleep” mode. $\overline{CE_1}$, CE_2, $\overline{CE_3}$, $\overline{ADSP}$, and $\overline{ADSC}$ must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

Interleaved Burst Address Table

(MODE = Floating or V_{DD})

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Address Table

(MODE = GND)

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
I_{DDZZ}	Sleep mode standby current	$ZZ \geq V_{DD} - 0.2$ V	–	50	mA
t_{ZZS}	Device operation to ZZ	$ZZ \geq V_{DD} - 0.2$ V	–	$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	$ZZ \leq 0.2$ V	$2t_{CYC}$	–	ns
t_{ZZI}	ZZ Active to Sleep current	This parameter is sampled	–	$2t_{CYC}$	ns
t_{RZZI}	ZZ Inactive to exit Sleep current	This parameter is sampled	0	–	ns

Truth Table

The truth table for CY7C1364C follows. [1, 2, 3, 4, 5]

Next Cycle	Address Used	ZZ	$\overline{CE}_3$	CE_2	$\overline{CE}_1$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{OE}$	DQ	Write
Unselected	None	L	X	X	H	X	L	X	X	Tri-State	X
Unselected	None	L	H	X	L	L	X	X	X	Tri-State	X
Unselected	None	L	X	L	L	L	X	X	X	Tri-State	X
Unselected	None	L	H	X	L	H	L	X	X	Tri-State	X
Unselected	None	L	X	L	L	H	L	X	X	Tri-State	X
Begin Read	External	L	L	H	L	L	X	X	X	Tri-State	X
Begin Read	External	L	L	H	L	H	L	X	X	Tri-State	Read
Continue Read	Next	L	X	X	X	H	H	L	H	Tri-State	Read
Continue Read	Next	L	X	X	X	H	H	L	L	DQ	Read
Continue Read	Next	L	X	X	H	X	H	L	H	Tri-State	Read
Continue Read	Next	L	X	X	H	X	H	L	L	DQ	Read
Suspend Read	Current	L	X	X	X	H	H	H	H	Tri-State	Read
Suspend Read	Current	L	X	X	X	H	H	H	L	DQ	Read
Suspend Read	Current	L	X	X	H	X	H	H	H	Tri-State	Read
Suspend Read	Current	L	X	X	H	X	H	H	L	DQ	Read
Begin Write	Current	L	X	X	X	H	H	H	X	Tri-State	Write
Begin Write	Current	L	X	X	H	X	H	H	X	Tri-State	Write
Begin Write	External	L	L	H	L	H	H	X	X	Tri-State	Write
Continue Write	Next	L	X	X	X	H	H	H	X	Tri-State	Write
Continue Write	Next	L	X	X	H	X	H	H	X	Tri-State	Write
Suspend Write	Current	L	X	X	X	H	H	H	X	Tri-State	Write
Suspend Write	Current	L	X	X	H	X	H	H	X	Tri-State	Write
ZZ “Sleep”	None	H	X	X	X	X	X	X	X	Tri-State	X

Notes

1. X = “Don't Care.” H = Logic HIGH, L = Logic LOW.
2. $\overline{WRITE}$ = L when any one or more Byte Write Enable signals ($\overline{BW}_A$, $\overline{BW}_B$, $\overline{BW}_C$, $\overline{BW}_D$) and $\overline{BWE}$ = L or $\overline{GW}$ = L. $\overline{WRITE}$ = H when all Byte Write Enable signals (BW_A,BW_B,BW_C,BW_D), $\overline{BWE}$, $\overline{GW}$ = H.
3. The DQ pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.
4. The SRAM always initiates a Read cycle when $\overline{ADSP}$ is asserted, regardless of the state of $\overline{GW}$, $\overline{BWE}$, or $\overline{BW}_{[A:D]}$. Writes may occur only on subsequent clocks after the $\overline{ADSP}$ or with the assertion of $\overline{ADSC}$. As a result, $\overline{OE}$ must be driven HIGH prior to the start of the Write cycle to allow the outputs to tri-state. $\overline{OE}$ is a don't care for the remainder of the Write cycle.
5. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during Write cycles. During a Read cycle all data bits are tri-state when $\overline{OE}$ is inactive or when the device is deselected, and all data bits behave as output when $\overline{OE}$ is active (LOW).

Truth Table for Read/Write

The Truth Table for Read/Write for CY7C1364C follows. [6, 7]

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{BW}_D$	$\overline{BW}_C$	$\overline{BW}_B$	$\overline{BW}_A$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte A – DQ_A	H	L	H	H	H	L
Write Byte B – DQ_B	H	L	H	H	L	H
Write Bytes B, A	H	L	H	H	L	L
Write Byte C – DQ_C	H	L	H	L	H	H
Write Bytes C, A	H	L	H	L	H	L
Write Bytes C, B	H	L	H	L	L	H
Write Bytes C, B, A	H	L	H	L	L	L
Write Byte D – DQ_D	H	L	L	H	H	H
Write Bytes D, A	H	L	L	H	H	L
Write Bytes D, B	H	L	L	H	L	H
Write Bytes D, B, A	H	L	L	H	L	L
Write Bytes D, C	H	L	L	L	H	H
Write Bytes D, C, A	H	L	L	L	H	L
Write Bytes D, C, B	H	L	L	L	L	H
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

Notes

6. X = "Don't Care." H = Logic HIGH, L = Logic LOW.
7. $\overline{WRITE}$ = L when any one or more Byte Write Enable signals ($\overline{BW}_A$, $\overline{BW}_B$, $\overline{BW}_C$, $\overline{BW}_D$) and $\overline{BWE}$ = L or $\overline{GW}$ = L. $\overline{WRITE}$ = H when all Byte Write Enable signals ($\overline{BW}_A$,$\overline{BW}_B$,$\overline{BW}_C$,$\overline{BW}_D$), $\overline{BWE}$, $\overline{GW}$ = H.

IEEE 1149.1 Serial Boundary Scan (JTAG)

The CY7C1364C incorporates a serial boundary scan test access port (TAP) in the BGA package only. The TQFP package does not offer this functionality. This part operates in accordance with IEEE Standard 1149.1-1900, but does not have the set of functions required for full 1149.1 compliance. These functions from the IEEE specification are excluded because their inclusion places an added delay in the critical speed path of the SRAM. Note that the TAP controller functions in a manner that does not conflict with the operation of other devices using 1149.1 fully compliant TAPs. The TAP operates using JEDEC-standard 3.3 V or 2.5 V I/O logic levels.

The CY7C1364C contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to V_{DD} through a pull-up resistor. TDO should be left unconnected. Upon power-up, the device comes up in a reset state which does not interfere with the operation of the device.

Test Access Port (TAP)

Test Clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this ball unconnected if the TAP is not used. The ball is pulled up internally, resulting in a logic HIGH level.

Test Data-In (TDI)

The TDI ball is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see TAP Controller State Diagram on page 12. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register.

Test Data-Out (TDO)

The TDO output ball is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine (see Instruction Codes on page 16). The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register.

Performing a TAP Reset

A RESET is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating.

At power-up, the TAP is reset internally to ensure that TDO comes up in a high Z state.

TAP Registers

Registers are connected between the TDI and TDO balls and enable data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI ball on the rising edge of TCK. Data is output on the TDO ball on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO balls as shown in the TAP Controller Block Diagram on page 13. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary “01” pattern to enable fault isolation of the board-level serial test data path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO balls. This enables data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all the input and bidirectional balls on the SRAM.

The boundary scan register is loaded with the contents of the RAM I/O ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO balls when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE Z instructions can be used to capture the contents of the I/O ring.

The Boundary Scan Order on page 17 show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in Identification Register Definitions on page 16.

TAP Instruction Set

Overview

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in Instruction Codes on page 16. Three of these instructions are listed as RESERVED and should not be used. The other five instructions are described in detail in this section.

The TAP controller used in this SRAM is not fully compliant to the 1149.1 convention because some of the mandatory 1149.1 instructions are not fully implemented.

The TAP controller cannot be used to load address data or control signals into the SRAM and cannot preload the I/O buffers. The SRAM does not implement the 1149.1 commands EXTEST or INTEST or the PRELOAD portion of SAMPLE/PRELOAD; rather, it performs a capture of the I/O ring when these instructions are executed.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO balls. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

EXTEST

EXTEST is a mandatory 1149.1 instruction which is to be executed whenever the instruction register is loaded with all 0s. EXTEST is not implemented in this SRAM TAP controller, and therefore this device is not compliant to 1149.1. The TAP controller does recognize an all-0 instruction.

When an EXTEST instruction is loaded into the instruction register, the SRAM responds as if a SAMPLE/PRELOAD instruction has been loaded. There is one difference between the two instructions. Unlike the SAMPLE/PRELOAD instruction, EXTEST places the SRAM outputs in a high Z state.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO balls and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state.

The IDCODE instruction is loaded into the instruction register upon power up or whenever the TAP controller is given a test logic reset state.

SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO balls when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a high Z state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. When the SAMPLE/PRELOAD instructions are loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 20 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To guarantee that the boundary scan register will capture the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller’s capture setup plus hold times (t_{CS} and t_{CH}). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and $\overline{CK}$ captured in the boundary scan register.

After the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

PRELOAD enables an initial data pattern to be placed at the latched parallel outputs of the boundary scan register cells prior to the selection of another boundary scan test operation.

The shifting of data for the SAMPLE and PRELOAD phases can occur concurrently when required – that is, while data captured is shifted out, the preloaded data can be shifted in.

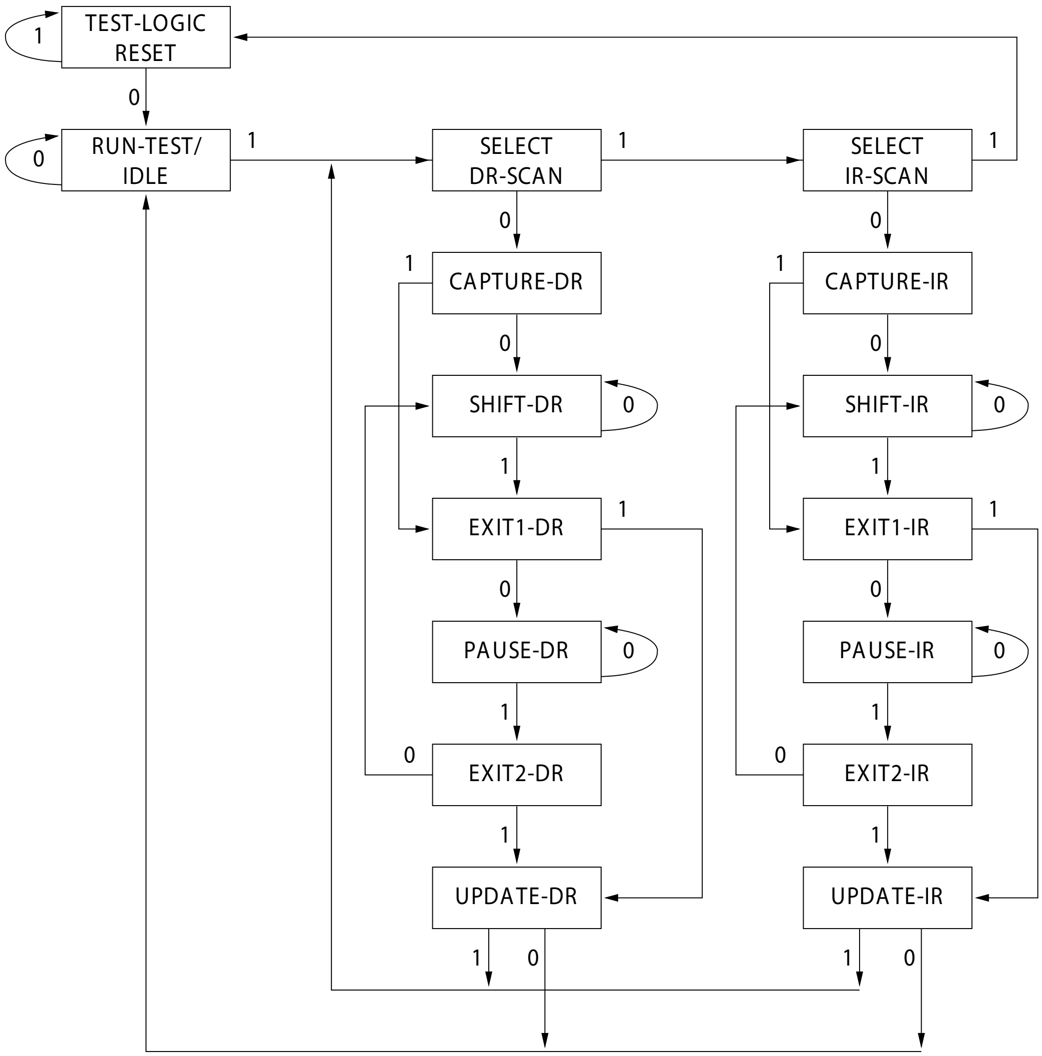
BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO balls. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

Reserved

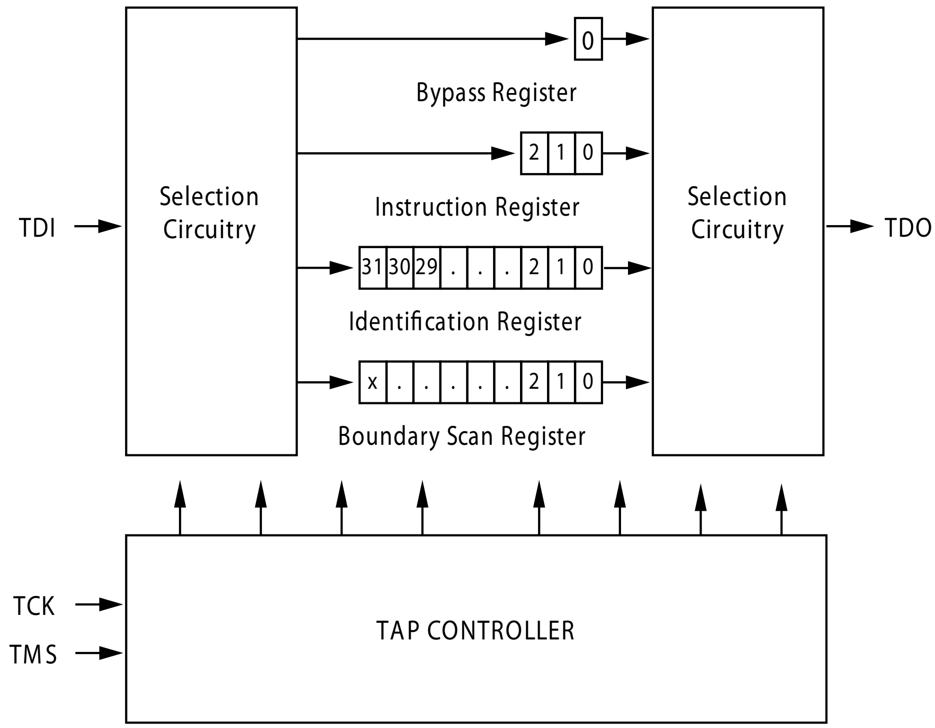
These instructions are not implemented but are reserved for future use. Do not use these instructions.

TAP Controller State Diagram

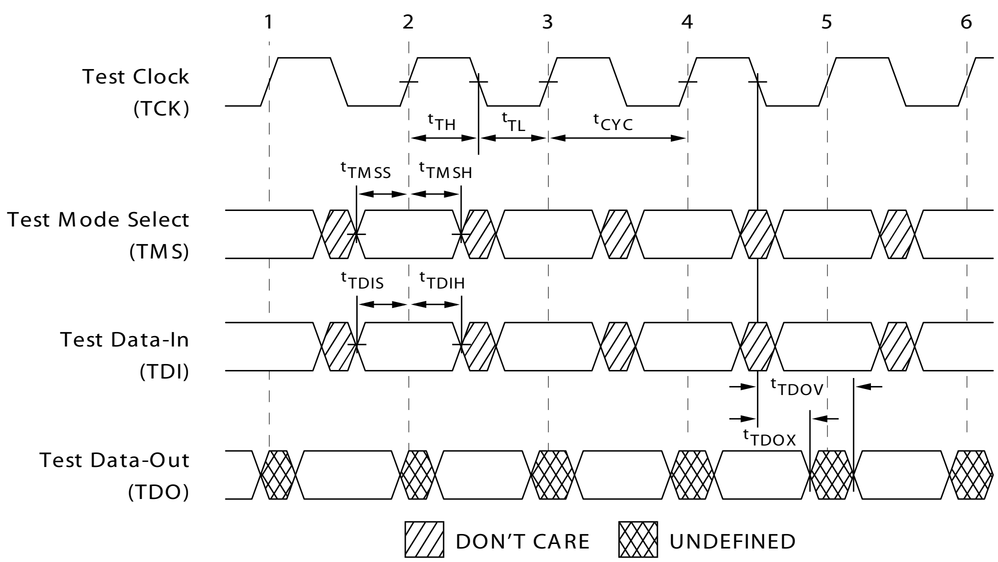


The 0/1 next to each state represents the value of TMS at the rising edge of TCK.

TAP Controller Block Diagram



TAP Timing



TAP AC Switching Characteristics

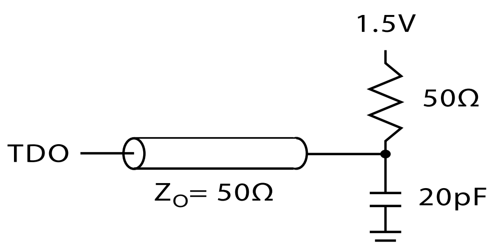
Over the Operating Range

Parameter [8, 9]	Description	Min	Max	Unit
Clock				
t_{TCYC}	TCK clock cycle time	50	–	ns
t_{TF}	TCK clock frequency	–	20	MHz
t_{TH}	TCK clock HIGH time	20	–	ns
t_{TL}	TCK clock LOW time	20	–	ns
Output Times				
t_{TDOV}	TCK clock LOW to TDO valid	–	10	ns
t_{TDOX}	TCK clock LOW to TDO invalid	0	–	ns
Setup Times				
t_{TMSS}	TMS setup to TCK clock rise	5	–	ns
t_{TDIS}	TDI setup to TCK clock rise	5	–	ns
t_{CS}	Capture setup to TCK rise	5	–	ns
Hold Times				
t_{TMSH}	TMS hold after TCK clock rise	5	–	ns
t_{TDIH}	TDI hold after clock rise	5	–	ns
t_{CH}	Capture hold after clock rise	5	–	ns

3.3 V TAP AC Test Conditions

Input pulse levels .... V_{SS} to 3.3 V
Input rise and fall times ....1 ns
Input timing reference levels .... 1.5 V
Output reference levels .... 1.5 V
Test load termination supply voltage .... 1.5 V

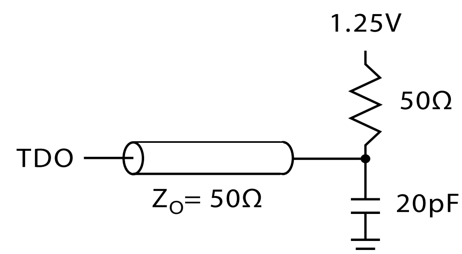
3.3 V TAP AC Output Load Equivalent



2.5 V TAP AC Test Conditions

Input pulse levels .... V_{SS} to 2.5 V
Input rise and fall time ....1 ns
Input timing reference levels .... 1.25 V
Output reference levels .... 1.25 V
Test load termination supply voltage .... 1.25 V

2.5 V TAP AC Output Load Equivalent



Notes
8. t_{CS} and t_{CH} refer to the setup and hold time requirements of latching data from the boundary scan register.
9. Test conditions are specified using the load in TAP AC test Conditions. t_R/t_F = 1 ns.

TAP DC Electrical Characteristics and Operating Conditions

(0 °C < T_A < +70 °C; V_{DD} = 3.3 V ± 0.165 V unless otherwise noted)

Parameter [10]	Description	Conditions		Min	Max	Unit
V_{OH1}	Output HIGH voltage	I_{OH} = –4.0 mA	V_{DDQ} = 3.3 V	2.4	–	V
		I_{OH} = –1.0 mA	V_{DDQ} = 2.5 V	2.0	–	V
V_{OH2}	Output HIGH voltage	I_{OH} = –100 µA	V_{DDQ} = 3.3 V	2.9	–	V
			V_{DDQ} = 2.5 V	2.1	–	V
V_{OL1}	Output LOW voltage	I_{OL} = 8.0 mA	V_{DDQ} = 3.3 V	–	0.4	V
		I_{OL} = 8.0 mA	V_{DDQ} = 2.5 V	–	0.4	V
V_{OL2}	Output LOW voltage	I_{OL} = 100 µA	V_{DDQ} = 3.3 V	–	0.2	V
			V_{DDQ} = 2.5 V	–	0.2	V
V_{IH}	Input HIGH voltage		V_{DDQ} = 3.3 V	2.0	V_{DD} + 0.3	V
			V_{DDQ} = 2.5 V	1.7	V_{DD} + 0.3	V
V_{IL}	Input LOW voltage		V_{DDQ} = 3.3 V	–0.5	0.7	V
			V_{DDQ} = 2.5 V	–0.3	0.7	V
I_X	Input load current	GND ≤ V_{IN} ≤ V_{DDQ}		–5	5	µA

Note

10. All voltages referenced to V_{SS} (GND).

Identification Register Definitions

Instruction Field	CY7C1364C (256 K × 32)	Description
Revision number (31:29)	000	Describes the version number
Device depth (28:24) [11]	01011	Reserved for internal use
Device width (23:18) 165-ball FBGA	000000	Defines memory type and architecture
Cypress device ID (17:12)	011110	Defines width and density
Cypress JEDEC ID code (11:1)	00000110100	Allows unique identification of SRAM vendor
ID register presence indicator (0)	1	Indicates the presence of an ID register

Scan Register Sizes

Register Name	Bit Size (× 32)
Instruction	3
Bypass	1
ID	32
Boundary scan order (165-ball FBGA package)	71

Instruction Codes

Instruction	Code	Description
EXTEST	000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM outputs to high Z state.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operations.
SAMPLE Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a high Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect SRAM operation.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operations.

Note

11. Bit #24 is “1” in the Register Definitions for both 2.5 V and 3.3 V versions of this device.

Boundary Scan Order

165-ball FBGA

CY7C1364C (256 K × 32)

Bit#	Ball ID	Signal Name
1	B6	CLK
2	B7	$\overline{GW}$
3	A7	$\overline{BWE}$
4	B8	$\overline{OE}$
5	A8	$\overline{ADSC}$
6	B9	$\overline{ADSP}$
7	A9	$\overline{ADV}$
8	B10	A
9	A10	A
10	C11	NC
11	E10	DQ_B
12	F10	DQ_B
13	G10	DQ_B
14	D10	DQ_B
15	D11	DQ_B
16	E11	DQ_B
17	F11	DQ_B
18	G11	DQ_B
19	H11	ZZ
20	J10	DQ_A
21	K10	DQ_A
22	L10	DQ_A
23	M10	DQ_A
24	J11	DQ_A
25	K11	DQ_A
26	L11	DQ_A
27	M11	DQ_A
28	N11	NC
29	R11	A
30	R10	A
31	P10	A
32	R9	A
33	P9	A
34	R8	A
35	P8	A
36	P11	A
37	R6	A0
38	P6	A1
39	R4	A
40	P4	A
41	R3	A
42	P3	A
43	R1	MODE
44	N1	NC
45	L2	DQ_D
46	K2	DQ_D
47	J2	DQ_D
48	M2	DQ_D
49	M1	DQ_D
50	L1	DQ_D
51	K1	DQ_D
52	J1	DQ_D
53	Internal	Internal
54	G2	DQ_C
55	F2	DQ_C
56	E2	DQ_C
57	D2	DQ_C
58	G1	DQ_C
59	F1	DQ_C
60	E1	DQ_C
61	D1	DQ_C
62	C1	NC
63	B2	A
64	A2	A
65	A3	CE_1
66	B3	CE_2
67	B4	BW_D
68	A4	$\overline{BW_C}$
69	A5	$\overline{BW_B}$
70	B5	$\overline{BW_A}$
71	A6	$\overline{CE_3}$

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. User guidelines are not tested.

Storage Temperature .... –65 °C to +150 °C

Ambient Temperature with Power Applied .... –55 °C to +125 °C

Supply Voltage on V_{DD} Relative to GND .....–0.5 V to +4.6 V

Supply Voltage on V_{DDQ} Relative to GND .... –0.5 V to $+V_{DD}$

DC Voltage Applied to Outputs in tri-state ....–0.5 V to V_{DDQ} + 0.5 V

DC Input Voltage ....–0.5 V to V_{DD} + 0.5 V

Current into Outputs (LOW) .... 20 mA

Static Discharge Voltage (per MIL-STD-883, Method 3015) .... >2001 V

Latch-up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Industrial	–40 °C to +85 °C	3.3 V – 5% / + 10%	2.5 V – 5% to V_{DD}

Electrical Characteristics

Over the Operating Range

Parameter [12, 13]	Description	Test Conditions		Min	Max	Unit
V_{DD}	Power Supply Voltage			3.135	3.6	V
V_{DDQ}	I/O Supply Voltage	for 3.3 V I/O		3.135	V_{DD}	V
		for 2.5 V I/O		2.375	2.625	V
V_{OH}	Output HIGH Voltage	for 3.3 V I/O, I_{OH} = –4.0 mA		2.4	–	V
		for 2.5 V I/O, I_{OH} = –1.0 mA		2.0	–	V
V_{OL}	Output LOW Voltage	for 3.3 V I/O, I_{OL} = 8.0 mA		–	0.4	V
		for 2.5 V I/O, I_{OL} = 1.0 mA		–	0.4	V
V_{IH}	Input HIGH Voltage [12]	for 3.3 V I/O		2.0	V_{DD} + 0.3	V
		for 2.5 V I/O		1.7	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage [12]	for 3.3 V I/O		–0.3	0.8	V
		for 2.5 V I/O		–0.3	0.7	V
I_X	Input Leakage Current except ZZ and MODE	GND ≤ V_I ≤ V_{DDQ}		–5	5	μA
	Input Current of MODE	Input = V_{SS}		–30	–	μA
		Input = V_{DD}		–	5	μA
	Input Current of ZZ	Input = V_{SS}		–5	–	μA
		Input = V_{DD}		–	30	μA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ $V_{DDQ,}$ Output Disabled		–5	5	μA
I_{DD}	V_{DD} Operating Supply Current	V_{DD} = Max, I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{CYC}$	6-ns cycle, 166 MHz	–	180	mA
I_{SB1}	Automatic CE Power-down Current – TTL Inputs	V_{DD} = Max, Device Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX} = $1/t_{CYC}$	6-ns cycle, 166 MHz	–	110	mA
I_{SB2}	Automatic CE Power-down Current – CMOS Inputs	V_{DD} = Max, Device Deselected, V_{IN} ≤ 0.3 V or V_{IN} ≥ V_{DDQ} – 0.3 V, f = 0	6-ns cycle, 166 MHz	–	40	mA

Notes

12. Overshoot: $V_{IH(AC)} < V_{DD}$ + 1.5 V (Pulse width less than $t_{CYC}/2$), undershoot: $V_{IL(AC)}$ > –2 V (Pulse width less than $t_{CYC}/2$).
13. $T_{Power-up}$: Assumes a linear ramp from 0 V to $V_{DD(min)}$ within 200 ms. During this time $V_{IH} < V_{DD}$ and $V_{DDQ} \leq V_{DD}$.

Electrical Characteristics (continued)

Over the Operating Range

Parameter [12, 13]	Description	Test Conditions		Min	Max	Unit
I_{SB3}	Automatic CE Power-down Current – CMOS Inputs	V_{DD} = Max, Device Deselected, $V_{IN} \le 0.3$ V or $V_{IN} \ge V_{DDQ} - 0.3$ V, $f = f_{MAX} = 1/t_{CYC}$	6-ns cycle, 166 MHz	–	100	mA
I_{SB4}	Automatic CE Power-down Current – TTL Inputs	V_{DD} = Max, Device Deselected, $V_{IN} \ge V_{IH}$ or $V_{IN} \le V_{IL}$, f = 0	6-ns cycle, 166 MHz	–	40	mA

Capacitance

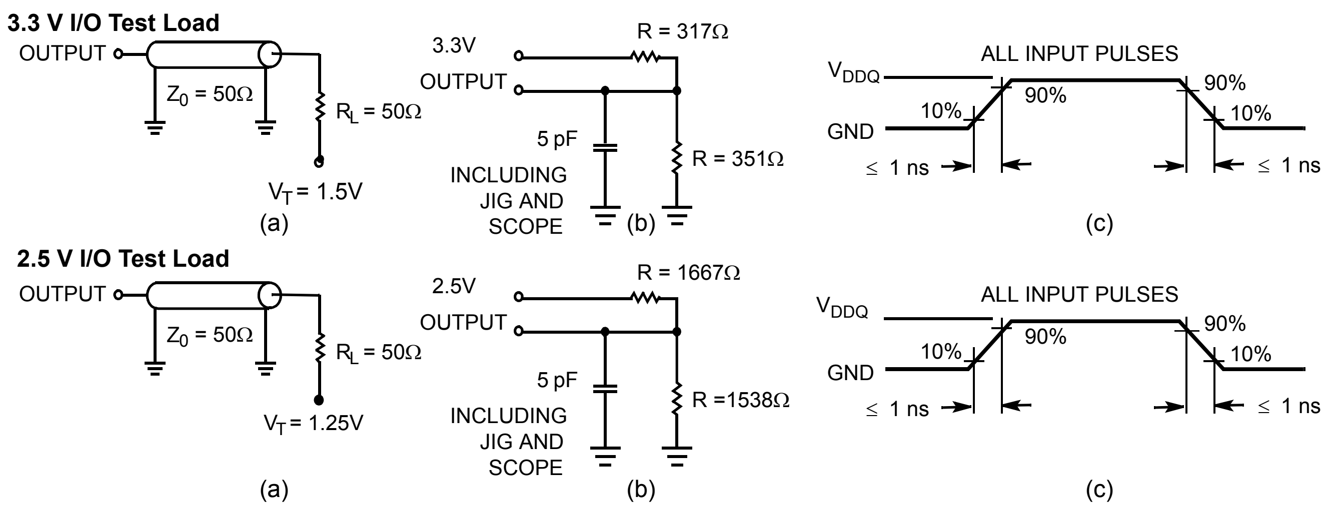
Parameter [14]	Description	Test Conditions	165-ball FBGA Max.	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{DD} = 3.3 V, V_{DDQ} = 2.5 V	5	pF
C_{CLK}	Clock input capacitance		5	pF
$C_{I/O}$	Input/Output capacitance		7	pF

Thermal Resistance

Parameter [14]	Description	Test Conditions	165-ball FBGA Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51	16.8	°C/W
Θ_{JC}	Thermal resistance (junction to case)		3	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Note
14. Tested initially and after any design or process change that may affect these parameters.

Switching Characteristics

Over the Operating Range

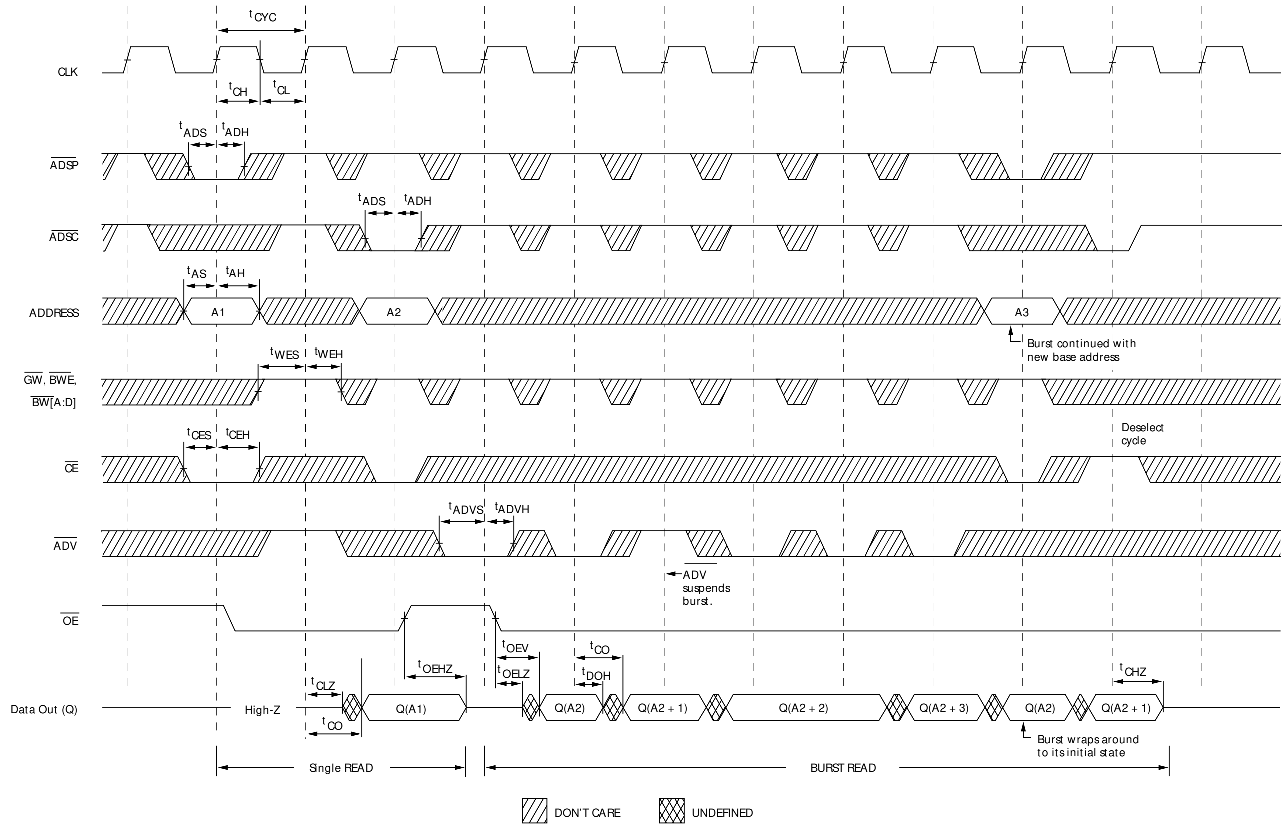
Parameter [15, 16]	Description	-166		Unit
		Min	Max	
t_{POWER}	V_{DD}(typical) to the first access [17]	1	–	ms
Clock				
t_{CYC}	Clock cycle time	6.0	–	ns
t_{CH}	Clock HIGH	2.4	–	ns
t_{CL}	Clock LOW	2.4	–	ns
Output Times				
t_{CO}	Data output valid after CLK rise	–	3.5	ns
t_{DOH}	Data output hold after CLK rise	1.25	–	ns
t_{CLZ}	Clock to low Z [18, 19, 20]	1.25	–	ns
t_{CHZ}	Clock to high Z [18, 19, 20]	1.25	3.5	ns
t_{OEV}	$\overline{OE}$ LOW to output valid	–	3.5	ns
t_{OELZ}	$\overline{OE}$ LOW to output low Z [18, 19, 20]	0	–	ns
t_{OEHZ}	$\overline{OE}$ HIGH to output high Z [18, 19, 20]	–	3.5	ns
Set-up Times				
t_{AS}	Address set-up before CLK rise	1.5	–	ns
t_{ADS}	$\overline{ADSC}$, $\overline{ADSP}$ set-up before CLK rise	1.5	–	ns
t_{ADVS}	$\overline{ADV}$ set-up before CLK rise	1.5	–	ns
t_{WES}	$\overline{GW}$, $\overline{BWE}$, $\overline{BW}_{[A:D]}$ set-up before CLK rise	1.5	–	ns
t_{DS}	Data input set-up before CLK rise	1.5	–	ns
t_{CES}	Chip enable set-up before CLK rise	1.5	–	ns
Hold Times				
t_{AH}	Address hold after CLK rise	0.5	–	ns
t_{ADH}	$\overline{ADSP}$, $\overline{ADSC}$ hold after CLK rise	0.5	–	ns
t_{ADVH}	$\overline{ADV}$ hold after CLK rise	0.5	–	ns
t_{WEH}	$\overline{GW}$, $\overline{BWE}$, $\overline{BW}_{[A:D]}$ hold after CLK rise	0.5	–	ns
t_{DH}	Data input hold after CLK rise	0.5	–	ns
t_{CEH}	Chip enable hold after CLK rise	0.5	–	ns

Notes

15. Timing reference level is 1.5 V when V_{DDQ} = 3.3 V and is 1.25 V when V_{DDQ} = 2.5 V.
16. Test conditions shown in (a) of Figure 2 on page 19 unless otherwise noted.
17. This part has a voltage regulator internally; t_{POWER} is the time that the power needs to be supplied above $V_{DD(minimum)}$ initially before a Read or Write operation can be initiated.
18. t_{CHZ}, t_{CLZ}, t_{OELZ}, and t_{OEHZ} are specified with AC test conditions shown in part (b) of Figure 2 on page 19. Transition is measured ±200 mV from steady-state voltage.
19. At any given voltage and temperature, t_{OEHZ} is less than t_{OELZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High Z prior to Low Z under the same system conditions.
20. This parameter is sampled and not 100% tested.

Switching Waveforms

Figure 3. Read Cycle Timing [21]

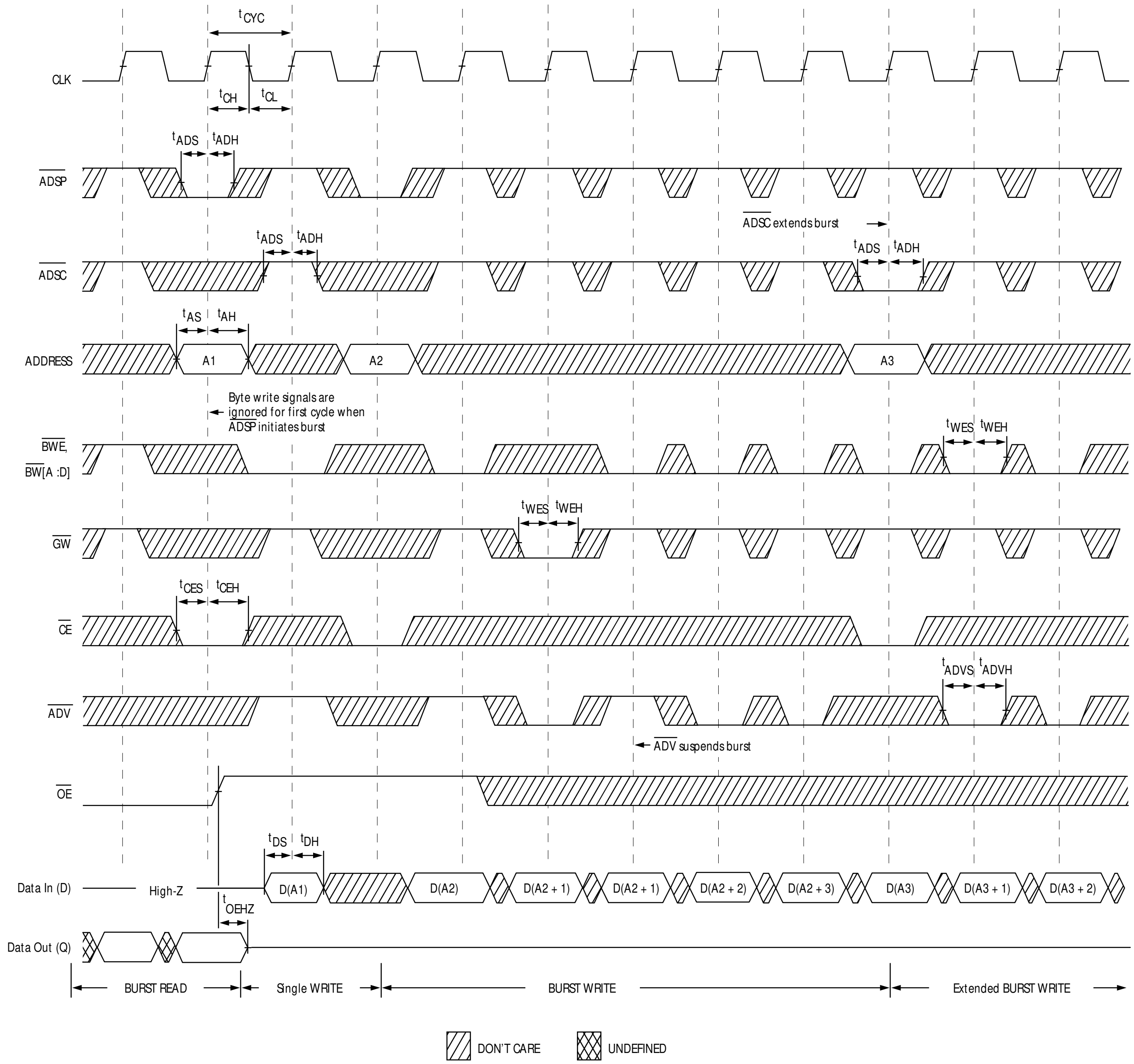


Note

21. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH, $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.

Switching Waveforms (continued)

Figure 4. Write Cycle Timing [22, 23]

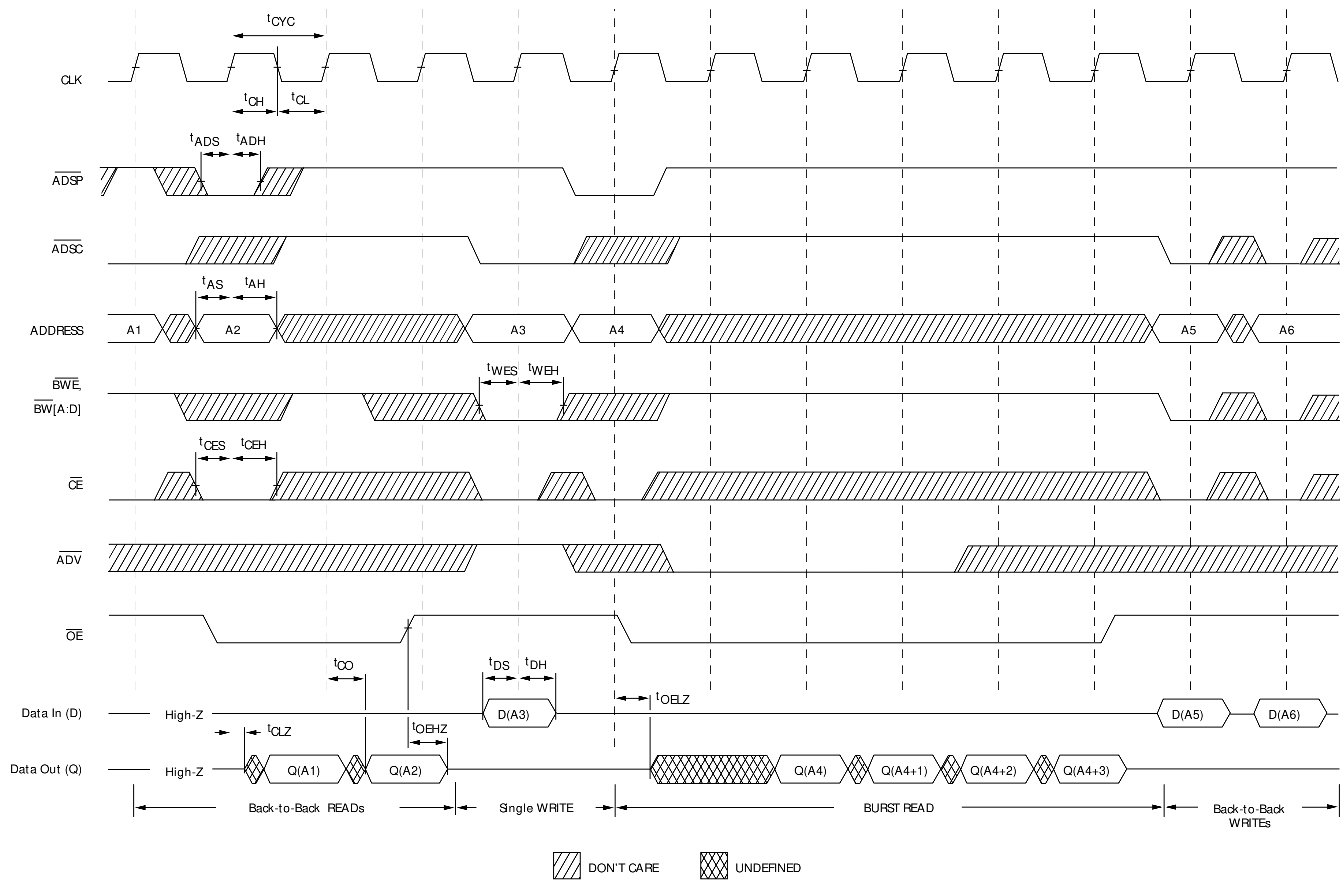


Notes

22. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE_1}$ is LOW, CE_2 is HIGH and $\overline{CE_3}$ is LOW. When $\overline{CE}$ is HIGH, $\overline{CE_1}$ is HIGH or CE_2 is LOW or $\overline{CE_3}$ is HIGH.
23. Full width Write can be initiated by either $\overline{GW}$ LOW; or by $\overline{GW}$ HIGH, $\overline{BWE}$ LOW and $\overline{BW}_{[A:D]}$ LOW.

Switching Waveforms (continued)

Figure 5. Read/Write Cycle Timing [24, 25, 26]

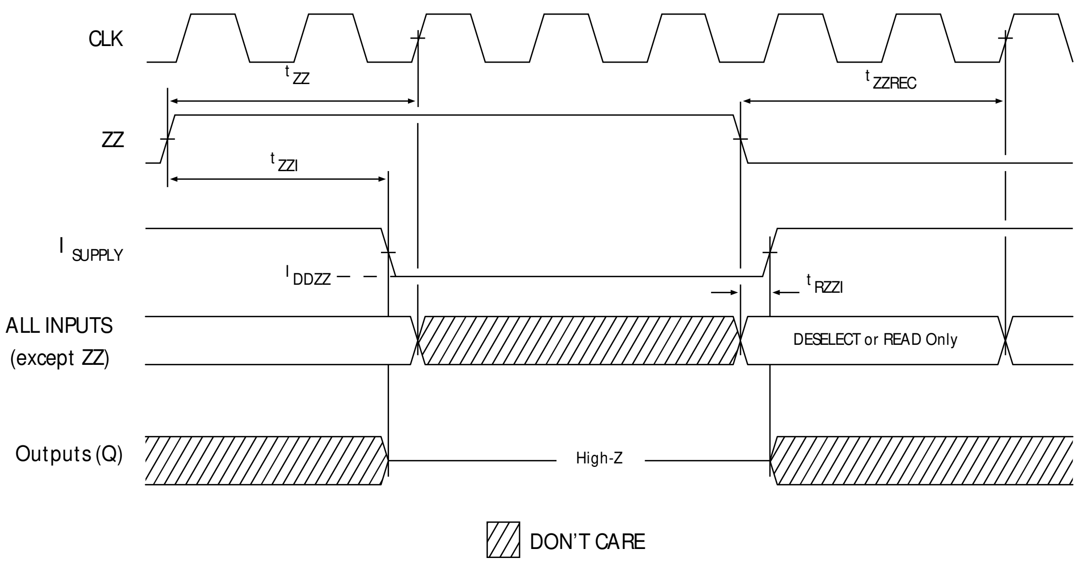


Notes

24. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE_1}$ is LOW, CE_2 is HIGH and $\overline{CE_3}$ is LOW. When $\overline{CE}$ is HIGH, $\overline{CE_1}$ is HIGH or CE_2 is LOW or $\overline{CE_3}$ is HIGH.
25. The data bus (Q) remains in High Z following a Write cycle unless an $\overline{ADSP}$, $\overline{ADSC}$, or $\overline{ADV}$ cycle is performed.
26. $\overline{GW}$ is HIGH.

Switching Waveforms (continued)

Figure 6. ZZ Mode Timing [27, 28]



Notes

27. Device must be deselected when entering ZZ mode. See Cycle Descriptions table for all possible signal conditions to deselect the device.
28. DQs are in High Z when exiting ZZ sleep mode.

Ordering Information

Not all of the speed, package and temperature ranges are available. Please contact your local sales representative or visit www.cypress.com for actual products offered.

Speed (MHz)	Ordering Code	Package Diagram	Part and Package Type	Operating Range
166	CY7C1364C-166BZI	51-85180	165-ball FBGA (13 × 15 × 1.4 mm)	Industrial

Ordering Code Definitions

CY 7 C 1364 C - 166 BZ I

Temperature range:
I = Industrial = –40 °C to +85 °C

Package Type:
BZ = 165-ball FBGA

Speed Grade: 166 MHz

Process Technology: C ≥ 90 nm

Part Identifier: 1364 = DCD, 256 K × 32 (9 Mb)

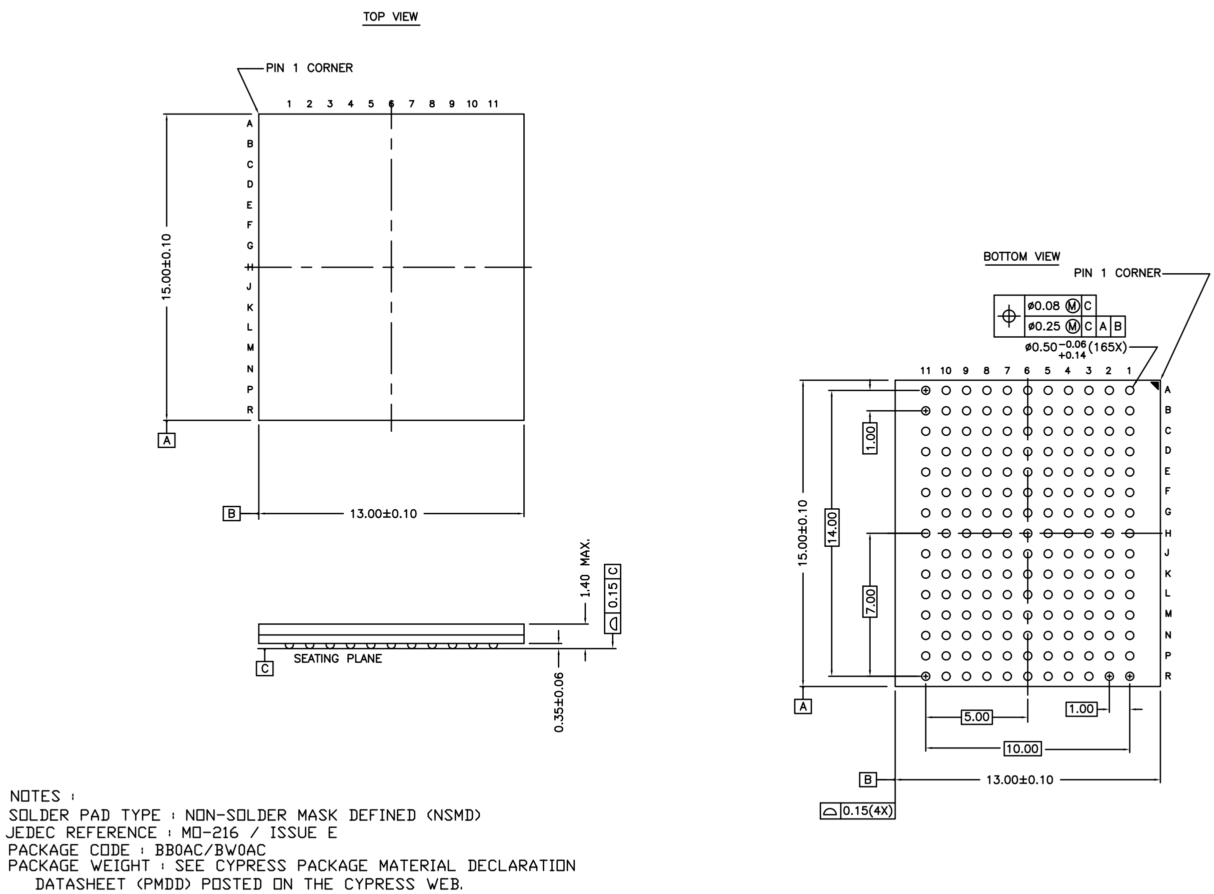
Technology Code: C = CMOS

Marketing Code: 7 = SRAM

Company ID: CY = Cypress

Package Diagram

Figure 7. 165-ball FBGA (13 × 15 × 1.4 mm) BB165D/BW165D (0.5 Ball Diameter) Package Outline, 51-85180



51-85180 *G

Acronyms

Acronym	Description
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
EIA	Electronic Industries Alliance
FBGA	Fine-Pitch Ball Grid Array
I/O	Input/Output
JEDEC	Joint Electron Devices Engineering Council
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
TTL	Transistor-Transistor Logic

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
mm	millimeter
ms	millisecond
mV	millivolt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1364C, 9-Mbit (256 K × 32) Pipelined Sync SRAM Document Number: 001-74592				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	3489597	01/10/2012	PRIT	New data sheet.
*A	3508648	01/25/2012	PRIT	Changed status from Preliminary to Final.
*B	3537338	02/28/2012	PRIT	Updated Pin Definitions. Added IEEE 1149.1 Serial Boundary Scan (JTAG). Added TAP Controller State Diagram. Added TAP Controller Block Diagram. Added TAP Timing. Added TAP AC Switching Characteristics. Added 3.3 V TAP AC Test Conditions. Added 3.3 V TAP AC Output Load Equivalent. Added 2.5 V TAP AC Test Conditions. Added 2.5 V TAP AC Output Load Equivalent. Added TAP DC Electrical Characteristics and Operating Conditions. Added Identification Register Definitions. Added Scan Register Sizes. Added Instruction Codes. Added Boundary Scan Order.
*C	3800880	11/02/2012	PRIT	Updated Package Diagram (spec 51-85180 (Changed revision from *E to *F)).
*D	4576419	11/24/2014	PRIT	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end.
*E	5071299	01/04/2016	PRIT	Updated Package Diagram: spec 51-85180 – Changed revision from *F to *G. Updated to new template. Completing Sunset Review.

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