Features

- SMPTE 292M, SMPTE 344M and SMPTE 259M compliant
- Automatic cable equalization
- Multi-standard operation from 143Mb/s to 1.485Gb/s
- Supports DVB-ASI at 270Mb/s
- Small footprint (4mm x 4mm)
- Pb-free and RoHS Compliant
- Pin compatible with the GS9074 Cable Equalizer
- Manual bypass (useful for low data rates with slow rise/fall times)
- Performance optimized for 270Mb/s and 1.485Gb/s
- Typical maximum equalized length of Belden 1694A cable: 140m at 1.485Gb/s, 350m at 270Mb/s
- 50Ω differential output (with internal 50Ω pull-ups)
- Manual output mute or programmable mute based on max cable length adjust
- Single 3.3V power supply operation
- Operating temperature range: 0°C to +70°C

Applications

- SMPTE 292M, SMPTE 344M and SMPTE 259M Coaxial Cable Serial Digital Interfaces.

Description

The GS1574 is a second-generation high-speed bipolar integrated circuit designed to equalize and restore signals received over 75Ω co-axial cable.

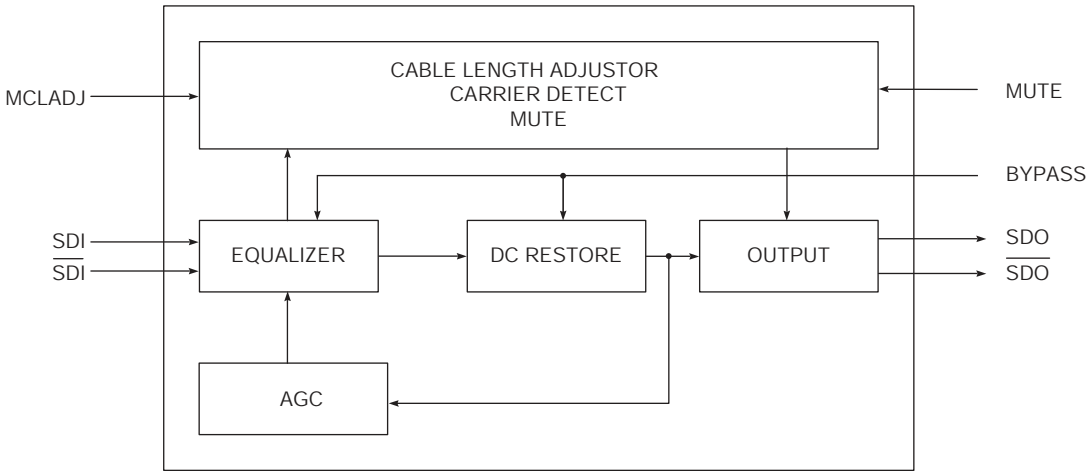
The GS1574 is designed to support SMPTE 292M, SMPTE 344M and SMPTE 259M, and is optimized for performance at 270Mb/s and 1.485Gb/s.

The GS1574 features DC restoration to compensate for the DC content of SMPTE pathological test patterns.

A voltage programmable mute threshold (MCLADJ) is included to allow muting of the GS1574 output when an approximate selected cable length is reached for SMPTE 259M signals. This feature allows the GS1574 to distinguish between low amplitude SD-SDI signals and noise at the input of the device. The serial digital outputs of the GS1574 may be forced to a mute state by applying a voltage to the MUTE pin.

Power consumption is typically 270mW using a 3.3V power supply. The GS1574 is lead-free, and the encapsulation compound does not contain halogenated flame retardant.

This component and all homogeneous subcomponents are RoHS compliant.



GS1574 Functional Block Diagram

Contents

1. Pin Out

1.1 GS1574 Pin Assignment

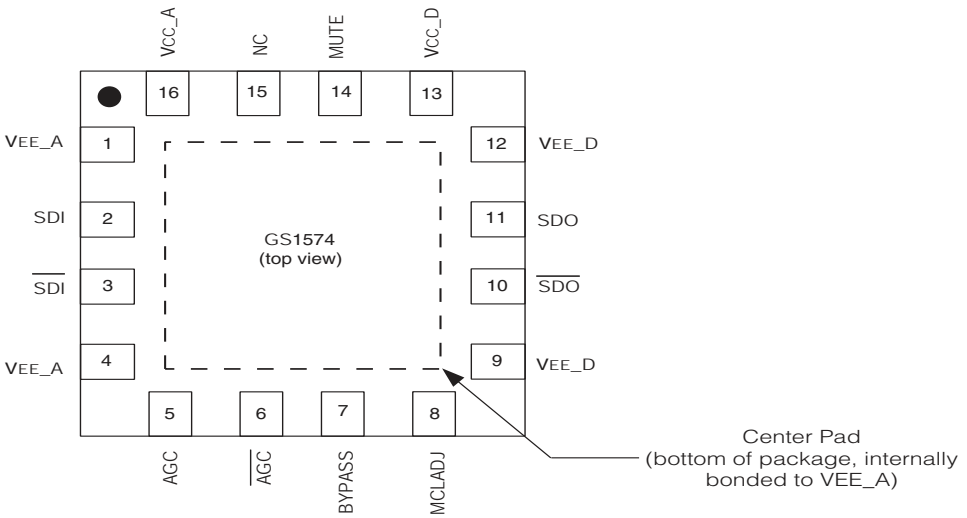


Figure 1-1: 16-Pin QFN

1.2 GS1574 Pin Descriptions

Table 1-1: GS1574 Pin Descriptions

Pin Number	Name	Timing	Type	Description
1, 4	VEE_A	Analog	Power	Most negative power supply for analog circuitry. Connect to analog GND.
2, 3	SDI, $\overline{\text{SDI}}$	Analog	Input	Serial digital differential input.
5, 6	AGC, $\overline{\text{AGC}}$	Analog	–	External AGC capacitor. Connect pin 5 and pin 6 together as shown in Typical Application Circuit A.
7	BYPASS	Not Synchronous	Input	Forces the Equalizing and DC RESTORE stages into bypass mode when HIGH. No equalization occurs in this mode.
8	MCLADJ	Analog	Input	Maximum cable length adjust. Adjusts the approximate maximum amount of cable to be equalized (from 0m to the maximum cable length). The output is muted (latched to the last state) when the maximum cable length is achieved. NOTE: MCLADJ is only recommended for data rates up to 360Mb/s. For data rates above this, MCLADJ should be left floating.
9	VEE_D	Analog	Power	Most negative power supply for the digital circuitry and output buffer. Connect to digital GND.
10, 11	$\overline{\text{SDO}}$, SDO	Analog	Output	Equalized serial digital differential output.

Table 1-1: GS1574 Pin Descriptions

Pin Number	Name	Timing	Type	Description
12	VEE_D	Analog	Power	Most negative power supply for the digital circuitry and output buffer. Connect to digital GND.
13	VCC_D	Analog	Power	Most positive power supply for the digital I/O pins of the device. Connect to +3.3V DC.
14	MUTE	Not Synchronous	Input	CONTROL SIGNAL INPUT levels are LVCMOS/LVTTL compatible. (3.3V Tolerant) When the MUTE pin is set HIGH by the application interface, the serial digital output of the device will be forced to a steady state. When the MUTE pin is set LOW, the serial digital output of the device will be active.
15	NC	–	–	No Connect.
16	VCC_A	Analog	Power	Most positive power supply for the analog circuitry of the device. Connect to +3.3V DC.
–	Center Pad	–	Power	Internally bonded to VEE_A.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Parameter	Value
Supply Voltage	-0.5V to +3.6 V_{DC}
Input ESD Voltage (Human Body Model)	500V
Storage Temperature Range	-50°C < T_s < 125°C
Input Voltage Range (any input)	-0.3 to (V_{CC} +0.3)V
Operating Temperature Range	0°C to 70°C
Power Dissipation	300mW
Lead Temperature (soldering, 10 sec)	260°C

2.2 DC Electrical Characteristics

Table 2-1: DC Electrical Characteristics

V_{CC} = 3.3V ±5%, T_A = 0°C to 70°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Test Levels	Notes
Supply Voltage	V_{CC}	–	3.135	3.3	3.465	V	–	±5%
Power Consumption	P_D	T_A = 25°C	–	265	–	mW	2	–
Supply Current	I_s	T_A = 25°C	–	80	–	mA	1	–
Output Common Mode Voltage	V_{CMOUT}	T_A = 25°C	–	V_{CC} - ΔV_{SDO}/2	–	V	7	–
Input Common Mode Voltage	V_{CMIN}	T_A = 25°C	–	1.75	–	V	8	–
Floating MCLADJ DC Voltage	–	0m, T_A = 25°C	–	1.3	–	V	7	–
MCLADJ Range	–	T_A = 25°C	–	0.69	–	V	7	–
Mute Input Voltage Required to Force Outputs to Mute	V_{Mute}	Min to Mute	3.0	–	–	V	7	–
Mute Input Voltage Required to Force Outputs Active	V_{Mute}	Max to Activate	–	–	2.0	V	7	–

2.3 AC Electrical Characteristics

Table 2-2: AC Electrical Characteristics

V_{CC} = 3.3V ±5%, T_A = 0°C to 70°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Test Levels	Notes
Serial input data rate	DR_{SDO}	GS1574	143	–	1485	Mb/s	6	–
Input Voltage Swing	ΔV_{SDI}	T_A =25°C, differential	720	800	950	mV_{p-p}	2	1
Output Voltage Swing	ΔV_{SDO}	100Ω load, T_A =25°C, differential	–	750	–	mV_{p-p}	1	–
Output Jitter for Various Cable Lengths and Data Rates	–	540Mb/s Belden 1694A: 0-140m Belden 8281: 0-100m	–	0.2	–	UI	8	5
	–	270Mb/s Belden 1694A: 0-350m	–	0.2	–	UI	5	2,5
	–	270Mb/s Belden 8281: 0-280m	–	0.2	–	UI	2	2,5
	–	1.485Gb/s Belden 1694A: 0-140m	–	0.25	–	UI	5	2,5
	–	1.485Gb/s Belden 8281: 0-100m	–	0.25	–	UI	2	2,5
Output Rise/Fall time	–	20% - 80%	–	80	220	ps	1	–
Mismatch in rise/fall time	–	–	–	–	30	ps	1	–
Duty cycle distortion	–	–	–	–	30	ps	1	1
Overshoot	–	–	–	–	10	%	7	–
Input Return Loss	–	–	15	–	–	dB	8	3
Input Resistance	–	single ended	–	1.64	–	kΩ	6	–
Input Capacitance	–	single ended	–	1	–	pF	6	–
Output Resistance	–	single ended	–	50	–	Ω	6	–

TEST LEVELS

1. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges.
2. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges using correlated test.
3. Production test at room temperature and nominal supply voltage.
4. QA sample test.
5. Calculated result based on Level 1, 2, or 3.
6. Not tested. Guaranteed by design simulations.
7. Not tested. Based on characterization of nominal parts.
8. Not tested. Based on existing design/characterization data of similar product.
9. Indirect test.

NOTES:

1. 0m cable length.
2. All parts production tested. In order to guarantee jitter over the full range of specification (V_{CC} = 3.3V ±5%, T_A = 0°C to 70°C, and 720-880mV launch swing from the SDI cable driver) the recommended applications circuit must be used.
3. Tested on CB1574 board from 5MHz to 2GHz.
4. Based on characterization data using the recommended applications circuit , at V_{CC} = 3.3V, T_A = 25°C, and 800mV launch swing from the SDI cable driver.
5. Equalizer Pathological test signal is used.

2.4 Solder Reflow Profiles

The device is manufactured with Matte-Sn terminations and is compatible with both standard eutectic and Pb-free solder reflow profiles. The recommended standard eutectic reflow profile is shown in Figure 2-1. MSL qualification was performed using the maximum Pb-free reflow profile shown in Figure 2-2.

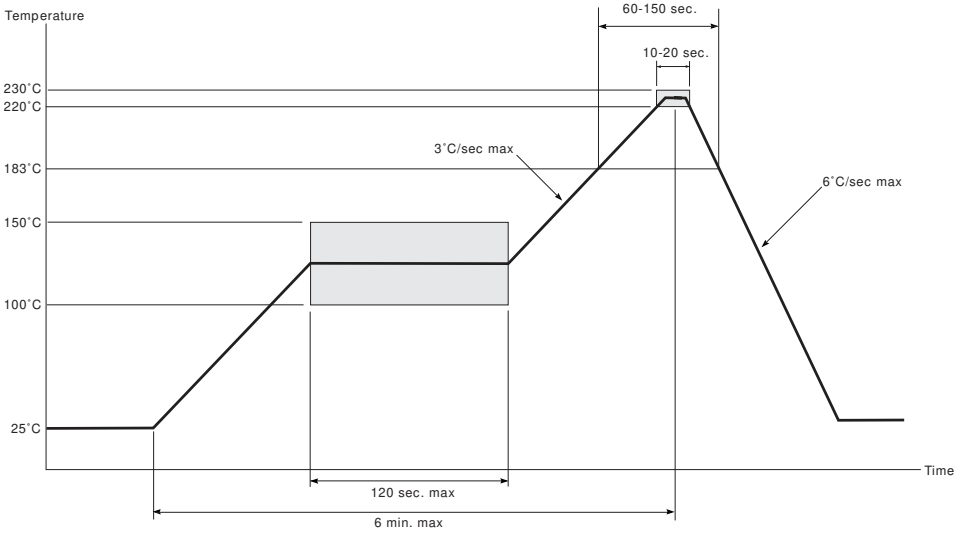


Figure 2-1: Standard Eutectic Solder Reflow Profile

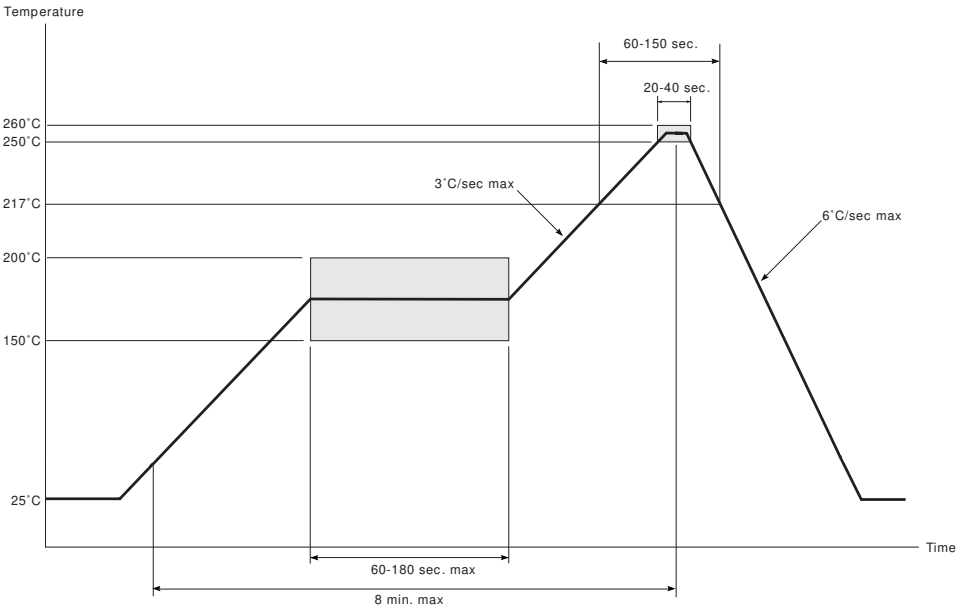


Figure 2-2: Maximum Pb-free Solder Reflow Profile (Pb-free package)

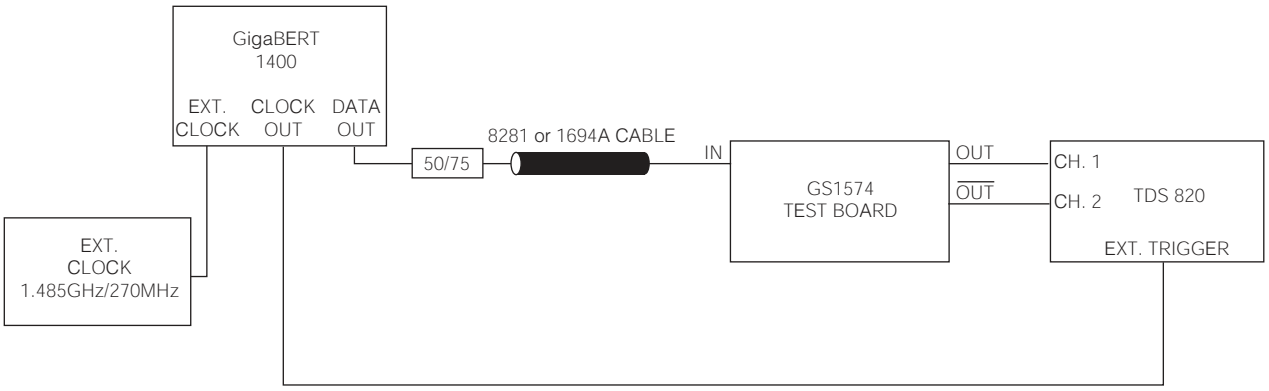


Figure 2-3: Test Circuit

3. Input / Output Circuits

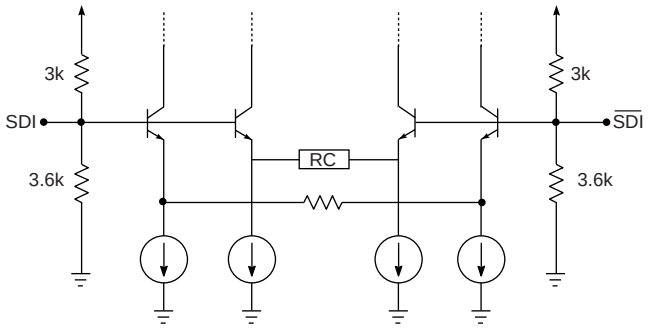


Figure 3-1: Input Equivalent Circuit

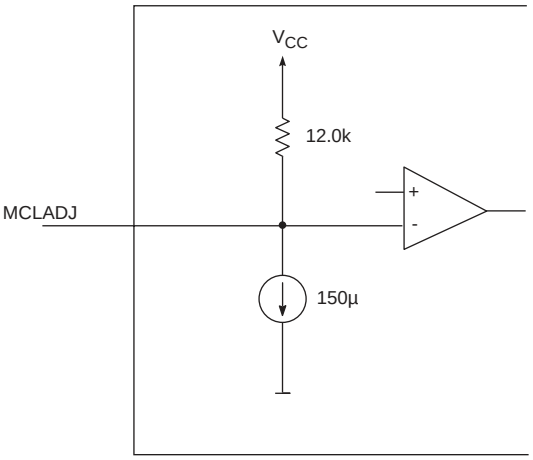


Figure 3-2: MCLADJ Equivalent Circuit

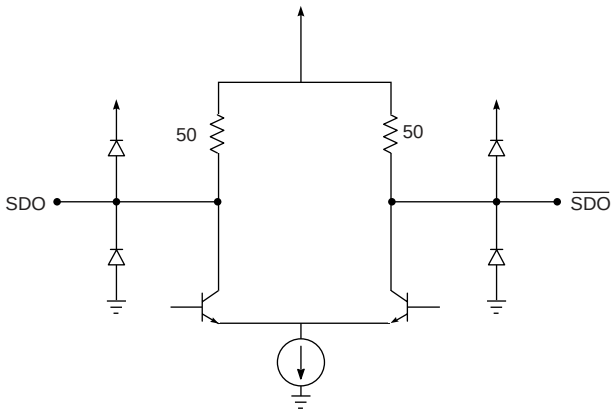


Figure 3-3: Output Circuit

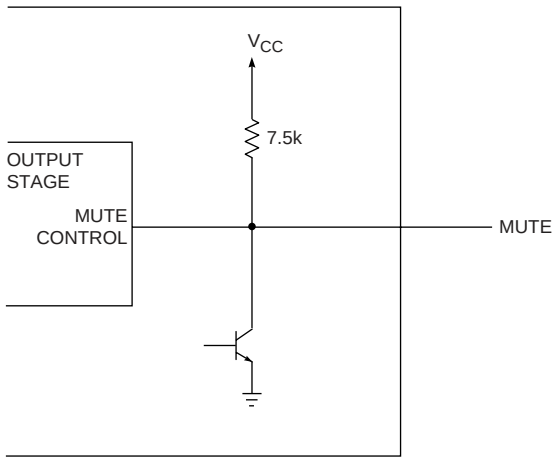


Figure 3-4: MUTE Circuit

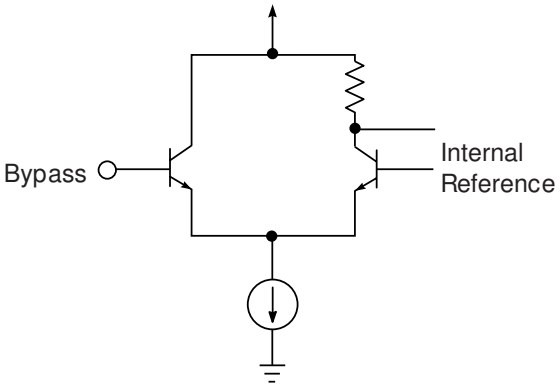


Figure 3-5: Bypass Circuit

4. Detailed Description

The GS1574 is a high speed bipolar IC designed to equalize serial digital signals.

The GS1574 can equalize both HD and SD serial digital signals, and will typically equalize greater than 140m of Belden 1694A cable at 1.485Gb/s and 350m at 270Mb/s.

The GS1574 is powered from a single +3.3V power supply and consumes approximately 270mW of power.

4.1 Serial Digital Inputs

The serial data signal may be connected to the input pins (SDI/$\overline{\text{SDI}}$) in either a differential or single ended configuration. AC coupling of the inputs is recommended, as the SDI and $\overline{\text{SDI}}$ inputs are internally biased at approximately 1.8V.

4.2 Cable Equalization

The input signal passes through a variable gain equalizing stage whose frequency response closely matches the inverse of the cable loss characteristic.

The edge energy of the equalized signal is monitored by a detector circuit which produces an error signal corresponding to the difference between the desired edge energy and the actual edge energy. This error signal is integrated by both an internal and an external AGC filter capacitor providing a steady control voltage for the gain stage. As the frequency response of the gain stage is automatically varied by the application of negative feedback, the edge energy of the equalized signal is kept at a constant level which is representative of the original edge energy at the transmitter. The equalized signal is also DC restored, effectively restoring the logic threshold of the equalized signal to its correct level independent of shifts due to AC coupling. The digital output signals have a nominal voltage of 750mV$_{pp}$ differential, or 375mV$_{pp}$ single ended when terminated with 50Ω as shown in Figure 4-1.

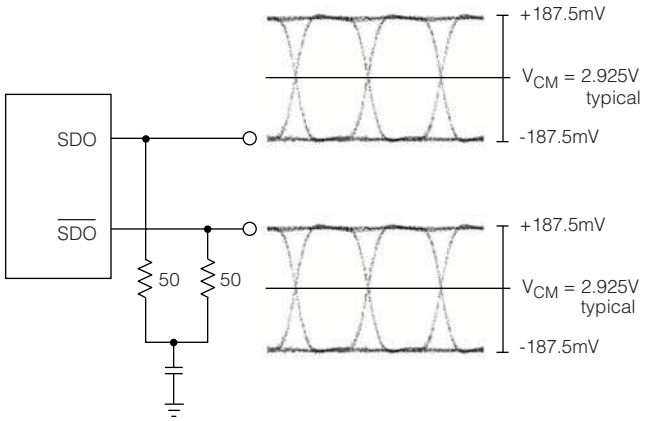


Figure 4-1: Typical Output Voltage Levels

4.3 Programmable Mute Output

For SMPTE 259M inputs, the GS1574 incorporates a programmable threshold output mute (MCLADJ).

In applications where there are multiple input channels using the GS1574, it is advantageous to have a programmable mute output to avoid signal crosstalk.

The output of the GS1574 can be muted when the input signal decreases below a certain input level. This threshold is determined using the input voltage applied to the MCLADJ pin. The MCLADJ pin may be left unconnected for applications where output muting is not required.

This feature has been designed for use in applications such as routers where signal crosstalk and circuit noise cause the equalizer to output erroneous data when no input signal is present. The use of a Carrier Detect function with a fixed internal reference does not solve this problem since the signal to noise ratio on the circuit board could be significantly less than the default signal detection level set by the on chip reference.

NOTE: MCLADJ is only recommended for data rates up to 360Mb/s. For data rates above this MCLADJ should be left floating.

4.4 Mute

In addition to the programmable mute output, the GS1574 includes a MUTE input pin that allows the application interface to mute the serial digital output at any time. Set the MUTE pin HIGH to mute SDO and $\overline{\text{SDO}}$.

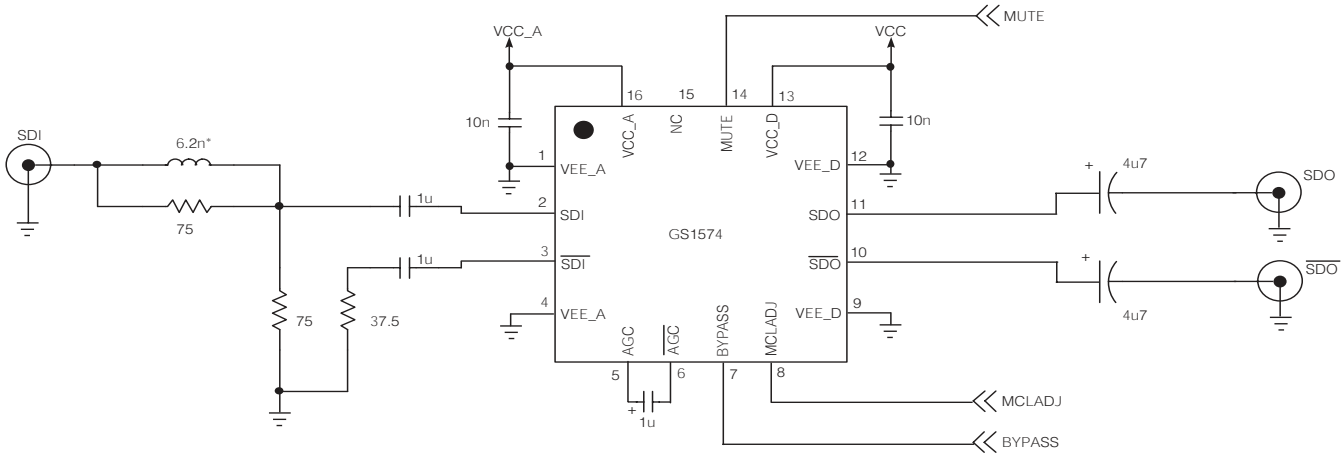
5. Application Information

5.1 PCB Layout

Special attention must be paid to component layout when designing serial digital interfaces for HDTV. An FR-4 dielectric can be used, however, controlled impedance transmission lines are required for PCB traces longer than approximately 1cm. Note the following PCB artwork features used to optimize performance:

- PCB trace width for HD rate signals is closely matched to SMT component width to minimize reflections due to change in trace impedance.
- The PCB ground plane is removed under the GS1574 input components to minimize parasitic capacitance.
- The PCB ground plane is removed under the GS1574 output components to minimize parasitic capacitance.
- High speed traces are curved to minimize impedance changes.

5.2 Typical Application Circuit A

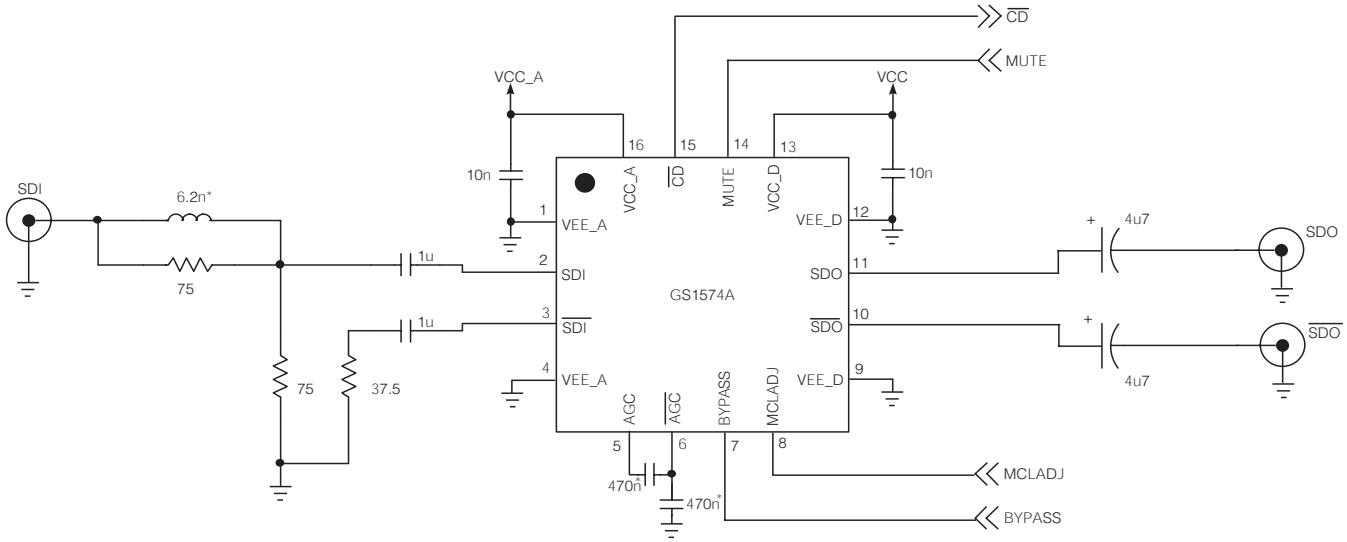


NOTE: All resistors in Ohms, capacitors in Farads, and inductors in Henrys, unless otherwise noted.
* Value dependent on layout

Figure 5-1: GS1574 Typical Application Circuit

5.3 Typical Application Circuit B

This application circuit should be used for future compatibility with the GS1574A. This circuit will work with GS1574 as well as the GS1574A and is recommended for all new designs.

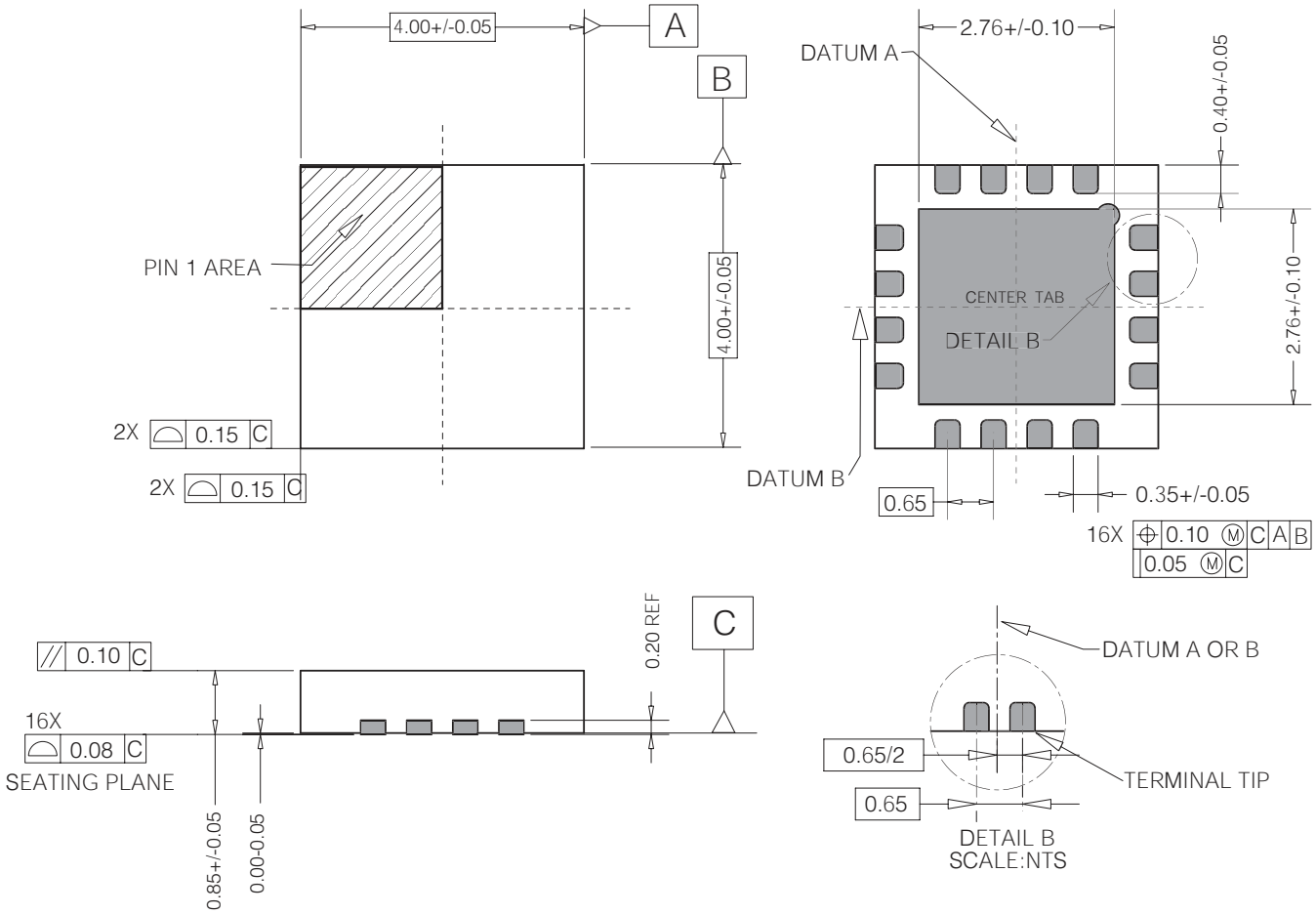


* Value subject to change.

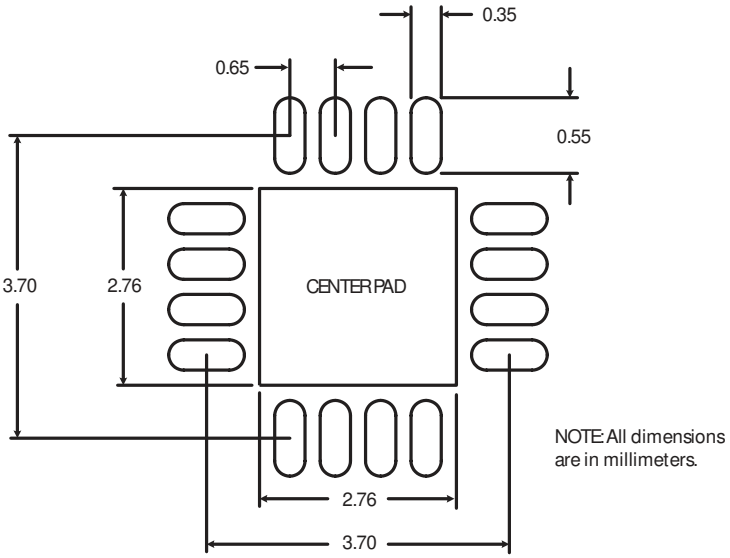
NOTE: All resistors in Ohms, capacitors in Farads, and inductors in Henrys, unless otherwise noted.
* Value dependent on layout

6. Package & Ordering Information

6.1 Package Dimensions



6.2 Land Information



The Center Pad should be connected to the most negative power supply plane for analog circuitry in the device (VEE_A) by a minimum of 5 vias.

NOTE: Suggested dimensions only. Final dimensions should conform to customer design rules and process optimizations.

6.3 Packaging Data

Parameter	Value
Package Type	4mm x 4mm 16-pin QFN
Package Drawing Reference	JEDEC M0220
Moisture Sensitivity Level	3
Junction to Case Thermal Resistance, θ_{j-c}	31.0°C/W
Junction to Air Thermal Resistance, θ_{j-a} (at zero airflow)	43.8°C/W
Psi	11.0°C/W
Pb-free and RoHS Compliant	Yes

6.4 Marking Diagram

6.5 Ordering Information

Part Number	Package	Temperature Range
GS1574-CNE3	Pb-free 16-pin QFN	0°C to 70°C

7. Revision History

Version	ECR	PCN	Date	Changes and/or Modifications
0	134166	–	August 2004	Upgrade to preliminary data sheet. Remove all information on the GS9074. Expand detailed description information. AC/DC parameters updated. Add Pb-free and conventional solder reflow profiles. Edit pin descriptions.
1	134891	–	November 2004	Added packaging data section. Added Pad Layout information. Updated Packaging Dimensions diagram. Corrected minor typing errors.
2	135370	–	December 2004	Added Typical Application Circuit section with application information for future drop-in compatibility with GS1574A part.
3	140439	39461	May 2006	Convert to Data Sheet. Modified inductor value in Application Information. Amended notes on MCLADJ above 360 Mb/s. Changed Green references to RoHS. Corrected typing errors in Package Dimensions.
4	142113	40438	September 2006	Modified format for output cable length jitter data in AC Electrical Characteristics.
5	145127	43739	May 2007	Updated Package Dimensions diagram. Added section 6.4 Marking Diagram.

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