

Dual N-Channel, Digital FET

FDG6301N-F085

Features

- 25 V, 0.22 A Continuous, 0.65 A Peak
- $R_{DS(ON)} = 4 \Omega @ V_{GS} = 4.5 \text{ V}$,
- $R_{DS(ON)} = 5 \Omega @ V_{GS} = 2.7 \text{ V}$.
- Very Low Level Gate Drive Requirements allowing Directop–
eration in 3 V Circuits ($V_{GS(th)} < 1.5 \text{ V}$)
- Gate–Source Zener for ESD Ruggedness ($>6 \text{ kV}$ Human Body
Model)
- Compact Industry Standard SC70–6 Surface Mount Package.
- AEC–Q101 Qualified and PPAP Capable
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS
Compliant

Applications

- Low Voltage Applications as a Replacement for Bipolar Digital
Transistors and Small Signal MOSFETs

MOSFET MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	25	V
V_{GS}	Gate to Source Voltage	8	V
I_D	Drain Current Continuous	0.22	A
	Pulsed	0.65	
P_D	Power Dissipation	0.3	W
T_J, T_{STG}	Operating and Storage Temperature	–55 to 150	$^\circ\text{C}$
ESD	Electrostatic Discharge Rating MIL–STD–883D Human Body Model (100 pF / 1500 W)	6.0	kV
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	415	$^\circ\text{C/W}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. $R_{\theta JA}$ is the sum of the junction–to–case and case–to–ambient thermal resistance, where the case thermal reference is defined as the Solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. $R_{\theta JA} = 415 \text{ }^\circ\text{C/W}$ on minimum pad mounting on FR–4 board in still air.
2. A suffix as “...F085P” has been temporarily introduced in order to manage a double source strategy as ON Semiconductor has officially announced in August 2014.
3. Pulse Test: Pulse Width $< 300 \mu\text{s}$, Duty Cycle $< 2.0\%$

ORDERING INFORMATION

Device	Device Marking	Package	Shipping†
FDG6301N–F085	FDG6301N	SC–88 (SC–70 6 Lead) (Pb–Free, Halogen Free)	3,000 units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

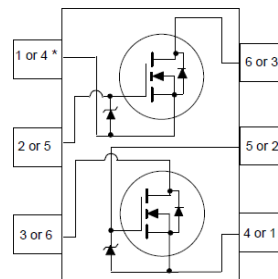


ON Semiconductor®

www.onsemi.com



SC–88 (SC–70 6 Lead), 1.25x2
CASE 419AD



FDG6301N-F085

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

Drain to Source Breakdown Voltage	B _{VDSS}	I _D = 250 μ A, V _{GS} = 0 V	25			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V			1	μA
					10	
Gate to Source Leakage Current	I _{GSS}	V _{GS} = \pm 8 V			±100	nA

On Characteristics

Gate to Source Threshold Voltage	V _{GS(th)}	V _{GS} = V _{DS} , I _D = 250 μ A	0.65	0.85	1.5	V
Drain to Source On Resistance	r _{DS(on)}	I _D = 0.22 A, V _{GS} = 4.5 V		2.6	4	Ω
		I _D = 0.19 A, V _{GS} = 2.7 V		3.7	5	
		I _D = 0.22 A, V _{GS} = 4.5 V, T _J = 125°C		5.3	7	
On-State Drain Current	I _{D(on)}	V _{GS} = 4.5 V, V _{DS} = 5 V	0.22			
Forward Transconductance	g _{FS}	I _D = 0.22 A, V _{DS} = 5 V		0.2		s

Dynamic Characteristics

Input Capacitance	C _{iss}	V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz		9.5		pF
Output Capacitance	C _{oss}			6		pF
Reverse Transfer Capacitance	C _{rss}			4.5		pF
Total Gate Charge at -4.5 V	Q _{g(TOT)}	V _{GS} = 0 to 4.5 V; V _{DD} = 5 V, I _D = 0.22 A		0.29	0.4	nC
Gate to Source Gate Charge	Q _{gs}	V _{DD} = 5 V, I _D = 0.22 A		0.12		
Gate to Drain "Miller" Charge	Q _{gd}			0.03		

Switching Characteristics

Turn-On Delay Time	t _{d(on)}	V _{DD} = 5 V, I _D = 0.5 A, V _{GS} = 4.5 V, R _{GEN} = 50 Ω		5	10	ns
Rise Time	t _r			4.5	10	ns
Turn-Off Delay Time	t _{d(off)}			4	8	ns
Fall Time	t _f			3.2	7	ns

Drain-Source Diode Characteristics

Maximum Continuous Source Current	I _S				0.25	A
Source to Drain Diode Voltage	V _{SD}	I _{SD} = 0.25 A, V _{GS} = 0 V		0.8	1.2	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

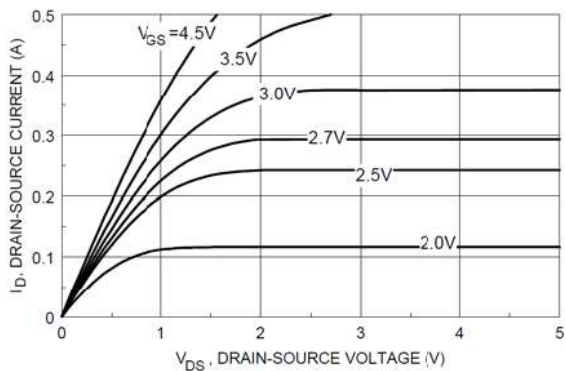


Figure 1. On-Region Characteristics

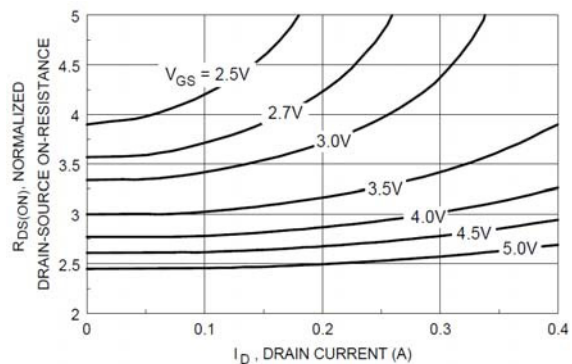


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

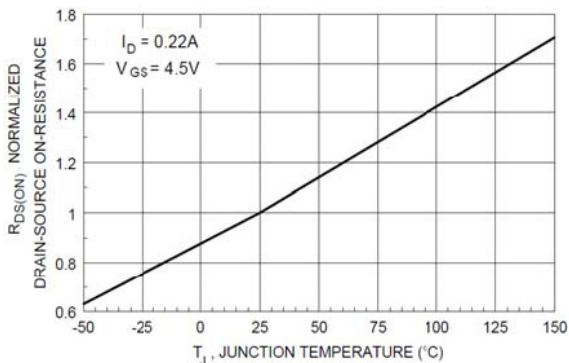


Figure 3. On-Resistance Variation with Temperature

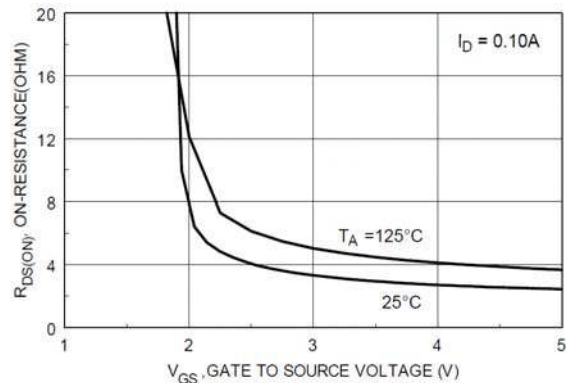


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

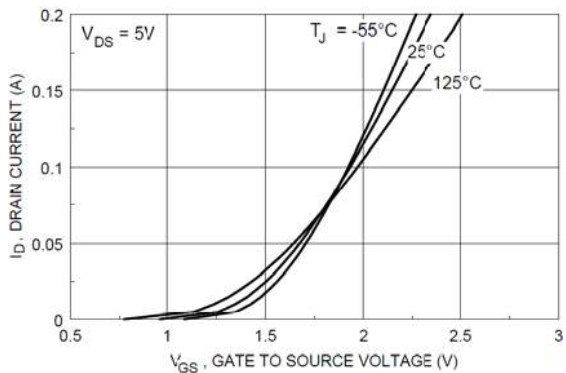


Figure 5. Transfer Characteristics

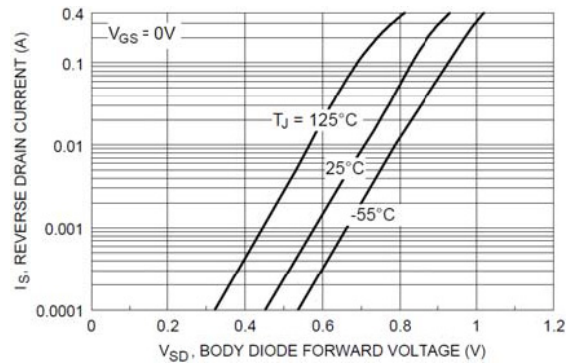


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL CHARACTERISTICS

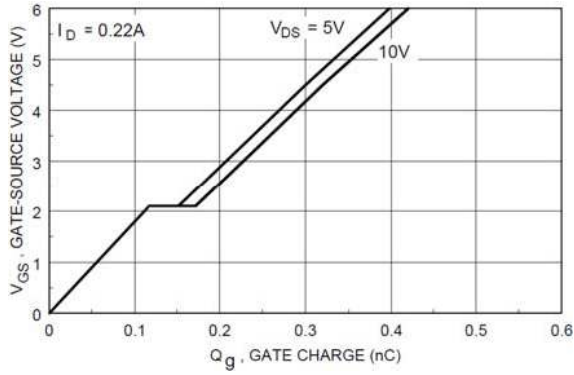


Figure 7. Gate Charge Characteristics

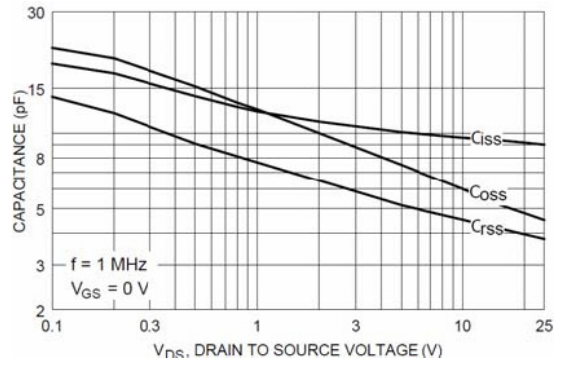


Figure 8. Capacitance Characteristics

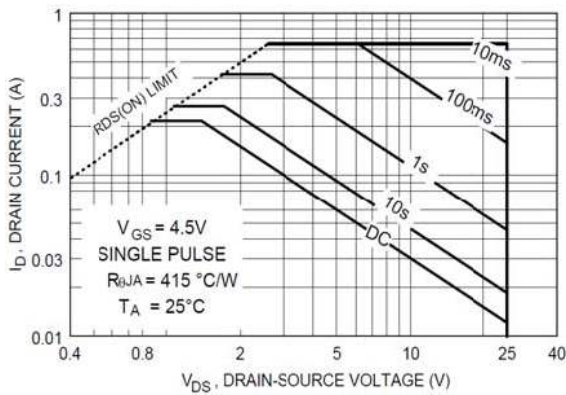


Figure 9. Maximum Safe Operating Area

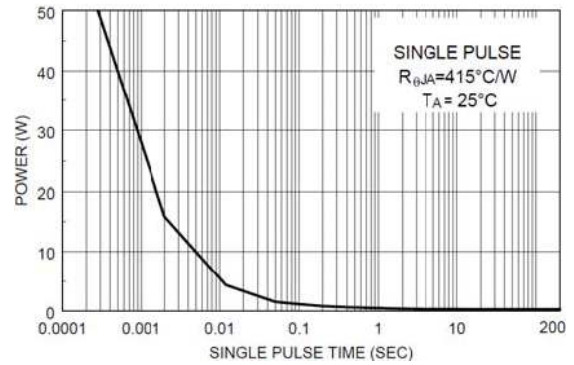


Figure 10. Single Pulse Maximum Power Dissipation

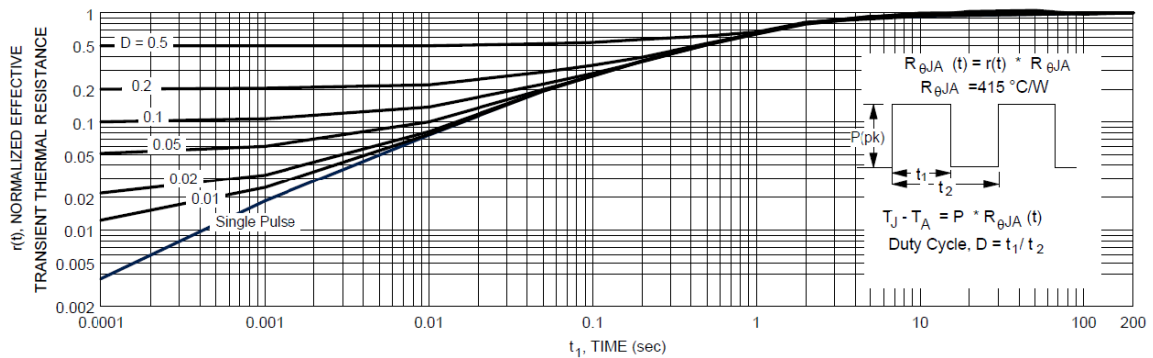
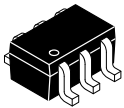


Figure 11. Transient Thermal Response Curve

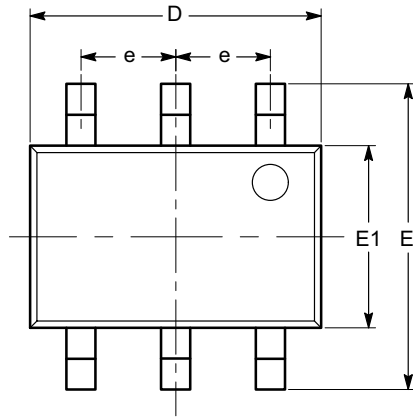
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



1

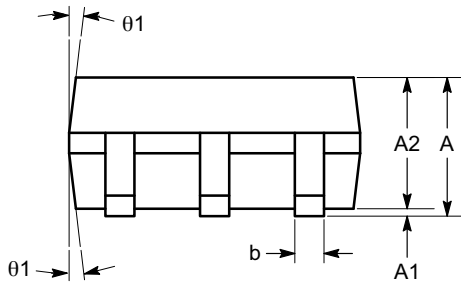
SC-88 (SC-70 6 Lead), 1.25x2
CASE 419AD
ISSUE A

DATE 07 JUL 2010

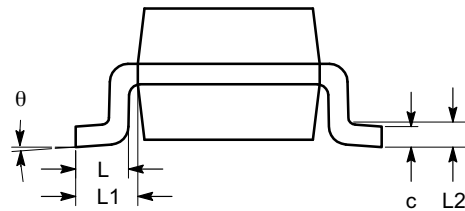


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	0.80		1.10
A1	0.00		0.10
A2	0.80		1.00
b	0.15		0.30
c	0.10		0.18
D	1.80	2.00	2.20
E	1.80	2.10	2.40
E1	1.15	1.25	1.35
e	0.65 BSC		
L	0.26	0.36	0.46
L1	0.42 REF		
L2	0.15 BSC		
θ	0°		8°
θ_1	4°		10°



SIDE VIEW



END VIEW

Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MO-203.

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