



# PJU18N20 / PJD18N20 / PJP18N20 / PJF18N20

## 200V N-Channel Enhancement Mode MOSFET

**Voltage**

**200 V**

**Current**

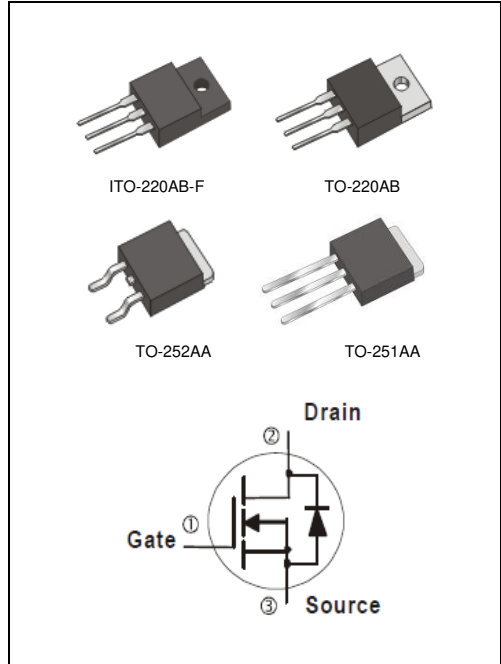
**18 A**

### Features

- $R_{DS(ON)}$ ,  $V_{GS}@10V, I_D@9A < 160m\Omega$
- High switching speed
- Improved dv/dt capability
- Low Gate Charge
- Low reverse transfer capacitance
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

### Mechanical Data

- Case : TO-251AA, TO-252AA, TO-220AB, ITO-220AB-F Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- TO-251AA Approx. Weight : 0.0104 ounces, 0.297grams
- TO-252AA Approx. Weight : 0.0105 ounces, 0.297grams
- TO-220AB Approx. Weight : 0.067 ounces, 1.89 grams
- ITO-220AB-F Approx. Weight : 0.068 ounces, 2 grams



### Maximum Ratings and Thermal Characteristics ( $T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	TO-251AA TO-252AA	TO-220AB	ITO-220AB-F	UNITS	
Drain-Source Voltage	$V_{DS}$	200			V	
Gate-Source Voltage	$V_{GS}$	$\pm 20$				
Continuous Drain Current	$I_D$	$T_C=25^\circ\text{C}$	18		A	
		$T_C=100^\circ\text{C}$	11			
Pulsed Drain Current <sup>(Note 1)</sup>	$I_{DM}$	72				
Power Dissipation	$P_D$	$T_C=25^\circ\text{C}$	83	89	50	W
		$T_C=100^\circ\text{C}$	33	35.6	20	
Single Pulse Avalanche Energy <sup>(Note 6)</sup>	$E_{AS}$	72			mJ	
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55~150			$^\circ\text{C}$	
Typical Thermal Resistance <sup>(Note 4,5)</sup>	$R_{\theta JC}$ $R_{\theta JA}$	1.5 110	1.4 62.5	2.5 120	$^\circ\text{C/W}$	
- Junction to Case						
- Junction to Ambient						

- Limited only By Maximum Junction Temperature



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### Electrical Characteristics ( $T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
<b>Static</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	200	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1	1.83	3	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=9A$	-	126	160	m $\Omega$
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=200V, V_{GS}=0V$	-	-	1.0	$\mu A$
Gate-Source Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>Dynamic</b> (Note 7)						
Total Gate Charge	$Q_g$	$V_{DS}=160V, I_D=18A,$ $V_{GS}=10V$ (Note 2,3)	-	24	-	nC
Gate-Source Charge	$Q_{gs}$		-	3.7	-	
Gate-Drain Charge	$Q_{gd}$		-	6.1	-	
Input Capacitance	$C_{iss}$	$V_{DS}=25V, V_{GS}=0V,$ $f=1.0\text{MHz}$	-	1017	-	pF
Output Capacitance	$C_{oss}$		-	148	-	
Reverse Transfer Capacitance	$C_{rss}$		-	36	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD}=100V, I_D=18A,$ $V_{GS}=10V, R_G=25\Omega$ (Note 2,3)	-	15	-	ns
Turn-On Rise Time	$t_r$		-	61	-	
Turn-Off Delay Time	$t_{d(off)}$		-	104	-	
Turn-Off Fall Time	$t_f$		-	99	-	
<b>Drain-Source Diode</b>						
Maximum Continuous Drain-Source Diode Forward Current	$I_S$	---	-	-	18	A
Maximum Pulsed Drain-Source Diode Forward Current	$I_{SM}$	---	-	-	72	
Diode Forward Voltage	$V_{SD}$	$I_S=1A, V_{GS}=0V$	-	0.73	1.0	V

**NOTES :**

1. Pulse width  $\leq 300\mu s$ , Duty cycle  $\leq 2\%$
2. Essentially independent of operating temperature typical characteristics.
3. Repetitive rating, pulse width limited by junction temperature  $T_{J(MAX)}=150^\circ\text{C}$ . Ratings are based on low frequency and duty cycles to keep initial  $T_J=25^\circ\text{C}$ .
4. The maximum current rating is package limited.
5.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch<sup>2</sup> with 2oz. square pad of copper.
6. The test condition is  $L=1\text{mH}$ ,  $I_{AS}=12A$ ,  $V_{DD}=50V$ ,  $R_G=25\text{ohm}$ , Starting  $T_J=25^\circ\text{C}$
7. Guaranteed by design, not subject to production testing.



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## TYPICAL CHARACTERISTIC CURVES

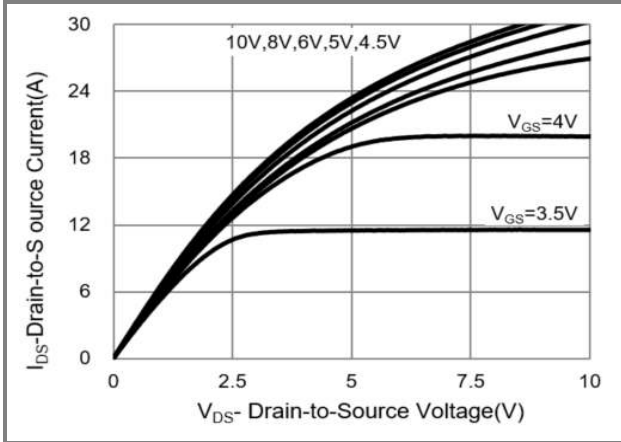


Fig.1 Output Characteristics

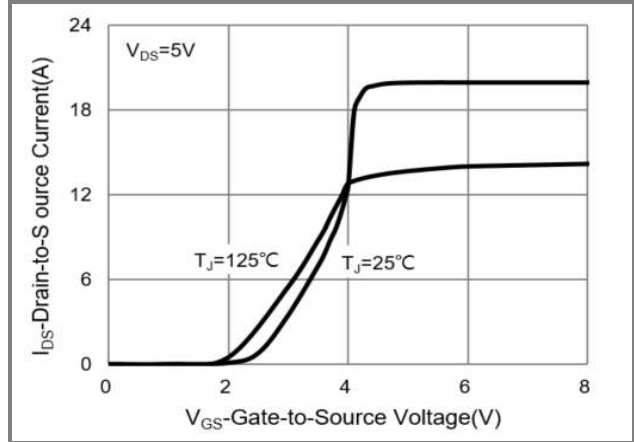


Fig.2 Transfer Characteristics

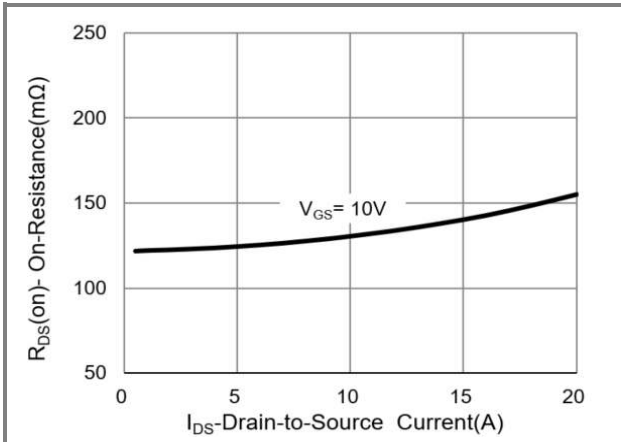


Fig.3 On-Resistance vs. Drain Current

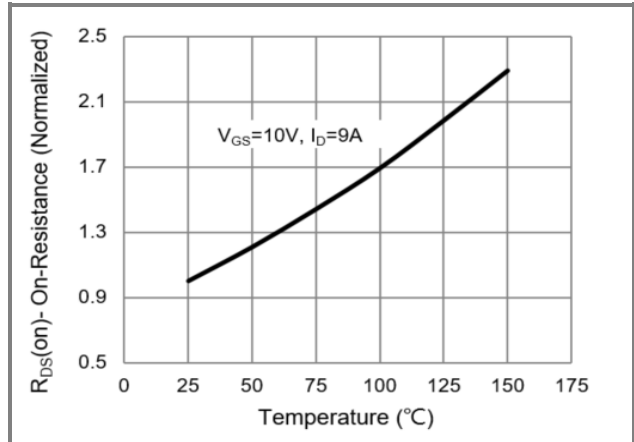


Fig.4 On-Resistance vs. Junction temperature

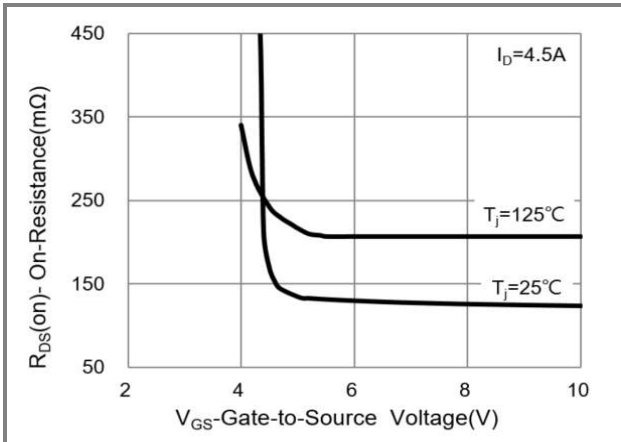


Fig.5 On-Resistance Variation with VGS

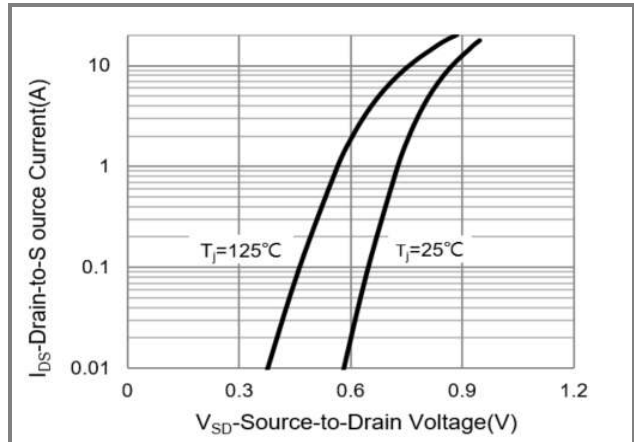


Fig.6 Source-Drain Diode Forward Voltage



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## TYPICAL CHARACTERISTIC CURVES

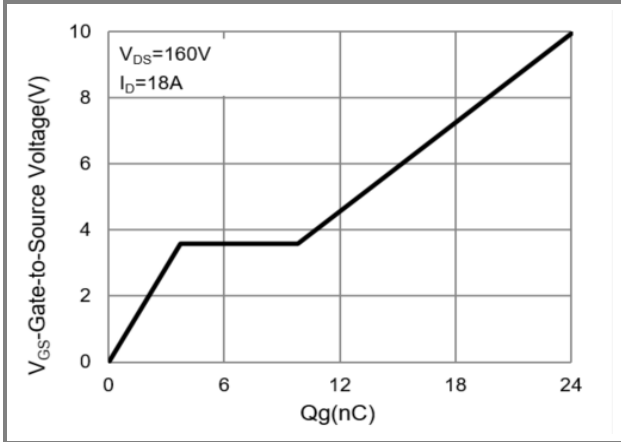


Fig.7 Gate-Charge Characteristics

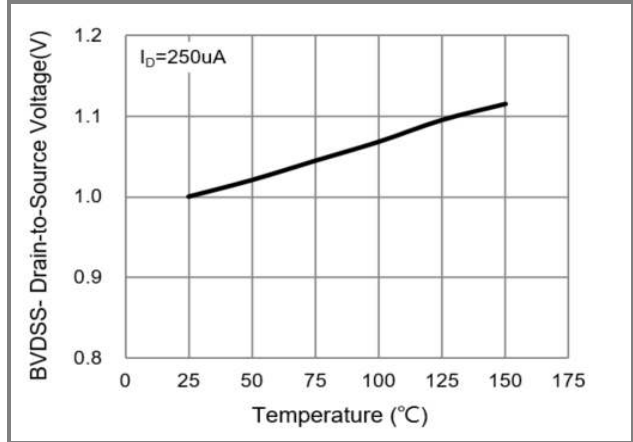


Fig.8 Breakdown Voltage Variation vs. Temperature

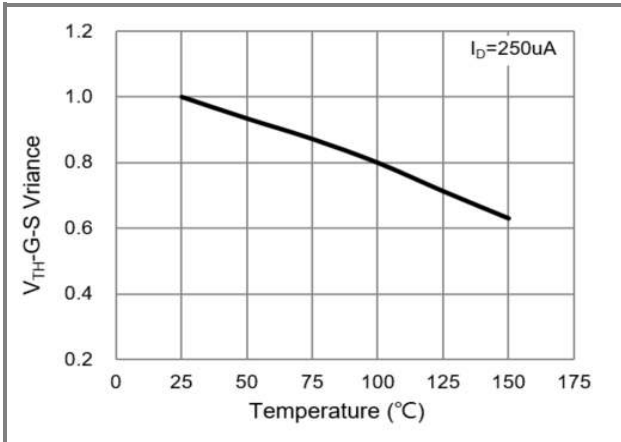


Fig.9 Threshold Voltage Variation with Temperature

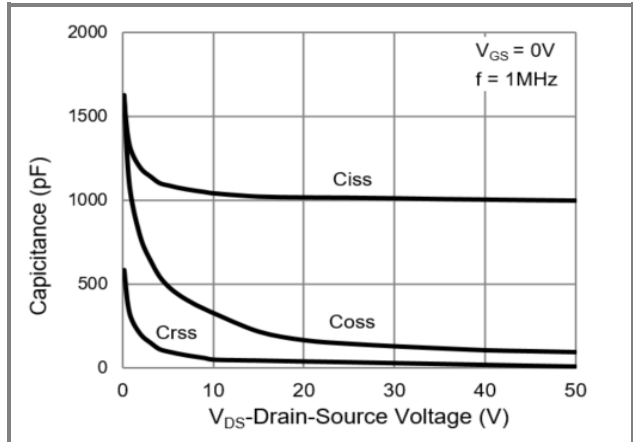


Fig.10 Capacitance vs. Drain-Source Voltage

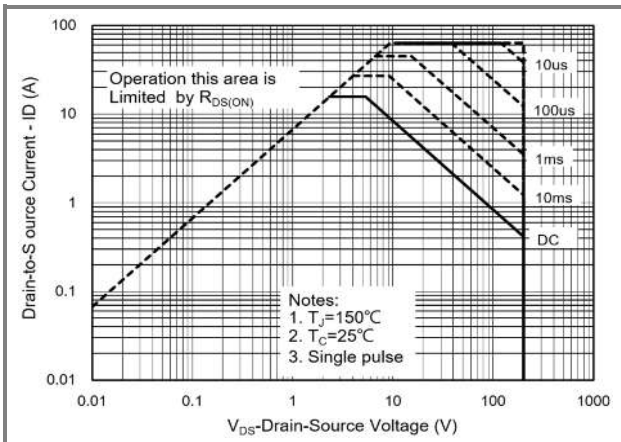


Fig.11 PJU/PJD Maximum Safe Operating Area

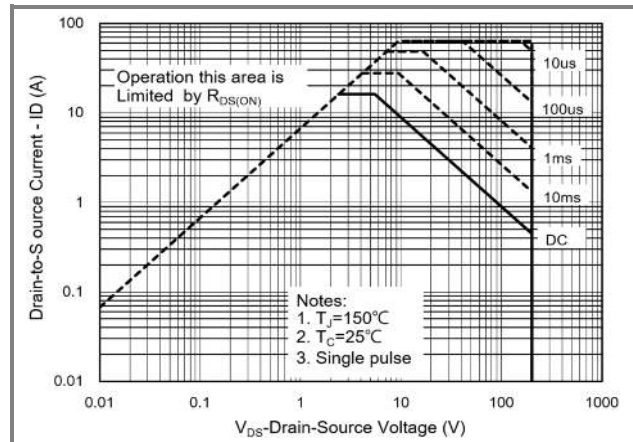


Fig.12 PJP18N20 Maximum Safe Operating Area



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## TYPICAL CHARACTERISTIC CURVES

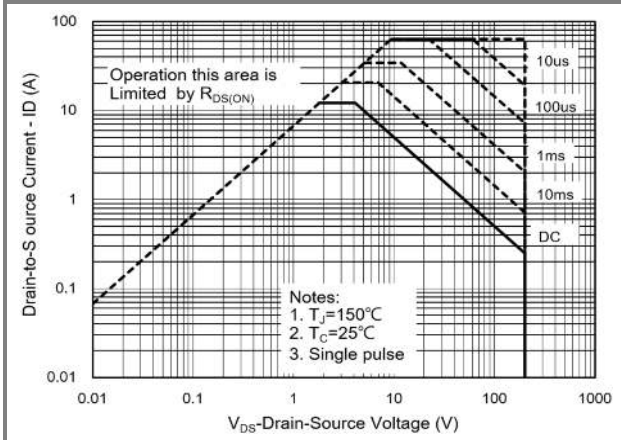


Fig.13 PJF18N20 Maximum Safe Operating Area

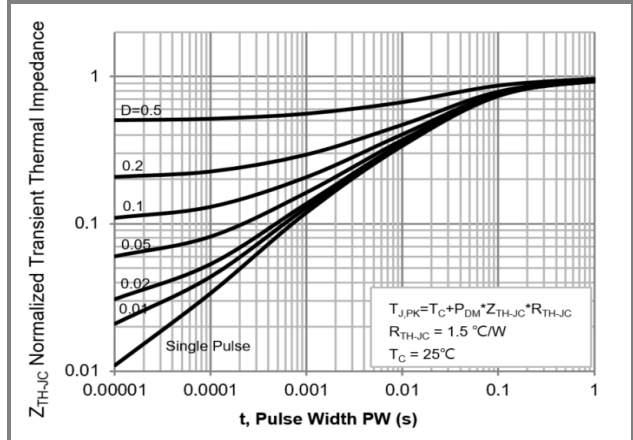


Fig.14 PJU/D Normalized Transient Thermal Impedance

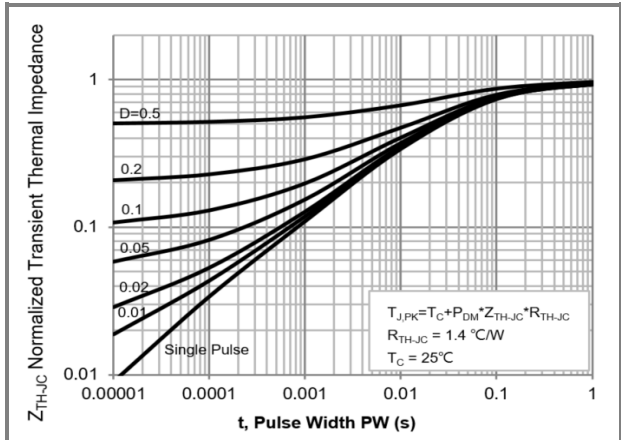


Fig.15 PJP Normalized Transient Thermal Impedance

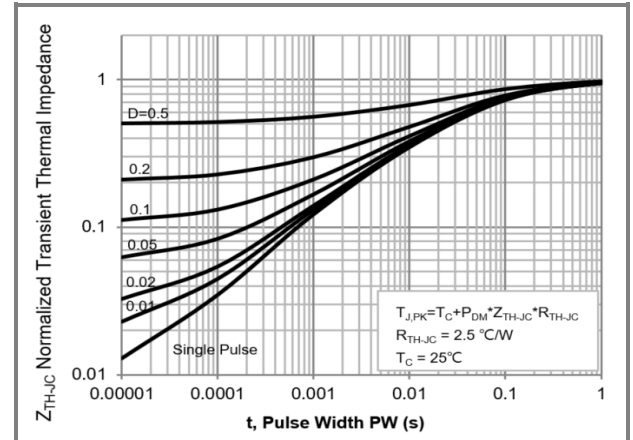
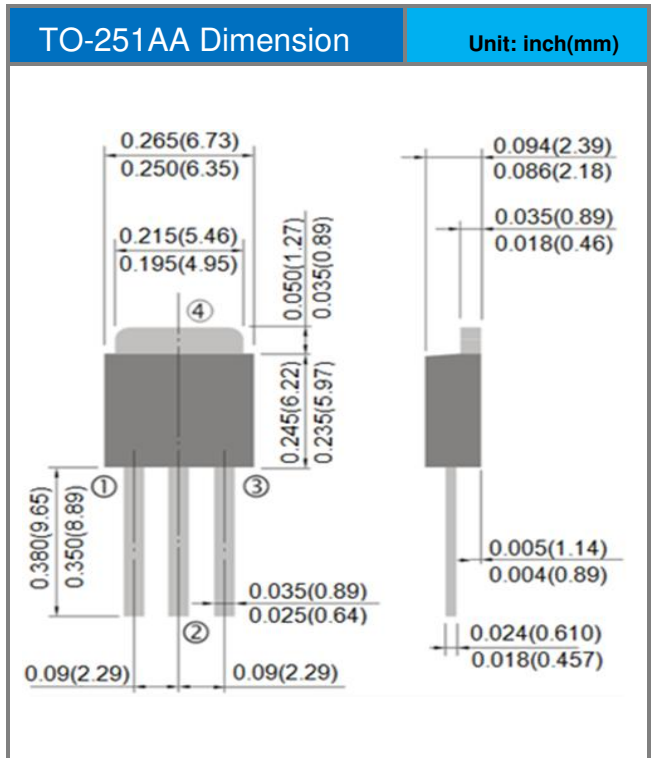
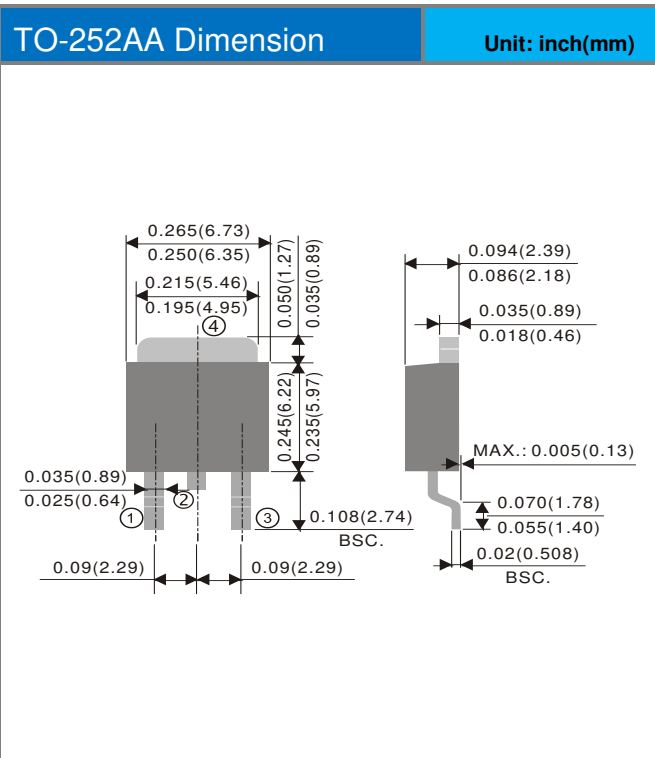
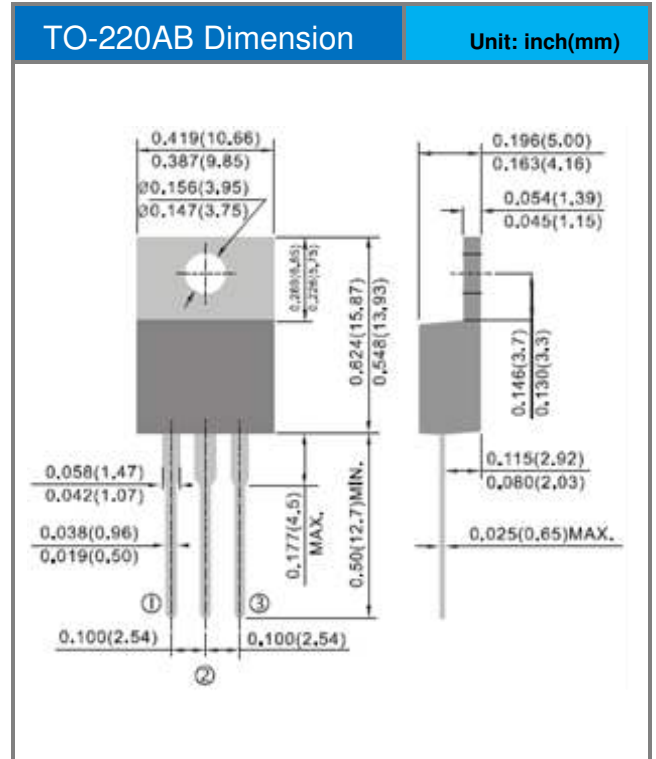
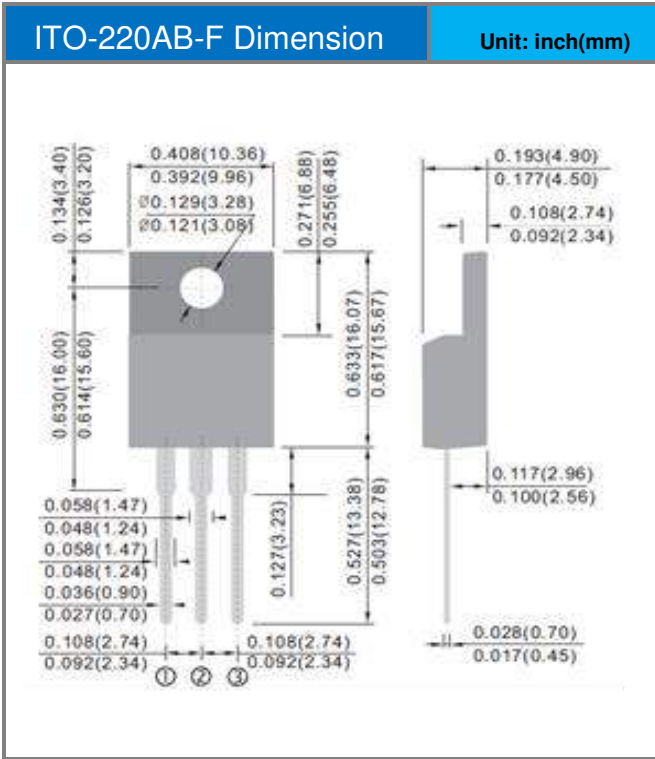


Fig.16 PJF Normalized Transient Thermal Impedance



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## Packaging Information



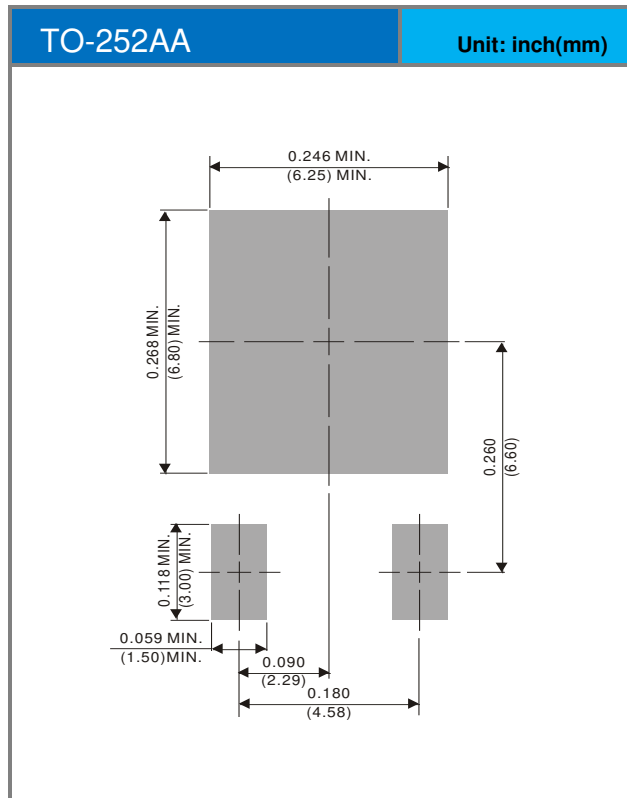


# PJU18N20 / PJD18N20 / PJP18N20 / PJF18N20

## Part No Packing Code Version

Part No Packing Code	Package Type	Packing Type	Marking	Version
PJU18N20_T0_00001	TO-251AA	80pcs / Tube	U18N20	Halogen free
PJD18N20_L2_00001	TO-252AA	3,000pcs / 13" reel	D18N20	Halogen free
PJP18N20_T0_00001	TO-220AB	50pcs / Tube	P18N20	Halogen free
PJF18N20_T0_00001	ITO-220AB-F	50pcs / Tube	F18N20	Halogen free

## Mounting Pad Layout





## **PJU18N20 / PJD18N20 / PJP18N20 / PJF18N20**

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