TPS7A39 Dual, 150-mA, Wide V_{IN} Positive and Negative LDO Voltage Regulator

1 Features

- Positive and Negative LDOs in One Package
- Wide Input Voltage Range: ±3.3 V to ±33 V
- Wide Output Voltage Range:
  - Positive Range: 1.2 V to 30 V
  - Negative Range: –30 V to 0 V
- Output Current: 150 mA per Channel
- Monotonic Start-Up Tracking
- High Power-Supply Rejection Ratio (PSRR):
  - 69 dB (120 Hz)
  - ≥ 50 dB (10 Hz to 2 MHz)
- Output Voltage Noise: 21 μV_{RMS} (10 Hz–100 kHz)
- Buffered 1.2-V Reference Output
- Stable With a 10-µF or Larger Output Capacitor
- Single Positive-Logic Enable
- Adjustable Soft-Start In-Rush Control
- 3-mm × 3-mm, 10-Pin WSON Package
- Low Thermal Resistance: $R_{\theta JA}$ = 44.4°C/W
- Operating Temperature Range: –40 to +125°C

2 Applications

- Supply Rails for Op Amps, ADCs, DACs, and Other High-Precision Analog Circuitry
- Post DC-DC Regulation and Filtering
- Analog I/O Modules
- Test and Measurement
- Rx, Tx, and PA Circuitry
- Industrial Instrumentation
- Medical Imaging

3 Description

The TPS7A39 device is a dual, monolithic, high-PSRR, positive and negative low-dropout (LDO) voltage regulator capable of sourcing (and sinking) up to 150 mA of current. The regulated outputs can be independently and externally adjusted to symmetrical or asymmetrical voltages, making this device an ideal dual, bipolar power supply for signal conditioning.

Both positive and negative outputs of the TPS7A39 ratiometrically track each other during startup to mitigate floating conditions and other power-supply sequencing issues common in dual-rail systems. The negative output can regulate up to 0 V, extending the common-mode range for single-supply amplifiers. The TPS7A39 also features high PSRR to eliminate power-supply noise, such as switching noise, that can compromise signal integrity.

Both regulators are controlled with a single positive logic enable pin for interfacing with standard digital logic. A capacitor-programmable soft-start function controls in-rush current and start-up time. The internal reference voltage of the TPS7A39 can be overridden with an external reference to enable precision outputs, output voltage margining, or to track other power supplies. Additionally, the TPS7A39 has a buffered reference output that can be used as a voltage reference for other components in the system.

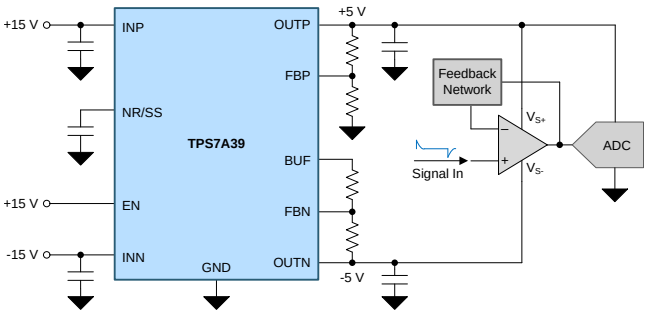
These features make the TPS7A39 a robust, simplified solution to power operational amplifiers, digital-to-analog converters (DACs), and other precision analog circuitry.

Device Information[1]

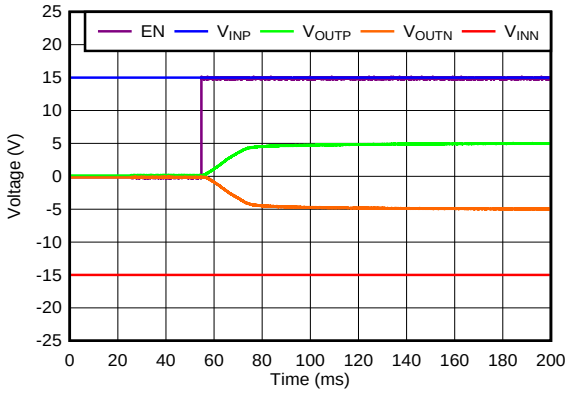
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS7A39	WSON (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Powering the Signal Chain



Monotonic Start-Up Tracking



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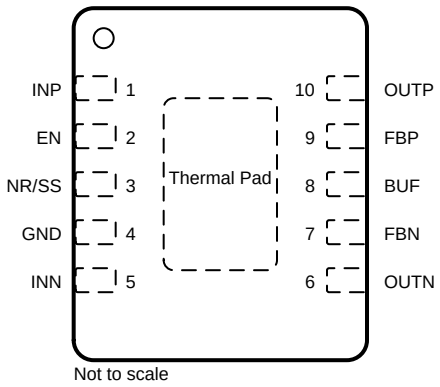
5 Pin Configuration and Functions

DSC Package
10-Pin WSON
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	INP	I	Positive input. A 10-µF(1) or larger capacitor must be tied from this pin to ground to ensure stability. Place the input capacitor as close to the input as possible; see the *Capacitor Recommendations* section for more information.
2	EN	I	Enable pin. Driving this pin to logic high ($V_{EN} \geq V_{IH(EN)}$) enables the device; driving this pin to logic low ($V_{EN} \leq V_{IL(EN)}$) disables the device. If enable functionality is not required, this pin must be connected to INP; see the *Application and Implementation* section for more detail. The enable voltage cannot exceed the input voltage ($V_{EN} \leq V_{INP}$).
3	NR/SS	—	Noise-reduction, soft-start pin. Connecting an external capacitor between this pin and ground reduces reference voltage noise and enables soft-start and start-up tracking. A 10-nF or larger capacitor ($C_{NR/SS}$) is recommended to be connected from NR/SS to GND to maximize or optimize ac performance and to ensure start-up tracking. This pin can also be driven externally to provide greater output voltage accuracy and lower noise, see the *User-Settable Buffered Reference* section for more information.
4	GND	—	Ground pin. This pin must be connected to ground and the thermal pad with a low-impedance connection.
5	INN	I	Negative input. A 10-µF(1) or larger capacitor must be tied from this pin to ground to ensure stability. Place the input capacitor as close to the input as possible; see the *Capacitor Recommendations* section for more information.
6	OUTN	O	Negative output. A 10-µF(1) or larger capacitor must be tied from this pin to ground to ensure stability. Place the output capacitor as close to the output as possible; see the *Capacitor Recommendations* section for more information.
7	FBN	I	Negative output feedback pin. This pin is used to set the negative output voltage. Although not required, a 10-nF feed-forward capacitor from FBN to OUTN (as close to the device as possible) is recommended to maximize ac performance. Nominally this pin is regulated to V_{FBN}. Do not connect to ground.
8	BUF	O	Buffered reference output. This pin is connected to FBN through R_2 and the voltage at this node is inverted and scaled up by the negative feedback network to provide the desired output voltage. The buffered reference can be used to drive external circuits, and has a 1-mA maximum load.
9	FBP	I	Positive output feedback pin. This pin is used to set the positive output voltage. Although not required, a 10-nF feed-forward capacitor from FBP to OUTP (as close to the device as possible) is recommended to maximize ac performance. Nominally this pin is regulated to V_{FBP}. Do not connect this pin directly to ground.
10	OUTP	O	Positive output. A 10-µF(1) or larger capacitor must be tied from this pin to ground to ensure stability. Place the output capacitor as close to the output as possible; see the *Capacitor Recommendations* section for more information.
Pad	Thermal Pad	—	Connect the thermal pad to a large-area ground plane. The thermal pad is internally connected to GND.

(1) The nominal input and output capacitance must be greater than 2.2 µF; throughout this document the nominal derating on these capacitors is 80%. Take care to ensure that the effective capacitance at the pin is greater than 2.2 µF.

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
Voltage	INP	–0.3	36	V
	INN	–36	0.3	
	OUTP	–0.3	V_{INP} + 0.3(3)	
	OUTN	V_{INN} – 0.3(4)	0.3	
	FBP	–0.3	V_{INP} + 0.3(5)	
	BUF	–1	V_{INP} + 0.3(5)	
	NR/SS	–0.3	V_{INP} + 0.3(6)	
	FBN	V_{INN} – 0.3(7)	0.3	
	EN	–0.3	V_{INP} + 0.3(8)	
Current	Output current	Internally limited		
	Buffer current		2	mA
Temperature	Operating junction temperature, T_J	–55	150	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages with respect to the ground pin, unless otherwise noted.
(3) The absolute maximum rating is V_{INP} + 0.3 V or 33 V, whichever is smaller.
(4) The absolute maximum rating is V_{INN} – 0.3 V or –33 V, whichever is greater.
(5) The absolute maximum rating is V_{INP} + 0.3 V or 3 V, whichever is smaller.
(6) The absolute maximum rating is V_{INP} + 0.3 V or 2 V, whichever is smaller.
(7) The absolute maximum rating is V_{INN} – 0.3 V or –3 V, whichever is greater.
(8) The absolute maximum rating is V_{INP} + 0.3 V or 36 V, whichever is smaller.

6.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$\|V_{INx}\|$	Supply voltage magnitude for either regulator	3.3		33	V
V_{EN}	Enable supply voltage	0		V_{INP}	V
V_{OUTP}	Positive regulated output voltage range	V_{FBP}		30	V
V_{OUTN}	Negative regulated output voltage range	–30		V_{FBN}	V
I_{OUTx}	Output current for either regulator	0.005(1)		150	mA
I_{BUF}	Output current from the BUF pin	0	120	1000	µA
C_{INx}	Input capacitor for either regulator	4.7	10(2)		µF
C_{OUTx}	Output capacitor for either regulator	4.7	10(2)		µF
$C_{NR/SS}$	Noise-reduction and soft-start capacitor	0(3)	10	1000	nF
C_{FFP}	Positive channel feed-forward capacitor; connect from V_{OUTP} to FBP	0	10	100	nF
C_{FFN}	Negative channel feed-forward capacitor; connect from V_{OUTN} to FBN	0	10	100	nF
R_{2P}	Lower positive feedback resistor		10	240	kΩ
R_{2N}	Lower negative feedback resistor (from FBN to BUF)		10	240	kΩ
T_J	Operating junction temperature	–40		125	°C

(1) Minimum load required when feedback resistors are not used. If feedback resistors are used, keeping R_{2x} below 240 kΩ satisfies this requirement.
(2) The nominal input and output capacitor value of 10-µF accounts for the derating factors that apply to X5R and X7R ceramic capacitors. The assumed overall derating is 80%.
(3) For startup tracking to function correctly a minimum 4.7-nF $C_{NR/SS}$ capacitor must be used.

6.4 Thermal Information

THERMAL METRIC(1)		TPS7A39 DSC (WSON) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	44.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	33.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	19.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	2.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

at T_J = –40°C to +125°C, $V_{INP(nom)} = V_{OUTP(nom)}$ + 1 V or $V_{IN(nom)}$ = 3.3 V (whichever is greater), $V_{INN(nom)} = V_{OUTN(nom)}$ – 1 V or $V_{INN(nom)}$ = –3.3 V (whichever is less), $V_{EN} = V_{INP}$, I_{OUT} = 1 mA, C_{INx} = 2.2 µF, C_{OUTx} = 10 µF, $C_{FFx} = C_{NR/SS}$ = open, $R_{1N} = R_{2N}$ = 10 kΩ, and FBP tied to OUTP (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{INP}	Input voltage range, positive channel			3.3		33	V
V_{INN}	Input voltage range, negative channel			–33		–3.3	V
$V_{UVLOP(rising)}$	Undervoltage lockout threshold, positive channel		V_{INP} rising, V_{INN} = –3.3 V	1.4		3.1	V
$V_{UVLOP(hys)}$	Undervoltage lockout threshold, positive channel hysteresis		V_{INP} falling, V_{INN} = –3.3 V		120		mV
$V_{UVLON(falling)}$	Undervoltage lockout threshold, negative channel		V_{INN} falling, V_{INP} = 3.3 V	–3.1		–1.4	V
$V_{UVLON(hys)}$	Undervoltage lockout threshold, negative channel, hysteresis		V_{INN} rising, V_{INP} = 3.3 V		70		mV
$V_{NR/SS}$	Internal reference voltage			1.172	1.19	1.208	V
V_{FBP}	Positive feedback voltage			1.170	1.188	1.206	V
V_{FBN}	Negative feedback voltage			–10	3.7	10	mV
V_{OUT}	Output voltage range[1]	Positive channel		V_{FBP}		30	V
		Negative channel		–30		V_{FBN}[2]	
	V_{OUTP} accuracy		$V_{INP(nom)} \le V_{INP} \le 33$ V, 1 mA $\le I_{OUTP} \le$ 150 mA, 1.2 V $\le V_{OUTP(nom)} \le$ 30 V	–1.5		1.5	$\%V_{OUT}$
	V_{OUTN} accuracy[3]		–33 V $\le V_{INN} \le V_{INN(nom)}$, –150 mA $\le I_{OUTN} \le$ –1 mA, –30 V $\le V_{OUTN(nom)} \le$ –1.2 V	–3		3	$\%V_{OUT}$
	Negative V_{OUT} channel accuracy		–33 V $\le V_{INN} \le V_{INN(nom)}$, –150 mA $\le I_{OUTN} \le$ 1 mA, –1.2 V < $V_{OUTN(nom)}$ < 0 V	–36		36	mV
			–33 V $\le V_{INN} \le V_{INN(nom)}$, –150 mA $\le I_{OUTN} \le$ 1 mA, $V_{OUTN(nom)}$ = 0 V	–12		12	
$\Delta V_{OUT}(\Delta V_{IN}) / V_{OUT(NOM)}$	Line regulation, positive channel		$V_{INP(nom)} \le V_{INP} \le 33$ V		0.035		$\%V_{OUT}$
	Line regulation, negative channel		–33 V $\le V_{INN} \le V_{OUT(nom)}$ + 1 V		0.125		
$\Delta V_{OUT}(\Delta I_{OUT}) / V_{OUT(NOM)}$	Load regulation, positive channel		1 mA $\le I_{OUTP} \le$ 150 mA		–0.09		$\%V_{OUT}$
	Load regulation, negative channel		–150 mA $\le I_{OUTN} \le$ –1 mA		0.715		
V_{DO}	Dropout voltage	Positive channel	I_{OUTP} = 50 mA, 3.3 V $\le V_{INP(nom)} \le$ 33.0 V, V_{FBP} = 1.070 V		175	300	mV
			I_{OUTP} = 150 mA, 3.3 V $\le V_{INP(nom)} \le$ 33.0 V, V_{FBP} = 1.070 V		300	500	
		Negative channel	I_{OUTN} = –50 mA, –3.3 V $\le V_{INN(nom)} \le$ –33.0 V, V_{FBN} = 0.0695 V	–250	–145		
			I_{OUTN} = –150 mA, –3.3 V $\le V_{INN(nom)} \le$ –33.0 V, V_{FBN} = 0.0695 V	–400	–275		
V_{BUF}	Buffered reference output voltage				$V_{NR/SS}$		V
V_{BUF}/I_{BUF}	Buffered reference load regulation		I_{BUF} = 100 µA to 1 mA		1		mV/mA
$V_{BUF} - V_{NR/SS}$	Output buffer offset voltage		$V_{NR/SS}$ = 0.25 V to 1.2 V	–4	3	8	mV
V_{OUTP}–V_{OUTN}	DC output voltage difference with a forced REF voltage		$V_{NR/SS}$ = 0.25 V to 1.2 V	–10		10	$\%V_{NR/SS}$
I_{LIM}	Current limit	Positive channel	V_{OUTP} = 90% $V_{OUTP(nom)}$	200	330	500	mA
		Negative channel	V_{OUTN} = 90% $V_{OUTN(nom)}$	–500	–300	–200	
I_{SUPPLY}	Supply current	Positive channel	I_{OUTP} = 0 mA, R_{2N} = open, V_{INP} = 33 V		75	150	µA
			I_{OUTP} = 150 mA, R_{2N} = open, V_{INP} = 33 V		904		
		Negative channel	I_{OUTN} = 0 mA, $V_{OUTN(nom)}$= 0 V, R_{2N} = open, V_{INN} = –33 V	–150	–60		
			I_{OUTN} = 150 mA, R_{2N} = open, V_{INN} = –33 V		–1053		
I_{SHDN}	Shutdown supply current	Positive channel	V_{EN} = 0.4 V, V_{INP} = 33 V		3.75	6.5	µA
		Negative channel	V_{EN} = 0.4 V, V_{INN} = –33 V	–4.5	–2.25		

(1) To ensure V_{OUT} does not drift up while the device is disabled, a minimum load current of 5 µA is required.
(2) $V_{OUT(target)}$ = 0 V, R_{1N} = 10 kΩ, R_{2N} = open.
(3) The device is not tested under conditions where the power dissipated across the device, P_D, exceeds 2 W.

Electrical Characteristics (continued)

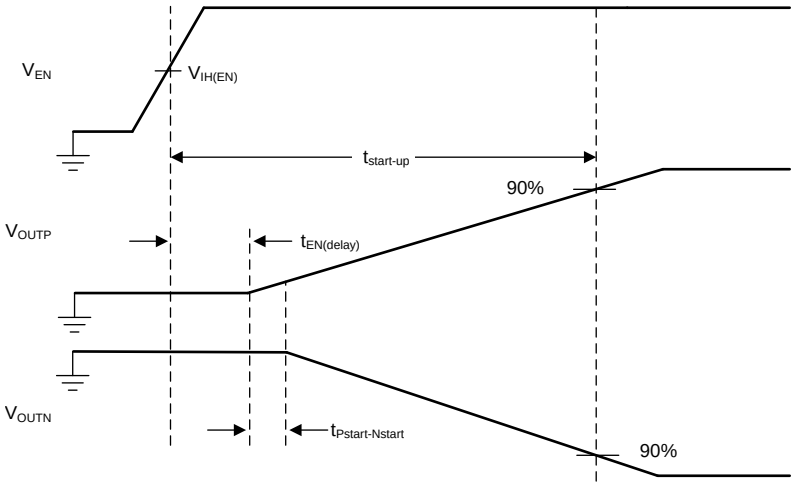
at T_J = –40°C to +125°C, $V_{INP(nom)} = V_{OUTP(nom)}$ + 1 V or $V_{IN(nom)}$ = 3.3 V (whichever is greater), $V_{INN(nom)} = V_{OUTN(nom)}$ – 1 V or $V_{INN(nom)}$ = –3.3 V (whichever is less), $V_{EN} = V_{INP}$, I_{OUT} = 1 mA, C_{INx} = 2.2 µF, C_{OUTx} = 10 µF, $C_{FFx} = C_{NR/SS}$ = open, $R_{1N} = R_{2N}$ = 10 kΩ, and FBP tied to OUTP (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{FBx}	Feedback pin leakage current	Positive channel			5.5	100	nA
		Negative channel		–100	–9.7		
$I_{NR/SS}$	Soft-start charging current		$V_{NR/SS}$ = 0.9 V	3	5.1	6.7	µA
I_{EN}	Enable pin leakage current		$V_{EN} = V_{INP}$ = 33 V		0.02	1	µA
$V_{IH(EN)}$	Enable high-level voltage			2.2		V_{INP}	V
$V_{IL(EN)}$	Enable low-level voltage			0		0.4	V
PSRR	Power-supply rejection ratio		$\|V_{IN}\|$ = 6 V, $\|V_{OUT(nom)}\|$ = 5 V, C_{OUT} = 10 µF, $C_{NR/SS} = C_{FF}$= 10 nF, f = 120 Hz		69		dB
V_n	Output noise voltage	Positive channel	V_{INP} = 3.3 V, $V_{OUTP(nom)} = V_{NR/SS}$, C_{OUTP} = 10 µF, $C_{NR/SS}$ = 10 nF, BW = 10 Hz to 100 kHz		20.63		μV_{RMS}
			V_{INP} = 6 V, $V_{OUTP(nom)}$ = 5 V, C_{OUTP} = 10 µF, $C_{NR/SS} = C_{FF}$ = 10 nF, BW = 10 Hz to 100 kHz		26.86		
		Negative channel	V_{INN} = –3 V, $V_{OUTN(nom)} = -V_{NR/SS}$, C_{OUTP} = 10 µF, $C_{NR/SS}$ = 10 nF, BW = 10 Hz to 100 kHz		22.13		
			V_{INN} = –6 V, $V_{OUTN(nom)}$ = –5 V, C_{OUTP} = 10 µF, $C_{NR/SS} = C_{FF}$= 10 nF, BW = 10 Hz to 100 kHz		28.68		
$R_{NR/SS}$	Filter resistor from band gap to NR pin				350		kΩ
T_{sd}	Thermal shutdown temperature		Shutdown, temperature increasing		175		°C
			Reset, temperature decreasing		160		

6.6 Startup Characteristics

at T_J = –40°C to +125°C, $V_{INP(nom)} = V_{OUTP(nom)}$ + 1 V or $V_{IN(nom)}$ = 3.3 V (whichever is greater), $V_{INN(nom)} = V_{OUTN(nom)}$ – 1 V or $V_{INN(nom)}$ = –3.3 V (whichever is less), $V_{EN} = V_{INP}$, I_{OUT} = 1 mA, C_{INx} = 2.2 µF, C_{OUTx} = 10 µF, $C_{FFx} = C_{NR/SS}$ = 4.7nF, $R_{1N} = R_{2N}$ = 10 kΩ, and FBP tied to OUTP (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{EN(delay)}$	Delay time from EN low-to-high transition to 2.5% V_{OUTP}	From EN low-to-high transition to V_{OUTP} = 2.5% × $V_{OUTP(nom)}$		300		µs
$t_{start-up}$	Delay time from EN low-to-high transition to both outputs reaching 95% of final value	From EN low-to-high transition to V_{OUTP} = $V_{OUTP(nom)}$ × 95% and V_{OUTN} = $V_{OUTN(nom)}$ × 95%		1.1		ms
$t_{Pstart-Nstart}$	Delay time from V_{OUTP} leaving a high-impedance state to V_{OUTN} leaving a high-impedance state	From V_{OUTP} = $V_{OUTP(nom)}$ × 2.5% to V_{OUTN} = $V_{OUTN(nom)}$ × 2.5%	–40	–17	40	µs
$\Delta\|V_{OUTP} - V_{OUTN}\|$	Voltage difference between the positive and negative output	During $t_{Pstart-Nstart}$		75	300	mV

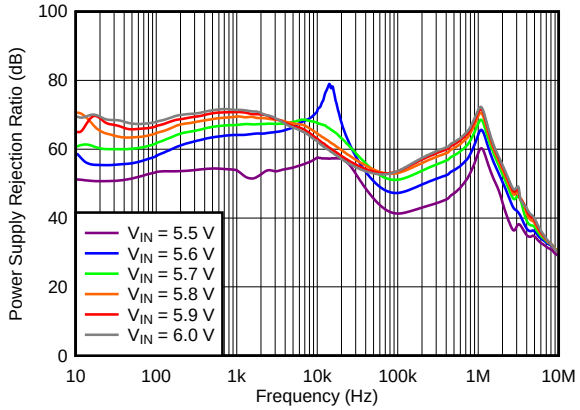


NOTE: Slow ramps ($t_{rise(VINx)}$ > 10 ms typically) on V_{INx} with EN tied to V_{INP} does not meet the tracking specification. Use a resistor divider from V_{INP} to EN for these applications.

Figure 1. Start-Up Characteristics

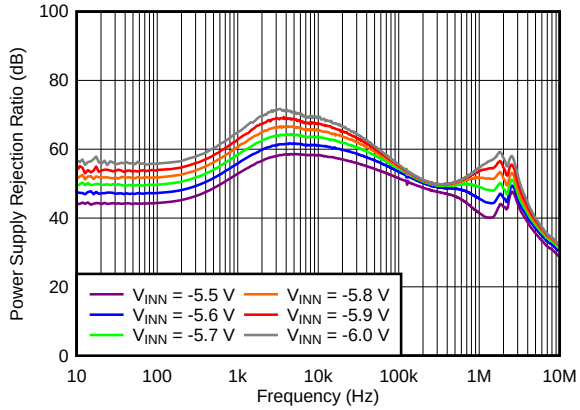
6.7 Typical Characteristics

at T_J = 25°C, V_{INP} = $V_{OUTP(nom)}$ + 1.0 V or V_{IN} = 3.3 V (whichever is greater), V_{INN} = $V_{OUTN(nom)}$ – 1 V or –3.3 V (whichever is less), V_{EN} = V_{IN}, I_{OUT} = 1 mA, C_{IN} = 10-µF ceramic, C_{OUT} = 10-µF ceramic, and C_{FFP} = C_{FFN} = $C_{NR/SS}$ = 10 nF (unless otherwise noted)



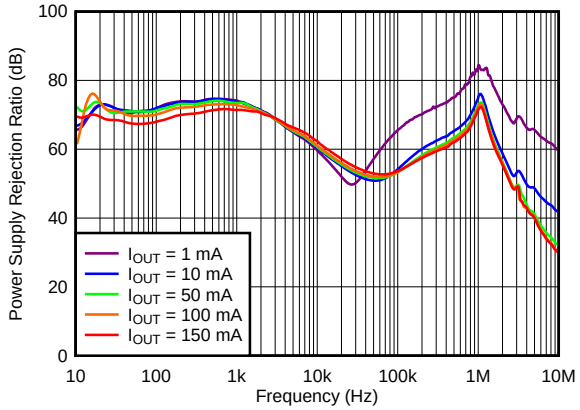
V_{OUTP} = 5 V, I_{OUTP} = 150 mA, V_{OUTN} = –5 V, I_{OUTN} = 0 mA, $C_{NR/SS}$ = C_{FFx} = 10 nF

Figure 2. Positive PSRR vs Frequency and V_{INP}



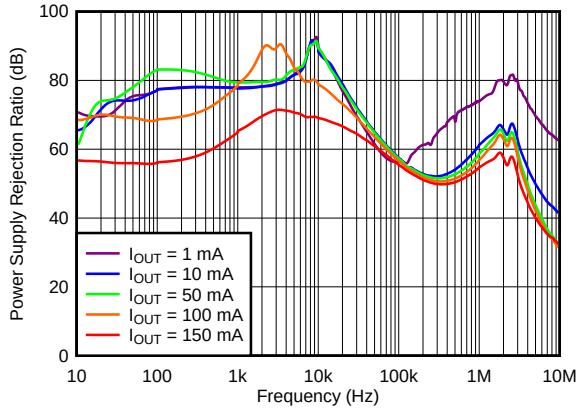
V_{OUTP} = 5 V, I_{OUTP} = 0 mA, V_{OUTN} = –5 V, I_{OUTN} = 150 mA, $C_{NR/SS}$ = C_{FFx} = 10 nF

Figure 3. Negative PSRR vs Frequency and V_{INN}



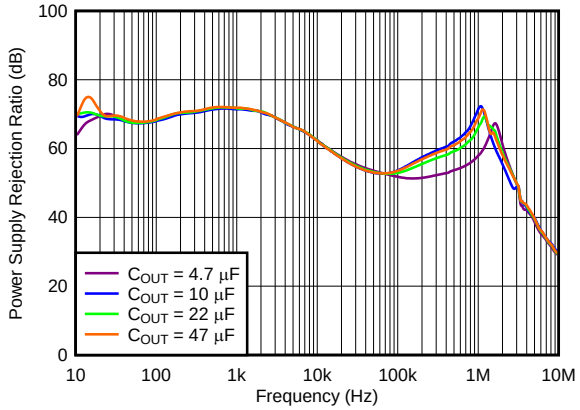
V_{OUTP} = 5 V, V_{INP} = V_{EN} = 6 V, V_{OUTN} = –5 V, I_{OUTN} = 0 mA, $C_{NR/SS}$ = C_{FFx} = 10 nF

Figure 4. Positive PSRR vs Frequency and I_{OUTP}



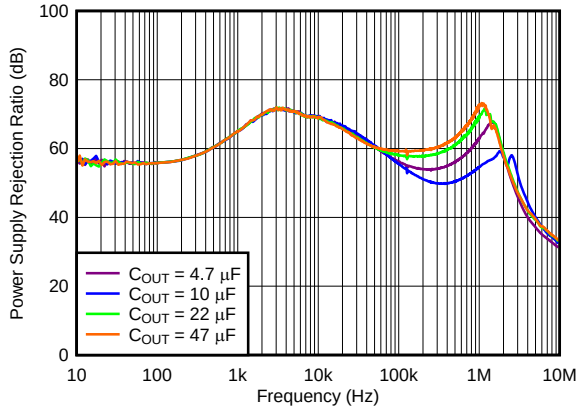
V_{OUTP} = 5 V, I_{OUTP} = 0 mA, V_{INN} = –6 V, V_{OUTN} = –5 V, $C_{NR/SS}$ = C_{FFx} = 10 nF

Figure 5. Negative PSRR vs Frequency and I_{OUTN}



V_{OUTP} = 5 V, V_{INP} = V_{EN} = 6 V, V_{OUTN} = –5 V, I_{OUTN} = 0 mA, $C_{NR/SS}$ = C_{FFx} = 10 nF

Figure 6. Positive PSRR vs Frequency and C_{OUTP}

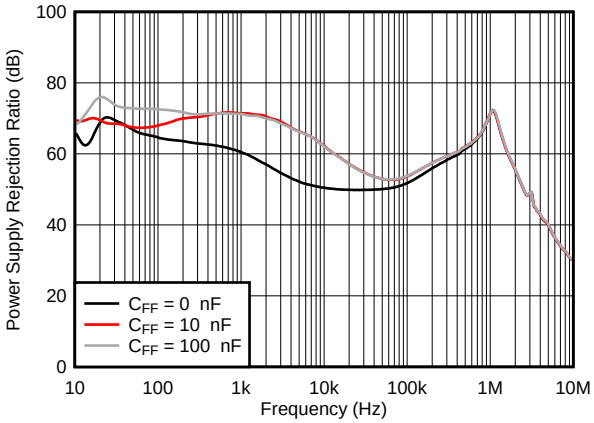


V_{OUTP} = 5 V, I_{OUTP} = 0 mA, V_{INN} = –6 V, V_{OUTN} = –5 V, $C_{NR/SS}$ = C_{FFx} = 10 nF, C_{OUTP} = 10 µF

Figure 7. Negative PSRR vs Frequency and C_{OUTN}

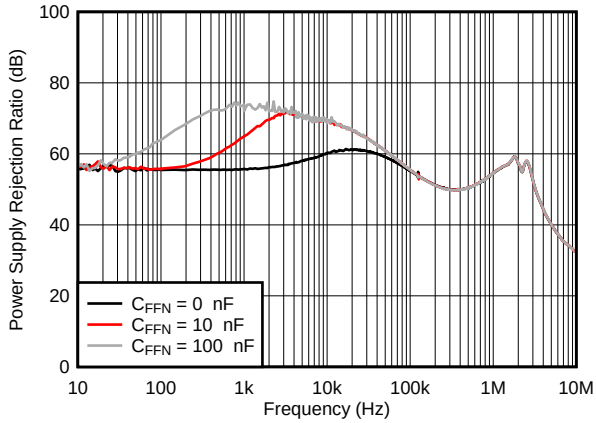
Typical Characteristics (continued)

at T_J = 25°C, V_{INP} = $V_{OUTP(nom)}$ + 1.0 V or V_{IN} = 3.3 V (whichever is greater), V_{INN} = $V_{OUTN(nom)}$ – 1 V or –3.3 V (whichever is less), V_{EN} = V_{IN}, I_{OUT} = 1 mA, C_{IN} = 10-µF ceramic, C_{OUT} = 10-µF ceramic, and C_{FFP} = C_{FFN} = $C_{NR/SS}$ = 10 nF (unless otherwise noted)



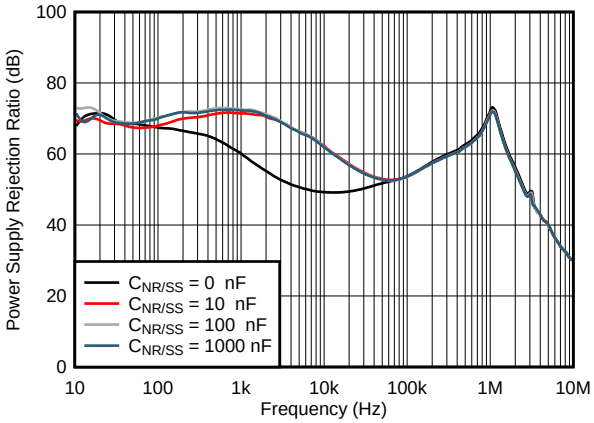
V_{OUTP} = 5 V, V_{INP} = V_{EN} = 6 V, V_{OUTN} = –5 V, I_{OUTN} = 0 mA, $C_{NR/SS}$ = 10 nF

Figure 8. Positive PSRR vs Frequency and C_{FFP}



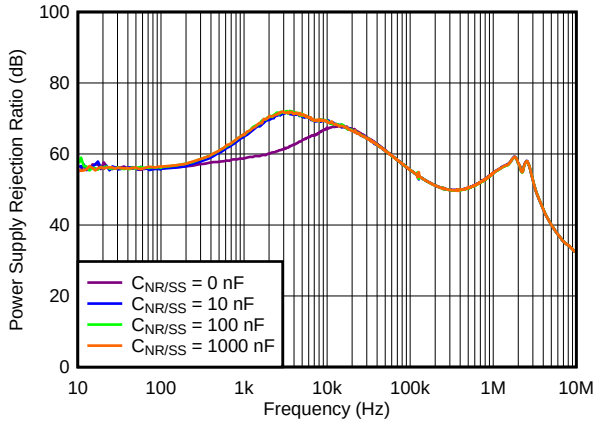
V_{OUTP} = 5 V, I_{OUTP} = 0 mA, V_{INN} = –6 V, V_{OUTN} = –5 V, $C_{NR/SS}$ = C_{FFP} = 10 nF

Figure 9. Negative PSRR vs Frequency and C_{FFN}



V_{OUTP} = 5 V, V_{INP} = V_{EN} = 6 V, V_{OUTN} = –5 V, I_{OUTN} = 0 mA, C_{FFx} = 10 nF

Figure 10. Positive PSRR vs Frequency and $C_{NR/SS}$



V_{OUTP} = 5 V, I_{OUTP} = 0 mA, V_{INN} = –6 V, V_{OUTN} = –5 V, C_{FFx} = 10 nF

Figure 11. Negative PSRR vs Frequency and $C_{NR/SS}$

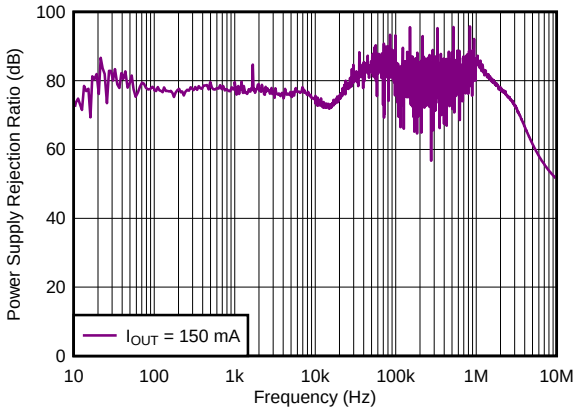


Figure 12. Crosstalk Positive to Negative

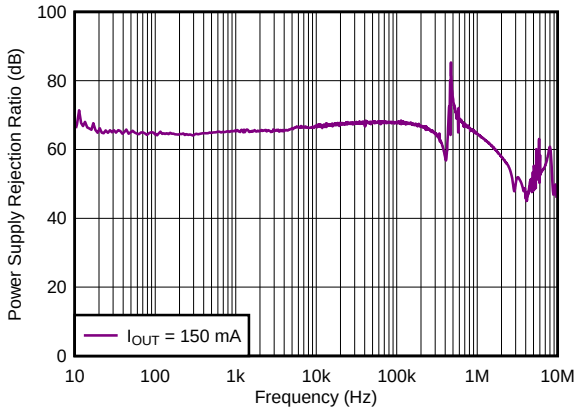
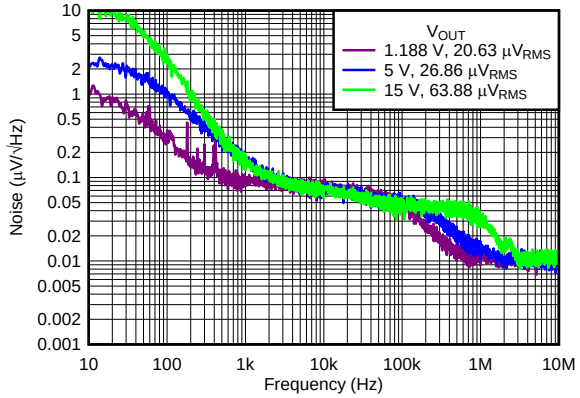


Figure 13. Crosstalk Negative to Positive

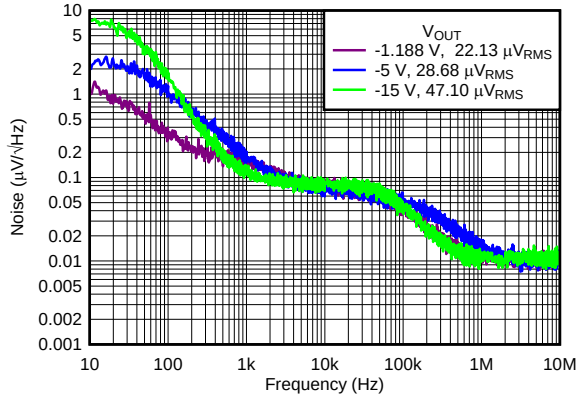
Typical Characteristics (continued)

at T_J = 25°C, V_{INP} = $V_{OUTP(nom)}$ + 1.0 V or V_{IN} = 3.3 V (whichever is greater), V_{INN} = $V_{OUTN(nom)}$ – 1 V or –3.3 V (whichever is less), V_{EN} = V_{IN}, I_{OUT} = 1 mA, C_{IN} = 10-µF ceramic, C_{OUT} = 10-µF ceramic, and C_{FFP} = C_{FFN} = $C_{NR/SS}$ = 10 nF (unless otherwise noted)



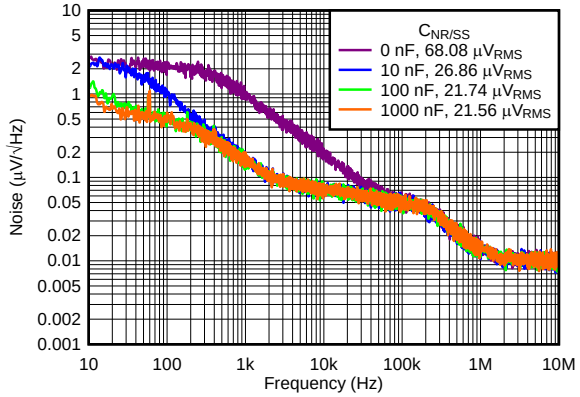
I_{OUTP} = 150 mA, V_{INP} = V_{EN}, V_{OUTN} = –V_{OUTP}, I_{OUTN} = 0 mA, $C_{NR/SS}$ = C_{FFx} = 10 nF

Figure 14. Positive Spectral Noise Density vs Frequency and V_{OUTP}



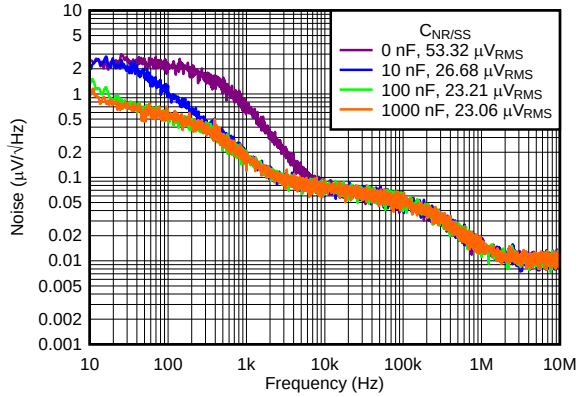
I_{OUTN} = –150 mA, V_{INP} = V_{EN}, V_{OUTN} = –V_{OUTP}, I_{OUTP} = 0 mA, $C_{NR/SS}$ = C_{FFx} = 10 nF

Figure 15. Negative Spectral Noise Density vs Frequency and V_{OUTN}



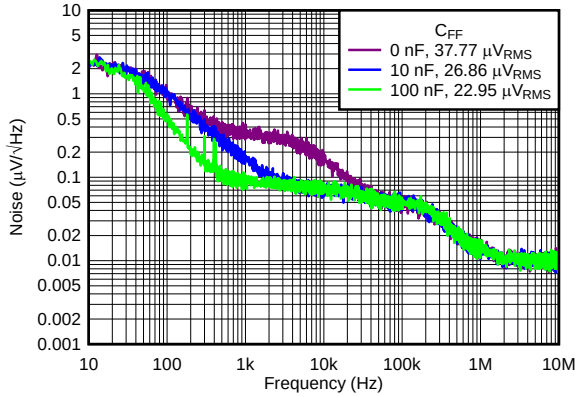
V_{OUTP} = 5 V, I_{OUTP} = 150 mA, V_{INP} = V_{EN} = 6 V, V_{OUTN} = –5 V, I_{OUTN} = 0 mA, C_{FFx} = 10 nF

Figure 16. Positive Spectral Noise Density vs Frequency and $C_{NR/SS}$



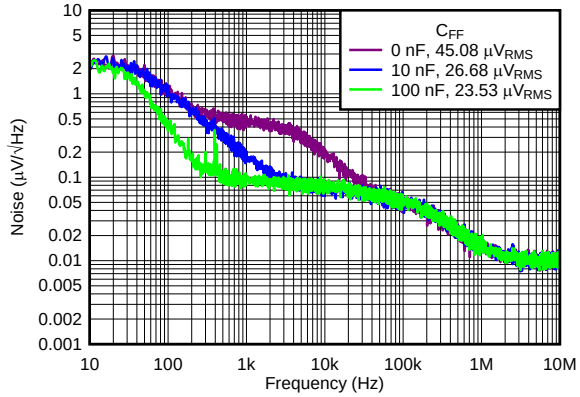
V_{OUTN} = –5 V, I_{OUTN} = –150 mA, V_{INP} = V_{EN} = 6 V, V_{OUTN} = –5 V, I_{OUTP} = 0 mA, C_{FFx} = 10 nF

Figure 17. Negative Spectral Noise Density vs Frequency and $C_{NR/SS}$



V_{OUTP} = 5 V, I_{OUTP} = 150 mA, V_{INP} = V_{EN} = 6 V, V_{OUTN} = –5 V, I_{OUTN} = 0 mA, $C_{NR/SS}$ = 10 nF

Figure 18. Positive Spectral Noise Density vs Frequency and C_{FF}

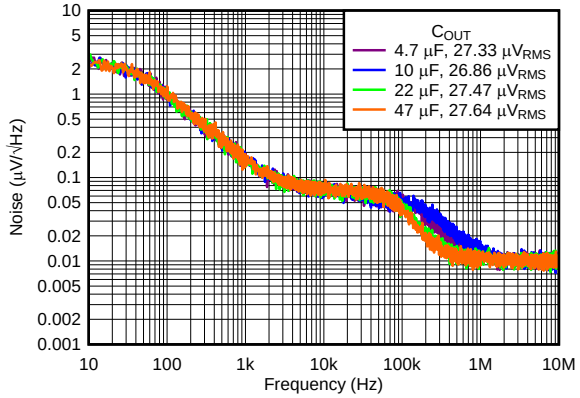


V_{OUTN} = –5 V, I_{OUTN} = –150 mA, V_{INP} = V_{EN} = 6 V, V_{OUTN} = –5 V, I_{OUTP} = 0 mA, $C_{NR/SS}$ = 10 nF

Figure 19. Negative Spectral Noise Density vs Frequency and C_{FF}

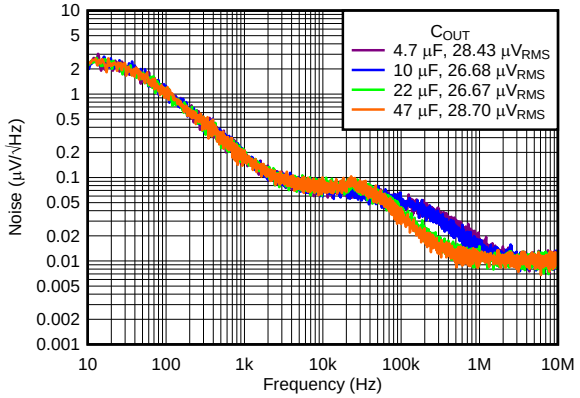
Typical Characteristics (continued)

at T_J = 25°C, V_{INP} = $V_{OUTP(nom)}$ + 1.0 V or V_{IN} = 3.3 V (whichever is greater), V_{INN} = $V_{OUTN(nom)}$ – 1 V or –3.3 V (whichever is less), V_{EN} = V_{IN}, I_{OUT} = 1 mA, C_{IN} = 10-µF ceramic, C_{OUT} = 10-µF ceramic, and C_{FFP} = C_{FFN} = $C_{NR/SS}$ = 10 nF (unless otherwise noted)



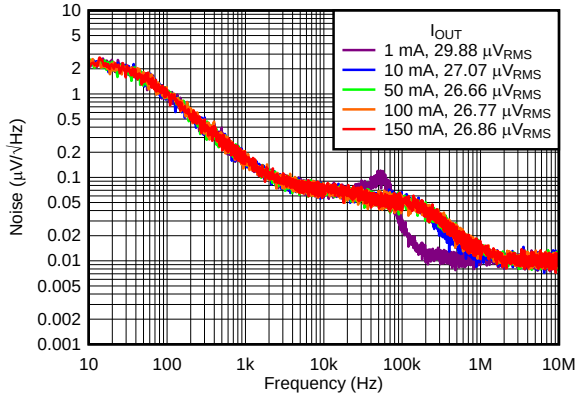
V_{OUTP} = 5 V, I_{OUTP} = 150 mA, V_{INP} = V_{EN} = 6 V, V_{OUTN} = –5 V, I_{OUTN} = 0 mA, $C_{NR/SS}$ = C_{FFx} = 10 nF

Figure 20. Positive Spectral Noise Density vs Frequency and C_{OUT}



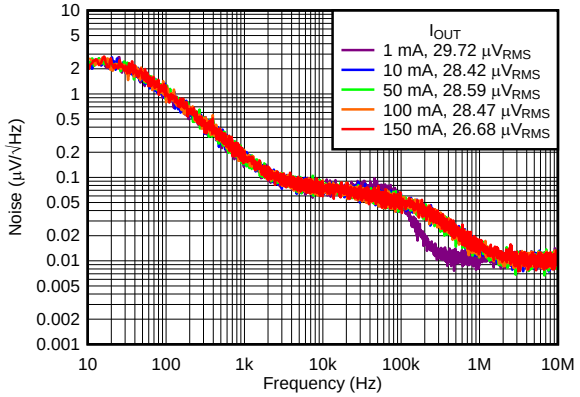
V_{OUTN} = –5 V, I_{OUTN} = –150 mA, V_{INP} = V_{EN} = 6 V, V_{OUTN} = –5 V, I_{OUTP} = 0 mA, $C_{NR/SS}$ = C_{FFx} = 10 nF

Figure 21. Negative Spectral Noise Density vs Frequency and C_{OUT}



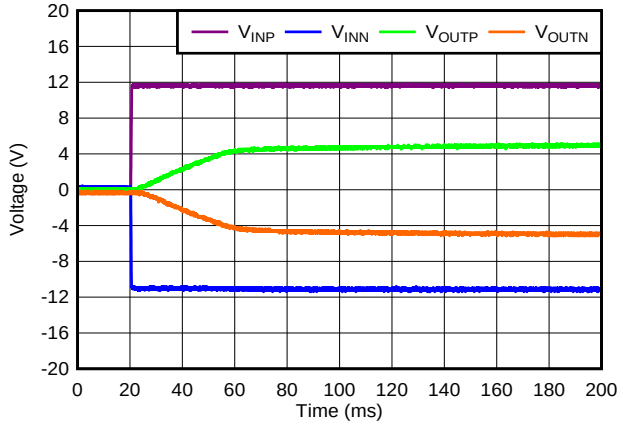
V_{OUTP} = 5 V, V_{INP} = V_{EN} = 6 V, V_{OUTN} = –5 V, I_{OUTN} = 0 mA, $C_{NR/SS}$ = C_{FFx} = 10 nF

Figure 22. Positive Spectral Noise Density vs Frequency and I_{OUT}



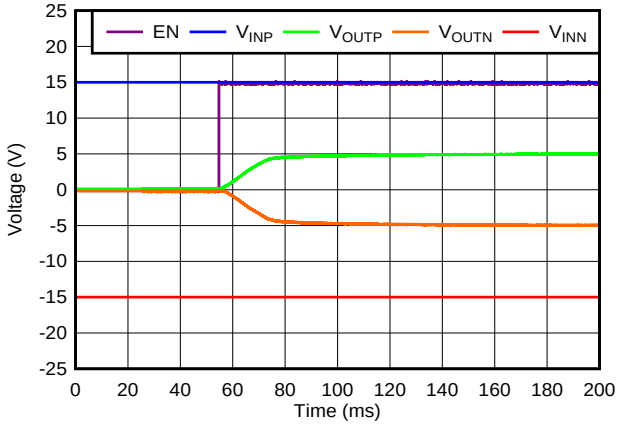
V_{OUTN} = –5 V, V_{INP} = V_{EN} = 6 V, V_{OUTN} = –5 V, I_{OUTP} = 0 mA, $C_{NR/SS}$ = C_{FFx} = 10 nF

Figure 23. Negative Spectral Noise Density vs Frequency and I_{OUT}



V_{OUTP} = –V_{OUTN} = 5 V, V_{INP} = –V_{INN} = 12 V

Figure 24. Startup (V_{INP} = V_{EN})

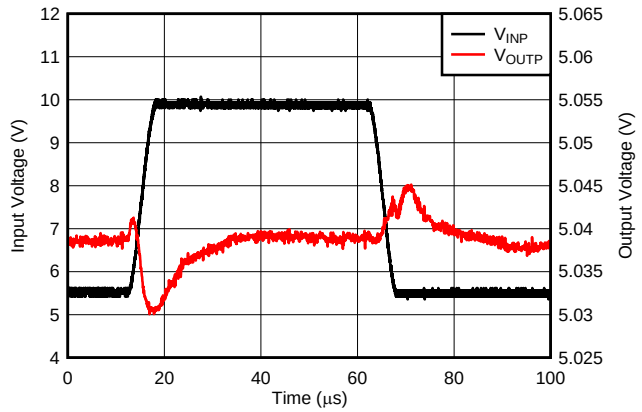


V_{OUTP} = –V_{OUTN} = 5 V, V_{INP} = –V_{INN} = 15 V

Figure 25. Startup With EN

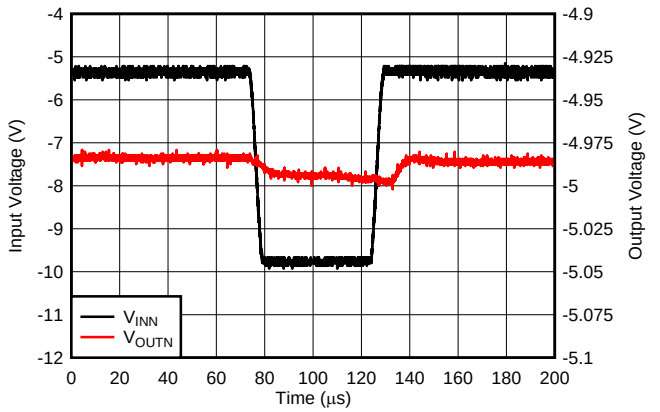
Typical Characteristics (continued)

at T_J = 25°C, V_{INP} = $V_{OUTP(nom)}$ + 1.0 V or V_{IN} = 3.3 V (whichever is greater), V_{INN} = $V_{OUTN(nom)}$ – 1 V or –3.3 V (whichever is less), V_{EN} = V_{IN}, I_{OUT} = 1 mA, C_{IN} = 10-µF ceramic, C_{OUT} = 10-µF ceramic, and C_{FFP} = C_{FFN} = $C_{NR/SS}$ = 10 nF (unless otherwise noted)



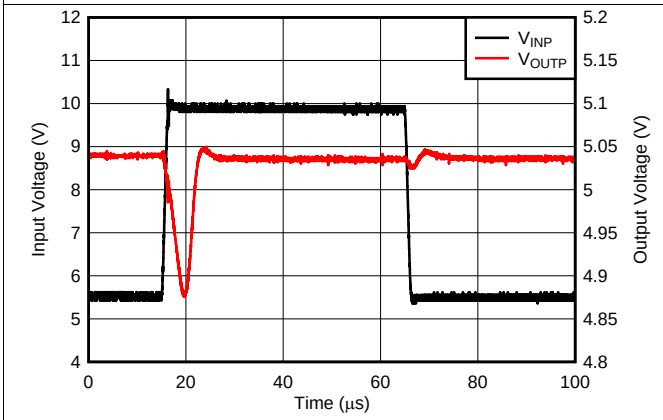
V_{INP} = 5.5 V to 10 V at 1 V/µs, V_{OUTP} = –V_{OUTN} = 5 V, I_{OUTN} = 0 mA, I_{OUTP} = 150 mA

Figure 26. Line Transient Positive Regulator



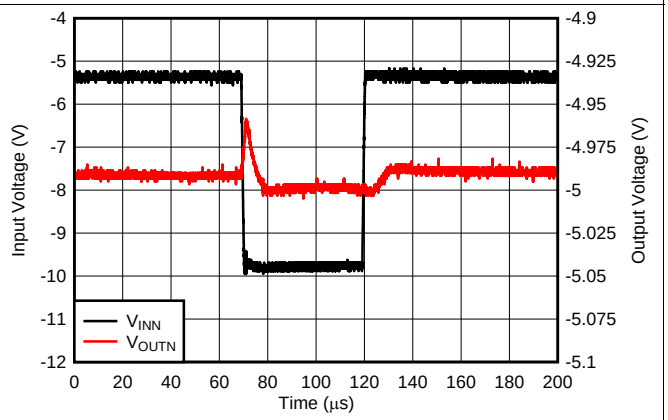
V_{INN} = –5.5 V to –10 V at 1 V/µs, V_{OUTP} = –V_{OUTN} = 5 V, I_{OUTN} = –150 mA, I_{OUTP} = 0 mA

Figure 27. Line Transient Negative Regulator



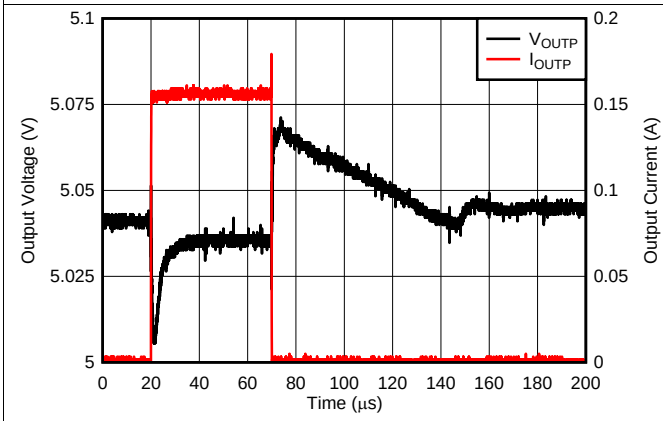
V_{INP} = 5.5 V to 10 V at 4 V/µs, V_{OUTP} = –V_{OUTN} = 5 V, I_{OUTN} = 0 mA, I_{OUTP} = 150 mA

Figure 28. Line Transient Positive Regulator



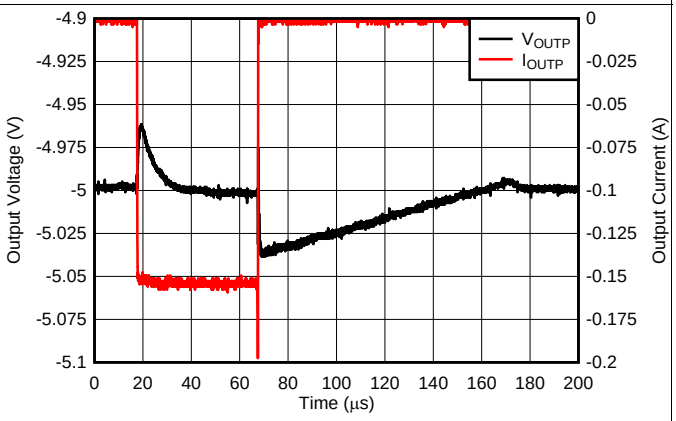
V_{INN} = –5.5 V to –10 V at 4 V/µs, V_{OUTP} = –V_{OUTN} = 5 V, I_{OUTN} = –150 mA, I_{OUTP} = 0 mA

Figure 29. Line Transient Negative Regulator



V_{INP} = 6 V, V_{OUTP} = –V_{OUTN} = 5 V, I_{OUTN} = 0 mA, I_{OUTP} = 1 mA to 150 mA at 1 A/µs

Figure 30. Load Transient Positive Regulator



V_{INN} = –6 V, V_{OUTP} = –V_{OUTN} = 5 V, I_{OUTN} = 0 mA, I_{OUTP} = –1 mA to –150 mA at 1 A/µs

Figure 31. Load Transient Negative Regulator

Typical Characteristics (continued)

at T_J = 25°C, V_{INP} = $V_{OUTP(nom)}$ + 1.0 V or V_{IN} = 3.3 V (whichever is greater), V_{INN} = $V_{OUTN(nom)}$ – 1 V or –3.3 V (whichever is less), V_{EN} = V_{IN}, I_{OUT} = 1 mA, C_{IN} = 10-µF ceramic, C_{OUT} = 10-µF ceramic, and C_{FFP} = C_{FFN} = $C_{NR/SS}$ = 10 nF (unless otherwise noted)

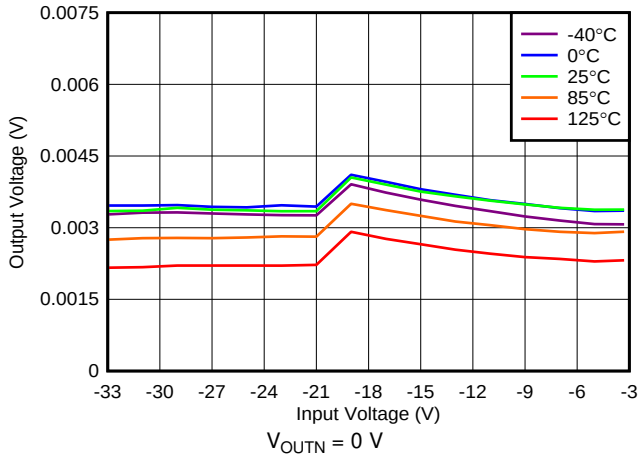


Figure 32. Negative Line Regulation

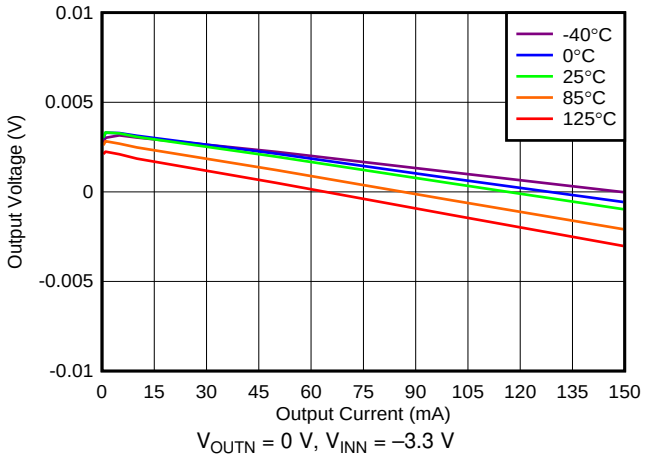


Figure 33. Negative Load Regulation

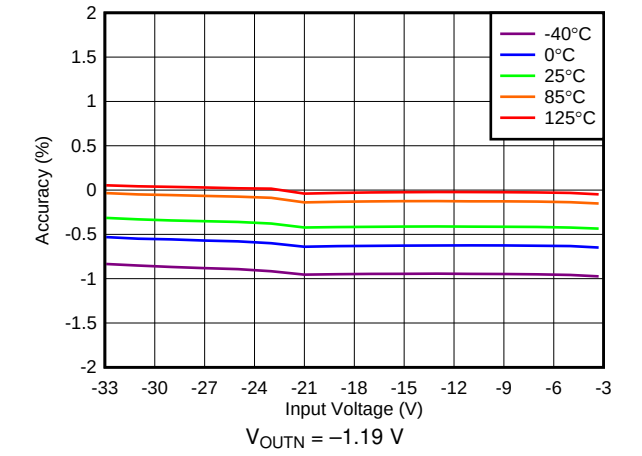


Figure 34. Negative Line Regulation

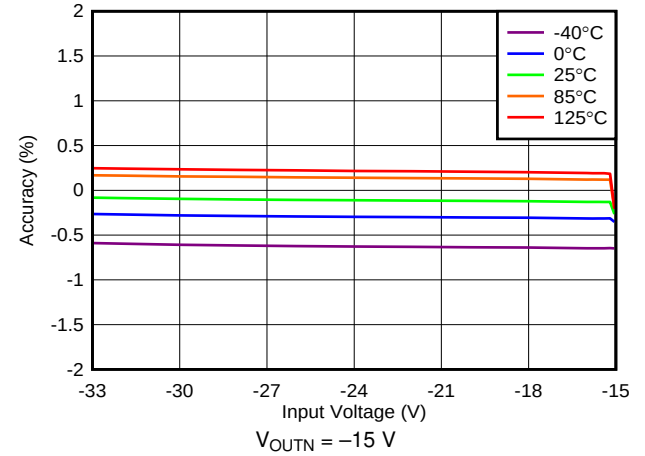


Figure 35. Negative Line Regulation

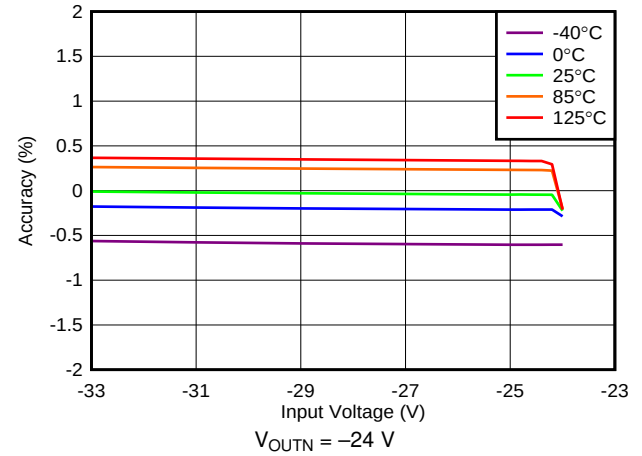


Figure 36. Negative Line Regulation

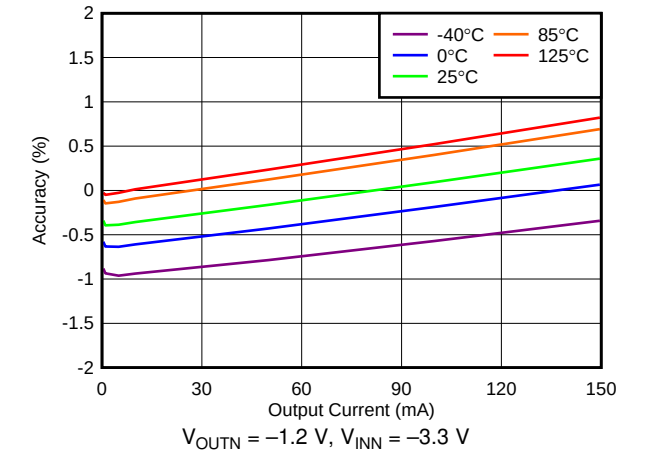


Figure 37. Negative Load Regulation

Typical Characteristics (continued)

at T_J = 25°C, V_{INP} = $V_{OUTP(nom)}$ + 1.0 V or V_{IN} = 3.3 V (whichever is greater), V_{INN} = $V_{OUTN(nom)}$ – 1 V or –3.3 V (whichever is less), V_{EN} = V_{IN}, I_{OUT} = 1 mA, C_{IN} = 10-µF ceramic, C_{OUT} = 10-µF ceramic, and C_{FFP} = C_{FFN} = $C_{NR/SS}$ = 10 nF (unless otherwise noted)

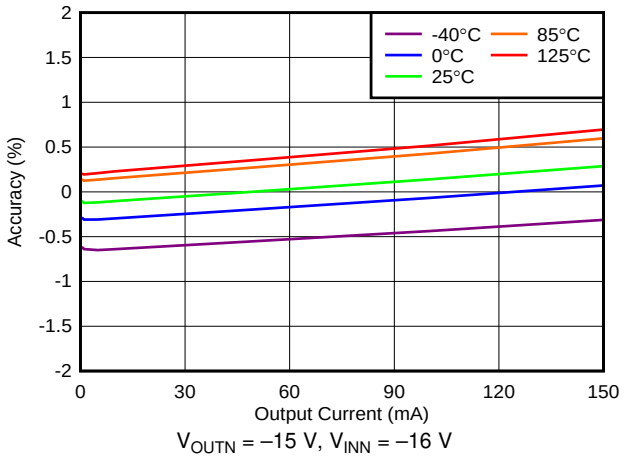


Figure 38. Negative Load Regulation

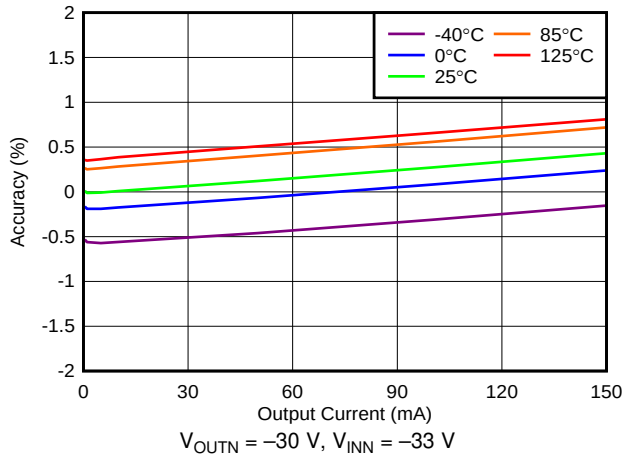


Figure 39. Negative Load Regulation

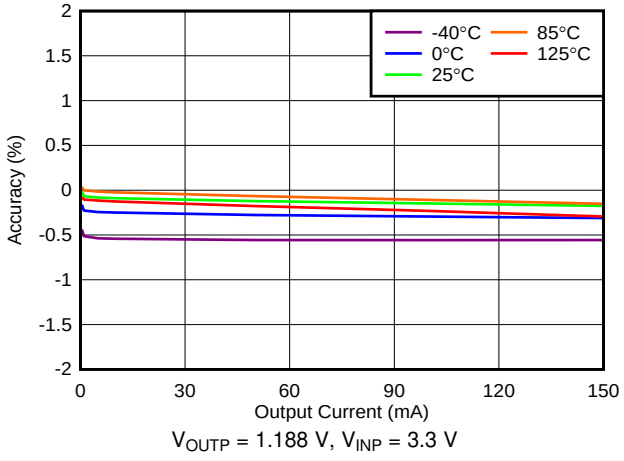


Figure 40. Positive Load Regulation

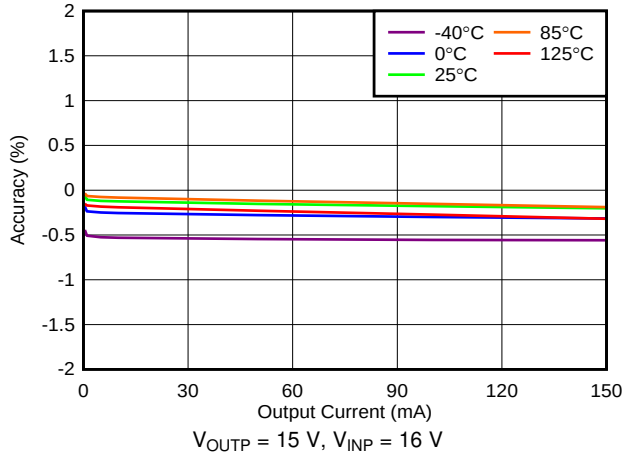


Figure 41. Positive Load Regulation

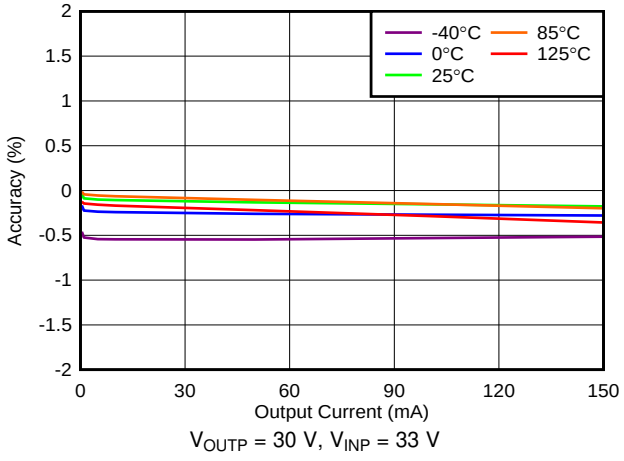


Figure 42. Positive Load Regulation

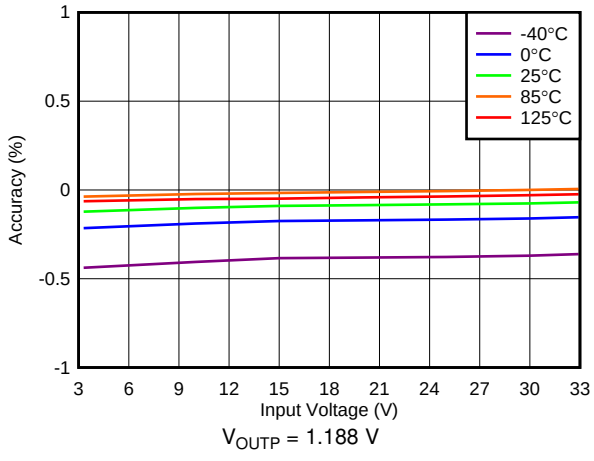


Figure 43. Positive Line Regulation

Typical Characteristics (continued)

at T_J = 25°C, V_{INP} = $V_{OUTP(nom)}$ + 1.0 V or V_{IN} = 3.3 V (whichever is greater), V_{INN} = $V_{OUTN(nom)}$ – 1 V or –3.3 V (whichever is less), V_{EN} = V_{IN}, I_{OUT} = 1 mA, C_{IN} = 10-µF ceramic, C_{OUT} = 10-µF ceramic, and C_{FFP} = C_{FFN} = $C_{NR/SS}$ = 10 nF (unless otherwise noted)

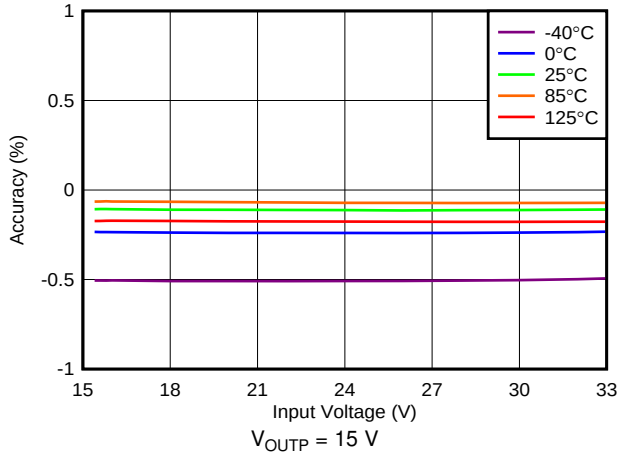


Figure 44. Positive Line Regulation

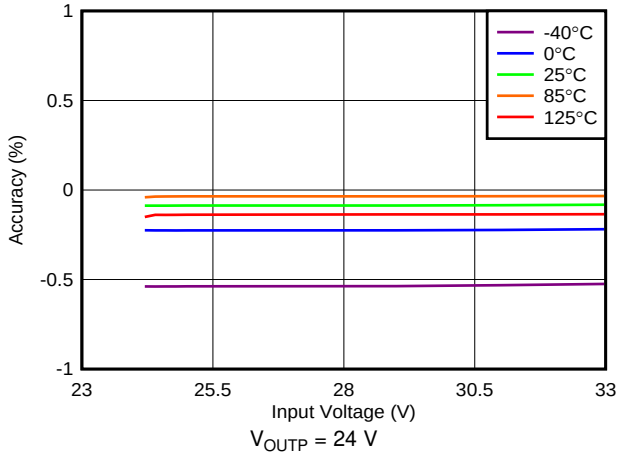


Figure 45. Positive Line Regulation

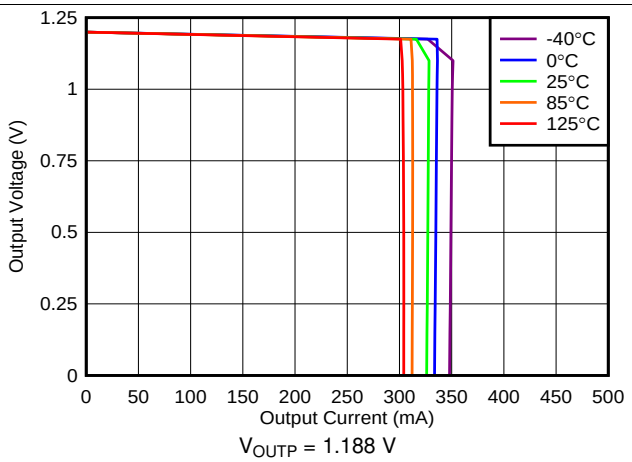


Figure 46. Positive Regulator Current Limit

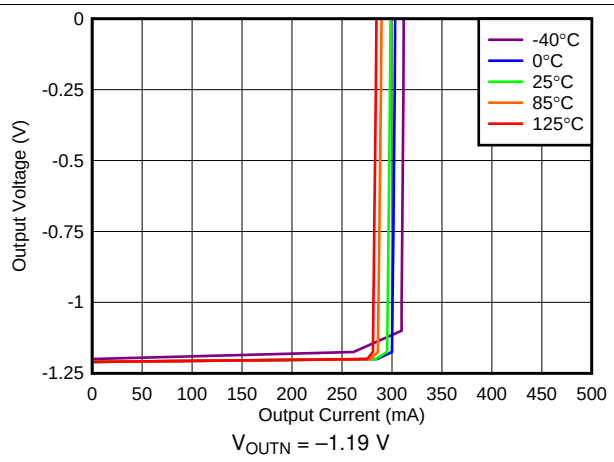


Figure 47. Negative Regulator Current Limit

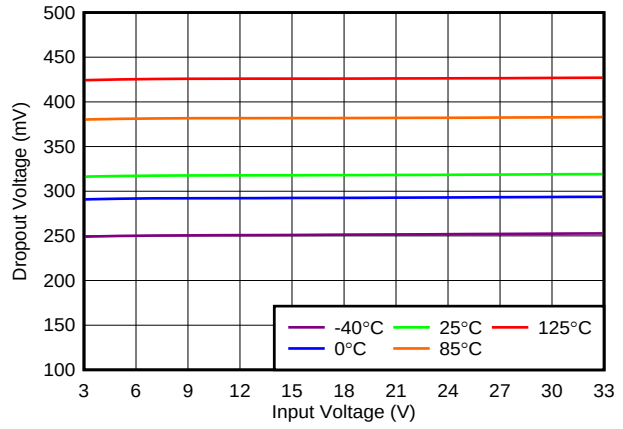


Figure 48. Positive Regulator Dropout Voltage vs Input Voltage

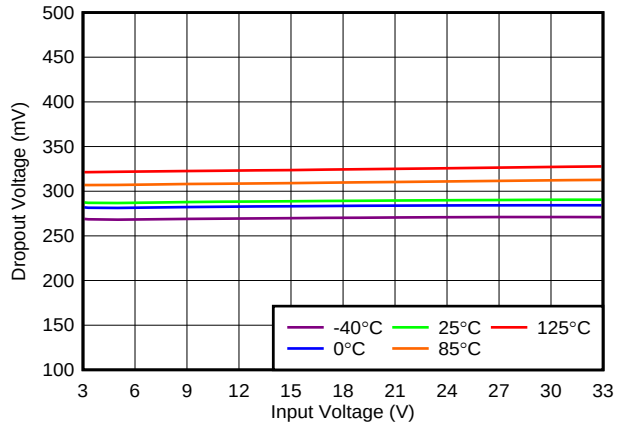


Figure 49. Negative Regulator Dropout Voltage vs Input Voltage

Typical Characteristics (continued)

at T_J = 25°C, V_{INP} = $V_{OUTP(nom)}$ + 1.0 V or V_{IN} = 3.3 V (whichever is greater), V_{INN} = $V_{OUTN(nom)}$ – 1 V or –3.3 V (whichever is less), V_{EN} = V_{IN}, I_{OUT} = 1 mA, C_{IN} = 10-µF ceramic, C_{OUT} = 10-µF ceramic, and C_{FFP} = C_{FFN} = $C_{NR/SS}$ = 10 nF (unless otherwise noted)

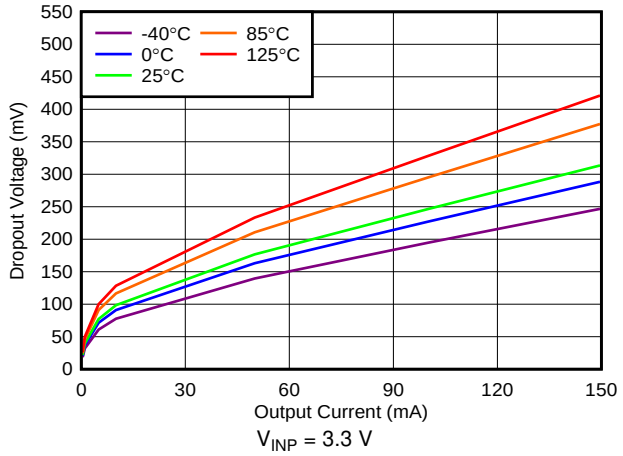


Figure 50. Positive Regulator Dropout Voltage vs Output Current

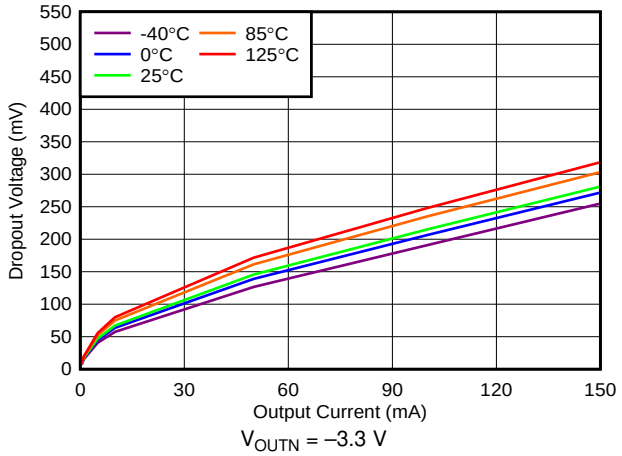


Figure 51. Negative Regulator Dropout Voltage vs Output Current

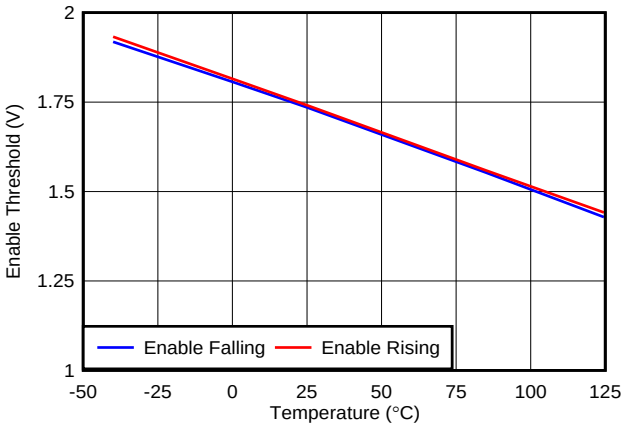


Figure 52. Enable Threshold vs Temperature

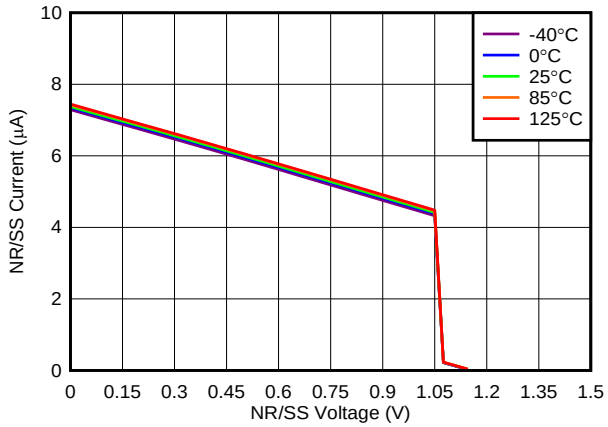


Figure 53. $I_{NR/SS}$ vs $V_{NR/SS}$

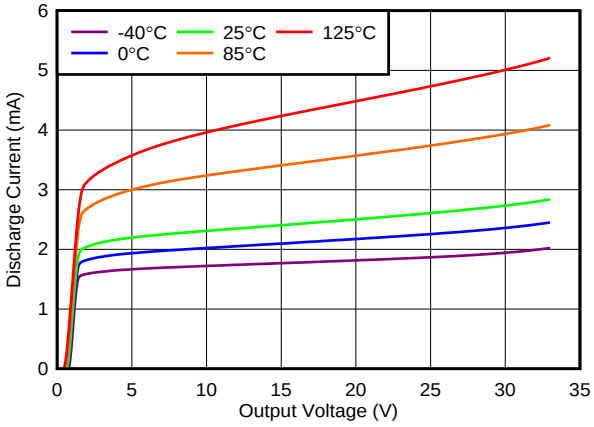


Figure 54. Positive Output Discharge Current vs Output Voltage

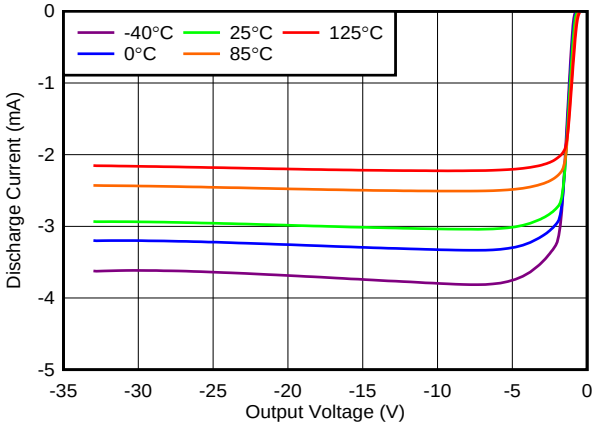


Figure 55. Negative Output Discharge Current vs Output Voltage

Typical Characteristics (continued)

at T_J = 25°C, V_{INP} = $V_{OUTP(nom)}$ + 1.0 V or V_{IN} = 3.3 V (whichever is greater), V_{INN} = $V_{OUTN(nom)}$ – 1 V or –3.3 V (whichever is less), V_{EN} = V_{IN}, I_{OUT} = 1 mA, C_{IN} = 10-µF ceramic, C_{OUT} = 10-µF ceramic, and C_{FFP} = C_{FFN} = $C_{NR/SS}$ = 10 nF (unless otherwise noted)

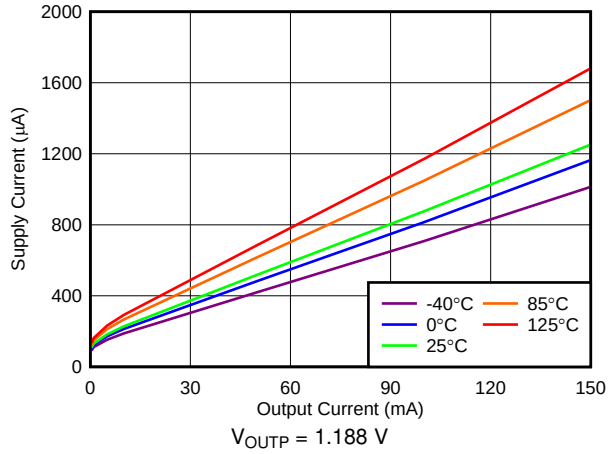


Figure 56. Positive Supply Current vs Output Current

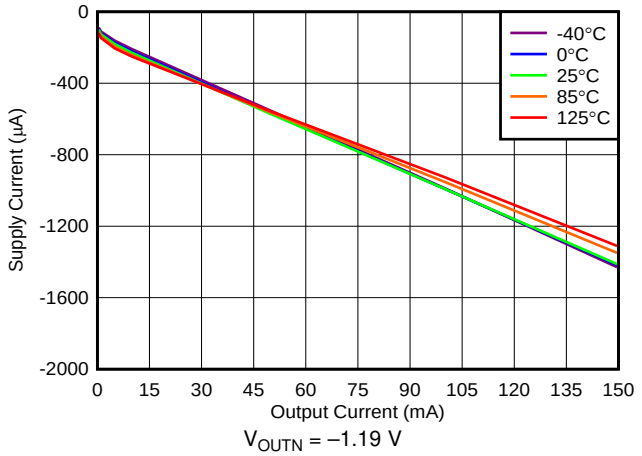


Figure 57. Negative Supply Current vs Output Current

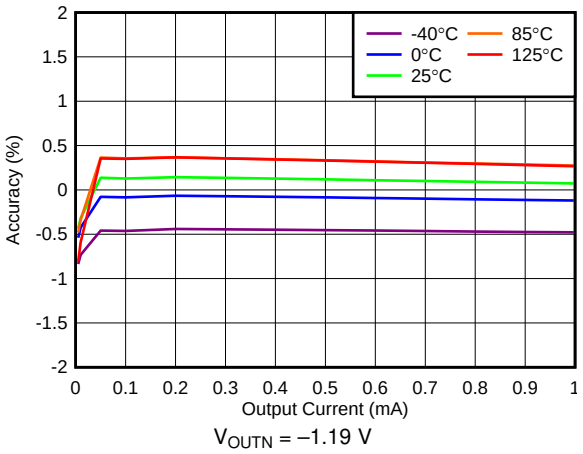


Figure 58. Buffer Accuracy vs Buffer Current

7 Detailed Description

7.1 Overview

The TPS7A39 is an innovative linear regulator (LDO) targeted at powering the signal chain, capable of up to ±33 V on the inputs and regulating up to ±30 V on the outputs at up to 150 mA of load current. The device uses an LDO topology that, by design, delivers ratiometric start-up tracking in most applications. The TPS7A39 has several other features, as listed in Table 1, that simplify using the device in a variety of applications.

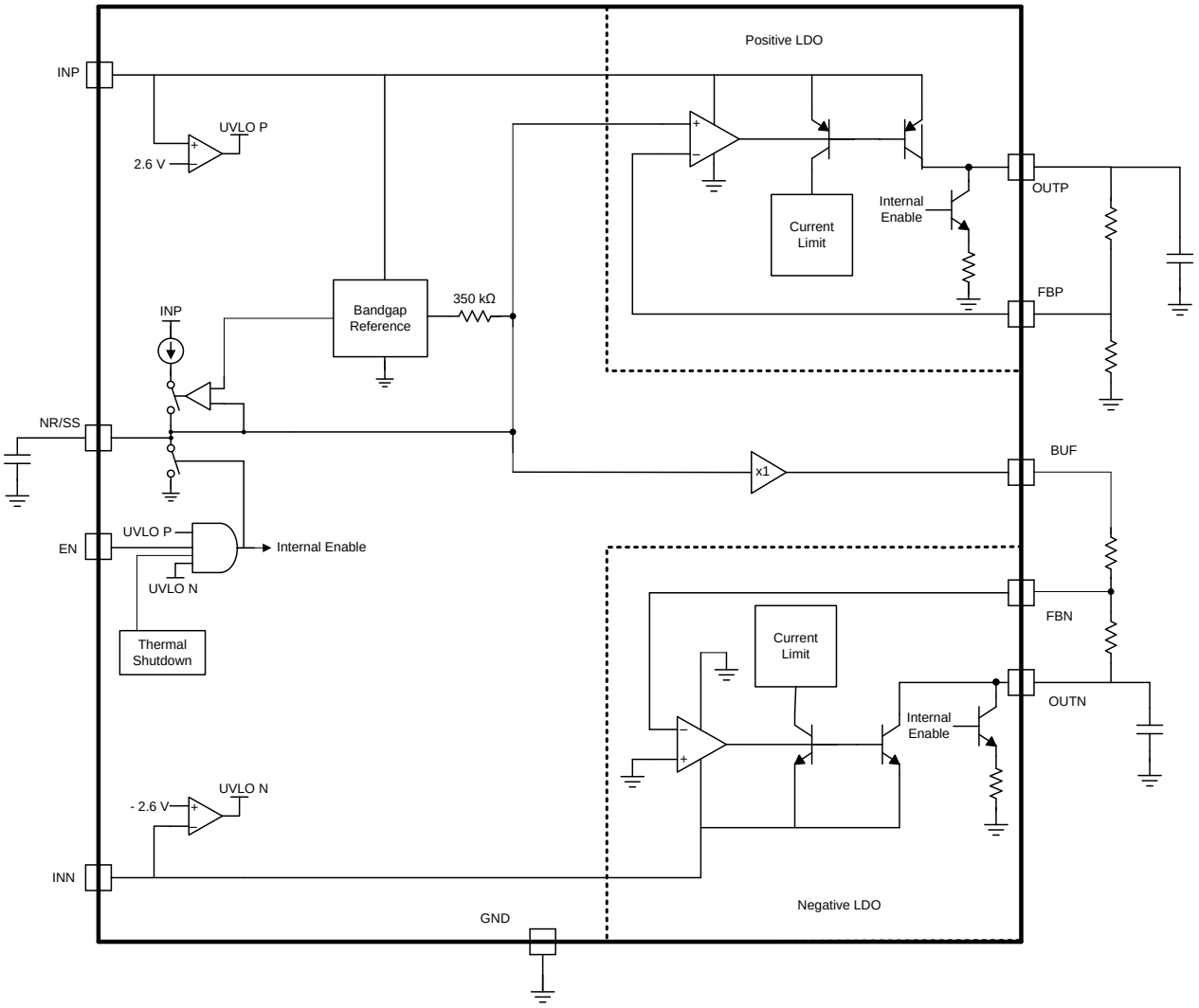
NOTE

Throughout this document, x is used to designate that the condition or component applies to both the positive and negative regulators (for example, C_{FFx} means C_{FFP} and C_{FFN}).

Table 1. TPS7A39 Features

VOLTAGE REGULATION	SYSTEM START-UP	INTERNAL PROTECTION
Reference input/output	Ratiometric start-up tracking	Current limit
High-PSRR output	Programmable soft-start	Thermal shutdown
Fast transient response	Sequencing controls	

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Voltage Regulation

7.3.1.1 DC Regulation

An LDO functions as a buffered op-amp in which the input signal is the internal reference voltage ($V_{NR/SS}$), as shown in Figure 59, and in normal regulation $V_{FBP} = V_{NR/SS}$. Sharing a single reference ensures that both channels track each other during start-up.

$V_{NR/SS}$ is designed to have a very low-bandwidth at the input to the error amplifier through the use of a low-pass filter. As such, the reference can be considered as a pure dc input signal.

As Figure 60 shows, the negative LDO on the device regulates with a V_{FBN} = 0 V and inverts the positive reference (V_{BUF}). This topology allows the negative regulator to regulate down to 0 V.

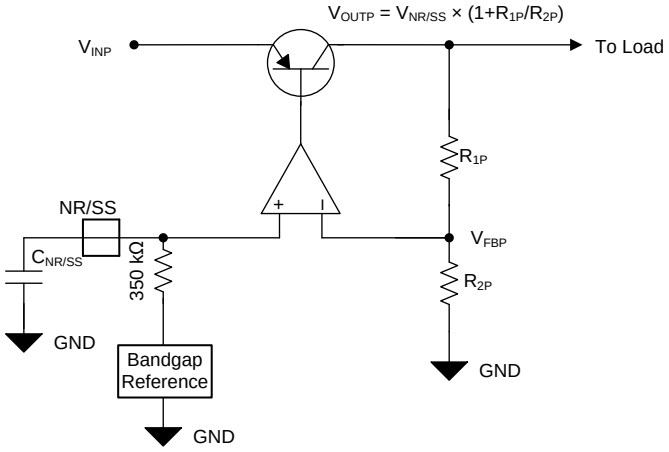


Figure 59. Simplified Positive Regulation Circuit

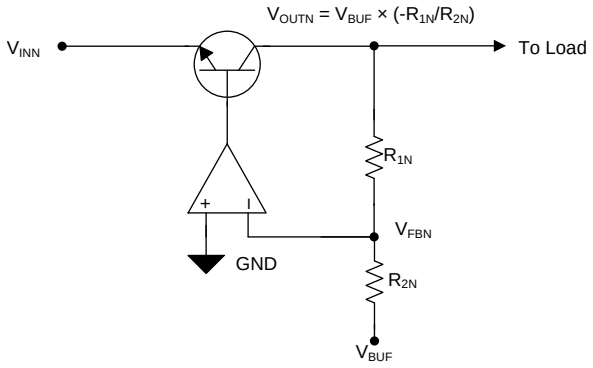


Figure 60. Simplified Negative Regulation Circuit

7.3.1.2 AC and Transient Response

Each LDO responds quickly to a transient on the input supply (line transient) or the output current (load transient). This LDO has a high power-supply rejection ratio (PSRR) and, when coupled with a low internal noise-floor (V_n), the LDO approximates an ideal power supply in ac and large-signal conditions.

The performance and internal layout of the device minimizes the coupling of noise from one channel to the other channel (crosstalk). Good printed circuit board (PCB) layout minimizes the crosstalk.

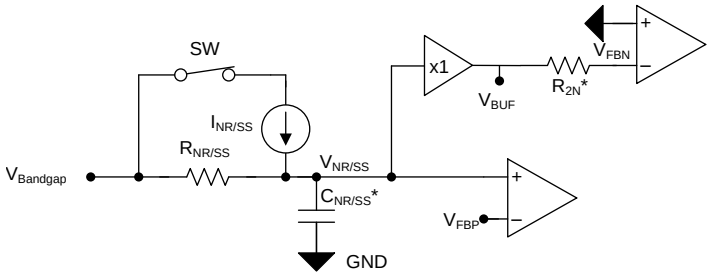
The noise-reduction and soft-start capacitor ($C_{NR/SS}$) and feed-forward capacitor (C_{FFx}) easily reduce the device noise floor and improve PSRR; see the *Optimizing Noise and PSRR* section for more information on optimizing the noise and PSRR performance.

Feature Description (continued)

7.3.2 User-Settable Buffered Reference

As Figure 61 shows, the device internally generated band-gap voltage outputs at the NR/SS pin. An internal resistor (R_{NR}) and an external capacitor ($C_{NR/SS}$) control the rise time of the voltage at the $V_{NR/SS}$ pin, setting the soft-start time. This network also filters out noise from the band gap, reducing the overall noise floor of the device.

Driving the NR/SS pin with an external source can improve the device accuracy and can reduce the device noise floor, along with enabling the device to regulate the positive channel to voltages below the device internal reference.



NOTE: * denotes external components.

Figure 61. Simplified Reference Circuit

7.3.3 Active Discharge

When either EN or UVLOx are low, the device connects a resistance from V_{OUTx} to GND, discharging the output capacitance. The active discharge circuit requires $|V_{OUTx}| \geq 0.6$ V (typ) to discharge the output because the NPN pulldown has a minimum V_{CE} requirement.

Do not rely on the active discharge circuit for discharging large output capacitors when the input voltage drops below the targeted output voltage. The TPS7A39 is a bipolar device, and as such, reverse voltage conditions ($|V_{OUTx}| \geq |V_{INX}| + 0.3$ V) can breakdown the emitter to base diode and also cause a breakdown of the parasitic bipolar formed in the substrate; see the *Reverse Current* section for more details.

When either EN or UVLOx are low, the device outputs a small amount of leakage current. The leakage current is typically handled by the maximum R_{2x} resistor value of 240 kΩ. However, if the device is placed in unity gain (no R_{2x} resistor) this leakage current causes the output to slowly rise until the discharge circuit (as shown in Figure 62) has enough headroom to clamp the output voltage (typically ±0.6 V).

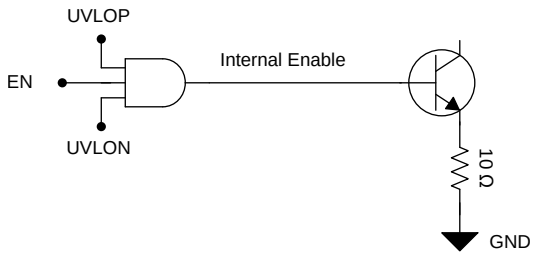


Figure 62. Simplified Active Discharge Circuit

7.3.4 System Start-Up Controls

In many different applications, the power-supply output must turn-on within a specific window of time because of sequencing requirements, ensuring proper operation of the load, or to minimize the loading on the input supply.

Both LDOs start-up are well-controlled and user-adjustable through the $C_{NR/SS}$ capacitor, solving the demanding requirements faced by many power-supply design engineers in a simple fashion. For start-up tracking to work correctly. a minimum 4.7-nF $C_{NR/SS}$ capacitor is required. For more information on startup tracking, see the *Noise-Reduction and Soft-Start Capacitor ($C_{NR/SS}$)* section.

Feature Description (continued)

7.3.4.1 Start-Up Tracking

Figure 63 shows how both regulators use a common reference, which enables start-up tracking. Using the same reference voltage for both the positive and negative regulators ensures that the regulators start-up together in a controlled fashion; see Figure 24 and Figure 25.

Ramps on V_{INx} with EN = V_{INP} that are slower than the soft-start time do not have start-up tracking. If ramps slower than the soft-start time are used then enable should be used to start the device to ensure start-up tracking. A small mismatch between the positive and negative internal enable thresholds means that one channel turns on at a slightly lower input voltage than the other channel. This mismatch is typically not a problem in most applications and is easily solved by controlling the start-up with enable. The external signal can come from the input power supply power-good indicator, a voltage supervisor output such as the TPS3701, or from another source.

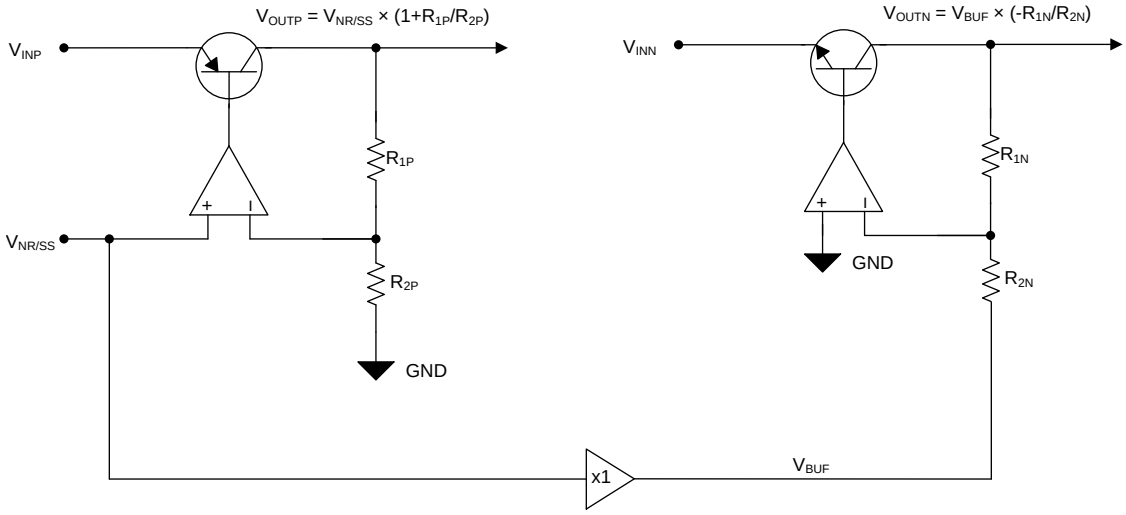


Figure 63. Simplified Regulation Circuit

7.3.4.2 Sequencing

Figure 64 and Table 2 describe how the turn-on and turn-off times of both LDOs (respectively) is controlled by setting the enable circuit (EN) and undervoltage lockout circuit (UVLOP and UVLON).

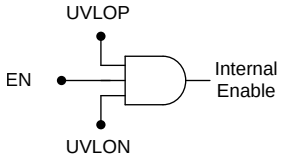


Figure 64. Simplified Turn-On Control

Table 2. Sequencing Functionality Table

POSITIVE INPUT VOLTAGE (V_{INP})	NEGATIVE INPUT VOLTAGE (V_{INN})	ENABLE STATUS	LDO STATUS	ACTIVE DISCHARGE
$V_{INP} \geq V_{UVLOP}$	$V_{INN} \leq V_{UVLON}$	EN = 1	On	Off
		EN = 0	Off	On(1)
$V_{INP} \geq V_{UVLOP}$	$V_{INN} > V_{UVLON}$	EN = don't care	Off	On(1)
$V_{INP} < V_{UVLOP}$	$V_{INN} \leq V_{UVLON}$	EN = don't care	Off	On(1)
$V_{INP} < V_{UVLOP} - V_{HYSP}$	$V_{INN} > V_{UVLON} - V_{HYSN}$	EN = don't care	Off	On(1)

(1) The active discharge remains on as long as V_{INx} and V_{OUTx} provide enough headroom for the discharge circuit to function.

7.3.4.2.1 Enable (EN)

The enable signal (V_{EN}) is an active-high digital control that enables the LDO when the enable voltage is past the rising threshold ($V_{EN} \geq V_{IH(EN)}$) and disables the LDO when the enable voltage is below the falling threshold ($V_{EN} \leq V_{IL(EN)}$). The exact enable threshold is between $V_{IH(EN)}$ and $V_{IL(EN)}$ because EN is a digital control. In applications that do not use the enable control, connect EN to V_{INP}.

A slow V_{INx} ramp directly connecting EN to V_{INP} can cause the start-up tracking to move out of specification. Under slow ramp conditions, use a resistor divider from V_{INP} to ensure start-up tracking.

7.3.4.2.2 Undervoltage Lockout (UVLO) Control

The UVLO circuit responds quickly to glitches on the input supplies and attempts to disable the output of the device if either of these rails collapse.

As a result of the fast response time of the input supply UVLO circuit, fast and short line transients well below the input supply UVLO falling threshold (brownouts) can cause momentary glitches during the edges of the transient. These glitches are typical in most LDOs. The local input capacitance prevents severe brown-outs in most applications; see the *Undervoltage Lockout (UVLOx) Control* section for more details. Fast line transients can cause the outputs to momentarily shut off, and can be mitigated through using the recommended 10-µF input capacitor. If this becomes a problem in the system, increasing the input capacitance prevents these glitches from occurring.

7.4 Device Functional Modes

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is at least as high as $|V_{INx(min)}|$
- The input voltage is greater than the nominal output voltage added to the dropout voltage
- The enable voltage has previously exceeded the enable rising threshold voltage and has not decreased below the enable falling threshold
- The output current is less than the current limit
- The device junction temperature is less than T_{SD}

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode of operation, the output voltage is the same as the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device (as a bipolar junction transistor, or BJT) is in saturation and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

7.4.3 Disabled

The device is disabled under the following conditions:

- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold
- The device junction temperature is greater than the thermal shutdown temperature

Table 3 shows the conditions that lead to the different modes of operation.

Table 3. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal mode	$\|V_{INx}\| > \|V_{OUT(nom)}\| + \|V_{DOx}\|$ and $\|V_{INx}\| > \|V_{INx(min)}\|$	$V_{EN} > V_{IH}$	$\|I_{OUTx}\| < \|I_{LIMx}\|$	$T_J < 125°C$
Dropout mode	$\|V_{INx(min)}\| < \|V_{INx}\| < \|V_{OUTx(nom)}\| + \|V_{DOx}\|$	$V_{EN} > V_{IH}$	—	$T_J < 125°C$
Disabled mode (any true condition disables the device)	—	$V_{EN} < V_{IL}$	—	$T_J > T_{SD}$

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

Successfully implementing an LDO in an application depends on the application requirements. This section discusses key device features and how to best implement the LDO to achieve a reliable design.

8.1.1 Setting the Output Voltages on Adjustable Devices

Figure 65 shows that each LDO resistor feedback network sets its output voltage. The positive LDO output voltage range is $V_{NR/SS}$ to 30 V and the negative LDO output voltage range is 0 V to –30 V.

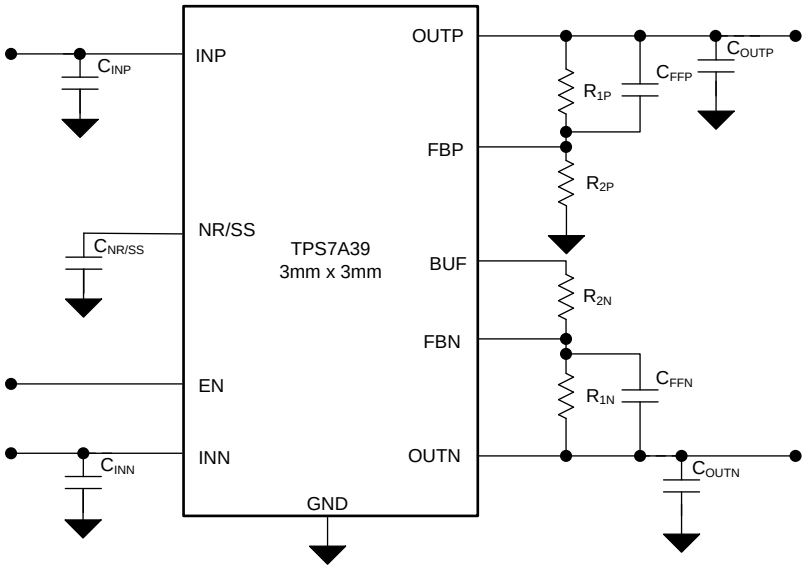


Figure 65. Adjustable Operation

Equation 1 relates the values of R_{1P} and R_{2P} to $V_{OUTP(NOM)}$ and $V_{NR/SS}$ to set the positive output voltage. Equation 2 relates the values of R_{1N} and R_{2N} to $V_{OUTN(NOM)}$ and $V_{NR/SS}$ to set the negative output voltage.

The positive LDO is configured as a noninverting op amp, whereas the negative LDO is an inverting op amp.

$$V_{OUTP} = V_{NR/SS} \times (1 + R_{1P} / R_{2P}) \quad (1)$$

$$V_{OUTN} = V_{NR/SS} \times (-R_{1N} / R_{2N}) \quad (2)$$

Substituting $V_{NR/SS}$ with V_{FBP} on the positive channel and $V_{NR/SS}$ with V_{BUF} on the negative channel gives a more accurate relationship.

Equation 3 and Equation 2 are rearranged versions of Equation 1 and Equation 2, with the above substitutions made.

$$R_{1P} = (V_{OUTP} / V_{FBP} - 1) \times R_{2P} \quad (3)$$

$$R_{1N} = -(V_{OUTN} \times R_{2P}) / V_{BUF} \quad (4)$$

The minimum bias current through both feedback networks is 5 µA to ensure accuracy.

For even tighter accuracy, take into account the input bias current into the error amplifiers (I_{FBP} and I_{FBN}) and use 0.1% resistors. Overriding the internal reference with a high accuracy external reference can also improve the accuracy of the device.

Application Information (continued)

Table 4 and Table 5 show the resistor combinations for several common output voltages using commercially available, 1% tolerance resistors.

Table 4. Recommended Feedback-Resistor Values for the Positive LDO

TARGETED OUTPUT VOLTAGE (V)	FEEDBACK RESISTOR VALUES(1)		CALCULATED OUTPUT VOLTAGE (V)
	R_{1P} (kΩ)	R_{2P} (kΩ)	
1.5	2.67	10.0	1.50
1.8	5.23	10.0	1.80
2.5	11.0	10.0	2.49
3.0	15.4	10.0	3.00
3.3	17.8	10.0	3.29
5.0	32.4	10.0	5.02
9.0	66.5	10.0	9.07
12.0	90.9	10.0	12.0
15.0	115	10.0	14.8
24.0	191	10.0	23.8
30.0	243	10.0	29.8

(1) R_{1P} is connected from OUTP to FBP, R_{2P} is connected from FBP to GND; see the *Setting the Output Voltages on Adjustable Devices* section.

Table 5. Recommended Feedback-Resistor Values for the Negative LDO

TARGETED OUTPUT VOLTAGE (V)	FEEDBACK RESISTOR VALUES(1)		CALCULATED OUTPUT VOLTAGE (V)
	R_{1N} (kΩ)	R_{2N} (kΩ)	
-0.3	2.55	10.0	-0.303
-1.5	12.7	10.0	-1.51
-1.8	15.0	10.0	-1.78
-2.5	21.0	10.0	-2.49
-3.0	25.5	10.0	-3.03
-3.3	28.0	10.0	-3.33
-5.0	42.2	10.0	-5.04
-9.0	75.0	10.0	-8.91
-12.0	100	10.0	-11.9
-15.0	127	10.0	-15.1
-24.0	200	10.0	-23.8
-30.0	255	10.0	-30.3

(1) R_{1N} is connected from OUTN to FBN, R_{2N} is connected from FBN to BUF; see the *Setting the Output Voltages on Adjustable Devices* section.

8.1.2 Capacitor Recommendations

The device is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output pins. The device is also designed to be stable with aluminum polymer and tantalum polymer capacitors with ESR < 75 mΩ.

Electrolytic capacitors (along with higher ESR polymer capacitors) can also be used if capacitors (meeting the minimum capacitance and ESR requirements) are used in parallel.

Take the effective ESR for stability when the impedance of the capacitor is at its minimum. At the minimum level, the capacitance and parasitic inductance cancel each other and provides the DC ESR.

Ceramic capacitors that employ X7R-, X5R-, and COG-rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, ceramic capacitance varies with operating voltage and temperature. As a rule of thumb, derate ceramic capacitors by at least 50%. The input and output capacitors recommended herein account for an effective capacitance derating of approximately 50%, but at higher V_{IN} and V_{OUT} conditions (that is, V_{IN} = 5.5 V to V_{OUT} = 5.0 V) the derating can be greater than 50% and must be taken into consideration.

For high performance applications polymer capacitors are ideal as they do not experience the large deratings of ceramic capacitors.

8.1.3 Input and Output Capacitor (C_{INx} and C_{OUTx})

The device is designed and characterized for operation with ceramic capacitors of 10 µF or greater (2.2 µF or greater of effective capacitance) at each input and output.

Locate the input and output capacitors as near as practical to the respective input and output pins to minimize the trace inductance from the capacitor to the device. If the LDO is used to produce low output voltages (below 5 V), a 4.7-µF output capacitor can be used. If a 4.7-µF output capacitor is used, be sure to account for the derating of the capacitors during design.

Large, fast line transients on the input supplies can cause the device output to momentarily turn off. Typically these transients do not occur in most applications, but when these transients do occur use a larger input capacitor to slow down the line transient. If the system has input line transients that are faster than 0.5 V/µs, increase the input capacitance.

8.1.4 Feed-Forward Capacitor (C_{FFx})

Although a feed-forward capacitor (C_{FFx}) from the FBx pin to the OUTx pin is not required to achieve stability, a 10-nF external C_{FFx} capacitor optimizes the transient, noise, and PSRR performance. The maximum recommended value for C_{FFx} is 100 nF.

A larger C_{FFx} can dominate the start-up time set by $C_{NR/SS}$, for more information see the *Pros and Cons of Using a Feed-Forward Capacitor with a Low Dropout Regulator* application report.

8.1.5 Noise-Reduction and Soft-Start Capacitor ($C_{NR/SS}$)

Although a noise-reduction and soft-start capacitor ($C_{NR/SS}$) from the NR/SS pin to GND is not required, $C_{NR/SS}$ is highly recommended to control the start-up time and reduce the noise-floor of the device. For start-up tracking to function correctly, a minimum 4.7-nF capacitor is required. As the time constant formed by the feedback resistors and feed-forward capacitors increases, the value of the $C_{NR/SS}$ capacitor must also be increased for startup tracking to work correctly. To figure out how to calculate the time constant of the feedback network see the *Pros and Cons of Using a Feed-Forward Capacitor with a Low Dropout Regulator* application report.

8.1.6 Buffered Reference Voltage

The voltage at the NR/SS pin, whether driven internally or externally, is buffered with a high-bandwidth, low-noise op amp. The BUF pin can be used as a voltage reference in many signal chain applications.

8.1.7 Overriding Internal Reference

The internal reference of the LDO can be overridden using an external source to increase the accuracy of the LDO and lower the output noise. To override the internal reference connect the external source to the NR/SS pin of the LDO. In order to overdrive the internal reference the external source must be able to source or sink 100 µA or greater.

The internal reference achieves a 2% accuracy from –40°C to +125°C; using an external reference can help achieve better accuracy over temperature.

8.1.8 Start-Up

8.1.8.1 Soft-Start Control (NR/SS)

Each output of the device features a user-adjustable, monotonic, voltage-controlled soft-start that is set with an external capacitor ($C_{NR/SS}$). This soft-start eliminates power-up initialization problems.

The output voltage (V_{OUTx}) rises proportionally to $V_{NR/SS}$ during start-up. As such, the time required for $V_{NR/SS}$ to reach its nominal value determines the rise time of V_{OUTx} (start-up time).

The soft-start ramp time depends on the soft-start charging current ($I_{NR/SS}$), the soft-start capacitance ($C_{NR/SS}$), and the internal reference ($V_{NR/SS}$). Equation 5 calculates the approximate soft-start ramp time (t_{SS}):

$$t_{SS} = R_{NR/SS} \times C_{NR/SS} \times \ln\left[(V_{NR/SS} + I_{NR/SS} \times R_{NR/SS}) / (I_{NR/SS} \times R_{NR/SS})\right] \quad (5)$$

Values for the soft-start charging currents, $R_{NR/SS}$, and the device internal $C_{NR/SS}$ are provided in the table.

8.1.8.1.1 In-Rush Current

In-rush current is defined as the current into the LDO at the INx pin during start-up. In-rush current then consists primarily of the sum of load current and the current used to charge the output capacitor. This current is difficult to measure because the input capacitor must be removed, which is not recommended. However, the in-rush current can be estimated by Equation 6:

$$I_{OUTx}(t) = \left[\frac{C_{OUTx} \times dV_{OUTx}(t)}{dt}\right] + \left[\frac{V_{OUTx}(t)}{R_{LOAD}}\right] \quad (6)$$

where:

- $V_{OUTx}(t)$ is the instantaneous output voltage of the turn-on ramp
- $dV_{OUTx}(t) / dt$ is the slope of the V_{OUTx} ramp
- R_{LOAD} is the resistive load impedance

8.1.8.2 Undervoltage Lockout (UVLOx) Control

The UVLOx circuit ensures that the device stays disabled before its input or bias supplies reach the minimum operational voltage range, and ensures that the device properly shuts down when the input supply collapses.

Figure 66 and Table 6 explain the UVLOx circuit response to various input voltage events, assuming $V_{EN} \geq V_{IH(EN)}$.

The positive and negative UVLO circuits are internally ANDed together. As such, if either supply collapses, both outputs turn-off and $V_{NR/SS}$ is pulled low internally.

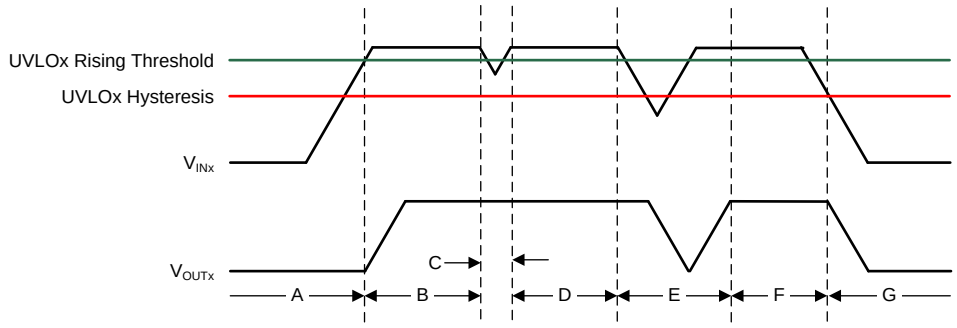


Figure 66. Typical UVLOx Operation

Table 6. Typical UVLOx Operation Description

REGION	EVENT	V_{OUTx} STATUS	COMMENT
A	Turn-on, $\|V_{INx}\| \le \|V_{UVLOx}\|$	0	Start-up
B	Regulation	1	Regulates to target V_{OUTx}
C	Brownout, $\|V_{INx}\| \ge \|V_{UVLOx} - V_{HYSx}\|$	1	The output can fall out of regulation but the device is still enabled
D	Regulation	1	Regulates to target V_{OUTx}
E	Brownout, $\|V_{INx}\| < \|V_{UVLOx} - V_{HYSx}\|$	0	The device is disabled and the output falls because of the load and active discharge circuit. The device is reenabled when the UVLOx rising threshold is reached by the input voltage and a normal start-up then follows.
F	Regulation	1	Regulates to target V_{OUTx}
G	Turn-off, $\|V_{INx}\| < \|V_{UVLOx} - V_{HYSx}\|$	0	The output falls because of the load and active discharge circuit

Similar to many other LDOs with this feature, the UVLOx circuit takes a few microseconds to fully assert. During this time, a downward line transient below approximately 0.8 V causes the UVLOx to assert for a short time; however, the UVLOx circuit does not have enough stored energy to fully discharge the internal circuits inside of the device. When the UVLOx circuit is not given enough time to fully discharge the internal nodes, the outputs are not fully disabled.

The effect of the downward line transient can be mitigated by using a larger input capacitor to increase the fall time of the input supply when operating near the minimum V_{INx}.

8.1.9 AC and Transient Performance

LDO ac performance for a dual-channel device includes power-supply rejection ratio, channel-to-channel output isolation, output current transient response, and output noise. These metrics are primarily a function of open-loop gain, bandwidth, and phase margin that control the closed-loop input and output impedance of the LDO. The output noise is primarily a result of the band-gap reference and error amplifier noise.

8.1.9.1 Power-Supply Rejection Ratio (PSRR)

PSRR is a measure of how well the LDO control-loop rejects signals from V_{INx} to V_{OUTx} across the frequency spectrum (usually 10 Hz to 10 MHz). Equation 7 gives the PSRR calculation as a function of frequency for the input signal [$V_{INx}(f)$] and output signal [$V_{OUTx}(f)$].

$$\text{PSRR (dB)} = 20\,\text{Log}_{10}\left(\frac{V_{INx}(f)}{V_{OUTx}(f)}\right) \tag{7}$$

Even though PSRR is a loss in signal amplitude, PSRR is shown as positive values in decibels (dB) for convenience.

Figure 67 shows a simplified diagram of PSRR versus frequency.

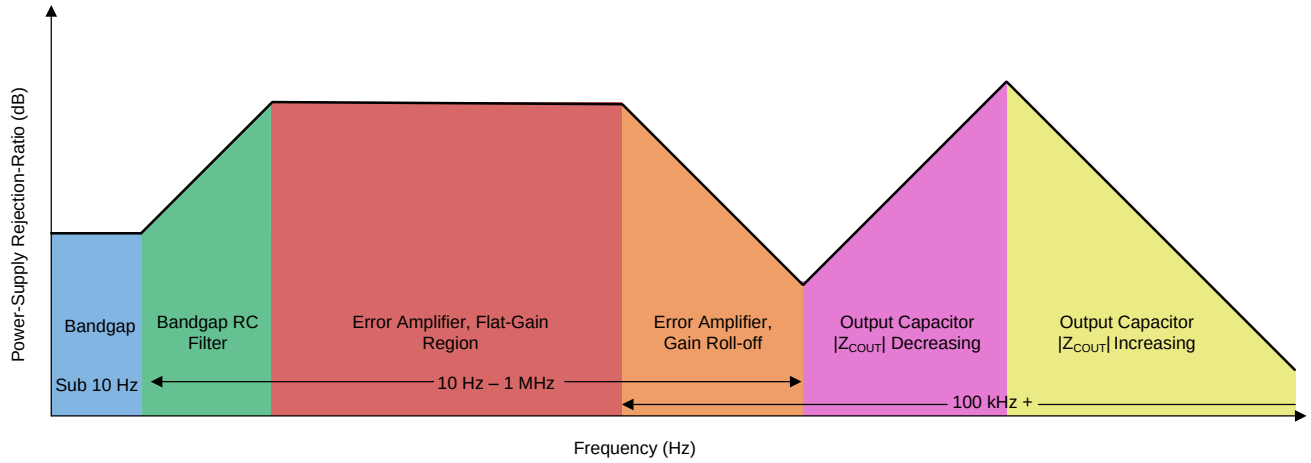


Figure 67. Power-Supply Rejection Ratio Diagram

An LDO is often employed not only as a dc-dc regulator, but also to provide exceptionally clean power-supply voltages that exhibit ultra-low noise and ripple to sensitive system components.

8.1.9.2 Channel-to-Channel Output Isolation and Crosstalk

Output isolation is a measure of how well the device prevents voltage disturbances on one output from affecting the other output. This attenuation appears in load transient tests on the other output; however, to numerically quantify the rejection, the output channel isolation is expressed in decibels (dB).

Output isolation performance is a strong function of the PCB layout. See the *Layout Guidelines* section on how to best optimize the isolation performance.

8.1.9.3 Output Voltage Noise

The TPS7A39 is designed for system applications where minimizing noise on the power-supply rail is critical to system performance. For example, the TPS7A39 can be used in a phase-locked loop (PLL)-based clocking circuit that can be used for minimum phase noise, or in test and measurement systems where even small power-supply noise fluctuations reduce system dynamic range.

LDO noise is defined as the internally-generated intrinsic noise created by the semiconductor circuits alone. This noise is the sum of various types of noise (such as shot noise associated with current-through-pin junctions, thermal noise caused by thermal agitation of charge carriers, flicker noise, or 1/f noise and dominates at lower frequencies as a function of 1/f). Figure 68 shows a simplified output voltage noise density plot versus frequency.

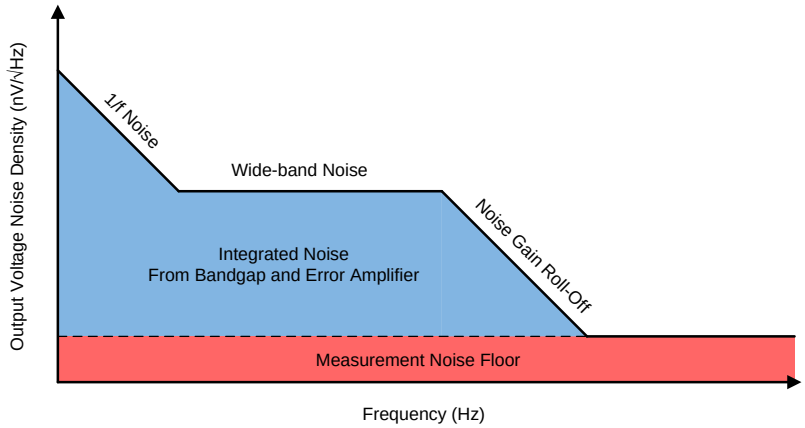


Figure 68. Output Voltage Noise Diagram

For further details, see the *How to Measure LDO Noise* white paper.

8.1.9.4 Optimizing Noise and PSRR

Table 7 describes how the ultra-low noise floor and PSRR of the device can be improved in several ways.

Table 7. Effect of Various Parameters on AC Performance(1)(2)

PARAMETER	NOISE			PSRR		
	LOW-FREQUENCY	MID-FREQUENCY	HIGH-FREQUENCY	LOW-FREQUENCY	MID-FREQUENCY	HIGH-FREQUENCY
$C_{NR/SS}$	+++	No effect	No effect	+++	+	No effect
C_{FFx}	++	+++	+	++	+++	+
C_{OUTx}	No effect	+	+++	No effect	+	+++
$\lvert V_{INx}\rvert - \lvert V_{OUTx}\rvert$	+	+	+	+++	+++	++
PCB layout	++	++	+	+	+++	+++

(1) The number of +s indicates the improvement in noise or PSRR performance by increasing the parameter value.
(2) Shaded cells indicate the easiest improvement to noise or PSRR performance.

The noise-reduction capacitor, in conjunction with the noise-reduction resistor, forms a low-pass filter (LPF) that filters out the noise from the reference before being gained up with the error amplifier, thereby minimizing the output voltage noise floor. The LPF is a single-pole filter and the cutoff frequency can be calculated with Equation 8. The effect of the $C_{NR/SS}$ capacitor increases when $V_{OUTx(NOM)}$ increases because the noise from the reference is gained up when the output voltage increases. For low-noise applications, a 10-nF to 1-µF $C_{NR/SS}$ is recommended.

$$f_{cutoff} = 1 / (2 \times \pi \times R_{NR/SS} \times C_{NR/SS}) \quad (8)$$

The feed-forward capacitor reduces output voltage noise by filtering out the mid-band frequency noise. The feed-forward capacitor can be optimized by placing a pole-zero pair near the edge of the loop bandwidth and pushing out the loop bandwidth, thus improving mid-band PSRR.

A larger C_{OUTx} or multiple output capacitors reduces high-frequency output voltage noise and PSRR by reducing the high-frequency output impedance of the power supply.

Additionally, a higher input voltage improves the noise and PSRR because greater headroom is provided for the internal circuits. However, a high power dissipation across the die increases the output noise because of the increase in junction temperature.

Good PCB layout improves the PSRR and noise performance by providing heatsinking at low frequencies and isolating V_{OUTx} at high frequencies.

8.1.9.5 Load Transient Response

The load-step transient response is the output voltage response by the LDO to a step in load current, whereby output voltage regulation is maintained. There are two key transitions during a load transient response: the transition from a light to a heavy load and the transition from a heavy to a light load. The regions illustrated in Figure 69 are broken down in this section and are described in Table 8. Regions A, E, and H are where the output voltage is in steady-state. Increasing the output capacitance improves the transient response (less dip); however, the transient takes longer to recover when using a large output capacitor.

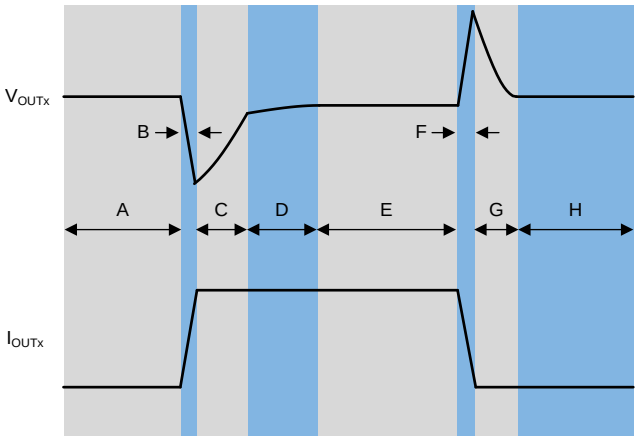


Figure 69. Load Transient Waveform

Table 8. Load Transient Waveform Description

REGION	DESCRIPTION	COMMENT
A	Regulation	Regulation
B	Output current ramping	Initial voltage dip is a result of the depletion of the output capacitor charge.
C	LDO responding to transient	Recovery from the dip results from the LDO increasing its sourcing current, and leads to output voltage regulation.
D	Reaching thermal equilibrium	At high load currents the LDO takes some time to heat up. During this time the output voltage changes slightly.
E	Regulation	Regulation
F	Output current ramping	Initial voltage rise results from the LDO sourcing a large current, and leads to the output capacitor charge to increase.
G	LDO responding to transient	Recovery from the rise results from the LDO decreasing its sourcing current in combination with the load discharging the output capacitor.
H	Regulation	Regulation

8.1.10 DC Performance

8.1.10.1 Output Voltage Accuracy (V_{OUTx})

The device features an output voltage accuracy that includes the errors introduced by the internal reference, load regulation, line regulation, process variation, and operating temperature as specified by the table. Output voltage accuracy specifies minimum and maximum output voltage error, relative to the expected nominal output voltage stated as a percent (for very low output voltages this specification is in mV).

8.1.10.2 Dropout Voltage (V_{DO})

Generally speaking, the dropout voltage often refers to the minimum voltage difference between the input and output voltage ($|V_{DO}| = |V_{INx}| - |V_{OUTx}|$) that is required for regulation. When V_{INx} drops below the required V_{DOx} for the given load current, the device functions as a resistive switch and does not regulate output voltage. Dropout voltage is proportional to the output current because the device is operating as a resistive switch.

8.1.11 Reverse Current

As with most LDOs, this device can be damaged by excessive reverse current.

Reverse current is current that flows through the substrate of the device instead of the normal conducting channel of the pass element. This current flow, at high enough magnitudes, degrades long-term reliability of the device resulting from risks of electromigration and excess heat being dissipated across the device.

Conditions where excessive reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUTP} > V_{INP} + 0.3$ V and $V_{OUTN} < V_{INN} – 0.3$ V:

- If the device has a large C_{OUTx} and the input supply collapses quickly with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If excessive reverse current flow is expected in the application, then external protection must be used to protect the device. Figure 70 shows one approach of protecting the device.

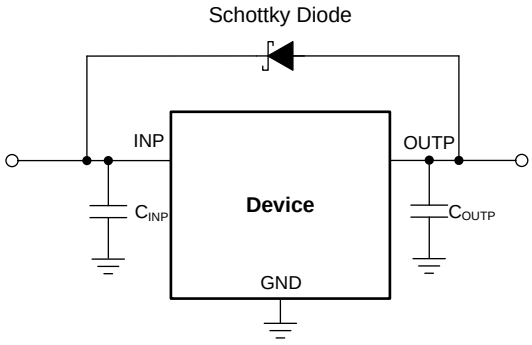


Figure 70. Example Circuit for Reverse Current Protection Using a Schottky Diode On Positive Rail

8.1.12 Power Dissipation (P_D)

Circuit reliability demands that proper consideration is given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must be as free as possible of other heat-generating devices that cause added thermal stresses.

As a first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. Use Equation 9 to approximate P_D:

$$P_D = (V_{INP} – V_{OUTP}) \times I_{OUTP} + (|V_{INN} – V_{OUTN}|) \times |I_{OUTN}| \quad (9)$$

Careful selection of the system voltage rails minimizes power dissipation and improves system efficiency. Proper selection allows the minimum input-to-output voltage differential to be obtained. The low dropout of the device allows for maximum efficiency across a wide range of output voltages.

The main heat conduction path for the device is through the thermal pad on the package. As such, the thermal pad must be soldered to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to any inner plane areas or to a bottom-side copper plane.

The maximum power dissipation determines the maximum allowable junction temperature (T_J) for the device. According to Equation 10, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance (θ_{JA}) of the combined PCB, device package, and the temperature of the ambient air (T_A).

$$T_J = T_A + \theta_{JA} \times P_D \quad (10)$$

Unfortunately, this thermal resistance (θ_{JA}) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The θ_{JA} recorded in the *Electrical Characteristics* table is determined by the JEDEC standard, PCB, and copper-spreading area, and is only used as a relative measure of package thermal performance. For a well-designed thermal layout, θ_{JA} is actually the sum of the WSON package junction-to-case (bottom) thermal resistance (θ_{JCbot}) plus the thermal resistance contribution by the PCB copper.

8.1.12.1 Estimating Junction Temperature

The JEDEC standard recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of the copper-spreading area. The key thermal metrics (Ψ_{JT} and Ψ_{JB}) are given in the *Electrical Characteristics* table and are used in accordance with Equation 11.

$$\Psi_{JT}: T_J = T_T + \Psi_{JT} \times P_D$$
$$\Psi_{JB}: T_J = T_B + \Psi_{JB} \times P_D$$

where:

- P_D is the power dissipated as explained in Equation 9
- T_T is the temperature at the center-top of the device package
- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

(11)

8.2 Typical Applications

8.2.1 Design 1: Single-Ended to Differential Isolated Supply

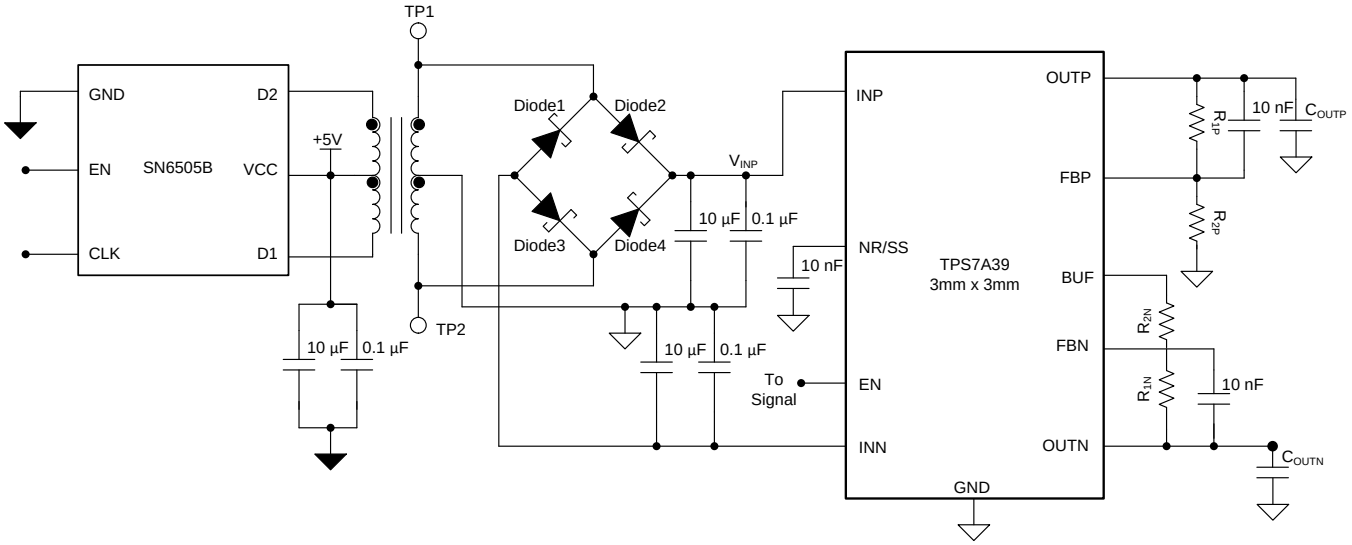


Figure 71. Single-Ended to Differential Isolated Supply Schematic

8.2.1.1 Design Requirements

Table 9. Design Requirements

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Input supply	Must operate off of 5-V input	5-V input supply
Output supply	Must have a 5-V and –5-V output	±5-V output, ±2% accuracy
Positive output current	Capable of sourcing 50 mA on positive output	50 mA (sourcing)
Negative output current	Capable of sinking 50 mA on negative output	50 mA (sinking)
Isolation from 5-V supply	Must be isolated from input supply	Isolated through center tapped transformer
Efficiency	Must have > 80% efficiency at 100 mA(1)	85% efficiency when I_{OUTN} = –50 mA and I_{OUTP} = 50 mA

(1) $|I_{OUTN}| = I_{OUTP} = 50$ mA.

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Switcher Choice

This design incorporates a push-pull driver for center-tapped transformers that takes a single-ended supply and converts the supply to an isolated split rail design. The SN6505B provides a simple small-form factor isolated supply. The input voltage of the SN6505B can vary from 2.25 V to 5 V, which allows for use with a wide range of input supplies. The output voltage can be adjusted through the turns ratio of the transformer. Based on the choice of the transformer this design can be used to create output voltages from ±3.3 V to ±15 V. In this design the SN6505B was paired with the 750315371 center-tapped transformer from Wurth Electronics™. This transformer has a turns ratio of 1:1.1 and an isolation rating of 2500 V_{RMS} (the total system isolation was never tested).

8.2.1.2.2 Full Bridge Rectifier With Center-Tapped Transformer

To create the isolated supply, the SN6505B uses a center-tapped transformer. A full bridge rectifier and capacitors are required to regulate the signal before reaching the LDO because of the alternating nature of the input signal. TI recommends having a fast switching and low forward voltage diode to improve efficiency because of how fast the SN6505 switches; Schottky diodes work well. Figure 73 shows the switching nodes of the SN6505 D1 and D2 and also shows where the transformer connects to the full bridge rectifier TP1 and TP2. Figure 73 shows the switching waveforms across the rectifier diodes.

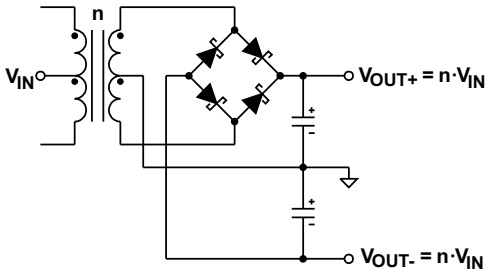


Figure 72. Bridge Rectifier With Center-Tapped Secondary Enables Bipolar Outputs

8.2.1.2.3 Total Solution Efficiency

Equation 12 shows how the efficiency of the system can be measured by taking the output power and dividing by the input power. $I_{OUTP} = |I_{OUTN}| = I_{OUT} / 2$ because this system has two output rails to simplify the efficiency measurement. When the necessary parameters are measured, and by using Equation 12, the overall system efficiency can be plotted as in Figure 74. Figure 74 shows the overall system efficiency for this design, at the maximum output current of 100 mA (I_{OUTP} = 50 mA, I_{OUTN} = –50 mA) the efficiency of the system is 85%.

$$\eta = (I_{OUTP} \times V_{OUTP} + I_{OUTN} \times V_{OUTN}) / (I_{IN} \times V_{IN}) \quad (12)$$

8.2.1.2.4 Feedback Resistor Selection

Equation 13 and Equation 14 calculate the values of the feedback resistors.

$$V_{OUTP} = V_{FBP} \times (1 + R_{1P} / R_{2P}) \quad (13)$$

$$V_{OUTN} = V_{BUF} \times (-R_{1N} / R_{2N}) \quad (14)$$

For this design the recommended 10-kΩ resistors are used for R_{2P} and R_{2N}. R_{1P} and R_{1N} can be calculated by substituting R_{2P} and R_{2N} into Equation 15 and Equation 16 because R_{2P} and R_{2N} are already selected

$$R_{1P} = [(V_{OUTP} / V_{FBP}) - 1] \times R_{2P} = [(5\text{ V} / 1.188\text{ V}) - 1] \times 10\text{ k}\Omega = 32.2\text{ k}\Omega \quad (15)$$

$$R_{1N} = -V_{OUTN} \times R_{2N} / V_{BUF} = -(-5\text{ V}) \times 10\text{ k}\Omega / 1.19\text{ V} = 42\text{ k}\Omega \quad (16)$$

After solving for Equation 15 and Equation 16, the closest one percent resistors are selected, R_{1N} = 42.2 kΩ and R_{1P} = 32.4 kΩ.

8.2.1.3 Application Curves

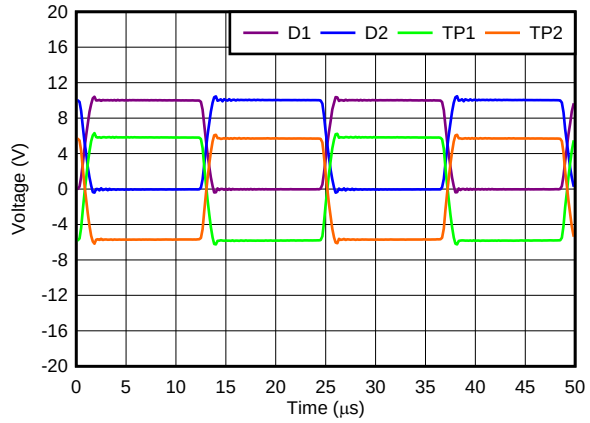


Figure 73. Switching Node of the SN6505B

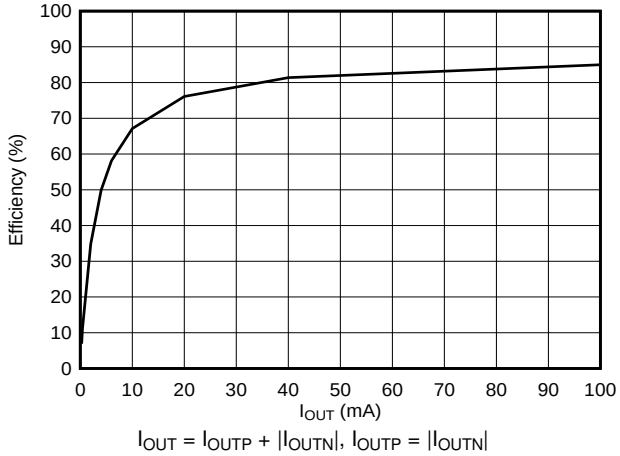


Figure 74. Efficiency vs Output Current

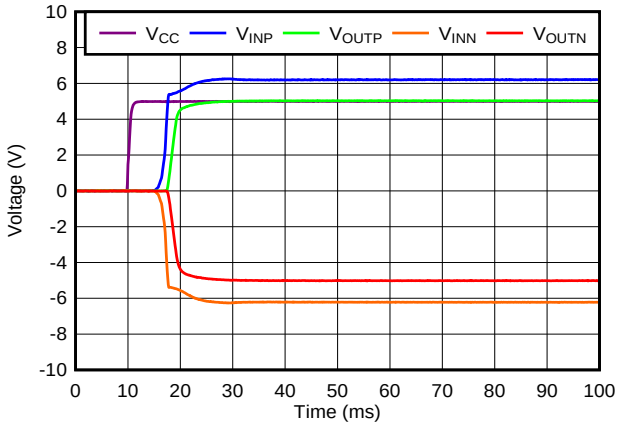


Figure 75. System Startup

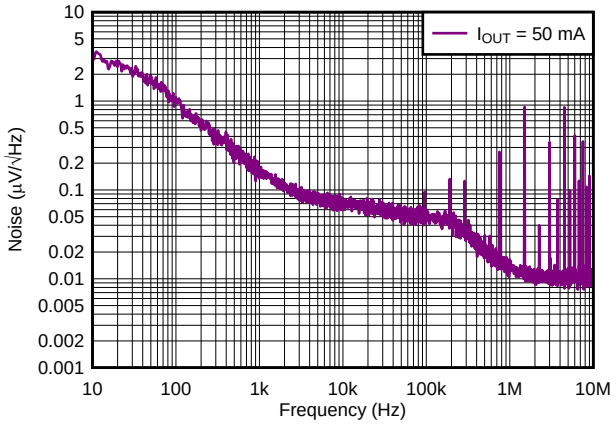


Figure 76. OUTP Noise

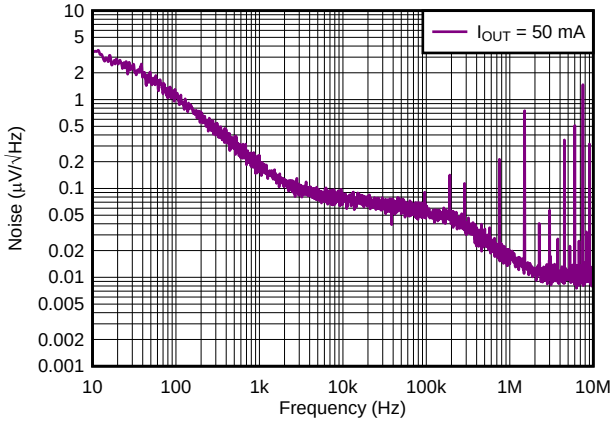


Figure 77. OUTN Noise

8.2.2 Design 2: Getting the Full Range of a SAR ADC

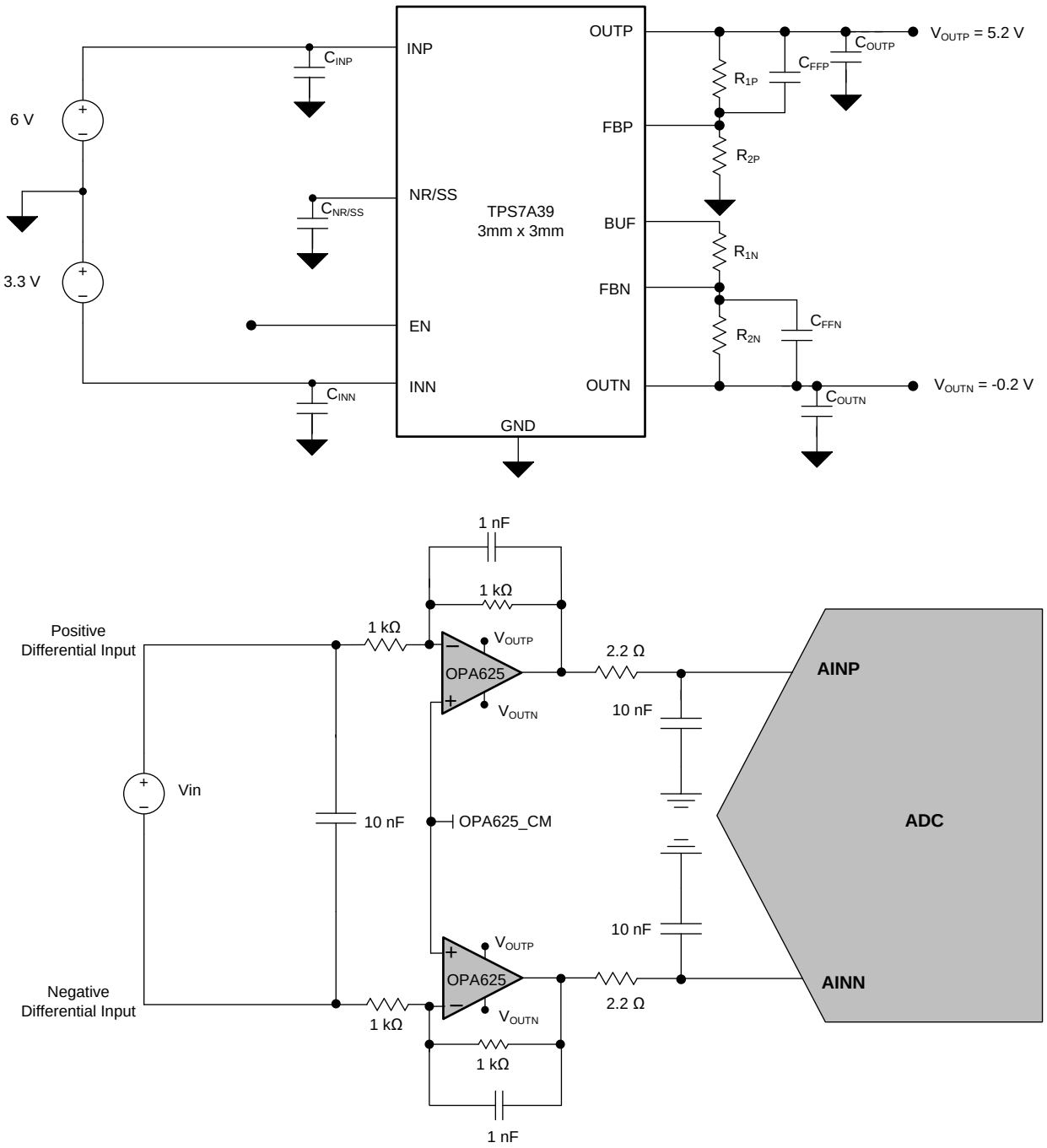


Figure 78. Creating Power Rails for an Analog Front-End of an ADC

8.2.2.1 Design Requirements

A common problem in analog-to-digital converters (ADCs) is that as the input signal approaches the edge of the range of the ADC, the signal begins to become distorted. Often times this is not because of a limitation of the ADC, but is a result of the analog front-end (AFE). In the AFE, the signal begins to approach the rails of the op amp and the signal begins to lose linearity and becomes distorted. This distortion is because when the rail-to-rail op amp begins to enter the nonlinear region of operation within 100 mV of the rail, the signal-to-noise ratio (SNR) starts to degrade and the total harmonic distortion (THD) of the ADC increases. To prevent the op amp from exiting the linear region of operation, the design must use a power supply that can generate rails 200 mV above and below the input range of the ADC.

8.2.2.2 Detailed Design Procedure

In this design, the ADS8900B is used as the ADC. This ADC features a differential input, so from a 5-V reference the ADC is able to encode values between ±5 V. In many applications, single-supply op amps are powered with rails from 0 V to 5 V, which causes the input signal to become distorted when the full range signal is applied. The FFT of a 10-V_{PP} (peak-to-peak) sine wave using a single 5-V rail to bias the amplifiers is illustrated in Figure 79. In this test the SNR was calculated to be 54.89 dB and the THD was calculated to be –40.68 dB.

There is a simple solution to improve the SNR and THD of the ADC: bias the amplifiers in the analog front end with a 5.2-V rail and a –0.2-V rail. Using these rails allows the amplifier to operate in the linear region in the 0-V to 5-V range needed by the ADC. The FFT of a 10-V_{PP} sine wave using a 5.2-V rail and a –0.2-V rail is illustrated in Figure 80. In this test the SNR was calculated to be 102.535 dB and the THD was calculated to be –121.66 dB. Using –0.2-V and 5.2-V rail voltages still allows for common 5-V (5.5 V max) op amps to be used in the design.

8.2.2.3 Detailed Design Description

8.2.2.3.1 Regulation of –0.2 V

The TPS7A39 has an innovative feature of regulating the negative rail down to zero volts. This regulation is achieved by using an inverting amplifier and using the positive-buffered reference as the input signal to the amplifier. Regulating to –0.2 V eliminates the nonlinearity and distortion present when using the full rail range of the amplifiers.

8.2.2.3.2 Feedback Resistor Selection

Use Equation 17 and Equation 18 to calculate the values of the feedback resistors:

$$V_{OUTP} = V_{FBP} \times (1 + R_{1P} / R_{2P}) \quad (17)$$

$$V_{OUTN} = V_{BUF} \times (-R_{1N} / R_{2N}) \quad (18)$$

For this design the recommended 10-kΩ resistors are used for R_{2P} and R_{2N}. R_{1P} and R_{1N} can be calculated by substituting R_{2P} and R_{2N} into Equation 19 and Equation 20 because R_{2P} and R_{2N} are already selected.

$$R_{1P} = [(V_{OUTP} / V_{FBP}) - 1] \times R_{2P} = [(5.2\ V / 1.188\ V) - 1] \times 10\ k\Omega = 33.8\ k\Omega \quad (19)$$

$$R_{1N} = -V_{OUTN} \times R_{2N} / V_{BUF} = -(-5\ V) \times 10\ k\Omega / 1.19\ V = 1.68\ k\Omega \quad (20)$$

After solving for Equation 19 and Equation 20, the closest one percent resistors are selected, R_{1N} = 1.69 kΩ and R_{1P} = 34 kΩ.

8.2.2.4 Application Curves

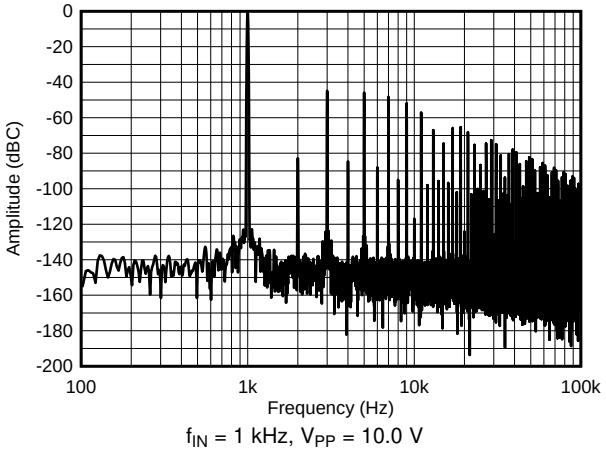


Figure 79. FFT Using 5-V and 0-V Supply Rails

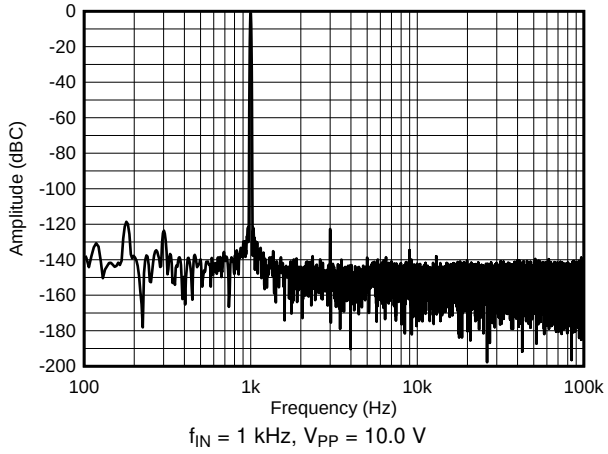


Figure 80. FFT Using 5.2-V and –0.2-V Supply Rails

9 Power-Supply Recommendations

The input supply for the LDO must be within the recommended operating conditions. The input voltage must provide adequate headroom in order for the device to have a regulated output. Place the 10-µF input capacitors as close to the device as possible. If the input supply is noisy, additional input capacitors can help improve the output noise performance.

10 Layout

10.1 Layout Guidelines

Layout is a critical part of good power-supply design. There are several signal paths that conduct fast-changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power-supply performance. To help eliminate these problems, bypass the IN pin to ground with capacitors.

Tie the GND pin directly to the thermal pad under the device. The thermal pad must be connected to any internal PCB ground planes using multiple vias directly under the device.

Every capacitor must be placed as close as possible to the device and on the same side of the PCB as the regulator itself.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because these circuits can impact system performance negatively, and even cause instability.

10.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

To improve ac performance (such as PSRR, output noise, and transient response), TI recommends that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with each ground plane star connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor must connect directly to the GND pin of the device.

10.2 Layout Example

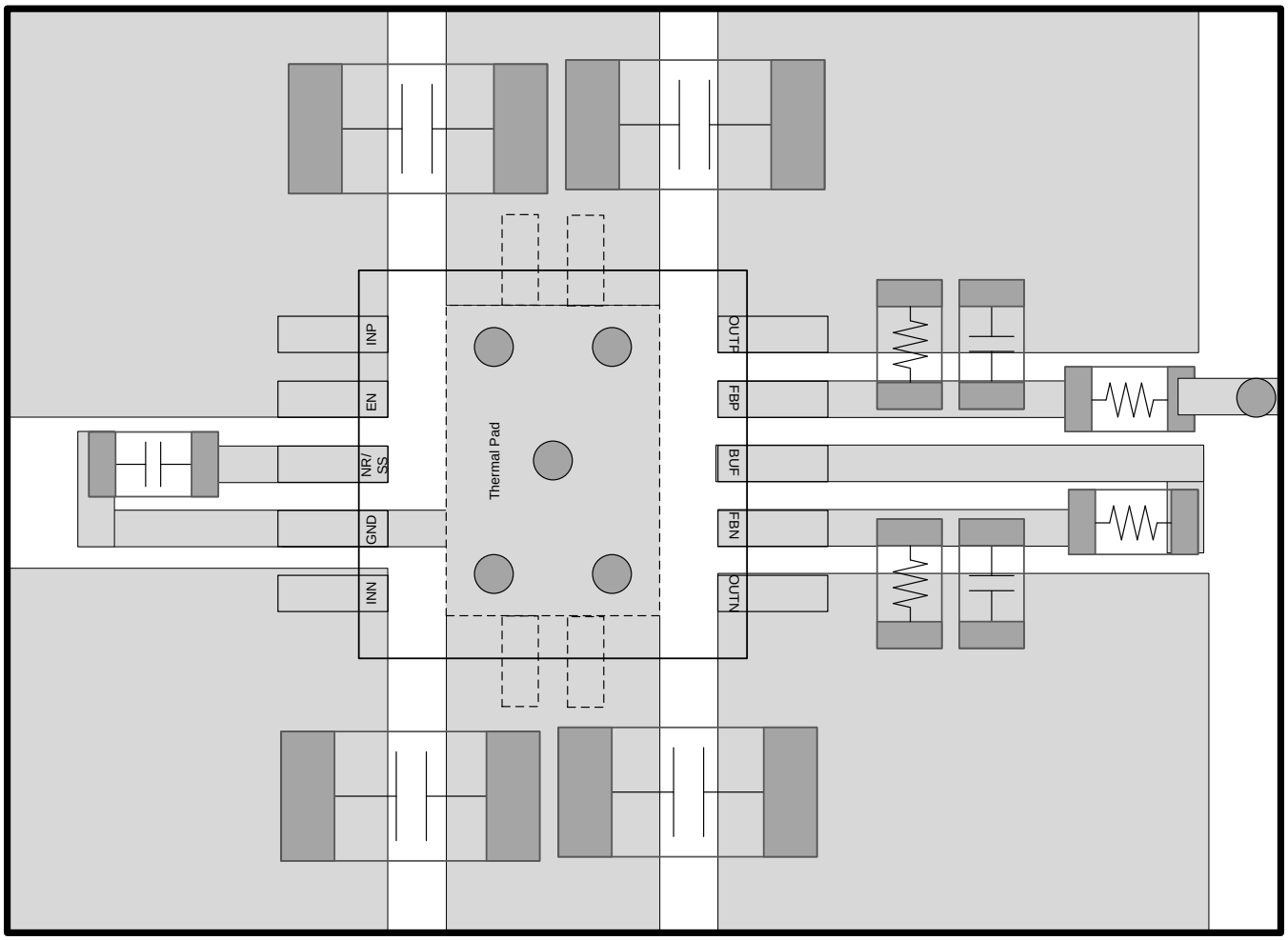


Figure 81. Layout Example for Adjustable Option

10.3 Package Mounting

Solder pad footprint recommendations for the TPS7A39 are available at the end of this document and at www.ti.com.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS7A39. The TPS7A39EVM-865 evaluation module (and related user guide) can be requested at the Texas Instruments website through the product folder or purchased directly from the TI eStore.

11.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS7A39 is available through the product folder under *Tools & Software*.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *TPS3701 36-V Window Comparator with Internal Reference for Over- and Undervoltage Detection*
- *SN6505 Low-Noise 1-A Transformer Drivers for Isolated Power Supplies*
- *ADS890xB 20-Bit, High-Speed SAR ADCs With Integrated Reference Buffer, and Enhanced Performance Features*
- *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator*
- *Using New Thermal Metrics*
- *TPS7A39EVM-865 User's Guide*

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
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All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A3901DSCR	ACTIVE	WSON	DSC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A3901	Samples
TPS7A3901DSCT	ACTIVE	WSON	DSC	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A3901	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

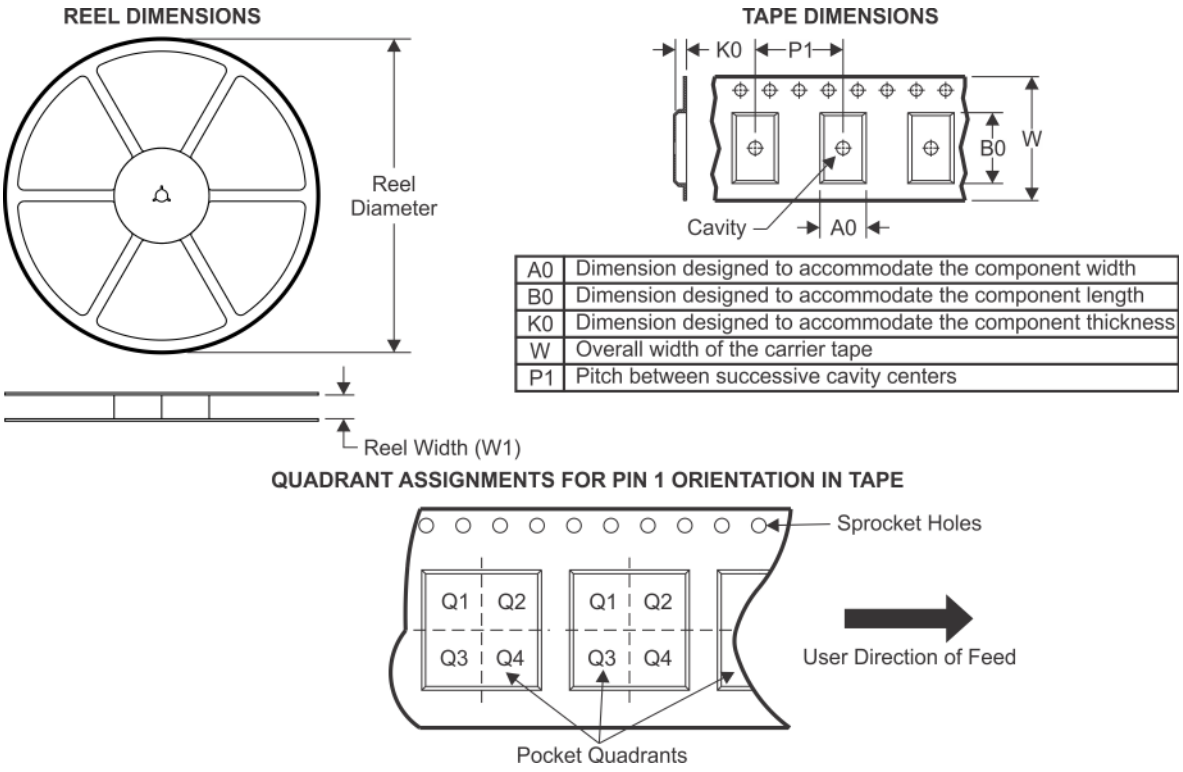
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

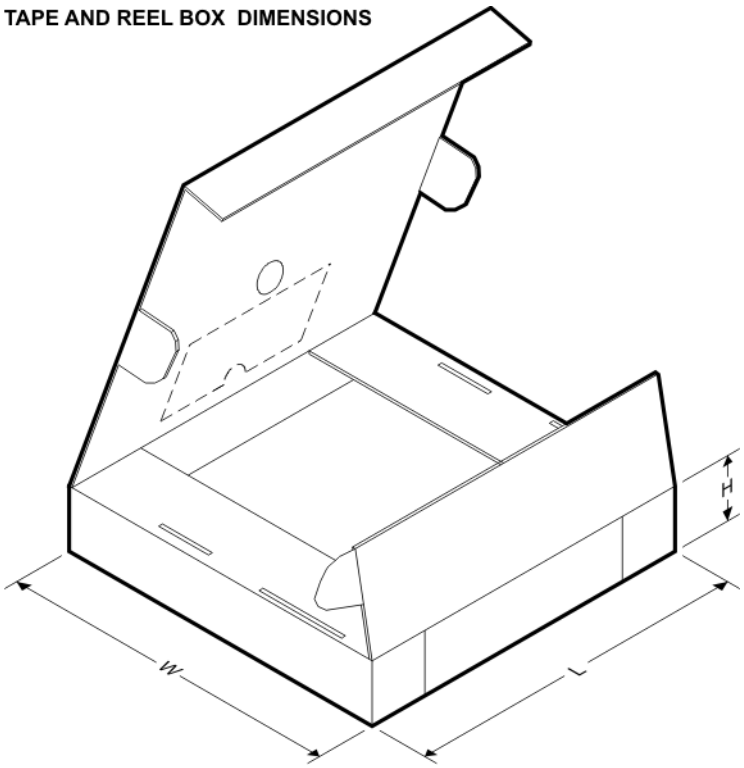


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A3901DSCR	WSON	DSC	10	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
TPS7A3901DSCT	WSON	DSC	10	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



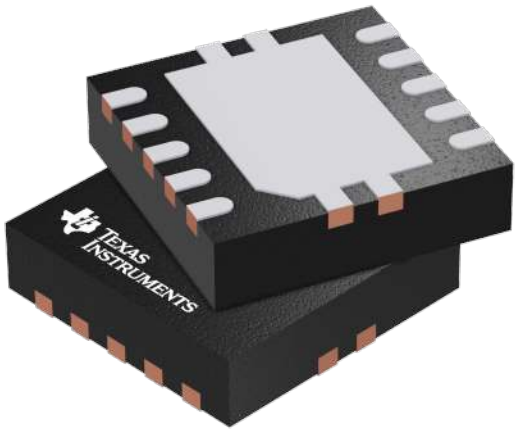
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A3901DSCR	WSON	DSC	10	3000	367.0	367.0	38.0
TPS7A3901DSCT	WSON	DSC	10	250	213.0	191.0	35.0

GENERIC PACKAGE VIEW

DSC 10 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



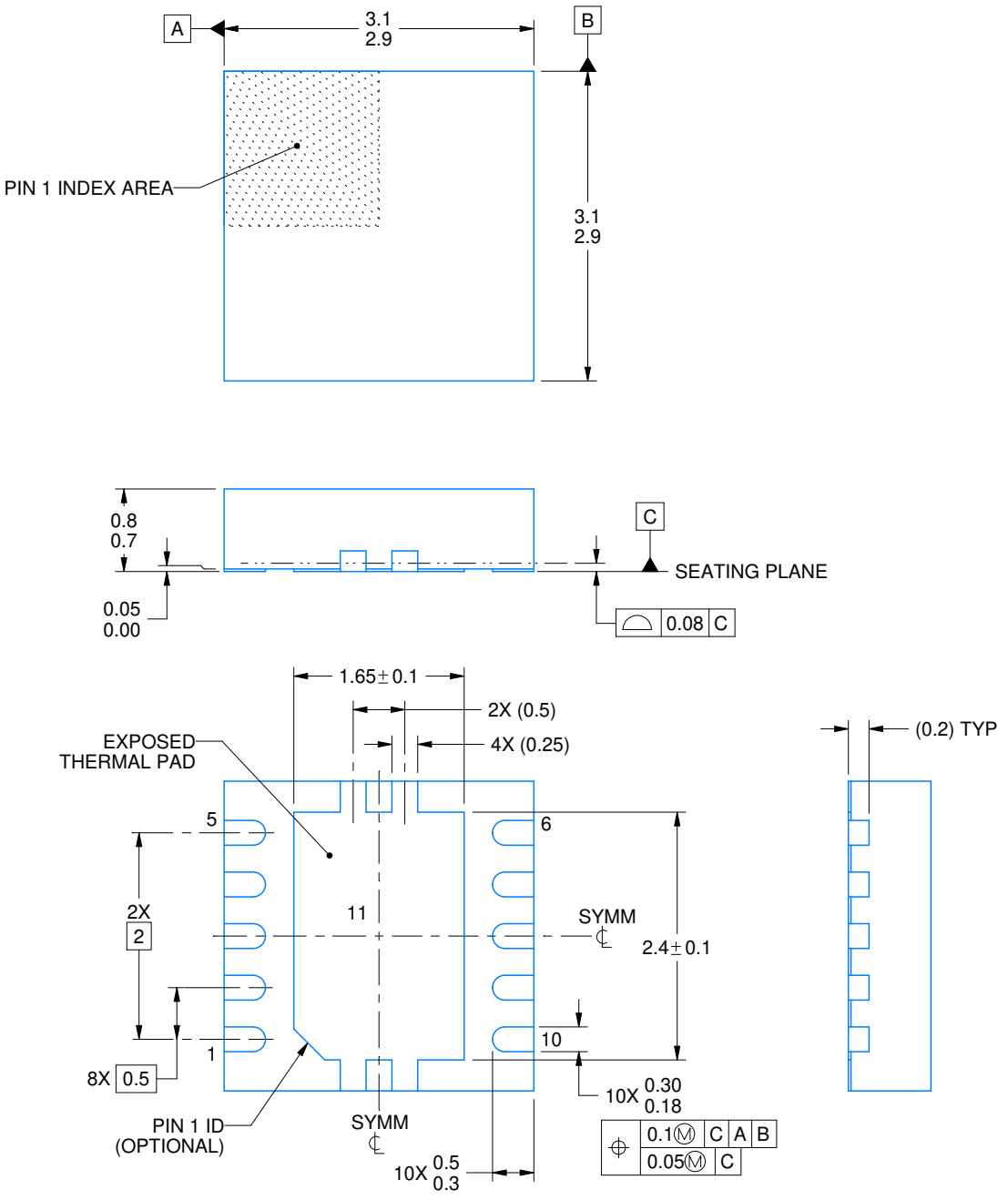
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DSC0010J

PACKAGE OUTLINE

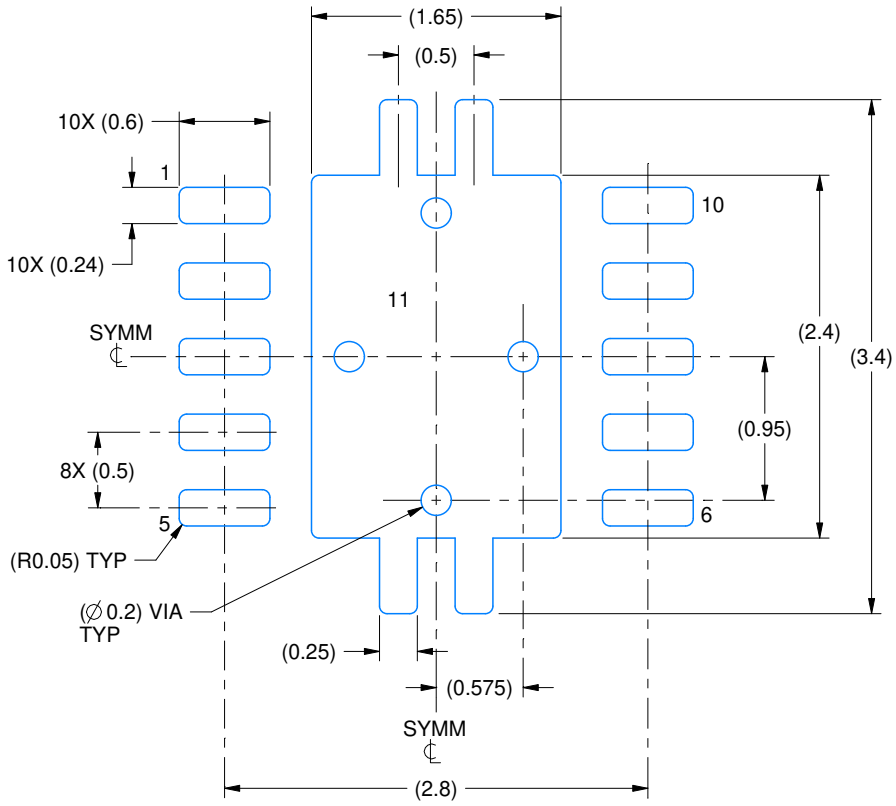
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

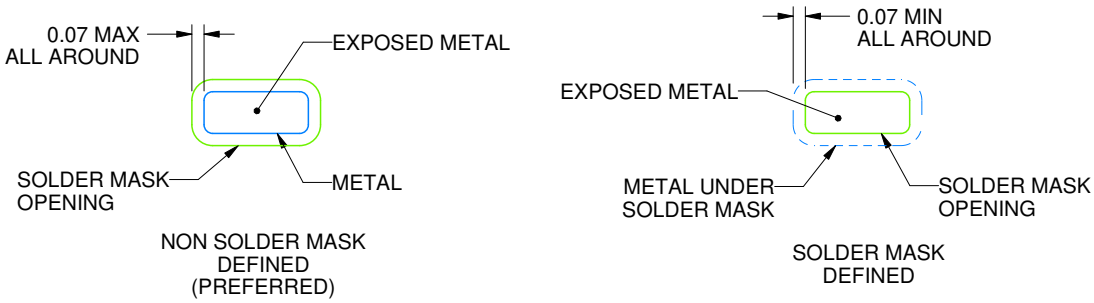


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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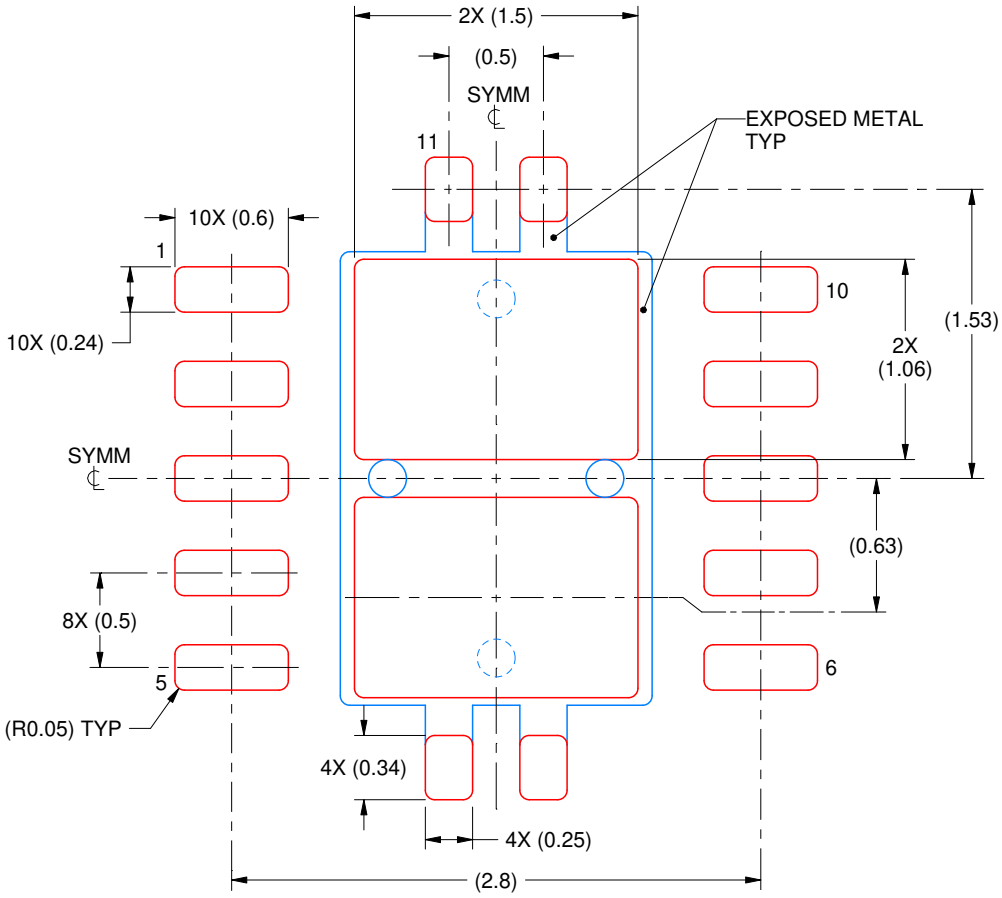
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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