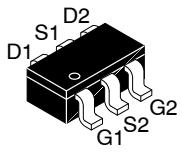
Field Effect Transistor - Dual, N-Channel, Enhancement Mode

NDC7002N



TSOT23 6−Lead
CASE 419BL

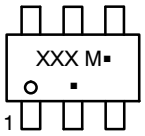
General Description

These dual N−Channel enhancement mode power field effect transistors are produced using **onsemi**'s proprietary, high cell density, DMOS technology. This very high density process has been designed to minimize on−state resistance, provide rugged and reliable performance and fast switching. These devices is particularly suited for low voltage applications requiring a low current high side switch.

Features

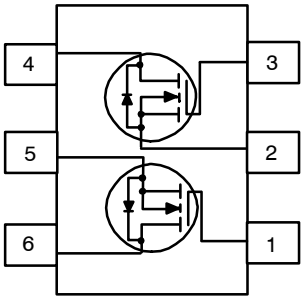
- 0.51 A, 50 V, $R_{DS(ON)}$ = 2 Ω @ V_{GS} = 10 V
- High Density Cell Design for Low $R_{DS(ON)}$
- Proprietary SUPERSOT™ −6 Package Design Using Copper Lead Frame for Superior Thermal and Electrical Capabilities
- High Saturation Current
- This is a Pb−Free Device

MARKING DIAGRAM



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PINOUT



SOT−6 (SUPERSOT™ −6)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DS}	Drain−Source Voltage	50	V
V_{GSS}	Gate−Source Voltage	20	V
I_D	Drain Current − Continuous (Note 1a) − Pulsed	 0.51 1.5	A
P_D	Power Dissipation (Note 1a) (Note 1b) (Note 1c)	 0.96 0.9 0.7	W
T_J, T_{STG}	Operating and Storage Temperature Range	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	60	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	130	

ORDERING INFORMATION

Device	Package	Shipping†
NDC7002N	TSOT−23−6 (Pb−free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain−Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	50			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 40 V, V_{GS} = 0 V			1	μA
		T_J = 125°C			500	
I_{GSSF}	Gate−Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate−Body Leakage, Reverse	V_{GS} = −20 V, V_{DS} = 0 V			−100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	1	1.9	2.5	V
		T_J = 125°C	0.8	1.5	2.2	
$R_{DS(ON)}$	Static Drain−Source On−Resistance	V_{GS} = 10 V, I_D = 0.51 A		1	2	Ω
		T_J = 125°C		1.7	3.5	
		V_{GS} = 4.5 V, I_D = 0.35 A		1.6	4	
$I_{D(on)}$	On−State Drain Current	V_{GS} = 10 V, V_{DS} = 10 V	1.5			A
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 0.51 A		400		mS
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz		20		pF
C_{oss}	Output Capacitance			13		pF
C_{rss}	Reverse Transfer Capacitance			5		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 25 V, I_D = 0.25 A, V_{GS} = 10 V, R_{GEN} = 25 Ω		6	20	ns
t_r	Turn−On Time			6	20	
$t_{d(off)}$	Turn−Off Delay Time			11	20	
t_f	Turn−Off Fall Time			5	20	
Q_g	Total Gate Charge	V_{DS} = 25 V, I_D = 0.51 A, V_{GS} = 10 V		1		nC
Q_{gs}	Gate−Source Charge			0.19		nC
Q_{gd}	Gate to Drain Charge			0.33		nC
DRAIN−SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuous Source Current				0.51	A
I_{SM}	Maximum Pulse Source Current (Note 2)				1.5	A
V_{SD}	Drain−Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 0.51 A (Note 2)		0.8	1.2	V

1. $R_{\theta JA}$ is the sum of the junction−to−case and case−to−ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)}@T_J$$

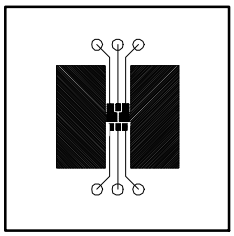
Typical $R_{\theta JA}$ for single device operation using the board layouts shown below on 4.5″ x 5″ FR−4 PCB in a still air environment:

a. 130°C/W when mounted on a 0.125 in^2 pad of 2oz copper.

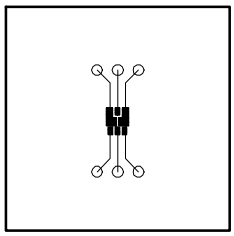
b. 140°C/W when mounted on a 0.005 in^2 pad of 2oz copper.

c. 180°C/W when mounted on a 0.0015 in^2 pad of 2oz copper.

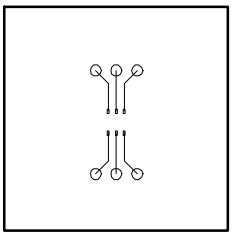
1a



1b



1c



Scale 1:1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300 μs, Duty cycle ≤ 2.0 %.

TYPICAL ELECTRICAL CHARACTERISTICS

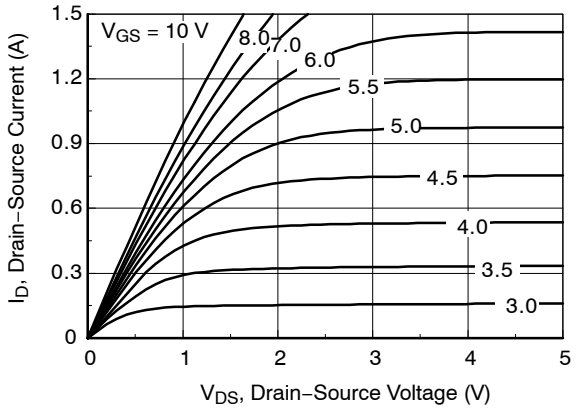


Figure 1. On−Region Characteristics

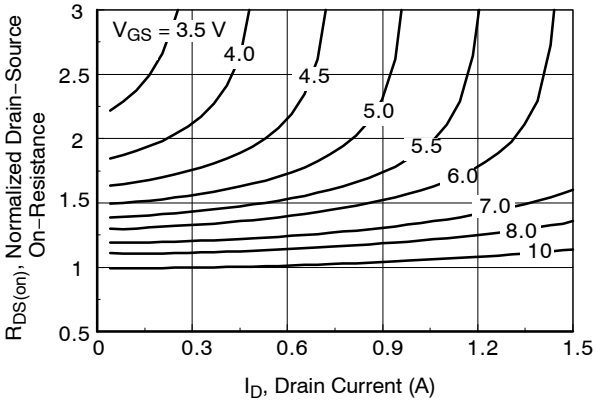


Figure 2. On−Resistance Variation with Gate Voltage and Current

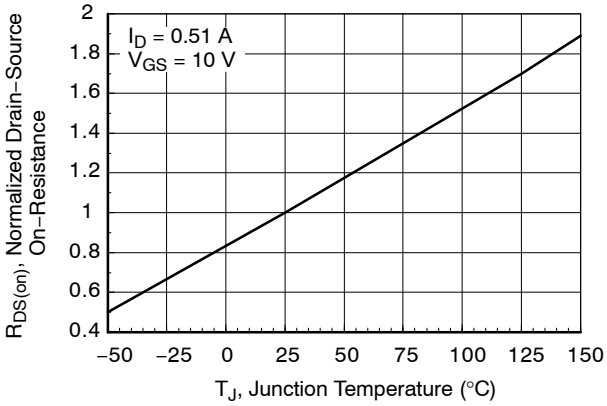


Figure 3. On−Resistance Variation with Temperature

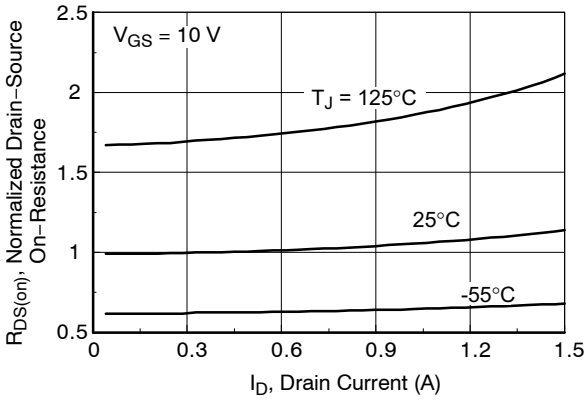


Figure 4. On−Resistance vs Variation with Drain Current and Temperature

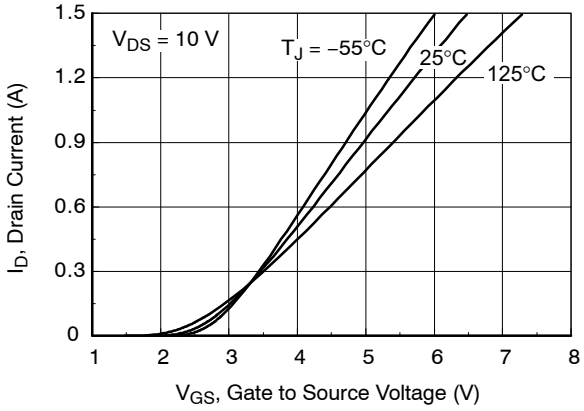


Figure 5. Transfer Characteristics

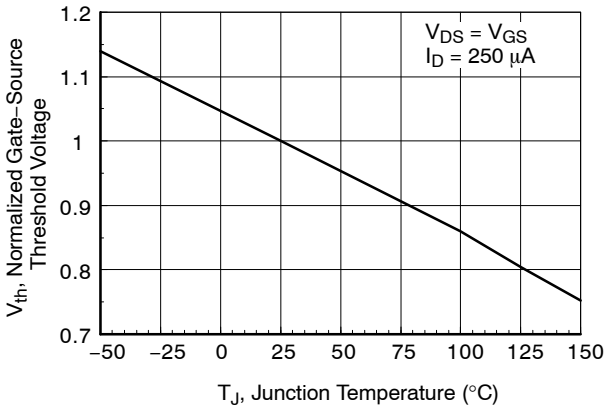


Figure 6. Gate Threshold Variation with Temperature

TYPICAL ELECTRICAL CHARACTERISTICS (continued)

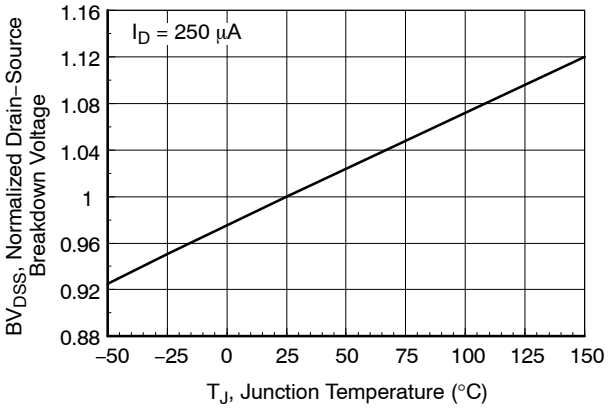


Figure 7. Breakdown Voltage Variation with Temperature

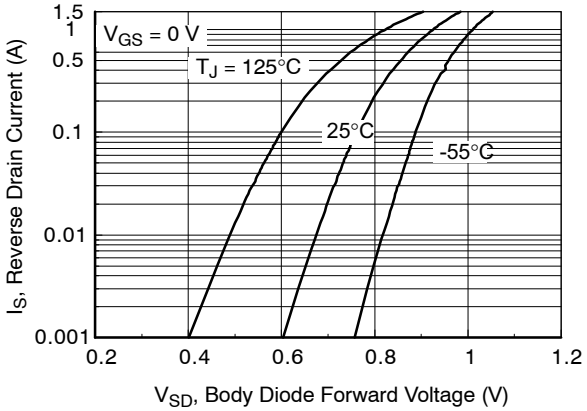


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

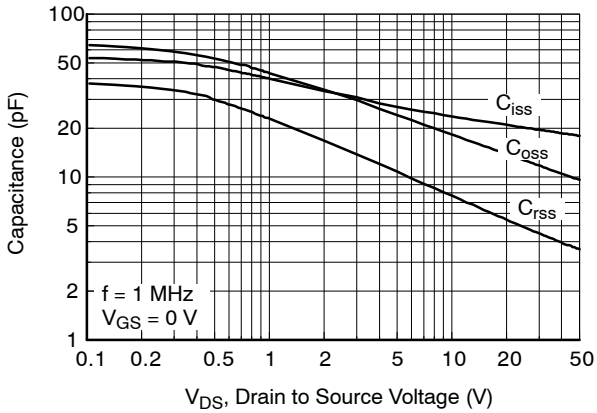


Figure 9. Capacitance Characteristics

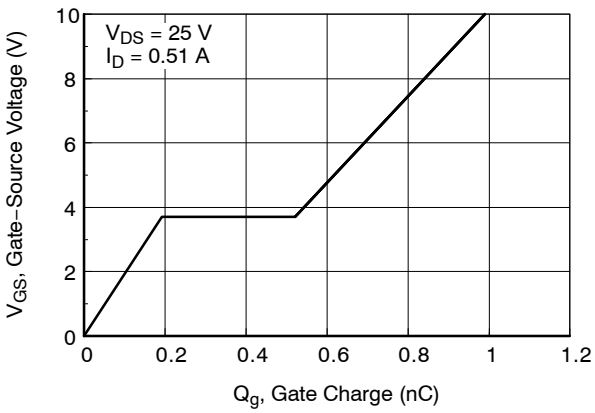


Figure 10. Gate Charge Characteristics

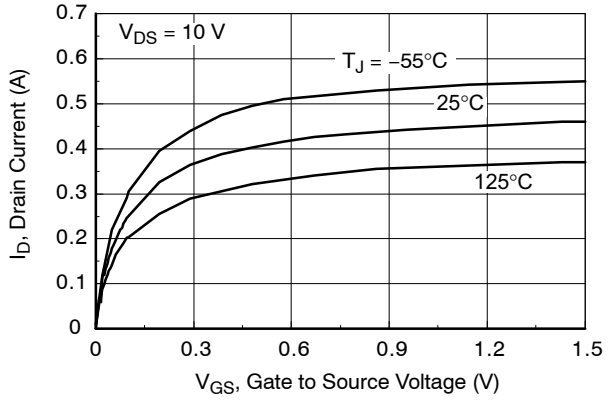


Figure 11. Transconductance Variation with Drain Current and Temperature

TYPICAL THERMAL CHARACTERISTICS

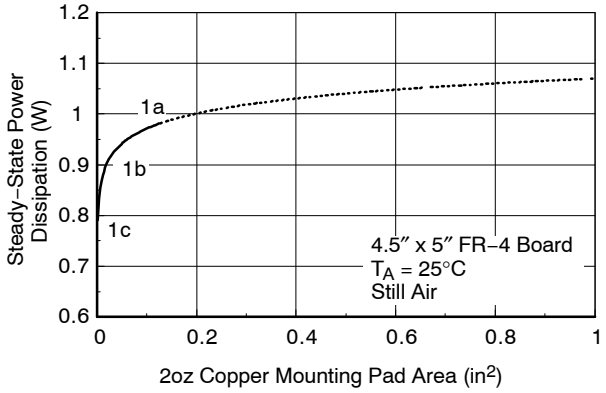


Figure 12. SOT−6 Dual Package Maximum Steady−State Power Dissipation versus Copper Mounting Pad Area

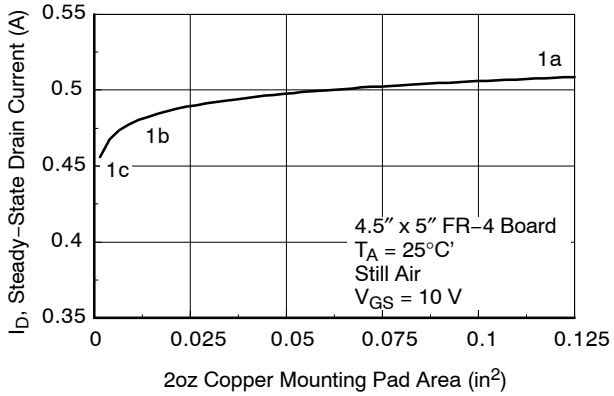


Figure 13. Maximum Steady−State Drain Current versus Copper Mounting Pad Area

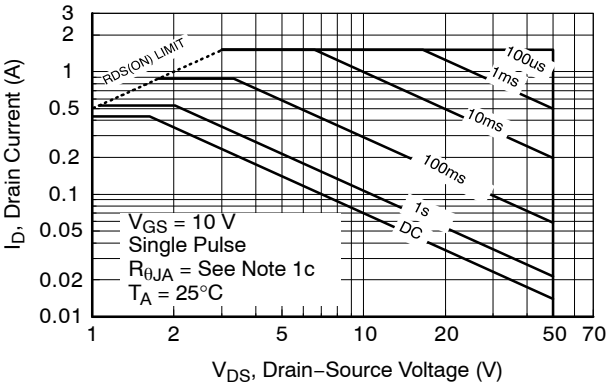


Figure 14. Maximum Safe Operating Area

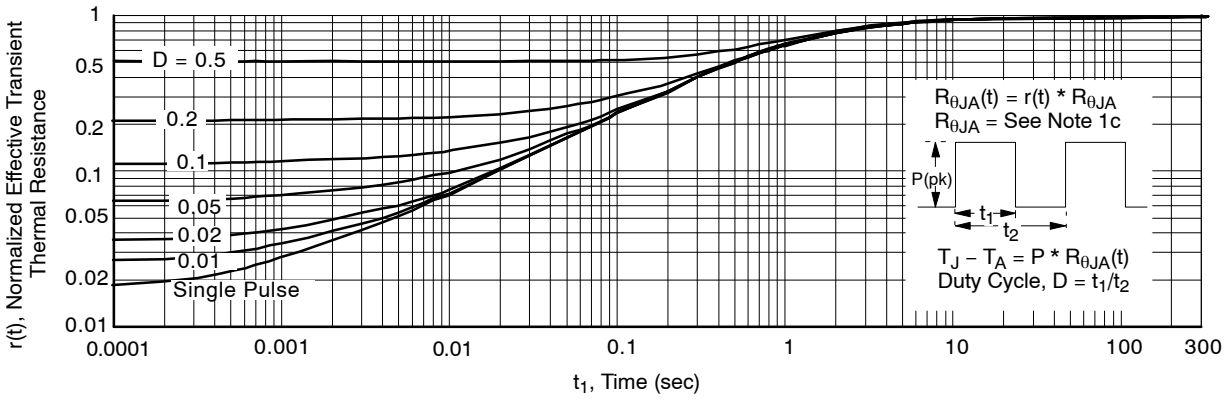


Figure 15. Transient Thermal Response Curve

(Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.)

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

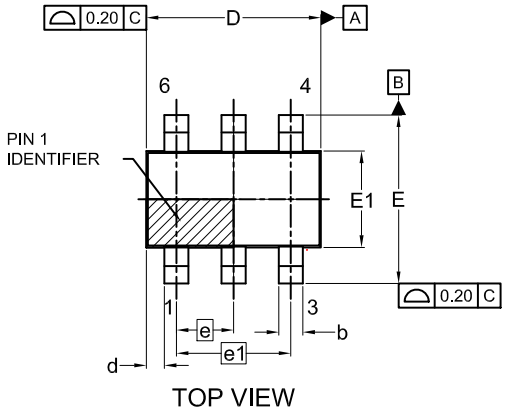
ON Semiconductor®

1

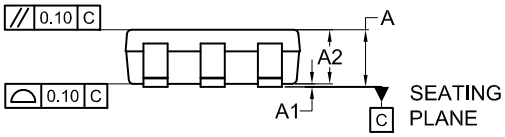
SCALE 2:1

TSOT23 6−Lead
CASE 419BL
ISSUE A

DATE 31 AUG 2020

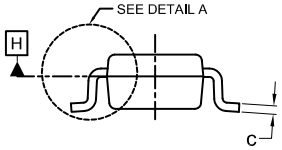


TOP VIEW

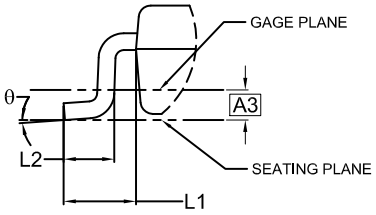


FRONT VIEW

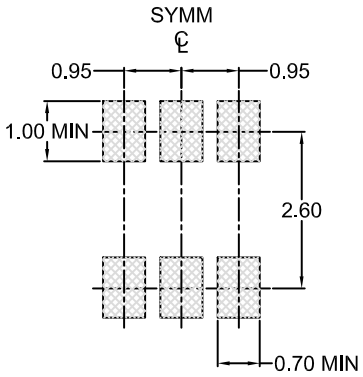
NOTE 4



SIDE VIEW



DETAIL A



LAND PATTERN
RECOMMENDATION

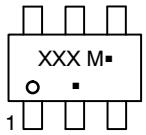
*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.25MM PER END. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	0.05	0.10
A2	0.70	0.85	1.00
A3		0.25 BSC	
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.80	2.95	3.10
d		0.30 REF	
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e		0.95 BSC	
e1		1.90 BSC	
L1		0.60 REF	
L2	0.20	0.40	0.60
θ	0°	---	10°

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON83292G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**TSOT23 6−Lead**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales