TCM8030
Data Manual

Baseband Processor for Analog Cellular Telephones

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1 Introduction

The TCM8030 baseband processor for analog cellular telephones provides all the baseband signal processing required for any of the following standards for mobile and hand-portable cellular telephones: advanced mobile telephone service (AMPS); extended advanced mobile telephone service (EAMPS); narrowband advanced mobile telephone service (NAMPS); total access communication system (TACS); extended total access communication system(ETACS); Japanese total access communication system (JTACS), and narrowband total access communications system (NTACS).

The analog section of the TCM8030 performs all filtering required for the speech, data, supervisory audio tone (SAT), and signaling tone (ST) paths. It has an integrated, International Telegraph and Telephone Consultative Committee (CCITT) compatible compandor as well as microphone preamplifiers and a differential, 32-Ω earpiece driver to complete the full integration of the baseband audio signal paths.

The digital section of the device implements the data transceiving, data processing, and SAT functions including data recovery, majority voting, Bose-Chaudhuri-Hocquenghem (BCH) decoding, BCH encoding, transmission (TX) frame assembly, and SAT generation, detection, and regeneration. The TCM8030 supports both narrowband standards, NTACS and NAMPS, with full implementation of the narrowband data, and digital supervisory audio tone (DSAT) and digital signaling tone (DST) filtering and processing functions. An on-chip, automatic frequency control (AFC) circuit also facilitates narrowband operation. Communication with the microcontroller is through a simple four-wire serial interface.

In addition to these basic signal processing requirements, the TCM8030 integrates many of the ancillary functions required in a typical FM cellular telephone. Included are three 8-bit digital-to-analog converters (DACs), a dual-tone multiple-frequency (DTMF) generator, an 8-bit programmable counter/timer, an independent watchdog timer, two 8-bit microcontroller expansion ports, and a 4-bit keyboard interrupt port. Clock operation is through a pin-selectable on-chip crystal-referenced oscillator, an external clock source, or an external temperature-controlled crystal oscillator (TCXO).

The TCM8030 is designed for ultra low-power applications and is manufactured using a low-power complementary metal-oxide semiconductor (CMOS) process. It operates from a single 2.7-V to 5.5-V supply and has five power-saving modes in addition to normal operation. The TCM8030 also features a total power-down mode in which the TCM8030 waits for the user to press the power-on key located on the telephone keyboard. Also implemented are two features that extend idle mode operation time.

One feature enables a reduction in the duty cycle of the microcontroller, and the other periodically shuts down the RF receiver. These features reduce the system power consumption to a minimum during idle mode and significantly increase the telephone standby time.

The gain and signal selection paths are software configurable so that audio trimming functions do not require manual intervention during telephone calibration on the production line. This production-time reduction feature, together with its high level of integration and low-power design, makes the TCM8030 an ideal solution for FM analog cellular telephones.

1.1 TCM8030 Features

The TCM8030 provides all data and audio processing functions for AMPS, NAMPS, TACS, ETACS, NTACS, and JTACS in a compact, low-power, baseband processor enclosed in an 80-pin TQFP package.

1.1.1 Data Processing Features

The TCM8030 provides data transceiver, data processing, and SAT functions, and includes the following data processing features:

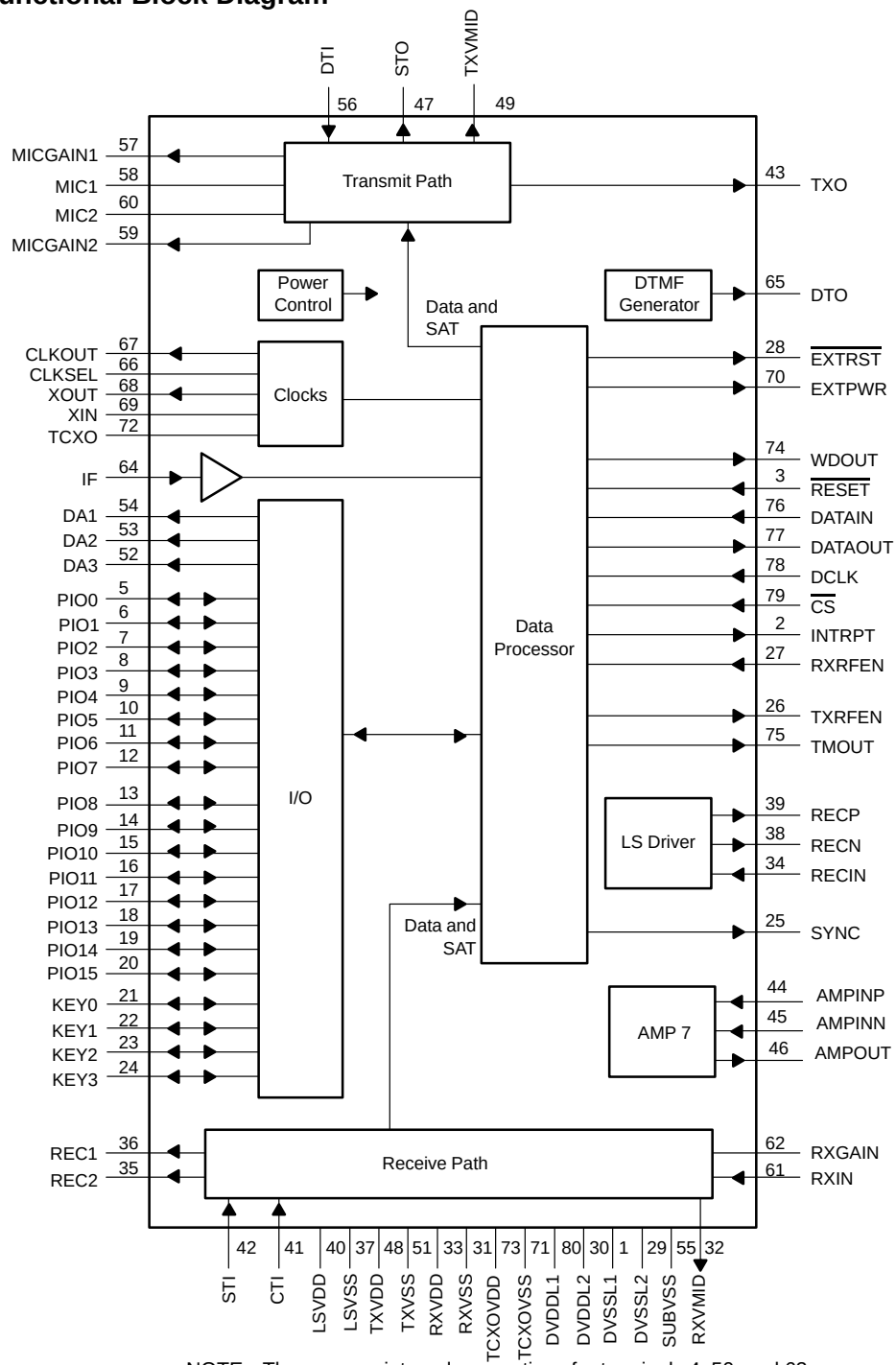
- Single-chip processing for AMPS, NAMPS, TACS, ETACS, NTACS, JTACS, SAT, and DSAT
- 2.7-V to 5.5-V operation
- Serial interface
- User-configurable interrupt structure
- Transmit (TX) and receive (RX) data buffers
- Integrated RX and TX data filters
- TX wideband (WB) SAT filter
- RX WB and narrowband (NB) SAT filters
- RX WB and NB data comparator
- Programmable timer
- Independent watchdog timer
- RX/TX automatic mute functions
- Arbitration processing
- Twenty programmable expansion I/O ports
- WB and NB-RX recovery
- Automatic frequency control (AFC)
- Multiple power-saving mode implementation
- Separate encoder for WB-TX and NB-TX

1.1.2 Audio Processing Features

The TCM8030 provides the following audio processing features:

- AMPS, NAMPS, TACS, ETACS, NTACS, and JTACS operation
- Integrated RX and TX voice filters
- Microphone amplifiers and loud speaker drivers
- Pre-emphasis and de-emphasis filtering
- Digitally-controlled gains and signal selection or muting
- Adjustable TX limiter
- Three 8-bit digital-to-analog converters (DAC) with output buffers
- Dual-tone multifrequency (DTMF) generator
- On-chip compandor
- Flexible clock and oscillator operation

1.2 Functional Block Diagram

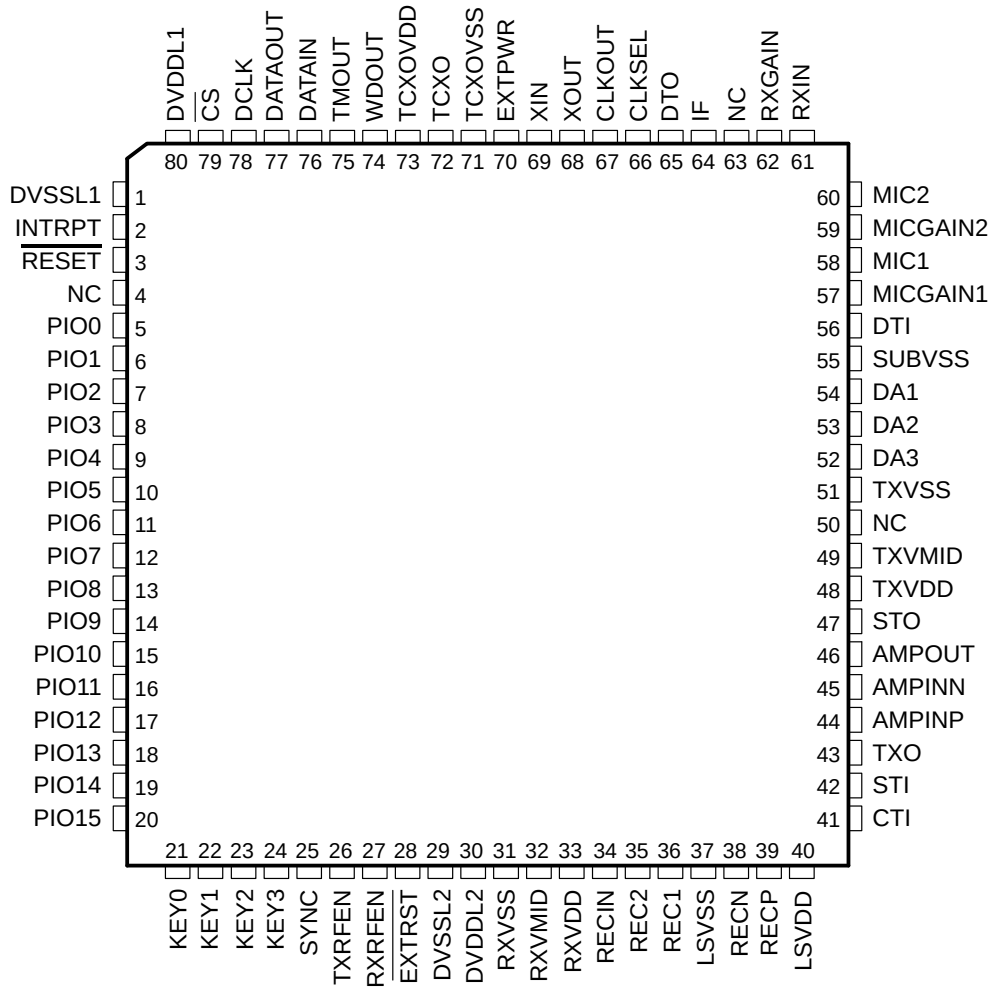


NOTE: There are no internal connections for terminals 4, 50, and 63.

Figure 1–1. Functional Block Diagram

1.3 Terminal Assignments

QFP PACKAGE
(TOP VIEW)



NC – No internal connection

Figure 1–2. Terminal Assignments

1.4 Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AMPINN	45	I	Operational amplifier inverting input (analog). AMPINN is the inverting analog input to the uncommitted operational amplifier, AMP7.
AMPINP	44	I	Operational amplifier noninverting input (analog). AMPINP is the noninverting analog input to the uncommitted operational amplifier, AMP7.
AMPOUT	46	O	Operational amplifier output (analog). AMPOUT is the analog output from the uncommittted operational amplifier, AMP7.
CLKOUT	67	O	Clock output (digital). CLKOUT provides an external digital clock that is one-half the frequency of either the temperature compensated crystal oscillator (TCXO) or the internal crystal oscillator (XTALOSC). The source chosen depends on the value of CLKSEL.
CLKSEL	66	I	Clock source select (digital). CLKSEL selects either the TCXO or the internal crystal XTALOSC as the frequency source for CLKOUT through the internal divide-by-two counter.
$\overline{CS}$	79	I	Chip select. $\overline{CS}$, active low (digital), selects the write function. When $\overline{CS}$ is high, the read function is selected.
CTI	41	I	Call tone input (analog). CTI is the DTMF call tone input terminal.
DA1 – DA3	54–52	O	Digital-to-analog converter output (analog). DA1 through DA3 are the output terminals for DACs 1 through 3.
DATAIN	76	I	Data input (digital). DATAIN is the digital data input that the TCM8030 microcontroller read (address) and write (address and data) operation.
DATAOUT	77	O	Data output (digital). DATAOUT is the digital output signal for the TCM8030 read (data) operation.
DCLK	78	I	Data clock input (digital). DCLK input provides a clocking source for the TCM8030 read and write operation.
DTI	56	I	DTMF Transmit input (analog). DTI is the analog DTMF signal and is selected for input to the transmit path by the transmission switch (TXSW).
DTO	65	O	DTMF generator output (analog). DTO is the analog output from the DTMF generator.
DVDDL1, DVDDL2	80, 30		Digital power supply No. 1 and No. 2. DVDDL1 and DVDDL2 are digital power supplies.
DVSSL1, DVSSL2	1, 29		Digital ground No. 1 and No. 2. DVSSL1 and DVSSL2 are the grounds for the digital power supplies No. 1 and No. 2.
$\overline{EXTRST}$	28	O	External reset (digital). $\overline{EXTRST}$ is the output to the rest of the telephone (used in total power-down mode).
EXTPWR	70	O	External power-on enable (digital). EXTPWR is a digital signal that is applied to the rest of the telephone (used in total-power-down mode).
IF	64	I	Intermediate frequency (analog). IF is the input from the receiver second IF to the AFC circuit.
INTRPT	2	O	Interrupt output (digital). INTRPT is a digital output from the TCM8030 to signal the telephone microcontroller that a specific event has occurred.
KEY0 – KEY3	21–24	I/O	Keyboard interrupts 0 through 3 (digital). KEY0 through KEY3 are programmable as input or output ports to/from the TCM8030 keyboard scan circuit.
LSVDD	40		Loudspeaker power supply
LSVSS	37		Loudspeaker ground

1.4 Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
MIC1, MIC2	58, 60	I	Microphone amplifier No. 1 and No. 2 (analog). MIC1 and MIC2 are analog inputs to the TCM8030 transmit audio path.
MICGAIN1 MICGAIN2	57, 59	O	Microphone amplifier No. 1 and 2 outputs (analog). MICGAIN1 and MICGAIN2 are amplified outputs that are applied to the TCM8030 transmit audio path.
NC	4, 50, 63		No internal connection
PIO0 – PIO15	5–20	I/O	Programmable input or output ports 0 through 15 (digital). PIO0 through PIO15 can be programmed as either an input or output port.
REC1, REC2	35, 36	O	Receive output No. 1 and No. 2 (analog). REC1 and REC2 are analog outputs from the TCM8030 receive audio path.
RECIN	34	I	Earpiece amplifier input (analog). RECIN is the analog input to the TCM8030 uncommitted loudspeaker driver circuit.
RECN	38	O	Earpiece amplifier differential output, negative (analog). RECN is the output from the TCM8030 uncommitted loudspeaker driver circuit.
RECP	39	O	Earpiece amplifier differential output, positive (analog). RECP is the analog output from the TCM8030 uncommitted loudspeaker driver circuit.
$\overline{\text{RESET}}$	3	I	Reset input, active low (digital). RESET is used to hard-reset the TCM8030.
RXGAIN	62	O	Receive amplifier output gain (analog). RXGAIN is the amplified signal that is applied to the TCM8030 receive audio path.
RXIN	61	I	Receive amplifier input (analog). RXIN is the analog input to the TCM8030 receive audio path.
RXRFEN	27	O	Receiver RF enable (digital). RXRFEN is an enable signal generated by the idle mode logic circuit.
RXVDD	33		Receive-analog power supply
RXVMID	32	O	Receive midsupply voltage (analog). RXVMID is a midrail voltage reference for internal audio circuits.
RXVSS	31		Receive-analog ground
STI	42	I	Sidetone input (analog). STI is the sidetone input to the summing circuitry (RECSUM) in the receiver audio path.
STO	47	O	Sidetone output (analog). STO is the sidetone output from the TCM8030 transmit audio path.
SUBVSS	55		Substrate ground connection
SYNC	25	O	Word sync (digital). SYNC is the digital output from the data processor wideband receive recovery circuitry.
TCXO	72	I	Temperature controlled crystal oscillator (analog). TCXO is the signal input from the TCXO to the input buffer, AFC and clock circuits.
TCXOVDD	73		XTALOSC and TCXO input buffer power supply
TCXOVSS	71		XTALOSC and TCXO input buffer ground
TMOUT	75	O	Counter/timer output (digital). TMOUT is the digital output from the data processor counter/timer circuit.
TXO	43	O	Transmit output (analog). TXO is the analog output from the TCM8030 transmit audio path.

1.4 Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
TXRFEN	26	O	Transmit RF enable (digital). TXRFEN is a digital output from the data processor arbitration logic circuit.
TXVDD	48		Transmit analog supply
TXVMID	49	O	TX midsupply voltage (analog). TXVMID is a midrail voltage reference for internal audio circuits.
TXVSS	51		Transmit analog ground
WDOUT	74	O	Watchdog timer output (digital). WDOUT is the output from the watchdog timer circuit. When WDOUT times out, the telephone microcontroller is reset.
XIN	69	I	External crystal input (analog). XIN is clock input terminal or, in conjunction with XOUT terminal, provides the means to connect an external crystal.
XOUT	68	O	External crystal output (analog). XOUT in conjunction with terminal XIN provides the means to connect an external crystal.

2 Electrical Specifications

2.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (see Note 1)†

Supply voltage range, V_{DD} . . . . . −0.5 V to 6.0 V
Input voltage range, V_I . . . . . −0.5 V to V_{DD} + 0.5 V
Output voltage range (includes open drain outputs), V_O . . . . . −0.5 V to V_{DD} + 0.5 V
Operating free-air temperature range, T_A . . . . . −40°C to 85°C
Continuous total power dissipation at (or below), T_A = 25°C . . . . . 500 mW
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to V_{SS}.

† Stresses beyond those listed under ”absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under ”recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2.2 Recommended Operating Conditions

PARAMETER		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage (see Note 2)	2.7	3	3.3	V
T_J	Operating junction temperature	−40		85	°C

NOTE 2: TCM8030 is designed such that all signal levels including trim settings, 0 dB (unity gain level) of compressor/expandor, limiter output level, TXVMID, and RXVMID scale proportionally with V_{DD} as follows:

Correction value: $k = 20 \log(V_{DDx}/3)$ [dB]

For example 0 dB (V_{ref}) = – 23.43 + k [dBV] for V_{DDx}

2.3 Electrical Characteristics Over Recommended Range of Supply Voltages and Operating Conditions (unless otherwise noted)

2.3.1 Electrical Characteristics Over Recommended Operating Conditions, V_{DD}=3.0 V, clocked by a crystal oscillator at 5.12 MHz

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
IDD_{PM1} Power mode No. 1	Total power-down mode, AUXPE (write address 30) = 0H		41	96	µA
IDD_{PM2} Power mode No. 2	Shutdown mode, AUXPE (write address 30) = 0H		0.34	0.5	mA
IDD_{PM3} Power mode No. 3	Idle mode, AUXPE (write address 30) = 0H		2.2	4.0	mA
IDD_{PM4} Power mode No. 4	Tone mode, AUXPE (write address 30) = 0H		5	8.5	mA
IDD_{PM5} Power mode No. 5	Full operation, DTMF off, AUXPE (write address 30) = 0H		21	36	mA
IDD_{PM6} Power mode No. 6	Full operation, DTMF on, AUXPE (write address 30) = 0H		22	37	mA
Auxiliary power modes	DAC1, AUXPE (write address 30) = 01H		0.6	0.85	mA
	DAC1 + DAC2, AUXPE (write address 30) = 03H		0.7	1.00	mA
	DAC1 + DAC2 + DAC3, AUXPE (write address 30) = 07H		0.8	1.225	mA
	AMP7, AUXPE (write address 30) = 08H		0.4	0.5	mA
	IFAMP, AUXPE (write address 30) = 10H		0.25	0.5	mA
	LS DRIVER, single ended, AUXPE (write address 30)= 20H		2	2.5	mA
TXVMID		1.3	1.5	1.7	V
RXVMID		1.3	1.5	1.7	V

2.3.2 DIGITAL I/Os, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_O	Source/sink current	All terminals except CLKOUT	1			mA
		CLKOUT	2			mA
	Open-drain output, sink current		1			mA
V_{OH}	High-level output voltage		V_{DD} – 0.4			V
V_{OL}	Low-level output voltage				V_{SS} + 0.4	V
T_P	Intrinsic delay			1		ns
ΔT_P	Delta delay, rise or fall			40		ns/pF
V_{IT+}	Positive - going input threshold voltage		0.7 V_{DD}			V
$V_{IT–}$	Negative - going input threshold voltage				0.3 V_{DD}	V
V_{Hys}	Hysteresis ($V_{IT+} – V_{IT–}$)			0.2 V_{DD}		V
I_{IH}	High-level input current	$V_I = V_{DD}$			1	µA
I_{IL}	Low-level input current	$V_I = V_{SS}$			1	µA
f_{clock}	Serial clock frequency			1	1.28	MHz
KEY0 - KEY3	Internal pullup current		–25		–1	µA

2.4 Transmit Path Specifications, V_{DD} = 2.7 V to 3.3 V

2.4.1 MICAMP1 and MICAMP2

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Unity gain frequency			1.5		MHz
Input current at MIC1 and MIC2			1		µA
Input offset voltage			±10		mV
Output load resistance at MICGAIN1 and MICGAIN2		47			kΩ
Output load capacitance at MICGAIN1 and MICGAIN2				20	pF
Input noise	R_{in} = 50 kΩ, psophometrically weighted		0.1		mVrms
Open loop gain			80		dB
Close loop gain			15	26	dB

2.4.2 Voice and DTMF (V/D) Trim, MIC1 to TXO

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Positive trim range	Code FH	3.225	3.725	4.225	dB
Negative trim range	Code 0H	–4.8	–4.3	–3.8	dB
Step size		0.3	0.5	0.7	dB
Nominal	Code 8H		0		dB

2.4.3 COMPRESSOR, MIC1 to TXO

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
0dB unity gain level (V_{ref})		–26	–24.43	–23.3	dBV
Linearity (relative error with respect to V_{ref}) (see Note 3)	V_I = (V_{ref} – 5.56 dB) to (V_{ref} + 15 dB)			± 0.5	dB
	V_I = (V_{ref} – 40 dB) to (V_{ref} – 5.56 dB)			± 1	
Attack time (see Note 4)		2.4	3	3.6	ms
Recovery time (see Note 5)		10.8	13.5	16.2	ms

NOTES: 3. Compressor Vref (– 24.43 dBV) = – 3.23 dBV with respect to 2.9 kHz FM deviation.
4. Time taken for the output to settle to 1.5 times the final value with a 12 dB input step
5. Time taken for the output to settle to 0.75 times the final value with a –12 dB input step

2.4.4 LIMITER, MIC1 to TXO

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Maximum output signal, with the limiter limiting and nominal settings	AMPS, TACS	Code AH, max. deviation, V_{DD} = 3 V, compressor bypassed, V_I = – 2 dBV, f = 1 kHz	–10.86	–9.80	–8.86	dBV
	NAMPS		–18.40		–16.16	
	NTACS		–16.16		–14.22	
Positive trim range		Code FH	2	2.5	3	dB
Negative trim range		Code 0H	–5.5	–5	–4.5	dB
Step size			0.3	0.5	0.7	dB
Nominal		Code AH		0		dB
Distortion	AMPS, TACS	2/3 of max. output signal, f = 1 kHz		0.4	3	%
	NAMPS, NTACS			0.4	3	
Limiter gain			4.75		6.75	dB

2.4.5 TXTRIM, MIC1 to TXO

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Positive trim range	Code 1FH	3.5	4	4.5	dB
Negative trim range	Code 0H	–4.9	–4.4	–3.9	dB
Step size		0.18	0.28	0.38	dB
Nominal	Code 10H		0		dB

2.4.6 Transmit Path, MIC1 to TXO

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Total transmit gain	AMPS, TACS	Compressor bypassed, V_I = –30 dBV, f = 1 kHz		4.75	5.75	6.75	dB
	NAMPS			–2.3		–1.3	
	NTACS			–0.2		0.8	
Output level	AMPS, TACS	Compressor bypassed, V_I = –30 dBV, f = 1 kHz		–25.25	–24.25	–23.25	dBV
TXSUM mute attenuation (voice)		V_I = –30 dBV, f = 1 kHz		–50	–80		dB
Distortion	AMPS, TACS, NAMPS, NTACS	Compressor enabled, f = 1 kHz, V_I = –30 dBV				1	%
Output noise	AMPS, TACS	MIC1, MIC2 = TXVMID, Compressor enabled, psophometrically weighted			2.3	4	mVrms
	NAMPS				1.0	1.5	
	NTACS				0.76		
Crosstalk in TXSW		f = 1 kHz, V_I = –30 dBV		50	70		dB
Crosstalk RX and TX path		f = 1 kHz, V_I = –30 dBV, MIC1/REC1, RXIN grounded		60	70		dB
Frequency response		0 dB reference, f = 1 kHz, V_I = –30 dBV, Compressor bypassed	< 200 Hz			–20	dB
			300 Hz	–13.46		–9.46	
			500 Hz	–9.02		–5.02	
			2 kHz	3.02		7.02	
			2.5 kHz	4.96		8.96	
			3 kHz	4.96		10.54	
			5.9 kHz			–35	
			> 6 kHz			–35	

2.4.7 Transmit Data at TXO

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Mute at TXSUM				−50	−80		dB
Output level	AMPS, TACS	f = 10 kHz, ST f = 100 Hz, data		−14.0	−12.4	−10.8	dBV
	NAMPS			−35.1	−33.6	−32.1	
	NTACS				−31.58		
Distortion	AMPS, TACS	f = 10 kHz			0.4	3.7	%
TXDATLPF	AMPS, TACS	0 dB reference, f = 1 kHz	8 kHz	−0.5		0.5	dB
			10 kHz	−0.5		0.5	
			14.4 kHz	−4		−1.7	
			17 kHz	−8.0		−5.5	
			24 kHz			−20	
			40 kHz			−50	
	NAMPS, NTACS	0 dB reference, f = 50 Hz	180 Hz	−7.0		−5.75	dB
			1 kHz			−20	

2.4.8 TX-DAT TRIM at TXO

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Positive trim range	Code 7H	1.4	1.8	2.2	dB
Negative trim range	Code 0H	−2.7	−2.3	−1.9	dB
Step size		0.4	0.6	0.8	dB
Nominal	Code 4H		0		dB

2.4.9 Transmit SAT at TXO

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output level	AMPS, TACS	f = 6 kHz, nominal settings	−26.04	−24.44	−22.84	dBV
Distortion		f = 6 kHz, nominal settings			0.5	%
TXSUM mute attenuation			−50	−80		dB
frequency response		3 kHz			−35	dB
		4.8 kHz			−25	
		5.1 kHz			−20	
		5.8 kHz	−5		0.5	
		5.94 kHz	−0.5		0.5	
		6.06 kHz	−0.5		0.5	
		6.2 kHz	−5		0.5	
		7.2 kHz			−20	
		9 kHz			−35	

2.4.10 SAT TRIM at TXO

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Positive trim range	Code FH	2	2.25	2.5	dB
Negative trim range	Code 0H	−2.5	−2.25	−2	dB
Step size		0.2	0.3	0.4	dB
Nominal	Code 8H		0		dB

2.5 Receive Path Specifications, V_{DD} = 2.7 V to 3.3 V, V_I = 171.2 mVrms

2.5.1 RXAMP

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Unity gain frequency			1.5		MHz
Input current			1		μA
Output load resistance at RXGAIN		47			kΩ
Output load capacitance at RXGAIN				20	pF
Input noise	R_{in} = 50 kΩ, psophometrically weighted			0.1	mVrms
Open loop gain			80		dB
Close loop gain			15	26	dB
Distortion	f = 1 kHz			0.5	%

2.5.2 RXTRIM, RXGAIN to REC1

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Positive trim range	Code FH	3.2	3.7	4.2	dB
Negative trim range	Code 0H	– 4.8	– 4.3	– 3.8	dB
Step size		0.35	0.5	0.65	dB
Nominal	Code 8H		0		dB

2.5.3 EXPANDOR, RXGAIN to REC1

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
0dB unity gain level (V_{ref})	V_{DD} = 3 V	– 4.23	– 3	– 2.24	dBV
Linearity (relative error with respect to V_{ref}), (see Note 6)	$V_I = V_{ref}$ to (V_{ref} – 12.34 dB)			± 1	dB
	V_I = (V_{ref} – 12.34 dB) to (V_{ref} – 33.5 dB)			± 2	
Attack time (see Note 7)		2.4	3	3.6	ms
Recovery time (see Note 8)		10.8	13.5	16.2	ms

NOTES: 6. Expandor V_{ref} (– 3 dBV) = – 12.34 dBV with respect to 2.9 kHz FM deviation.
7. Time taken for the output to settle to 0.57 times the final value with a 6 dB input step.
8. Time taken for the output to settle to 1.5 times the final value with a –6 dB input step.

2.5.4 Receive Path, RXGAIN to REC1

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
REC1SW mute attenuation		RXIN = – 15.3 dBV, f = 1 kHz		50	80		dB
Distortion at REC1/REC2		RXIN = – 15.3 dBV, f = 1 kHz, No load	Expandor bypassed			0.2	%
			Expandor enabled			1	%
Noise at REC1/REC2	AMPS, TACS NAMPS	RXIN = RXVMID, expandor bypassed, psophometrically weighted			0.05	3	mVrms
Output load at REC1/REC2				150	500		Ω
Output voltage at REC1/REC2		Load = 500 Ω, with less than 5% distortion		1.5			Vpp
Overall receive gain	AMPS,TACS	Expandor bypassed, nominal settings		– 1.6	0	1.4	dB
	NAMPS			6		9	
	NTACS			4		7	
Voice frequency response	RXBPF	0 dB reference, f= 1 kHz, RXIN = –15.3 dBV, expandor bypassed	<100 Hz			–20	dB
			240 Hz	1.0		2.25	
			300 Hz			11	
			400 Hz	7.5		8.5	
			2.4 kHz	–8.2		–7.1	
			3 kHz	–12		–9	
			5.9 kHz			–40	

2.5.5 VOL CTRL, RXGAIN to REC1

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Positive range	Code FH	17.0	17.5	18.0	dB
Negative range	Code 0H	– 20.5	– 20	– 19.5	dB
Step size		2	2.5	2.75	dB
Nominal	Code 8H		0		dB

2.5.6 LS DRIVER, at RECP and RECN, Input at RECIN

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Open loop gain			70		dB
Unity gain frequency			1.5		MHz
Load		25	32		Ω
Differential output level	V_{DD} = 3 V, V_I = 0.74 Vpp, 25-Ω differential load		1.48		Vpp
Distortion	V_{DD} = 3 V, V_I = 0.74 Vpp, 25-Ω differential load		5	10	%
Distortion	V_{DD} = 3 V, V_I = 0.5 Vpp, 25-Ω differential load		2.5	5	%

2.5.7 Receive Data Detect, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Level at RXGAIN	TACS, JTACS				– 6.43		dBV
	AMPS				– 6.52		
	NAMPS				– 21.68		
	NTACS				– 19.65		
Must-not-detect level	AMPS, TACS	Levels at RXGAIN	10 kHz			– 34.9	dBV
	NAMPS, NTACS		100 Hz			– 50.45	
Must-detect level	AMPS, TACS	Levels at RXGAIN	10 kHz	– 20			dBV
	NAMPS, NTACS		100 Hz	– 27.13			
NB frequency response	NB-RX LPF	0 dB reference, f = 80 Hz, RXIN = – 26.7 dBV, test-mode	160 Hz	– 5		– 2.75	dB
			240 Hz	– 19.5		– 17.25	
			2 kHz			– 30	

2.5.8 Receive SAT Detect

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Level at RXGAIN	TACS, JTACS	f = 6 kHz			– 17.95		dBV
	AMPS				– 18.56		
Frequency response		0 dB reference, f = 6 kHz	3 kHz			– 35	dB
			4.8 kHz			– 25	
			5.1 kHz			– 20	
			5.8 kHz	–5		0.5	
			5.94 kHz	–0.5		0.5	
			6.06 kHz	–0.5		0.5	
			6.2 kHz	–5		0.5	
			7.2 kHz			–20	
			9 kHz			–35	
Must-not-detect level		Levels at RXGAIN				– 47.6	dBV
Must-detect level		Levels at RXGAIN		– 29.0			dBV
Output duty cycle		RXIN = 900 mVpp		47.5		52.5	%

2.6 Miscellaneous Block Specifications, V_{DD} = 3 V

2.6.1 Digital-to-Analog Converters DAC1, DAC2, and DAC3

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC output voltage	Full range	Code FFH	V_{DD} – 0.1			V
	Half range		(V_{DD}/2) – 0.1			
DAC zero code dc offset	Full range	Code 0H		0	100	mV
	Half range			0	100	
Differential nonlinearity		Codes 05H to FAH	–1		1	LSB
Integral nonlinearity		Codes 05H to FAH	–4		4	LSB
Load resistance			30			kΩ
Load capacitance					50	pF
Conversion time				3		µs

2.6.2 TCXO Amplifier

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Level at TCXO amplifier	f = 17.92 MHz		–9.0		dBV
Clock time (see Note 9)			100		µs
Must-not-detect level	Input level at TCXO 17.92 MHz			– 27.45	dBV
Must-detect level	Input level at TCXO 17.92 MHz	– 15.05			dBV

NOTE 9: Time needed for TCXO amplifier to become active after $\overline{\text{EXTRST}}$ goes high.

2.6.3 IF Amplifier

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Level at IF amplifier	f = 450 kHz		– 15		dBV
Must-not-detect level	Input level at IF 450 kHz			– 33.9	dBV
Must-detect level	Input level at IF 450 kHz	– 17.67			dBV

2.6.4 DTMF Generator

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DTO output level low	AMPS	At DTO output	697 Hz	– 12.4		– 10.1	dBV
			770 Hz	– 12.4		– 10.1	
			852 Hz	– 12.4		– 10.1	
			941 Hz	– 12.4		– 10.1	
DTO output level high	AMPS	At DTO output	1150 Hz	– 12.4		– 10.1	dBV
			1209 Hz	– 12.4		– 10.1	
			1336 Hz	– 12.4		– 10.1	
			1477 Hz	– 12.4		– 10.1	
			1633 Hz	– 12.4		– 10.1	
			2048 Hz	– 12.4		– 10.1	
Skew change between high and low tones	TACS	At DTO output	697 Hz	1.5	2	2.5	dB
			1477 Hz	1.5	2	2.5	
Distortion products relative to low tones		f = 697 Hz				2	%
Output load to ground				100			kΩ

2.6.5 AMP7

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Unity gain frequency			1.5		MHz
Input current			1		μA
Input offset voltage		– 15		15	mV
Output load resistance at AMPOUT		47			kΩ
Output load capacitance at AMPOUT				20	pF
Input noise	R_{in} = 50 kΩ, psophometrically weighted			0.1	mVrms
Open loop gain		70	83		dB
Closed loop gain			15	26	dB
Distortion	V_{DD} = 3.0 V, input at AMP7 = –3 dBV at f = 1 kHz			0.01	%
Common mode rejection ratio (CMRR)	f = DC		70		dB
Common mode input range			0.5 to 2		V

2.7 Timing Requirements Over Recommended Ranges of Operating Conditions (see Figure 3–1)

		MIN	NOM	MAX	UNIT
$t_{su}1$	Setup time, $\overline{CS}$ to DCLK ↑	200			ns
$t_{su}2$	Setup time, DATAIN before DCLK ↑	200			ns
t_h	Hold time, DATAIN after DCLK ↑	200			ns
t_d	Delay time, DCLK ↑ to $\overline{CS}$ ↓ (start of next cycle)	1000			ns
DCLK				1	MHz

3 Parameter Measurement Information

Figure 3–1 shows the write timing diagram for the microcontroller interface and Figure 3–2 shows the read timing diagram for the microcontroller interface. Refer to Section 5.10 for a detailed description.

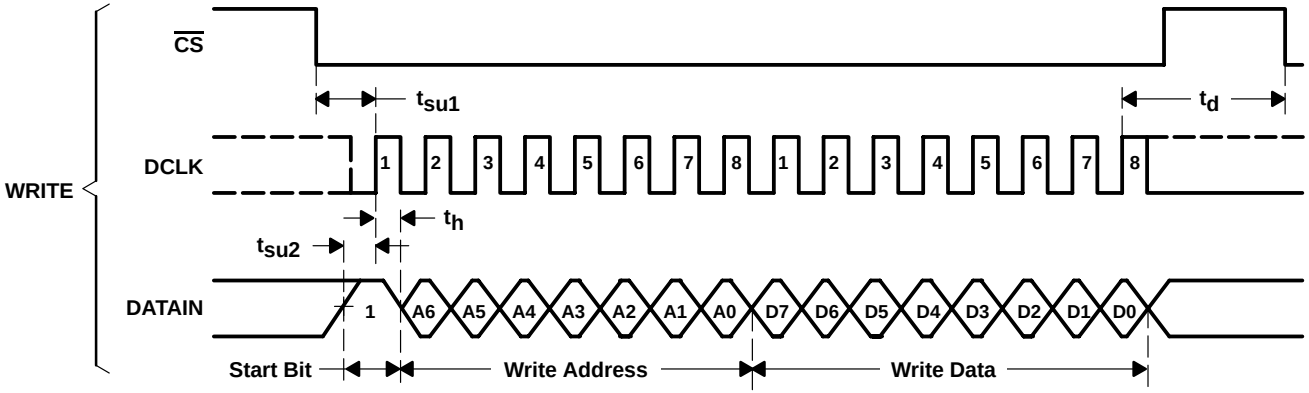


Figure 3–1. Microcontroller Interface Write Timing Diagram

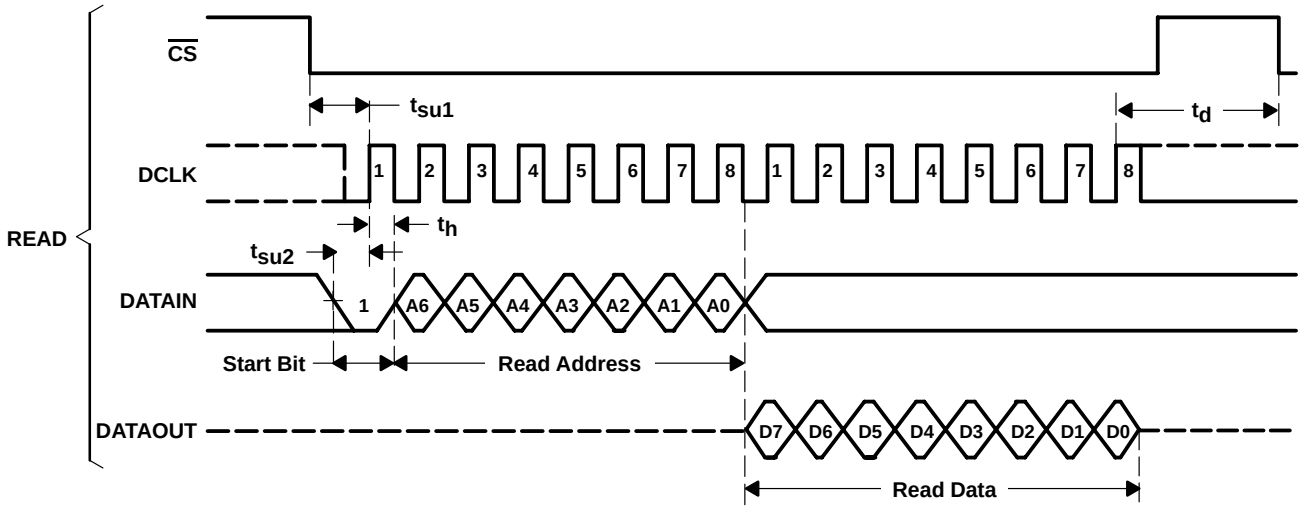


Figure 3–2. Microcontroller Interface Read Timing Diagram

4 Typical Characteristics

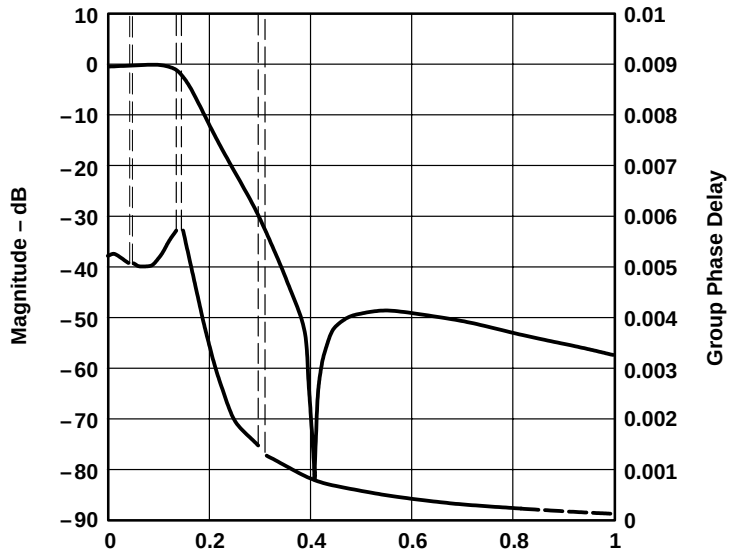


Figure 4–1. NBRXLPF Magnitude and Phase Response

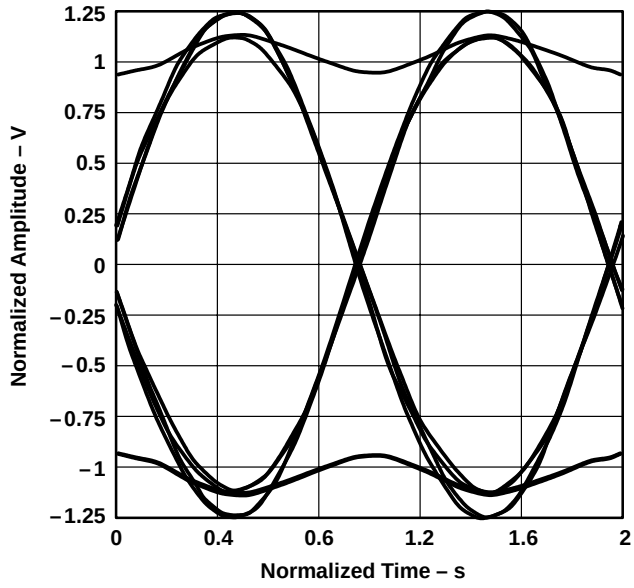


Figure 4–2. NBRXLPF Eye Pattern

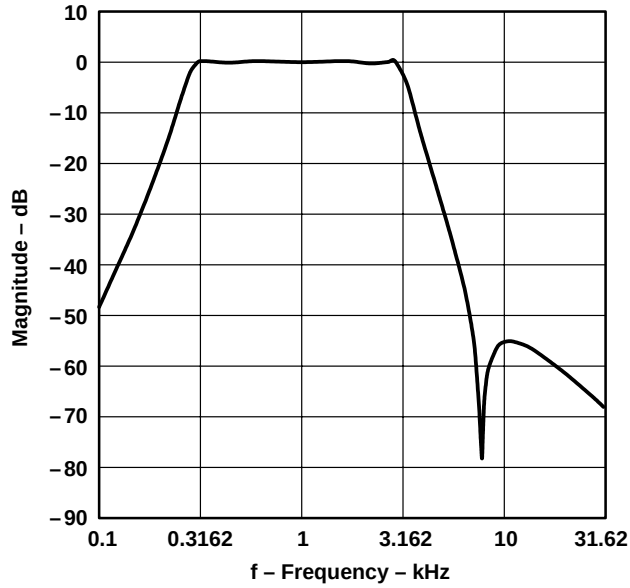


Figure 4–3. TXBPF Frequency Response

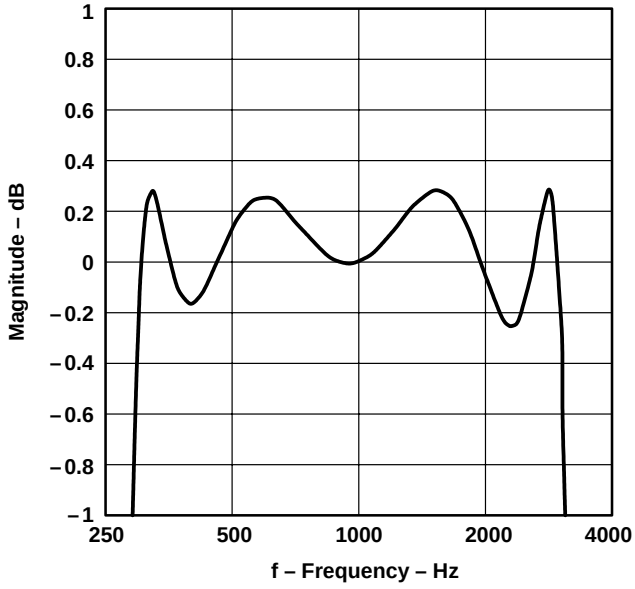


Figure 4–4. TXBPF Frequency Response

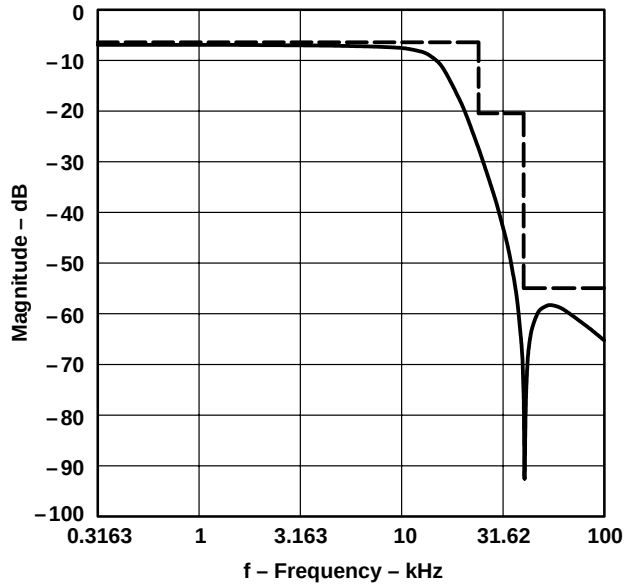


Figure 4–5. TXDATLPF and TXSUMLPF Combined Response

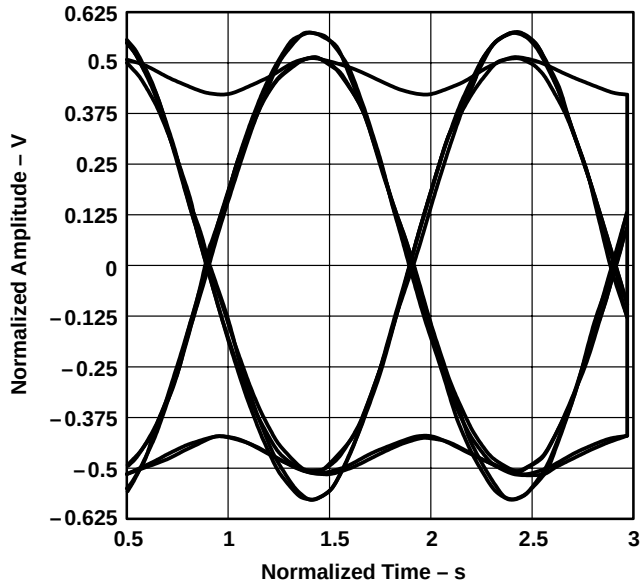


Figure 4–6. Eye Pattern for TXDALPF and TXSUMLPF Combined (Narrowband)

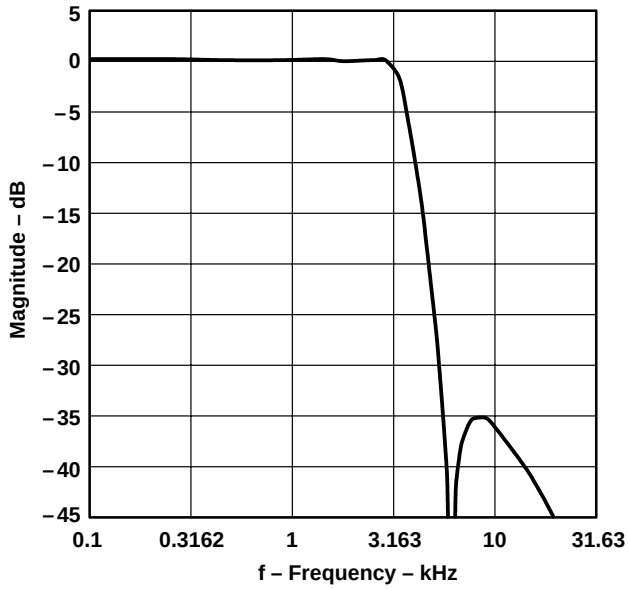


Figure 4–7. TXLPF Frequency Response

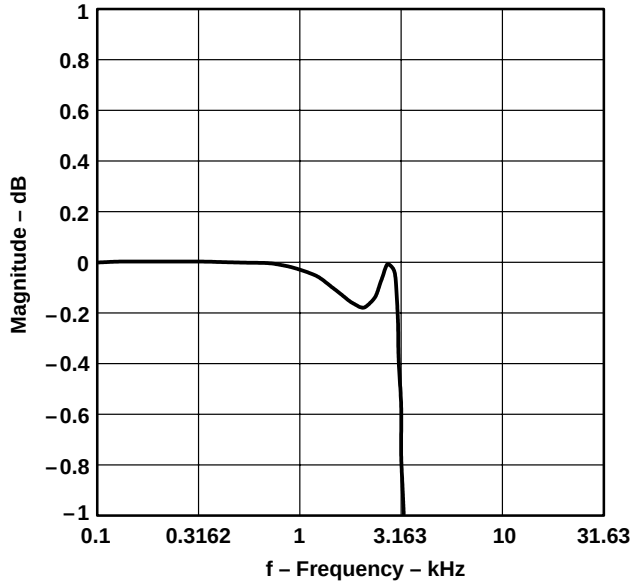


Figure 4–8. TXLPF Frequency Response

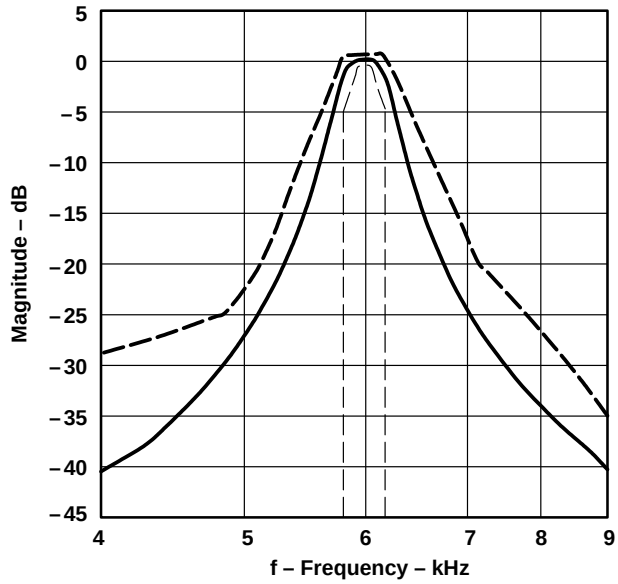


Figure 4–9. TXSATBPF Response Profile

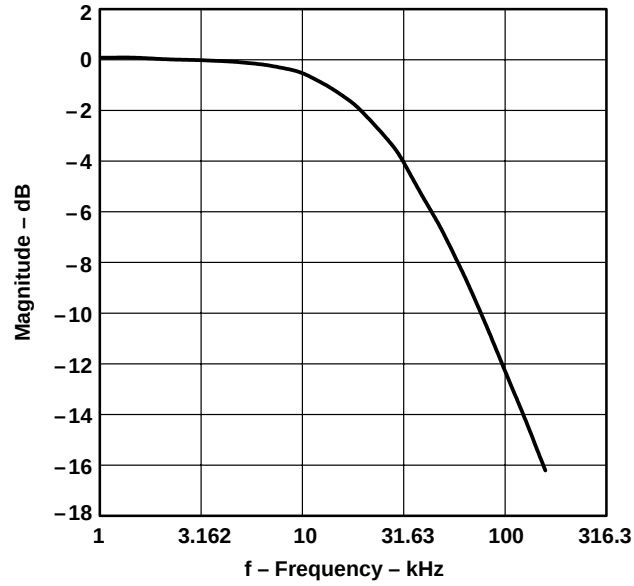


Figure 4–10. TXSUMLPF Frequency Response

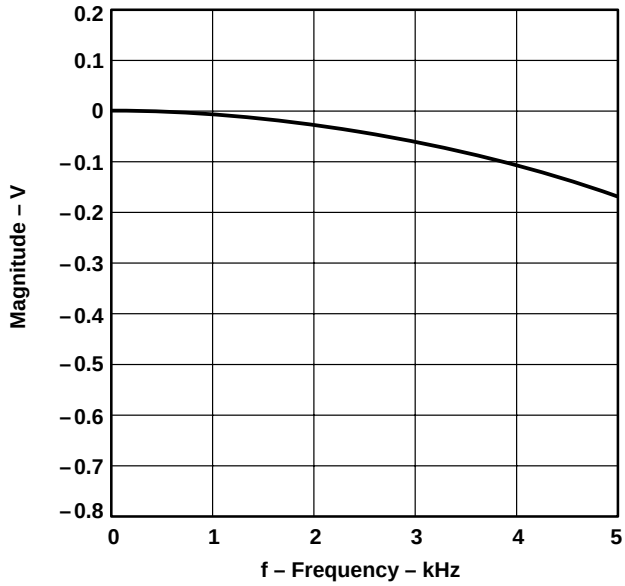


Figure 4–11. TXSUMLPF Frequency Response

5 Principles of Operation

5.1 Overview

The TCM8030 provides a complete, low-power, integrated solution for FM analog cellular telephones by integrating the analog processing and digital data processing functions onto one chip.

The TCM8030 contains transmit (TX) and receive (RX) analog paths, a digital data processor with filters, a compressor and expandor, routing switches, data input/output (I/O), an audio power amplifier, an uncommitted operational amplifier, and a DTMF generator. With these circuits, the TCM8030 applies appropriate signal levels for AMPS, NAMPS, TACS, ETACS, JTACS, and NTACS standards. In addition, both analog paths are software configurable such that all audio trimming functions can be achieved without manual intervention.

The TCM8030 data processor has several functional features: it performs transmit encoding and receive decoding, as well as majority voting and data recovery; it generates supervisory audio tone (SAT) and digital supervisory audio tone (DSAT); and it implements a number of independent circuits for arbitration logic, timers, and power logic. These features, along with a simple serial peripheral interface (SPI™) that interfaces with an external microcontroller, make the TCM8030 data processor extremely effective for all of the analog standards.

The TCM8030 provides greater integration than typical analog cellular baseband systems; thus, it reduces power consumption and increases talk and standby time. This integration, along with the other TCM8030 features, offers an efficient and effective cost solution for FM analog telephones and related applications.

Figure 5–1 shows a detailed functional block diagram of the device.

SPI is a trademark of Motorola, Inc.

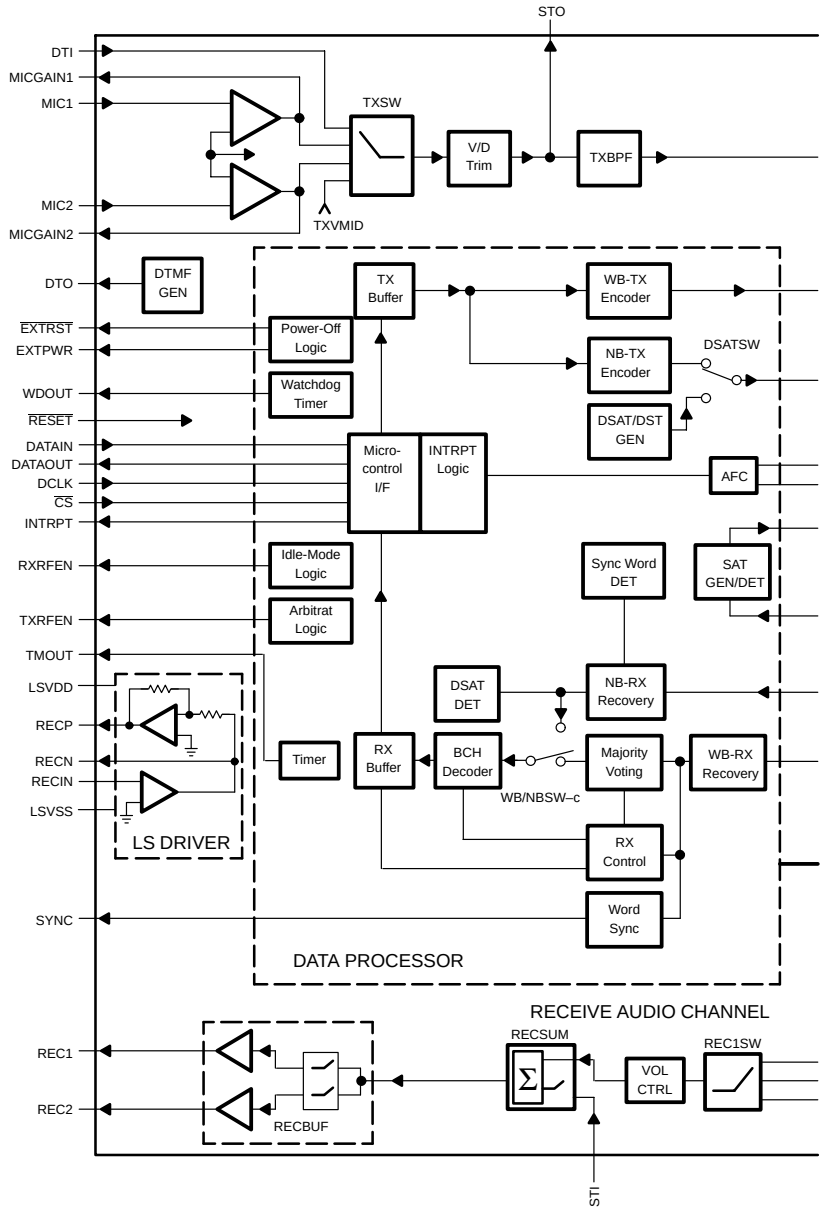


Figure 5–1. TCM8030 Detailed Functional Block Diagram

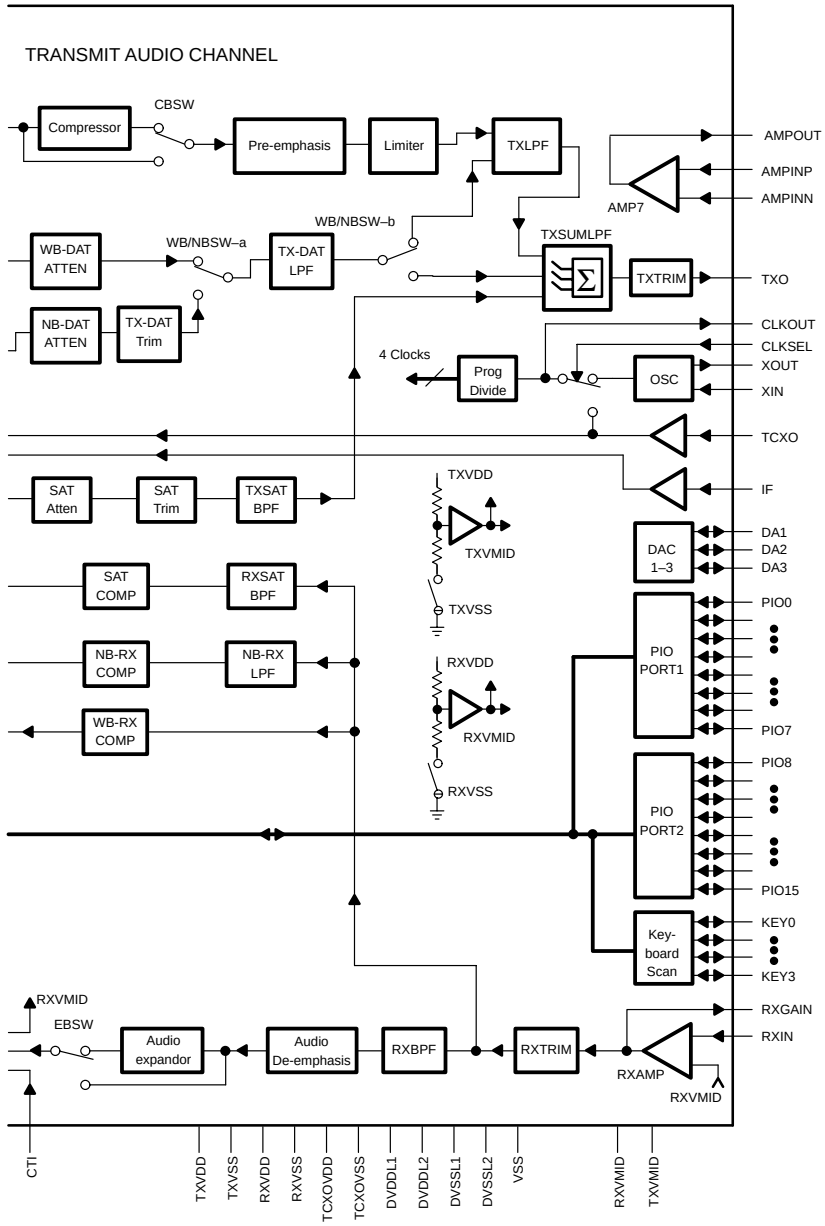


Figure 5–1. TCM8030 Detailed Functional Block Diagram (Continued)

5.2 Receive Audio Path

Figure 5–2 shows the receive audio path. A pair of external gain-setting resistors (R1 and R2) adjusts the input sensitivity to system requirements. A second digitally programmable gain trim is provided in RXTRIM, followed by a band-pass filter (BPF). The filter output drives the data/SAT blocks and the de-emphasis block.

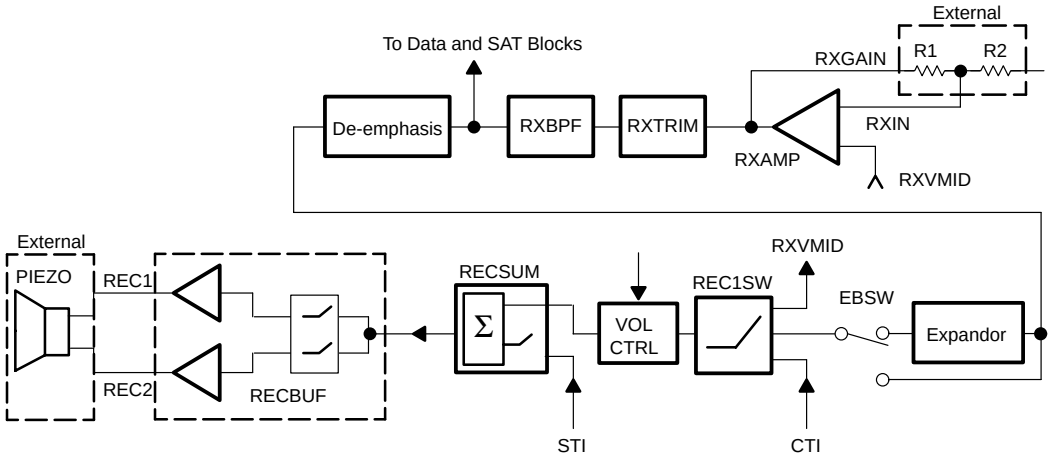


Figure 5–2. Receive Audio Path

You can bypass the expandor for testing purposes or for applying linear functions. The switch REC1SW allows you to select either the transmit loop-back, the expandor output, or the call tone input (CTI) to feed into the digitally programmable volume control (VOL CTRL).

The receive summing block (RECSUM) sums (or does not sum) the sidetone input (STI) with the audio signal, based on a software command. The final stage consists of a pair of configurable receive buffers (RECBUF) that drives a piezo speaker or other light load. A separate loudspeaker driver block (LS DRIVER) is discussed later.

5.3 Transmit Audio Path

Figure 5–3 shows the block diagram for the transmit path. Here, you can select transmit inputs by using software control for the transmit switch (TXSW). The MIC1 and MIC2 inputs have operational amplifiers that you can configure with external gain-setting resistors R2/R1 and R4/R3. A selectable DTMF signaling input (DTI) is provided. You can use this with a programmable DTMF generator that has an independent output (DTO).

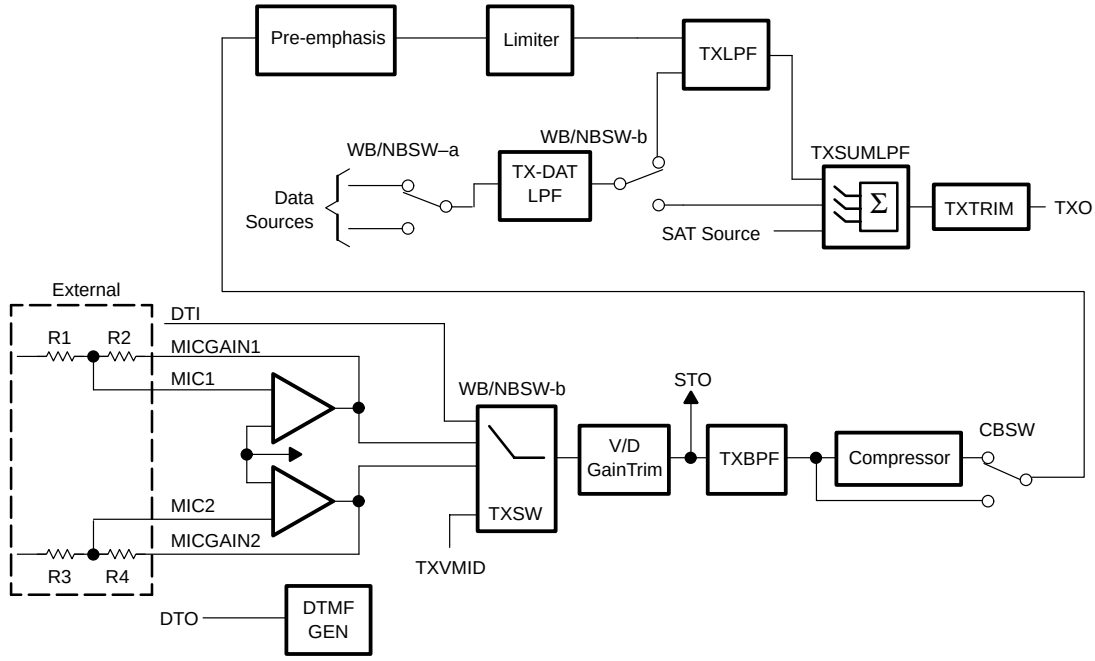


Figure 5–3. Transmit Audio Path

A programmable voice/DTMF gain trim stage (V/D TRIM) outputs to the sidetone output (STO) and drives the transmit band-pass filter (TXBPF). The signal from the TXBPF goes to the audio compressor. A bypass switch (CBSW) allows you to bypass the compressor for DTMF tones, as well as other uncompressed functions that might require testing.

The pre-emphasis and (deviation) limiter blocks then drive the transmit low-pass filter (TXLPF). This attenuates the harmonics caused by limiting the signal. Some data transmission modes use the TXLPF route, which inverts the signal. This requires reinversion of the data signal polarity using either inversion set/reset bits or external means.

The transmit summer and low-pass filter block (TXSUMLPF) selects voice, data, or SAT signals and sums them together. It also provides a continuous-time smoothing filter that removes high-frequency products. The transmit gain-trim (TXTRIM) is the final stage that drives the output terminal (TXO).

5.4 Data Processor

The data processor, shown in Figure 5–4, provides a large number of functions for processing cellular data streams and controlling other functions of the TCM8030. The microcontroller interface is a simple serial-shift register function that uses DATAIN, DATAOUT, DCLK, and $\overline{CS}$ (active-low chip select), and has an interrupt output (INTRPT). This interface allows the TCM8030 to communicate with the microcontroller that is operating the telephone.

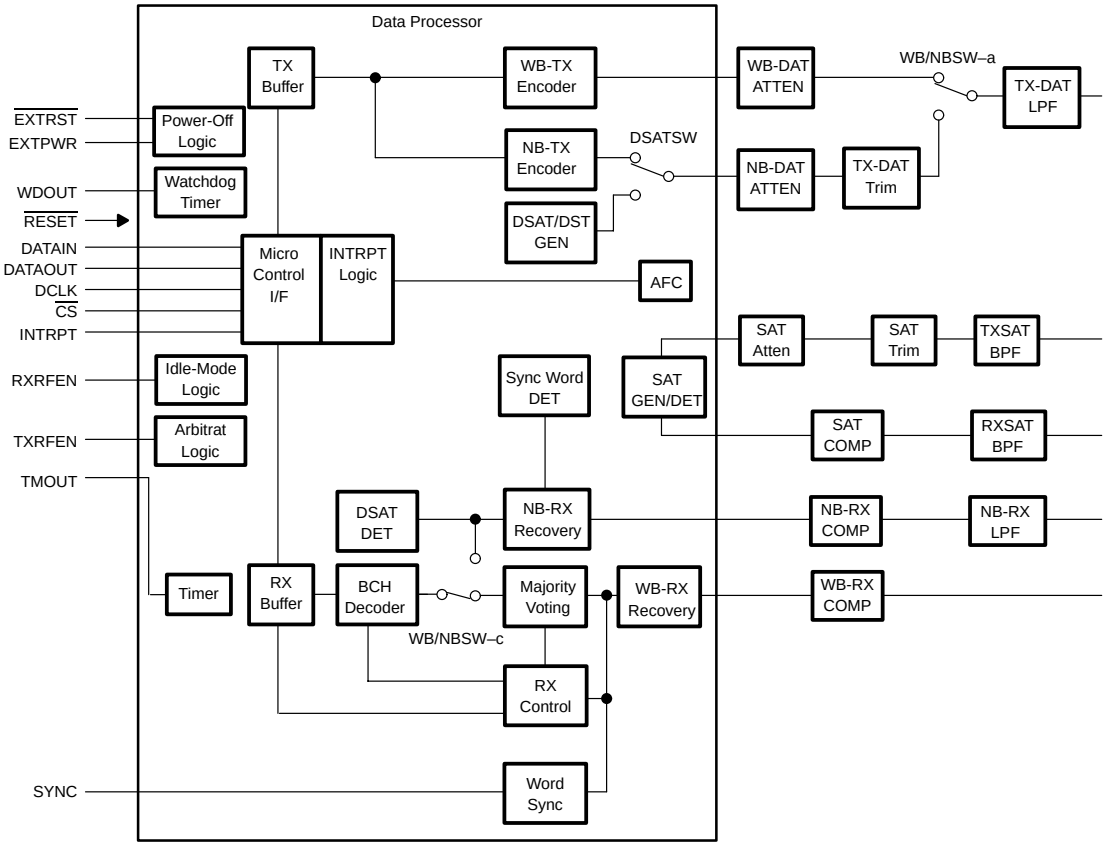


Figure 5–4. Data Processor Block Diagram

Power-off and idle-mode logic are provided, together with both standard and watchdog timers. The data processor selects incoming receive (RX) data according to standard (for example, WB/NB). The filters/comparators process the data to comply with the standard. After majority voting and/or BCH decoding, the data processor buffers the data and applies it to the microcontroller interface. On the transmit side, data moves to the TX buffer after the data processor selects the appropriate encoder. The encoded data goes through the attenuator and/or trim stage to the transmit data low-pass filter (TX-DAT LPF) and switches to the transmit (TX) audio path.

The RXSAT filter and SAT comparator recover the supervisory audio tone (SAT) from the receive audio path and feed it to the data processor detector/generator. The SAT GEN/DET block generates TXSAT and applies it through programmable attenuator/trim stages to the band-pass filter that feeds the transmit path.

The NB data recovery block detects a digital supervisory audio tone (DSAT) signal. The DSAT/DST GEN regenerates the DSAT signal and sends it through the normal NB-DAT path to the transmit path.

5.5 Miscellaneous Circuits

Figure 5–5 shows miscellaneous circuit block diagrams. The LS DRIVER block provides the capability to drive loudspeakers. The external resistor pair R2/R1 sets the gain. An uncommitted operational amplifier (AMP7) is provided, and the external resistor pair R4/R3 sets the gain.

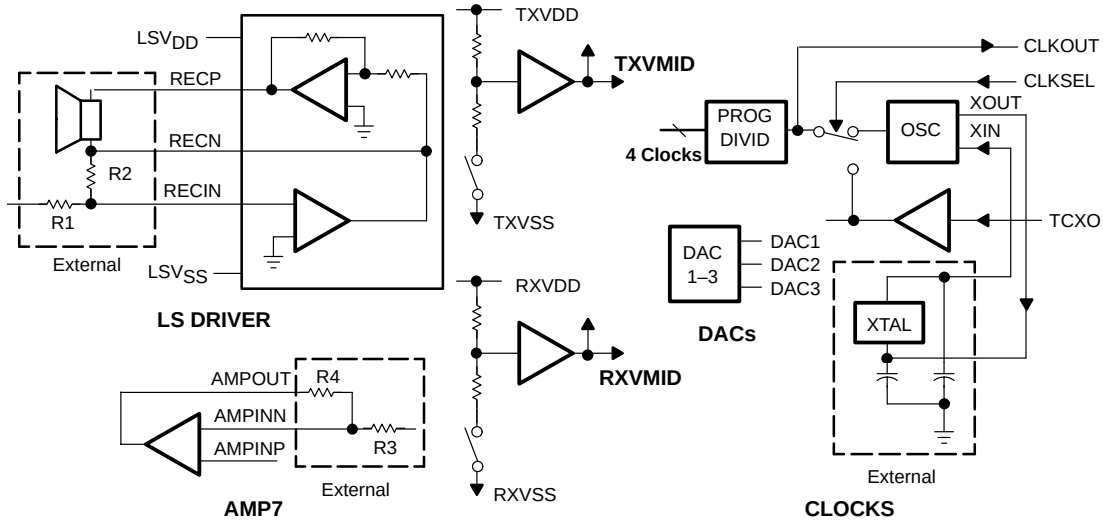


Figure 5–5. Miscellaneous Circuit Block Diagrams

A separate mid-rail voltage source is provided for both the receive and transmit paths (RXVMID and TXVMID). Each is deselected when its part of the circuit powers down.

You may program the TCM8030 clocking source (oscillator signal or external clock) that applies to a programmable divide (PROG DIVID). PROG DIVID divides the clocking source into four separate internal clocking signals. The oscillator block requires only a crystal oscillator (XTAL) and a pair of capacitors for operation. Alternatively, you can connect an external clock at XIN, or you may select a TCXO, as required. A triple DAC is also provided for oscillator trim functions. When used in conjunction with the AFC control in the data processor block, the triple DAC allows you to use lower stability oscillators successfully, to save system costs.

5.6 Clocks

The TCM8030 oscillator and programmable divider (OSC and PROG DIVID) circuits generate internal clocks and an external clock output on the CLKOUT terminal. The circuits are shown in Figure 5–1.

The TCM8030 CLKSEL terminal selects the clocking source, as described in Table 5–1.

Table 5–1. Clock Sources

TCM8030 Clocking Scheme	CLKSEL	Description
XTALOSC	LOW	Clock Source is the internal crystal oscillator (XTALOSC). An external crystal oscillator is required and is connected between XIN and XOUT (terminals 69 and 68). Only a 5.12-MHz frequency source is allowed. In addition, TCXOAMP can be enabled by selecting IFAMPEN in register AUXPE (write address 30H, bit 4).
External square wave	LOW	Clock source is an external square wave frequency with a standard CMOS logic level input applied to XIN (terminal 69). Any frequency in Table 5–2 is allowed. In addition, TCXOAMP can be enabled by selecting IFAMPEN in register AUXPE (write address 30H, bit 4).
External TCXO (temperature-compensated crystal oscillator)	HIGH	Clock source is an external TCXO with a minimum amplitude of 0.5-Vp-p applied to TCXO (terminal 72). Any frequency in Table 5–2 is allowed. In this mode, the XTALOSC block is powered down and TCXOAMP is enabled independent of the settings of register AUXPE (write address 30H).

The TCM8030 has an automatic frequency control (AFC) circuit that maintains the accuracy of an external temperature-compensated crystal oscillator (TCXO). For the first two clock sources (XTALOSC or external square wave), the AFC circuit operates with any TCXO operating at a frequency less than 20 MHz. However, for the third clock source (external TCXO), the AFC operates with a TCXO at a frequency associated with CKRT (write address 31H, bits 0 – 2), as described in Table 5–2.

Table 5–2. Master Clock Input Frequency and CLKOUT Select

Bit 2 CKRT2	Bit 1 CKRT1	Bit 0 CKRT0	Bit 3 CLKOUT-SEL	Frequency Selected	Terminal CLKOUT
0	0	0	X	5.12 MHz	X
0	0	1	X	7.68 MHz	X
0	1	0	X	10.24 MHz	X
0	1	1	X	12.8 MHz	X
1	0	0	X	15.36 MHz	X
1	0	1	X	17.92 MHz	X
1	1	0	X	†	X
1	1	1	X	†	X
X	X	X	0	X	Active
X	X	X	1	X	Hi-Z

† CKRT(bits 0–2) = 110 and 111 are not allowed.

The TCM8030 also provides an external divide-by-two counter clock (CLKOUT). If CLKSEL is high, the internal XTALOSC or external square wave-frequency signal source routes through a divide-by-two counter to CLKOUT. If CLKSEL is low, the external TCXO frequency routes through the divide-by-two counter to CLKOUT. When CLKOUTSEL is low, CLKOUT is active. When CLKOUTSEL is high, CLKOUT is in a high-Z state. CLKOUTSEL is low after reset.

The TCM8030 also possesses a frequency divider circuit that derives the internal and external reference clocks (2.56 MHz to the data processor and 1.28 MHz, 320 kHz, 160 kHz, and 10 kHz to the audio processor).

The internal crystal oscillator (XTALOSC), TCXO input recovery circuit (TCXOAMP), and internal dividers (PROG DIVID) share their own dedicated power supply terminals. This minimizes crosstalk from the rest of the circuit, therefore reducing the amount of clock jitter.

All the clock circuits power down in the TCM8030 power-down mode. In all other modes, the clock circuits stay active. Program the appropriate external clock or crystal frequencies using the clock source frequency-select, write address 31H, CLKSRC. Use CKRT0 – CKRT2 (CLKSRC bits 0 – 2) to program the frequency, and CLKOUTSEL (CLKSCR bit 3) to enable or disable CLKOUT. A reset will select, by default, a 5.12-MHz frequency(CKRT0 – CKRT2 = 000) and CLKOUT will become active (CLKOUTSEL = 0) (see Table 5–2). Figure 5–6 illustrates the TCM8030 clocking scheme.

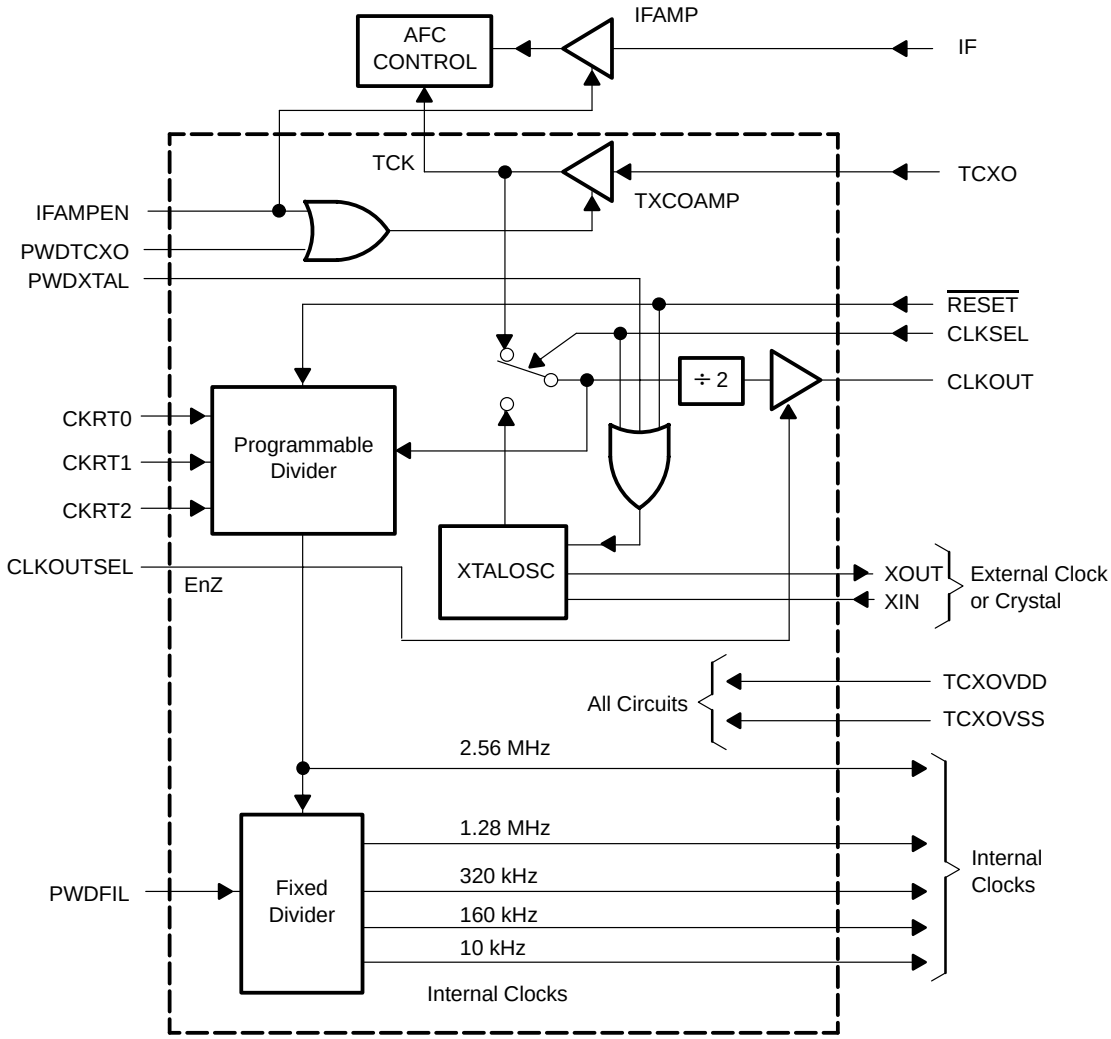
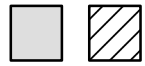
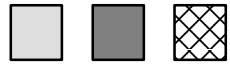


Figure 5–6. Clocking Scheme Functional Block Diagram

5.7 Power Modes

The TCM8030 contains power-off logic circuitry that implements six modes of operation, as shown in Table 5–3 and Figure 5–7. These modes are selected by control word 4, write address 03H. In total power-down mode, all internal circuits, including the crystal oscillator (XTALOSC), are disabled.

Table 5–3. Power Modes Block Diagram Legend

Power Modes	Description	Coding
1. Total power-down mode	Power is applied to the TCM8030, but all circuits are powered down. EXTPWR is low to disable power supply to the rest of the phone. Only a static power-up using one of the keyboard interrupt ports allows the TCM8030 to exit total power-down mode. When this happens, the TCM8030 enters shutdown mode.	
2. Shutdown mode	Power is applied to the TCM8030, but the phone is unable to receive calls. The microcontroller may access internal registers, but it may not issue commands. Only the circuits with the following coding are on.	
3. Idle mode	Power is applied to the TCM8030, and the phone is monitoring the forward control channel (FOCC) from the base station. Only the circuits with the following coding are on.	
4. Tone mode	Power is applied to the TCM8030, but the phone is not in communication with the base station. The user interface (via the I/O ports) is enabled. Only the circuits with the following coding are on.	
5. Full operation mode, DTMF off	Power is applied to the TCM8030. The phone is in conversation mode, but the DTMF generator is not enabled. All circuits except the circuit with the following coding are on.	
6. Full operation mode, DTMF on	Power is applied to the TCM8030. The phone is in conversation mode, but the DTMF generator is enabled. All circuits are on.	
Auxiliary Circuits *Power enabled independently*	Independent enabling can be applied to IFAMP, DAC1–3, and AMP7. Only the circuits with the following coding have this feature. In total power-down mode, this feature and these circuits are disabled.	

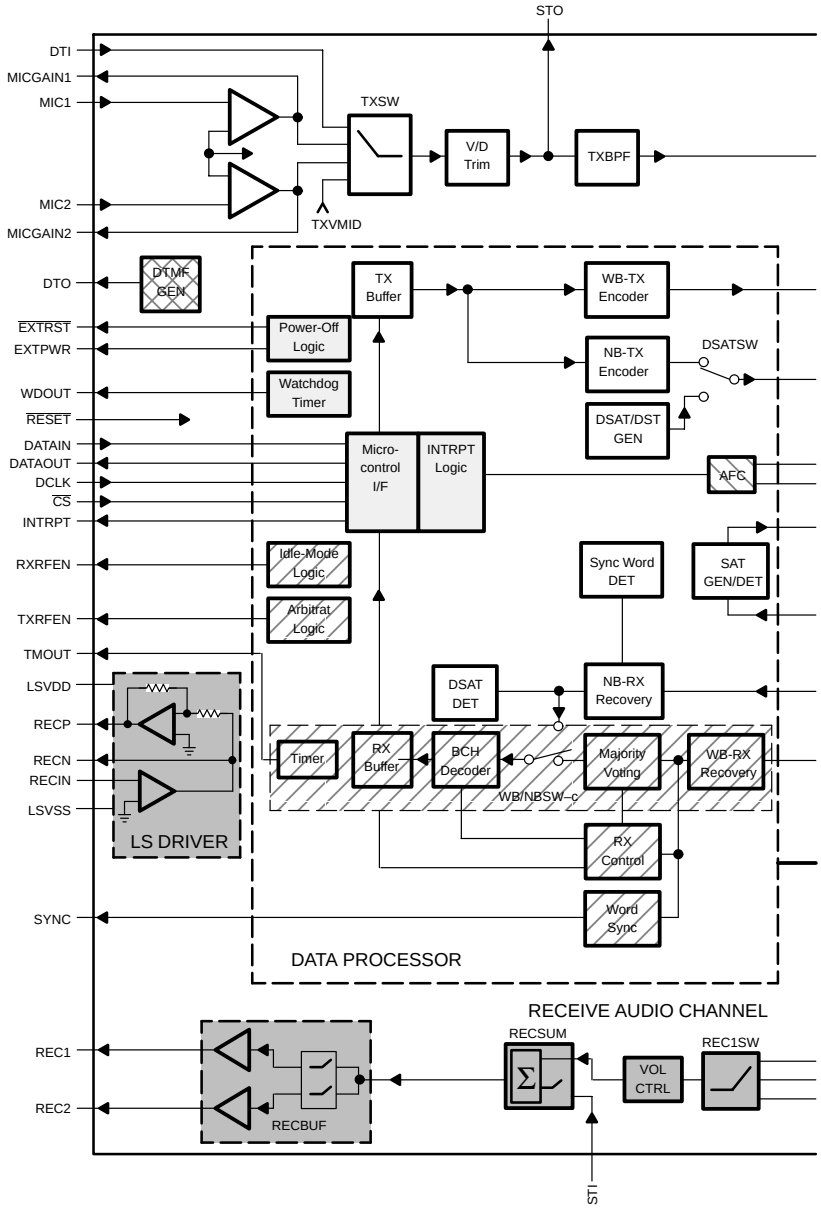


Figure 5–7. Power Modes Block Diagram

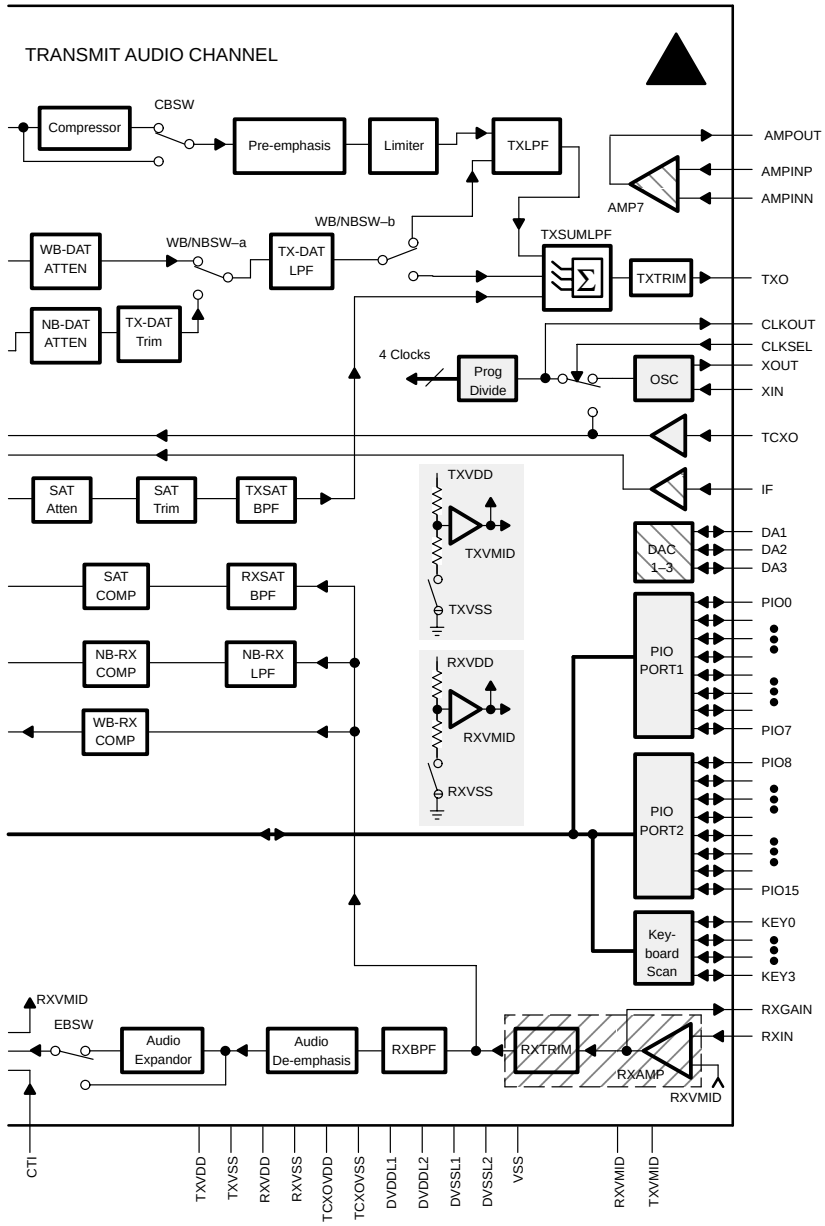


Figure 5–7. Power Modes Block Diagram (Continued)

5.7.1 Total Power-Down Mode

In this mode, power is still applied to the TCM8030, but the device is in total power-down mode. All circuits, including CLOCK, bias circuits, PIOs, and the watchdog timer, power down. The TCM8030 stops so it draws minimal leakage current, as illustrated in Figure 5–7. The EXTPWR output terminal is low to disable the power supply to the rest of the telephone (including the MCU). The $\overline{\text{EXTRST}}$ terminal is also low, and the TCM8030 microcontroller interface is disabled.

The TCM8030 is the only device in the telephone with its power supply enabled in total power-down mode. Static power-up logic, implemented using one of the keyboard interrupt ports, waits for the power-on key to be pressed. After the key is pressed, the TCM8030 exits the total power-down mode, reactivates the oscillator, enables the regulators to the rest of the telephone (using the EXTPWR enable signal), and holds the $\overline{\text{EXTRST}}$ terminal low for 0.1 to 0.2 second, to allow the rest of the telephone to go to power-up reset mode when the system is stable.

The TCM8030 goes into total power-down mode by writing to control word 4, (write address 03H, C4 bits 4–0). You must toggle both control word 4 (C4) bits 1–0, with this write transaction. The security bit, C4 bit 1, reduces the probability that the total power-down mode is entered erroneously, for example, by RFI (radio frequency interference).

The independent analog circuits IFAMP, AMP7, and DAC1–3 also power down in total power-down mode, independent of the status of their own power-down control bits in register AUXPE (write address 30H).

The cellular telephone uses the total power-down mode from the first connection of the battery as follows:

1. The telephone receives power for the first time when the battery is connected. Only TCM8030 initially connects to its power supply, powering up in shutdown mode. In this mode, CLKSEL sets the TCM8030 master clock source (see Section 5.6), and it immediately sets EXTPWR high.
2. The power-up $\overline{\text{RESET}}$ input to the TCM8030 is held low during the operation of the external power-on-reset (RC) circuit. This also holds $\overline{\text{EXTRST}}$ at low.
3. When the external power-on reset mode finishes, $\overline{\text{EXTRST}}$ transitions to high, the TCM8030 microcontroller interface enables, and the MCU starts its boot routine. Because the TCM8030 INTRPT terminal is not set to one, the MCU knows that it was reset by a battery connect power up. (In this situation the telephone should appear to be off until the power-on key is pressed). The MCU then writes to the TCM8030 to:

- Enable a keypad interrupt on the appropriate KEY pin. This requires four write transactions to TCM8030 registers:
  - PI3INT (write address 1CH) to enable the pin interrupt
  - PI3PULL (write address 1BH) to enable or disable the pullup as required
  - PIOC3 (write address 19H) to set direction as input
  - IE2 (write address 06H) to enable interrupts from the PIO3, keypad port
- Set the C4 bits 4–0 to 02H to enter total power-down mode.

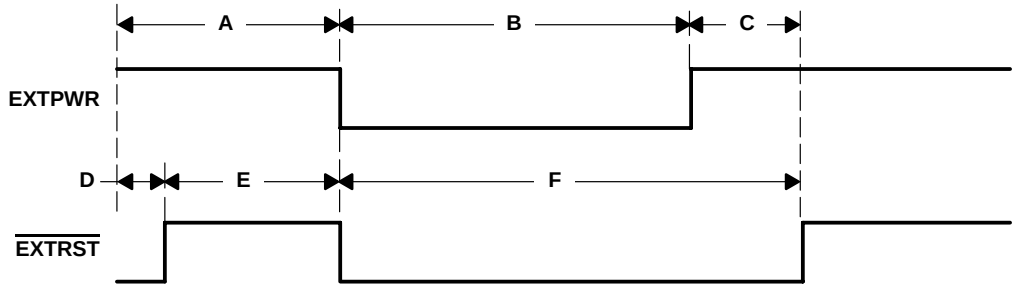
4. The MCU must first enable the keypad port terminal connected to the power-on key before entering total power-down mode. If the MCU does not, only a $\overline{\text{RESET}}$ to the TCM8030 will re-enable it.
5. At this point the clock stops, EXTPWR transitions to low, $\overline{\text{EXTRST}}$ transitions to low, and the MCU and other parts of the system power off, waiting for the power-on key to be pressed.
6. When you press the power-on key, it is sensed on one of the KEY inputs. Asynchronous logic, which does not need the clock, reads the power-on key, forces TCM8030 back into shutdown

mode, and turns EXTPWR back on. The TCM8030 event register also records the fact that a keypad interrupt was received.

7. EXTPWR transitions to high and powers up the microcontroller, and after a timed interval of between 0.1 and 0.2 second, plus the XTALOSC warm-up time, TCM8030 releases $\overline{\text{EXTRST}}$, allowing the rest of the system to power up and reset when the system is stable. The MCU then executes its boot routine.

8. At this time, the INTRPT terminal from the TCM8030 is in active mode, and the microcontroller checks the TCM8030 event register and determines it was awakened by a keypad event, such as a pressed power-on key. When the MCU is awakened, the microcontroller starts to initialize the entire system, as appropriate.

Figure 5–8 summarizes the TCM8030 power sequence.



NOTES: A. A battery is connected and power is applied the first time. (TCM8030 powers up in shutdown mode.)
B. The TCM8030 is waiting for power key to be pressed.
C. The microcontroller powers up and $\overline{\text{EXTRST}}$ is released after 0.1 to 0.2 second delay (plus XTALOSC warm–up time).
D. $\overline{\text{RESET}}$ and $\overline{\text{EXTRST}}$ low during the power up-reset mode.
E. Power-up reset cycle starts, and microcontroller enables keypad interrupts. TCM8030 enters the total power-down mode.
F. A keypad sense power-on event, such as the power-on key, is pressed. EXTPWR is re-enabled, after 0.1 to 0.2 second plus the XTALOSC warm up time.

Figure 5–8. Summary of TCM8030 Power-Up Events

5.7.2 Shutdown Mode

The microcontroller interface, clock, bias circuits, watchdog timer blocks, and all three PIOs remain operational in the shutdown mode, as illustrated in Figure 5–7. The shutdown mode can be used when the telephone is switched on but cannot receive calls, for example, while the battery is recharging. The microcontroller interface may access all internal registers during shutdown mode, but may not issue commands (addresses 08H to 0CH and 0EH) except for the reset command (address 0DH).

5.7.3 Idle Mode

In addition to the circuits that are operational in shutdown mode, the wideband receive data path is enabled, as illustrated in Figure 5–7. This corresponds to the telephone being in idle mode, on a forward-control channel (FOCC). Two submodes also activate within the idle mode to further minimize power consumption in the telephone. First, the MCU idle submode (see the *TCM8030 Analog Baseband Data Manual* description for register E2 in read address map – read address 06H) enables the MCU to go to sleep when it does not receive any new messages, and the RXRF idle submode (see the *TCM8030 Analog Baseband Data Manual* description for register RXRFTIM in write address map – write address 20H) powers down the RF receiver when it is not needed.

5.7.4 Tone Mode

In addition to the circuits in shutdown mode, the DTMF generator and the section of the RX audio path that follows the call tone input (CTI) power up in tone mode, as illustrated in Figure 5–7. This mode is used when the telephone powers up, and when the user interface, such as the keypad and user memories, is enabled but the telephone does not communicate with the base station.

5.7.5 Full Operation Mode, DTMF TX Off

This mode corresponds to a telephone conversation in progress. All circuits are on, except the DTMF generator, as illustrated in Figure 5–7.

5.7.6 Full Operation Mode, DTMF TX On

This mode is enabled so that a DTMF tone can be transmitted during a telephone conversation. All circuits are on, as illustrated in Figure 5–7.

5.7.7 Independent Circuits

The IFAMP, DAC1–3, and AMP7 blocks can be individually powered down as described in the AUXPE register (write address 30H). These bits are overridden, and all circuits power down in total power-down mode, as illustrated in Figure 5–7. The current consumption in these circuits is specified as auxiliary power modes in the electrical characteristics over recommended operating conditions section.

5.8 Circuit Definitions

Within the TCM8030, certain circuits control specific analog baseband processor operations. The following sections give descriptions of these circuits and their functions.

5.8.1 Transmit Path Audio Processing Functions

The TCM8030 audio transmit path is composed of the following circuits, as shown in Figure 5–1. A brief functional description is given for each circuit.

5.8.1.1 MIC1 and MIC2 amplifier

A pair of single-ended microphone amplifiers accept two input signals (MIC1 and MIC2). Gains for MIC1 and MIC2 are set using external resistors. Output from each amplifier is fed back through terminals MICGAIN1 and MICGAIN2.

5.8.1.2 TXSW

The transmit switch (TXSW) selects one of four transmit audio sources. It selects either the voice signal from MICAMP1 or MICAMP2; the input pin DTI, which connects externally to the DTMF generator; or connects to TXVMID to mute the transmit path.

5.8.1.3 V/D Trim

The voice or DTMF trim (V/D TRIM) circuit uses an antialiasing filter to process the audio signal before it is applied to the transmit band-pass filter. This circuit block also provides a means to trim the voice and DTMF signal levels.

5.8.1.4 TXBPF

The transmit band-pass filter (TXBPF) is a switched capacitor band-pass filter that passes only the transmit audio frequencies from 300 Hz to 3 kHz.

5.8.1.5 Compressor

The compressor circuit compresses the audio signal and outputs a signal with a change of 1 dB for an input signal change of 2 dB.

5.8.1.6 CBSW

The compressor bypass switch (CBSW) permits the routing of the audio signal around the audio compressor circuit when testing the audio channel or passing DTMF signals.

5.8.1.7 Pre-emphasis

As audio frequencies increase, the pre-emphasis circuit increases the signal gain at a rate of 6 dB per octave across the 300-Hz to 3-kHz audio passband.

5.8.1.8 Limiter

The limiter circuit limits the transmit signal deviation within an acceptable range. The limiter has a set gain of +6.0 dB. The limiter also maintains a software programmable trim with a trim range from –10.97 dB to 7.5 dB.

5.8.1.9 TXLPF

The transmit low-pass filter (TXLPF) is a switched-capacitor filter that removes harmonics caused by the (deviation) limiter. Linear-phase design prevents overshoots. This circuit is also used in narrowband mode to filter switched-capacitor output noise from TX-DAT LPF.

5.8.1.10 TXSUMLPF

The transmit-summing and low-pass filter (TXSUMLPF) is a switched-capacitor filter that selectively sums voice, data, or SAT into the audio output. It also includes a low-pass switched-capacitor filter to reduce spurious output emissions above 10 kHz.

5.8.1.11 TXTRIM

The transmit trim stage (TXTRIM) trims the FM deviation by transmitting either ST or wideband data prior to its output on the TXO terminal. This stage has a continuous second-order smoothing filter that removes noise.

5.8.2 Receive Path Audio Processing Functions

The TCM8030 audio receive path is composed of the following circuits, as shown in Figure 5–1. A brief functional description is given for each circuit.

5.8.2.1 RXAMP

The receive amplifier circuit (RXAMP) receives its input from the RXIN terminal. A portion of the RXAMP output is applied, through the RXGAIN terminal, to a pair of external resistors that set the stage gain. The RXAMP noninverting input internally connects to the RXVMID reference level.

5.8.2.2 RXTRIM

The receive trim (RXTRIM) stage compensates for FM discriminator variations. This block also contains a switched-capacitor filter to perform antialiasing.

5.8.2.3 RXBPF

The receive band-pass filter (RXBPF) is a switched-capacitor filter with a pass band from 300 Hz to 3 kHz.

5.8.2.4 DE-EMPHASIS

As audio frequencies increase, the de-emphasis circuit decreases the signal gain at a rate of 6 dB per octave across the 300-Hz to 3-kHz audio pass band.

5.8.2.5 EXPANDOR

The audio expandor circuit expands the audio signal and outputs the signal with a change of 2 dB for an input signal change of 1 dB.

5.8.2.6 EBSW

The expandor bypass switch (EBSW) permits the routing of the received audio signal around the expandor during testing.

5.8.2.7 REC1SW

The receive 1 switch (REC1SW) selects one of three receive sources. REC1SW selects either the output from the expandor circuit (expanded or bypassed), the call tone (CTI) input, or selects and connects REC1SW to RXVMID to mute the receive path.

5.8.2.8 VOL CTRL

The volume control (VOL CTRL) circuit can be programmed to provide a nominal gain of –20 dB to 17.5 dB for the outputs REC1 and REC2.

5.8.2.9 RECSUM

The receiver summing circuit and switch (RECSUM) provide the means for adding sidetone (STI) input into the receive audio path.

5.8.2.10 RECBUF

The receiver buffer (RECBUF) switches or mutes two output buffers independently, or it connects these buffers in differential mode so that a piezo- speaker can be connected to REC1 and REC2 terminals. Independent control of the two audio outputs allows one to be used for external hands-free operation.

5.8.2.11 LS DRIVER

The loudspeaker driver (LS DRIVER) circuit is a selectable differential or single-ended output earpiece amplifier. It drives a 32 Ω dynamic earpiece (or a piezoearpiece).

5.8.3 Transmit Path Data Processing Functions

The TCM8030 data processing functions associated with the transmit path are performed by the following circuits as shown in Figure 5–1. A brief functional description is given for each circuit.

5.8.3.1 TX BUFFER

The transmit buffer (TX BUFFER) buffers both narrowband and wideband data that is loaded from the five transmit-data word registers (TXD0 – TXD4, write addresses 10H–14H).

5.8.3.2 WB-TX ENCODER

The wideband transmit data encoder circuit (WB-TX ENCODER) receives the data from the transmit buffer and performs all the necessary operations for both the reverse control channel (RECC) and reverse voice channel (RVC) data transmission. It calculates and adds BCH parity bits to the data, along with word sync and dotting. The data is repeated as specified for analog cellular. The wideband signaling tone (ST) is generated when required.

5.8.3.3 NB-TX ENCODER

The narrowband transmit data encoder circuit (NB-TX ENCODER) calculates the BCH encoding parity bits from the data in the transmit buffer and adds the 30-bit synch word to synchronize the transmission of RVC data to the DSAT.

5.8.3.4 DSATSW

The digital supervisory audio tone switch (DSATSW) selects either narrow-band data or the output from the DSAT/DST GEN stage for application to the NB-DAT ATTEN stage. The fifth and sixth bits of the operational control word C1 (write address 00H) control the operation of the DSATSW. When bits 5 and 6 are set to zero, the switch connects to the NB-TX encoder input.

5.8.3.5 WS/NBSW-a, -b, and -c

The wideband and narrowband switches (WB/NBSW -a through -c), grouped together, select either narrowband or wideband transmission operation. The switch position is controlled by the value in bit one of the operational control word C1 (write address 00H).

5.8.3.6 DSAT/DST GEN

The digital supervisory audio tone/digital signaling tone generator (DSAT/DST GEN) circuit generates the narrowband DSAT and DST signals.

5.8.3.7 NB-DAT ATTEN and WB-DAT ATTEN

These two circuits are fixed narrowband and wideband data attenuators (NB-DAT ATTEN AND WB-DAT ATTEN) that set a fixed attenuation to provide the correct data signal levels.

5.8.3.8 TX-DAT TRIM

The transmit data trim circuit (TX-DAT TRIM) trims the DSAT, DST, and narrowband data levels.

5.8.3.9 TX-DAT LPF

The transmit data low-pass filter circuit (TX-DAT LPF) provides low-pass switched-capacitor filtering of the DST, DSAT, narrowband, and wideband data to minimize output harmonics and correct narrowband transmitted data eye patterns.

5.8.4 Receive Path Data Processing Functions

The TCM8030 data processing functions associated with the receive path are performed by the following circuits as shown in Figure 5–1. A brief functional description is given for each circuit.

5.8.4.1 WB-RX COMP

This wideband receive comparator circuit (WB-RX COMP) features built-in hysteresis to reject noise.

5.8.4.2 WB-RX RECOVERY

This circuit performs the wideband data recovery function (WB-RX RECOVERY), including dotting.

5.8.4.3 WORD SYNC

This circuit performs frame synchronization (WORD SYNC) recovery for the wideband data channel.

5.8.4.4 NB-RX LPF

The narrowband receive data and low-pass filter circuit (NB-RX LPF) contains a low-pass switched-capacitor filter for filtering DSAT and audio signals. This circuit also includes a decimating antialiasing stage at the input.

5.8.4.5 NB-RX COMP

The narrowband receive and DSAT comparator circuit (NB-RX COMP) features built-in hysteresis to reject noise.

5.8.4.6 NB-RX RECOVERY

The narrowband data and DSAT recovery circuit (NB-RX RECOVERY) recovers the narrow-band data and DSAT components for application to the BCH decoder circuit.

5.8.4.7 SYNC WORD DET

The sync word detect circuit (SYNC WORD DET) detects the narrowband data sync word.

5.8.4.8 DSAT DET

The digital supervisory audio tone detector circuit (DSAT DET) monitors the narrowband receive recovery data for the DSAT signal.

5.8.4.9 Majority voting

In wideband mode, each of the 40 receive data bits is majority voted. The number of repeats is read using the microcontroller interface.

5.8.4.10 BCH decoder

The wideband and narrowband BCH decoder stage can correct up to two errors in the received signal and give a 4-bit error correction status report.

5.8.4.11 RX BUFFER

The receive buffer (RX BUFFER) stage provides a buffer for both wideband and narrowband received data.

5.8.4.12 RX CONTROL

The receive control (RX CONTROL) functional block controls the wideband/narrowband receive data recovery and decoding stages. It splits the time-multiplexed busy/idle bits, chooses word A or B, and starts the majority vote and error correction processes, when required.

5.8.4.13 ARBITRAT LOGIC

The arbitration logic circuit (ARBITRAT LOGIC) arbitrates wideband data busy/idle bits majority voting and outputs the results to the TXRFEN terminal.

5.8.4.14 IDLE MODE LOGIC

The idle-mode logic circuit senses the microcontroller unit (MCU) idle mode and receive RF (RXRF) idle-mode functions, and applies an enable signal to the output terminal RXRFEN to control external power consumption.

5.8.5 Transmit Path SAT Processing Functions

The TCM8030 supervisory audio tone (SAT) transmit-path processing functions are performed by the following circuits, as shown in Figure 5–1. A brief functional description is given for each circuit.

5.8.5.1 SAT GEN/DET

The supervisory audio tone generator and detector (SAT GEN/DET) circuit is primarily a transponding digital phased-locked loop (PLL) circuit. It is used in wideband mode only. The circuit is an enhanced design that improves SAT sensitivity. SAT outputs can also be programmed without a SAT input to facilitate phone testing.

5.8.5.2 SAT ATTEN

The supervisory audio tone attenuator (SAT ATTEN) circuit is a fixed attenuator used to set the correct TX SAT signal level.

5.8.5.3 SAT TRIM

The supervisory audio tone trim (SAT TRIM) circuit sets the wideband SAT level trim. Output from this circuit is applied to the TXSAT BPF antialiasing filter.

5.8.5.4 TXSAT BPF

The transmit band-pass filter (TXSAT BPF) circuit is a switched-capacitor band-pass filter that performs antialiasing.

5.8.6 Receive Path SAT Processing Functions

The TCM8030 supervisory audio tone (SAT) receive-path processing functions are performed by the following circuits, as shown in Figure 5–1. A brief functional description is given for each circuit.

5.8.6.1 RXSAT BPF

The receive band-pass filter (RXSAT BPF) circuit for the supervisory audio tone is a switched-capacitor band-pass filter.

5.8.6.2 SAT COMP

The supervisory audio tone comparator (SAT COMP) circuit slices the received SAT signal before sending it to the SAT GEN/DET circuit. This circuit also contains built-in hysteresis to aid in noise rejection.

5.9 Miscellaneous Functions

The TCM8030 contains several circuits that perform specific functions as previously shown in Figure 5–1. A brief functional description is given for each circuit.

5.9.1 Power-Off Logic

This function implements total power-down mode logic. In this mode, all internal circuits, including the XTALOSC, are disabled. The TCM8030 is the only device in the phone with its power supply enabled in this mode. Static power-up logic, implemented via one of the keyboard interrupt ports, waits for a pressed power-on key. Then TCM8030 exits total power-down mode, reactivates the oscillator, enables the regulators to the rest of the phone via EXTPWR, and holds $\overline{\text{EXTRST}}$ low for 0.1 to 0.2 second, to allow the rest of the phone to power up cleanly.

5.9.1.1 TXVMID and RXVMID

The TXVMID and RXVMID functional blocks are separate transmit and receive analog-reference voltage generators. The circuits contain resistive dividers fed from analog voltage supplies. The outputs are buffered and then decoupled externally, to provide accurate, quiet, mid-rail reference to internal audio circuits.

5.9.1.2 AFC

The automatic frequency control (AFC) circuit receives one input from an external TCXO (temperature -compensated crystal oscillator) and another input from the receiver IF (intermediate frequency) stage. The counters in this block then process the inputs and provide a count that can be read using the microcontroller interface.

5.9.1.3 DAC 1–3

DACs 1–3 are each 8-bit linear digital-to-analog converters.

5.9.1.4 AMP7

AMP7 is an uncommitted operational amplifier.

5.9.1.5 DTMF GEN

The dual-tone multifrequency generator (DTMF GEN) circuit generates the tones for push-button dialing and provides the user-alert tone.

5.9.1.6 Timer

The timer circuit is a programmable 8-bit counter. The timer can either count down once or cycle continuously. When the counter reaches zero, the output changes state.

5.9.1.7 Watchdog timer

The watchdog timer circuit starts by writing to a location in the microcontroller interface. If the location is not written to again within the time-out period, the watchdog timer times out and the output changes state. This change in output resets the telephone microcontroller.

5.9.1.8 PIO Port 1 and PIO Port 2

PIO Port 1 and PIO Port 2 are two 8-bit wide programmable ports. Each line of each port can be individually programmed as either an input or an output.

5.9.1.9 Keyboard scan

The keyboard scan port is a 4-bit port that accepts inputs from a keyboard and generates interrupts to the microcontroller. The port can also be reconfigured as a general purpose input/output (I/O) port. One I/O terminal connected to the telephone ON/OFF key supplies a wake-up signal that terminates the total power-down mode.

5.9.1.10 MICRO CONTRL I/F and INTRPT LOGIC

All wideband and narrowband data communications are transmitted to and received from the telephone microcontroller using the microcontroller interface (MICRO CONTRL I/F) circuitry. Internal data, command, and interrupt registers are programmed using the write operation. Other internal data, status, and interrupt registers are monitored using read operations.

5.10 Microcontroller Interface Operation

The TCM8030 microcontroller interface consists of four terminals: $\overline{CS}$, DATAIN, DATAOUT, and DCLK. CS is the active low chip-select control that enables the TCM8030 microcontroller interface to either write data to or read data from the TCM8030. During the time $\overline{CS}$ is low, sampling of input data on DATAIN occurs on the rising edge of DCLK while changes in output data on DATAOUT occur on the falling edge of DCLK. DCLK may begin and end in either the high or low state.

The microcontroller interface can be operated from software using the microcontroller general purpose I/O terminals. Alternatively, the interface can be operated using a peripheral that has an SPI, which is compatible with a 2-byte transfer as shown in Figure 5–9 and Figure 5–10. This timing is also compatible with clock-synchronous transfers from the general-purpose 8-bit universal asynchronous receiver-transmitter (UART) when an additional microcontroller I/O port is used to generate the $\overline{CS}$ signal. In the latter case, the duration of the eighth clock pulse shown can be increased so that two consecutive 8-bit write transactions can be used for a TCM8030 write operation, or a consecutive 8-bit write transaction and an 8-bit read transaction can be used for a TCM8030 read operation.

The DATAOUT terminal has a three-state driver and normally presents a high impedance as indicated in Figure 5–10. This allows both the DATAIN and the DATAOUT terminals to connect to a bidirectional microcontroller pin.

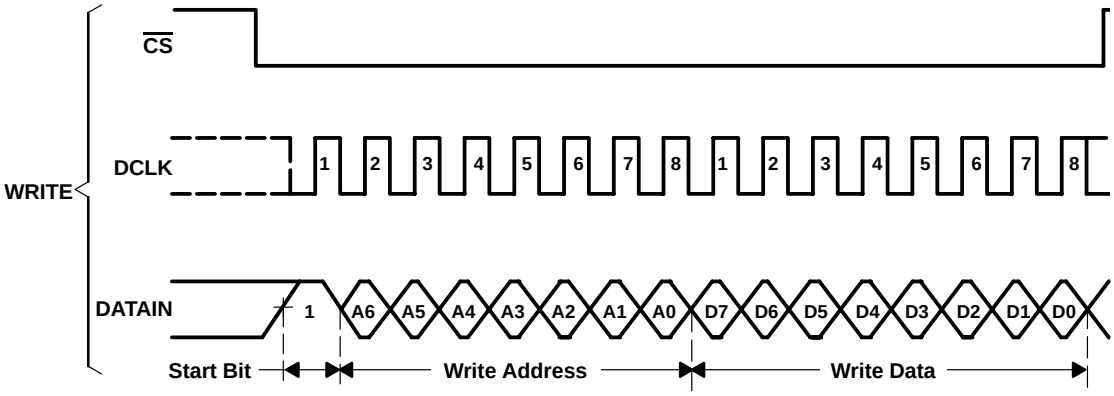


Figure 5–9. Microcontroller Interface Write Timing Diagram

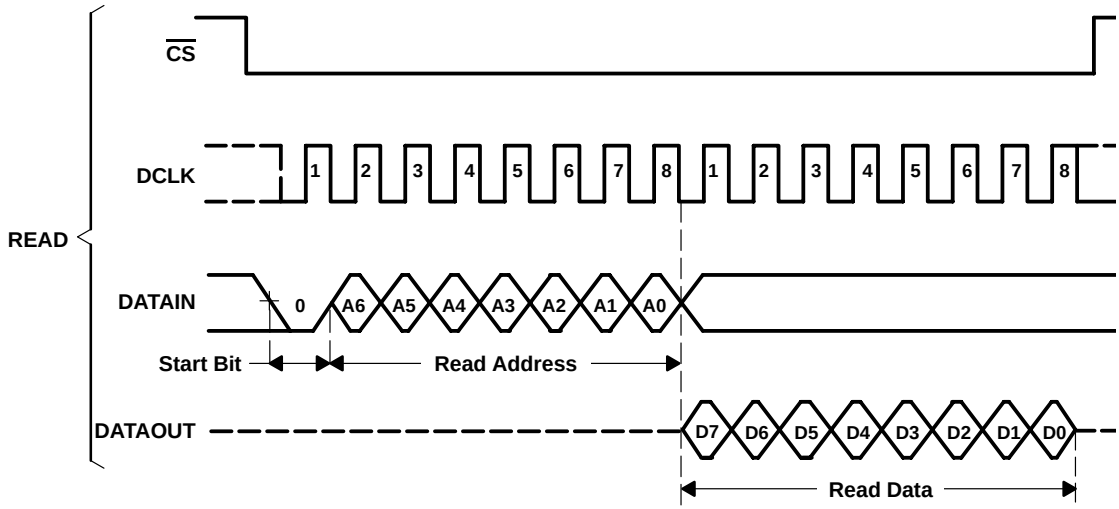


Figure 5–10. Microcontroller Interface Read Timing Diagram

5.11 Microcontroller Write Operation

For a write operation, the $\overline{CS}$ transitions to low and data on the DATAIN terminal clocks into the TCM8030 on each rising edge of DCLK. The input sequence consists of a start bit (logic 1), a 7-bit address, and then eight bits of data.

The write address map, Table 5–4, details the address and data to be written to the interface to control the TCM8030 and to transmit Manchester-encoded signals. Eight bits of data are always written to the interface and the data is right justified.

For those write operations to addresses with less than eight significant data bits, you must supply the full complement of eight data clock cycles on DCLK, although the state of DATAIN during these nonsignificant write data clock cycles is not important.

Table 5–4. Write Address Map

HEXADECIMAL ADDRESS (7 BITS)	NAME	REGISTER NAME	FUNCTION	NO. OF SIGNIFICANT BITS	DEFAULT VALUE (HEX)
00	Control word 1	C1	Operational control word	8	00
01	Control word 2	C2	DCC/SAT/DSAT control word	7	00
02	Control word 3	C3	Signal polarity selection	4	0
03	Control word 4	C4	Master power-enabling	5	1
04	Control word 5	C5	FOCC/FVC optional modes	4	0
05	Interrupt control word 1	IE1	Interrupt enables	7	00
06	Interrupt control word 2	IE2	Interrupt enables	8	00
07	Not used				
08	Commence TX	TXSTART	Commence TX command	0	–
09	Start watchdog	WDSTART	Start/restart watchdog	0	–
0A	Abort TX	TXABORT	Abort TX command	0	–
0B	Clear TX buffer	TXCLEAR	Clear TX buffer command	0	–
0C	Restart frame sync	FRAMESYNC	Restarted frame sync command	0	–
0D	Reset	RST	Reset chip command	0	–
0E	Reset arbitration	ARBITRST	Reset arbitration	0	–
0F	Not used				
10	TX data word 0	TXD0	TX data bits 35 – 28	8	00
11	TX data word 1	TXD1	TX data bits 27 – 20	8	00
12	TX data word 2	TXD2	TX data bits 19 – 12	8	00
13	TX data word 3	TXD3	TX data bits 11 – 4	8	00
14	TX data word 4	TXD4	TX data bits 3 – 0 (LSBs)	4	0
15	PIO1 control word	PIOC1	PIO1 direction selection	8	00

Table 5–4. Write Address Map (continued)

HEXADECIMAL ADDRESS (7 BITS)	NAME	REGISTER NAME	FUNCTION	NO. OF SIGNIFICANT BITS	DEFAULT VALUE (HEX)
16	PIO1 output word	PO1	PIO1 values for outputs	8	00
17	PIO2 control word	PIOC2	PIO2 direction selection	8	00
18	PIO2 output word	PO2	PIO2 values for outputs	8	00
19	PIO3 control word	PIOC3	PIO3 direction selection	4	0
1A	PIO3 output word	PO3	PIO3 values for outputs	4	0
1B	PIO3 pullup control	PI3PULL	PIO3 input pullup enable	4	F
1C	PIO3 interrupt control	PI3INT	Enable event monitoring on PI3, set sense of input	8	00
1D – 1F	Not used				
20	RXRF idle mode timer	RXRFTIM	RXRFTIM, RF power-saving duration	6	2B
21	Counter/timer coef.	TIMER	Coefficient and start command	8	00
22	Mismatch	FRAMEMIS	Frame mismatch coefficient - wideband	3	05
23	FOCC dotting	FCCDOT	Detect coefficient - wideband	4	07
24	FVC dotting	FVCDOT	Detect coefficient - wideband	7	1D
25	Narrowband error coef.	NBCOEF	Allowed narrowband errors	7	00
26	SAT coef.	SATCOEF	SAT lock determination - wideband	6	3F
27 – 2D	Not used				
2E	Data processor test control 1	DTEST1	Data processor test control	7	0
30	Auxiliary power enable register	AUXPE	Power enables DACs, IFAMP, AMP7, and LSDRIVER	6	00
31	Clock source frequency select	CLKSRC	Frequency of external clock source, and CLKOUT 3-state enabling	4	08
32	Receive audio path config	RXCFG	Receive audio path switch settings	8	00
33	Transmit audio path config	TXCFG	Transmit audio path switch settings	6	00
34	Microphone and TX DTMF trim	VDTRIM	Voice and DTMF trim gain setting	4	08
35	Limiter trim	LIMITER	Limiter gain setting	4	0A
36	Transmit SAT trim	SATTRIM	Transmit SAT trim gain setting	4	08

Table 5–4. Write Address Map (continued)

HEXADECIMAL ADDRESS (7 BITS)	NAME	REGISTER NAME	FUNCTION	NO. OF SIGNIFICANT BITS	DEFAULT VALUE (HEX)
37	Transmit data trim	TXDATRIM	Transmit Data trim gain setting	3	04
38	Transmit trim	TXTRIM	Final TX trim gain setting	5	10
39	Receive trim	RXTRIM	Receive trim gain setting	4	08
3A	Volume control	VOLCTRL	Loudspeaker volume control	4	08
3B	DTMF control	DTMFCTRL	DTMF frequency setting	7	3F
3C	Analog test modes	ATEST	Analog test mode control	4	0
3D – 3F	Not used				
40	DAC range select	DACRANGE	DAC range setting	3	0
41	DAC1 data	DAC1DAT	DAC1 input data code	8	0
42	DAC2 data	DAC2DAT	DAC2 input data code	8	0
43	DAC3 data	DAC3DAT	DAC3 input data code	8	0
44	AFC control	AFCCTRL	AFC control	5	00

In the following descriptions for the write address registers, a bit position within a register is identified by prefixing the bit number with its register name. For example, bit 6 of control word 1 in write address 00 is identified as C1.6.

5.11.1 Address 00 - Operational Control Word 1 (C1)

Control word C1 is composed of eight bits. When you use the SPI to set a C1 bit to 1, the TCM8030 performs the functions listed in Table 5–5. When you use the SPI to set a C1 bit to 0, the TCM8030 performs the function in brackets, or it does not perform any function at all.

Table 5–5. Control Word 1 (C1) Definition

BIT	FUNCTION
0	AMPS/(TACS)
1	Narrowband mode/(wideband mode)
2	Voice channel operation (RVC)/(Control channel operation RECC)
3	Receive FOCC B-word/(receive FOCC A-word)
4	Enable automatic arbitration logic. RXRFEN goes low, TXOUT is disabled on arbitration fail.
5	Enable SATOUT output — wideband Enable DSAT/DST output — narrowband
6	Enable signaling tone (ST) generation — wideband Enable digital signaling tone (DST) generation — narrowband
7	Timer continuously cycles/(stops when it reaches 00 count)

5.11.1.1 Transmit Mode Operation

Bits C1.1, C1.2, C1.5, and C1.6 of operational control word 1 (C1) in write address 00, together with the control word TXSUM control bits TXVEN, TXDEN, and TXSEN (write address 33), control the transmit mode of the TCM8030 as described in Table 5–6. No other combination of these control bits should be used.

Table 5–6. Transmit Signal Selection

TXCFG.3 (TXVEN)	TXCF.4 (TXDEN)	TXCFG.5 (TXSEN)	C1.1 (NB NOT WB)	C1.2 (RVCN OTRE CC)	C1.5 (SAT/ DSAT)	C1.6 (ST/DST)	TRANSMITTED SIGNAL AT TXO TERMINAL
0	0	0	X	X	X	X	Transmitter muted at TXSUM
0	1	0	X	0	X	X	Wideband data on RECC
1	1	0	0	1	0	0	Wideband data on RVC
1	1	0	0	1	0	1	ST and voice on RVC mixed together at TXSUM
1	0	1	0	1	1	0	SAT and voice on RVC mixed together at TXSUM
1	1	1	0	1	1	1	ST and SAT and voice on RVC mixed together at TXSUM
1	0	0	1	1	0	0	Narrowband data and voice on RVC mixed together at TXSUM
1	0	0	1	1	1	1	DST and voice on RVC mixed together at TXSUM
1	0	0	1	1	1	0	DSAT and voice on RVC mixed together at TXSUM

5.11.1.2 Arbitration

Table 5–7 defines how arbitration is controlled and how the TXRFEN terminal is used.

Table 5–7. Operational Control Word 1, Bit 4 Definition C1.4

C1.4 (WRITE ADDR 00)	ARBITRATION	RXRFEN TERMINAL
0	Software controlled Arbitration failure indicated by event bit E1.2 (read address 05) and status bit S1.2 (read address 00)	Always inactive – sense set by C3.2 (write address 02)
1	Hardware controlled (RF amplifier directly switched off using TXRFEN terminal and TXOUT disabled on arbitration failure. Also arbitration failure still indicated by event bit E1.2 (read address 05) and status bit S1.2 (read address 00))	Used for arbitration circuit. Terminal goes active on arbitration failure and only returns high after reset arbitration command – sense set by C3.2 (write address 02)

5.11.2 Address 01 - DCC/SAT/DSAT Control Word (C2)

Control word C2 is seven bits wide. When you use the SPI to set a C2 bit to 1, the TCM8030 performs the functions listed inTable 5–8.

Table 5–8. Control Word 2 (C2) Definition

BIT	FUNCTION
0	Digital color code 1st bit (DCC)
1	Digital color code 2nd bit (DCC)
2	SAT color code 1st bit (SCC) - wideband
3	SAT color code 2nd bit (SCC) - wideband
4	DSAT color code 1st bit (DSCC) - narrowband
5	DSAT color code 2nd bit (DSCC) - narrowband
6	DSAT color code 3rd bit (DSCC) - narrowband
7	Not used

5.11.2.1 Digital Color Codes (DCC)

The DCC control bits result in the inclusion of sequences in the transmitted RECC message as listed in Table 5–9.

Table 5–9. Digital Color Codes — Narrowband

CONTROL WORD 2		TRANSMITTED CODE
BIT 1	BIT 0	
0	0	0 0 0 0 0 0 0
0	1	0 0 1 1 1 1 1
1	0	1 1 0 0 0 1 1
1	1	1 1 1 1 1 0 0

5.11.2.2 SAT Reception - Wideband

A digital phase-locked loop locks onto the received SAT signal when it is in the frequency band that corresponds to the SAT color code (SCC) bits as listed in Table 5–10.

Table 5–10. SAT Color Codes — Wideband

CONTROL WORD 2		SAT FREQUENCY BAND
BIT 3	BIT 2	
0	0	5955 Hz < f < 5985 Hz
0	1	5985 Hz < f < 6015 Hz
1	0	6015 Hz < f < 6045 Hz
1	1	Transmit test

When the input frequency is not in the expected band, the TCM8030 sets the invalid SAT status flag, S1.6 (read address 00). The SAT status flag is high when the TCM8030 initializes the SAT circuit. Initialization occurs when entering wideband voice channel mode and also when you use the SPI to rewrite control word 2 (write address 01); however, the phase of the regenerated SAT is not disturbed.

The TCM8030 sets the associated event flag E1.6 (read address 05) when the SAT status changes from valid to invalid, when it changes from invalid to valid, and also on the first SAT evaluation after initialization. This event generates an interrupt if you use the SPI to set mask bit IE1.6 (write address 05).

The TCM8030 SAT GEN/DET block evaluates the SAT lock status over a 0.1 second interval to avoid the temporary phasing of the reference and input signals. A programmable coefficient, SATCOEF (write address 26), controls the evaluation of lock status.

5.11.2.3 SAT Transmission - Wideband

The SAT circuit always generates a valid SAT within the band defined by the written SCC, independent of the received signal. The microcontroller must turn off the SAT by resetting C1.5 (write address 00) to 0, after a lost SAT event occurs. The exact SAT frequency transmitted depends on the state of the SAT comparator output:

1. When a SAT is received that is outside the SCC band, the transmitted SAT is within ±15 Hz of the center frequency of the band. It is not steady. Typically, it alternates between 15 Hz and –15 Hz.
2. When no SAT signal is received and the SAT comparator output is at logic 0, the transmitted SAT is within the range ±1 Hz of the SCC center frequency. This situation is detected and the invalid SAT flag transitions to high.

Because a valid SAT within the SCC band is always transmitted, all three SAT frequencies can be generated during the production test of the telephone simply by writing the correct bits in C2.2 and C2.3 (SCC) as listed in Table 5–10. When there is no received signal, the SAT output is within ±1 Hz of the SCC center frequency. In addition, when SCC is set to 11, a 6-kHz test frequency is generated that is uneffected by any received signal and which does not attempt to lock onto it.

5.11.2.4 DSAT Reception - Narrowband

In narrowband mode (C1.1 = 1, write address 00) the received signal is continuously compared with the DSAT word that corresponds to the DSAT color code (DSCC) bits as listed in Table 5–11.

Table 5–11. DSAT Color Codes — Narrowband

CONTROL WORD 2			DSAT WORD
BIT 6	BIT 5	BIT 4	
0	0	0	2556CB
0	0	1	255B2B
0	1	0	256A9B
0	1	1	25AD4D
1	0	0	26AB2B
1	0	1	26B2AD
1	1	0	2969AB
1	1	1	AAAAAA

A DSAT word is regarded as correctly detected and the receiver is locked onto the voice channel when the number of errors is less than or equal to that written to the NBCOEF register (write address 25). When the DSAT is not detected, the TCM8030 sets the invalid DSAT status flag, S1.6 (read address 00), to 1. The DSAT status flag is high when the TCM8030 initializes the DSAT circuit.

The DSAT circuit is initialized after entering narrowband mode and also whenever you use the SPI to write control word 2 (write address 01). The TCM8030 sets the associated event flag E1.6 (read address 05) whenever the status changes from valid to invalid or from invalid to valid, and also after the first evaluation, which takes place 0.12 seconds after the TCM8030 initializes the circuit. This event generates an interrupt when you use the SPI to set mask bit IE1.6 (write address 05).

The base station stops DSAT transmission when data is transmitted. The effect of this on DSAT determination is described in subsection 5.12.11 and subsection 5.14.6.

5.11.2.5 DSAT Transmission - Narrowband

The DSAT circuit always generates the DSAT corresponding to the DSCC, independent of the received DSAT. It is up to the microcontroller to turn the DSAT off by writing 0 to C1.5 (write address 00) after a lost DSAT event occurs.

Control bit C1.6 (write address 00) determines whether DSAT or DST is output. When this bit transitions to high, DST is generated instead of DSAT. DST is simply the inverted DSAT. The transition from DSAT to DST and DST to DSAT only takes place at specific places in the code sequence, as defined by the NAMPS/NTACS specifications. The switching point is handled automatically.

During the production test of the telephone, all DSATs can be transmitted even when no DSAT is received.

5.11.3 Address 02 - Signal Polarity Selection (C3)

The signal polarity selection control word (C3) is four bits wide. The functions of the high and low bit positions are listed in Table 5–12.

Table 5–12. Signal Polarity Selection Control Word (C3) Definition

BIT	FUNCTION
0	When cleared, 0 = normal logic: RXIN data zero = logic low, RXIN data one = logic high When set to 1 = inverted logic: RXIN data zero = logic high, RXIN data one = logic low
1	When cleared, 0 = normal logic: TXO data zero = logic low, TXO data one = logic high When set to 1 = inverted logic: TXO data zero = logic high, TXO data one = logic low
2	When cleared, 0 = TXRFEN and RXRFEN are active high (high = arbitration failure/RXRF idle mode active)† When set to 1 = TXRFEN and RXRFEN are active low (low = arbitration failure/RXRF idle mode active)†
3	When cleared, 0 = INTRPT is active high (high = interrupt valid) When set to 1 = INTRPT is active low (low =interrupt valid)
4–7	Not used

† TXRFEN and RXRFEN have open-drain output drivers. These terminals have active pulldown transistors, and require external pullup transistors.

5.11.4 Address 03 - Master Power Enable Modes (C4)

This register controls the operation of the different power modes as listed in Table 5–13. When you use the SPI to set a bit in this register to 1, a section of the TCM8030 is powered up. After a $\overline{\text{RESET}}$, only bit 0 is enabled so that the device is initially in shutdown mode. To disable sections of the TCM8030, use the SPI to write a 0 to the appropriate bit.

Table 5–13. Master Power Enable Modes (C4) Definition

BIT	FUNCTION
0	Power up of CLOCK (TCXOAMP, XTALOSC and PROGDIV). When clock is powered down (0 in this bit), all circuits in the data processor and PIO ports are also off. Only the keypad port remains active to receive an external-power key press. Reset state is 1 so that the TCM8030 powers up in shutdown mode.
1	Security bit. Reset to 0. It must always be the inverse of C4.0 and must be set to 1 at same time as C4.0 is reset to 0 to enter total power-down mode.
2	FOCC data reception enabled. Reset to 0.
3	DTMF generator and DTMF receive path enabled. Reset to 0.
4	Transmission circuits for speech, data, SAT/DSAT, and ST/DST, and receive circuit for speech enabled, reset to 0.
5–7	Not used

When you use the SPI to write the following bits to control word C4, it sets the six power modes as listed in Table 5–14. Only these combinations are valid. All others are not allowed.

Table 5–14. TCM8030 Power Modes

C4.4	C4.3	C4.2	C4.1	C4.0	POWER MODE
0	0	0	1	0	Total power-down mode
0	0	0	0	1	Shutdown mode
0	0	1	0	1	Idle mode
0	1	0	0	1	Tone mode
1	0	1	0	1	Full operation mode, DTMF TX off
1	1	1	0	1	Full operation mode, DTMF TX on

5.11.5 Address 04 - FOCC/FVC Optional Controls (C5)

The FOCC/FVC optional controls word C5 is four bits wide. The function of each bit depends on its value (0 or 1) as listed in Table 5–15.

Table 5–15. Optional Controls Word 5 (C5) Definition

BIT	FUNCTION
0	0 = One busy/idle bit examined to detect busy/idle status 1 = Two busy/idle bits examined to detect busy/idle status
1	0 = Maximum of eleven FVC word repeats used - wideband 1 = Maximum of five FVC word repeats used - wideband
2	0 = Auto muting is enabled when transmitting and receiving a message on voice channel - wideband 1 = Auto muting is disabled when transmitting and receiving a message on voice channel - wideband
3	0 = RXRF idle mode disabled 1 = RXRF idle mode enabled
4–7	Not used

5.11.6 Address 05 - Interrupt Control Word 1 (IE1)

The interrupt control word 1 (IE1) is seven bits wide. When you use the SPI to set a bit to 1, the TCM8030 performs the functions listed in Table 5–16.

Table 5–16. Interrupt Control Word 1 (IE1) Definition

BIT	FUNCTION
0	RX data available
1	TX buffer available
2	Arbitration failure
3	TX sequence completed
4	Change of RECC busy/idle status
5	Counter/timer reaches zero state
6	Wideband SAT/narrowband DSAT status changed
7	Not used

5.11.7 Address 06 - Interrupt Control Word 2 (IE2)

The interrupt control word 2 (IE2) is eight bits wide. When you use the SPI to set a bit to 1, the TCM8030 performs the functions listed inTable 5–17.

Table 5–17. Interrupt Control Word 2 (IE2) Definition

BIT	FUNCTION
0	FOCC data changed, (different from previously received word)
1	FVC dotting detected - wideband
2	FVC frame sync achieved (wideband word sync/narrowband sync word received)
3	Change of FOCC frame sync status
4	Change of RXRF idle mode power-saving status
5	NRZ error count register (NBERRS) updated - narrowband
6	PI03 input port signal sensed
7	AFC has reached terminal count

5.11.8 Address 08 - Commence TX (TXSTART)

Writing (the data is not significant) to this address starts transmission of the data word precursor. After sending the precursor, the encoder takes the content of the TX buffer, the generation of the event *TX buffer available* follows, and the encoder encodes and transmits the data.

You can start the data transmission before loading the TX data words 0 to 3 (write addresses 10H to 13H), but the write transaction to these registers must complete two clock cycles before the precursor completes transmission.

5.11.9 Address 09 - Start Watchdog (WDSTART)

Writing (the data is not significant) to this address starts one cycle of the watchdog timer. Unless restarted, the watchdog times out in 1.5 to 1.6 seconds. Timeout is indicated by the WDOUT output terminal transitioning to low for 100 ms. The TXRFEN terminal is also disabled until the next chip reset or WDSTART command occurs.

The WDSTART command should be given at intervals of 1.4 seconds or less.

5.11.10 Address 0A - Abort TX (TXABORT)

Writing (the data is not significant) to this address immediately stops a transmission sequence that is in progress; however, the contents of the TX buffer are not cleared.

5.11.11 Address 0B - Clear TX Buffer (TXCLEAR)

Writing (the data is not significant) to this address stops the transmission sequence after the fifth repeat of the data word starts. The word that is written to the TX buffer is neither transmitted nor cleared.

5.11.12 Address 0C - Restart Frame Sync (FRAMESYNC)

Writing (the data is not significant) to this address resets the data recovery circuit to achieve bit synchronization to the received data. It can be used when the telephone switches to a new forward control channel (FOCC) to reduce the time taken to acquire bit synchronization. The data recovery circuit does not have to wait until it detects loss of bit synchronization to change to fast-lock mode.

5.11.13 Address 0D - Reset (RST)

Writing (the data is not significant) to this address resets the chip. Its function is identical to that of the $\overline{\text{RESET}}$ input terminal, except that it does not affect the WDOUT terminal. The TCM8030 loads the default values listed in the write address map

5.11.14 Address 0E - Reset Arbitration (ARBITRST)

Writing (the data is not significant) to this address resets the arbitration circuit. After an arbitration failure, You must send this command to re-enable the transmission of data. The contents of the TX buffer are not cleared with this command.

5.11.15 Address 10 - TX Data Word 0 (TXD0)

This register contains the transmitted data bits 35 to 28 (bit 35 is the MSB).

5.11.16 Address 11 - TX Data Word 1 (TXD1)

This register contains the transmitted data bits 27 to 20 (bit 27 is the MSB).

5.11.17 Address 12 - TX Data Word 2 (TXD2)

This register contains the transmitted data bits 19 to 12 (bit 19 is the MSB).

5.11.18 Address 13 - TX Data Word 3 (TXD3)

This register contains the transmitted data bits 11 to 4 (bit 11 is the MSB).

5.11.19 Address 14 - TX Data Word 4 (TXD4)

This register contains the transmitted transmit data word 4, bits 4–7 as listed in Table 5–18.

Table 5–18. Transmit Data Word 4 (TXD4) Definition

BIT	FUNCTION
3 – 0	Not used
4	TX data bit 0
5	TX data bit 1
6	TX data bit 2
7	TX data bit 3

Use the SPI to write the transmit data to five addresses (10 – 14), which loads the transmit buffer. Write data word TXD4 last as it is the least significant byte.

5.11.20 Addresses 15, 17, 19 - PIO Control Words (PIOC1, PIOC2, PIOC3)

These control words select whether the individual terminals of the port are configured as inputs or used as outputs as listed in Table 5–19.

Table 5–19. PIO Control Words (PIO C1,2,3) Definition

VALUE	CORRESPONDING TERMINAL FUNCTION
0	Input
1	Output

The eight terminals (four for PIO3) of each port are configured as inputs by default.

5.11.21 Addresses 16, 18, 1A - PIO Output Words (PO1, PO2, PO3)

Addresses 16, 18, and 1A set the state of the PIO terminals that are configured as outputs.

5.11.22 Address 1B - PIO3 Pullup Enable Transistors (PI3PULL)

When set to 1, bits 0 to 3 of this register activate a small pullup transistor. The transistor allows PIO3, when configured as input, to be driven by open-drain drivers that are external to the TCM8030. If these transistors are not enabled, the logic level from the open-drain drivers may not be sufficient to drive PIO3 input to a high position. Therefore, the pullup transistor insures that when driving to a high position, the open-drain driver maintains the input signal at high.

5.11.23 Address 1C - PIO3 Interrupt Control (PI3INT)

Table 5–20 and Table 5–21 list the function of bits 0 through 7 for PI3INT (PIO3 interrupt control).

Table 5–20. PIO3 Interrupt Control (PI3INT, bits 3–0) Definition

PI3INT BIT(0–3)	FUNCTION
0	PIO3 operates as normal port
1	Signal sensed on PI3INT causes interrupt when IE2.6 is high.†

† The port may still be read at address 20 in this mode.

Table 5–21. PIO3 Interrupt Control (PI3INT bits 7–4) Definition

PI3INT BIT (4–7)	FUNCTION
0	Active low interrupt
1	Active high interrupt

5.11.24 Address 20 - RXRF Idle Mode Timer (RXRFTIM)

Writing to this 6-bit address sets the duration of RXRF idle (RF receiver powered down) mode. In RXRF idle mode, the RF receiver may be powered down for part of the FOCC data frame using the RXRFEN terminal. This should only be used under good signal conditions when multiple repeats of the word are not required.

The default value of 2BH ensures that the receiver has five bit periods within which to power up before the start of the dotting sequence of the next frame. For AMPS, a bit period is 0.1 ms; for TACS, it is 0.125 ms. The timer is clocked at the bit rate divided by 8. For example, RFRXTIM = 2AH allows an additional 8-bit period in which to stabilize before the start of dotting.

The FOCC data stream is purposely redundant to cope with poor reception conditions. This redundancy is in the form of both BCH error correction and five repeats of the transmitted word.

Under good reception conditions these repeats are also redundant but the RXRF power-saving mode allows the receiver to be turned off for a duration controlled by RXRFTIM. During the power saving time-out, the RXRFEN output terminal transitions to low and should be used to turn off the phone radio receiver.

In FOCC mode only, and when C5.3=1, the following conditions result in RXRFEN being disabled:

1. Zero errors detected in the first repeat
2. One error in the first repeat, plus the corrected data looks the same as the corrected word from the previous frame. This is typically the case when control filler messages are being received.

When one of the previous conditions is detected, RXRFEN transitions to low from the start of the second repeat until a few bits before the start of dotting for the next frame.

NOTE:

Condition 2 is closely related to the MCU power saving mode in which the MCU only has to process data words when the word has a different value from the word in the previous frame (see subsection 5.12.2*)*.

In addition, an AB power-saving mode is supported. Each word repeat contains an A word and a B word. The phone is programmed to check either A or B. The unused word is not required so the radio receiver may be turned off. AB power-saving mode functions independently, regardless of errors in the first repeat.

RXRFTIM controls the power down for normal power saving and AB power saving. If RXRFTIM is set to 2B, then for normal power saving RXRFEN is re-enabled five bits before dotting. For AB power saving, RXRFEN is re-enabled for a similar interval before the start of the next A or B word. Reducing RXRFTIM reduces the power-down times by eight bits in both normal and AB modes. If RXRFTIM is less than or equal to 29h, the AB mode turns off automatically because the receiver on/off switch is not sufficiently quick and the AB mode may therefore not be useful. There is no other way to enable/disable this mode.

5.11.25 Address 21 - Counter/Timer Coef (TIMER)

Writing to this address sets the count length and starts the counter. The timer counts in units of 12.8 ms, giving a maximum time interval of 3.264 seconds (255 counts). A TMZERO terminal and status bit S1.5 indicate the timer status. When the timer is counting, TMZERO and S1.5 are low but when the timer reaches zero, they transition to high and stay high until TIMER is written again unless C1.7 is high to indicate recycling mode. In recycling mode, the timer automatically reloads the count coefficient and starts the count again so that TMZERO and S1.5 are only low for 12.8 ms. In the recycling mode, with the timer set to 255, the output would be high for 255 counts and low for 1 count, giving an overall period of 256 counts.

The timer can be stopped either by a chip reset or by writing 00 to TIMER. This keeps the TMZERO signal and S1.5 low.

NOTE:

After sending the start command, there is a latency of 12.8 ms before the TCM8030 loads the timer.

When you use the SPI to set IE1.5 (write address 05), an interrupt is generated when the counter reaches zero.

5.11.26 Address 22 - Mismatch Wideband (FRAMEMIS)

This is the number of invalid wideband word syncs allowed during data recovery on both FVC and FOCC before bit synchronization with the dotting pattern is restarted.

5.11.27 Address 23 - FOCC Dotting Coefficient (FCCDOT) - Wideband

This is a coefficient for the data recovery circuit. It sets how much of the dotting preamble of the FOCC data is required before it acknowledges successful bit synchronization. It applies only to wideband mode.

5.11.28 Address 24 - FVC Dotting Coefficient (FVCDOT) - Wideband

This is a coefficient for the data recovery circuit. It sets how much of the dotting preamble of the FVC data is required before it acknowledges successful bit synchronization. It applies only to wideband mode.

5.11.29 Address 25 - Allowed Narrowband Errors (NBCOEF) - Narrowband

This register defines how many errors are allowed in the detection of the DSAT and SYNC words as listed in Table 5–22. When errors received in a DSAT word exceed the error threshold, the DSAT is assumed lost and the event bit E1.6 (change in DSAT status) is set. When a SYNC word is transmitted but the number of errors exceeds the error threshold, the SYNC word and the data following it are not recognized. Even when the SYNC word is correctly detected, a bad DSAT status is reported. This is cleared when 24 bits of DSAT are received following the data word (up to 670 milliseconds from the time the DSAT went bad).

Table 5–22. Narrowband Error Coefficient Setting

BITS	FUNCTION	DEFAULT	MAXIMUM BIT ERRORS ALLOWED	MAXIMUM BIT ERRORS RECOMMENDED
0 – 3	DSATERRS	0	6	3
3	Not used	–	–	–
6 – 4	SYNCERRS	0	6	4
7	Not used	–	–	–

The two error coefficients are initialized to 0 on reset. They may be set to any value up to and including 6. It is recommended, however, that the DSAT and SYNC word-error thresholds not exceed 3 and 4, respectively, as these values correspond to the maximum bit error rates documented in the NAMPS specification.

5.11.30 Address 26 - SAT Lock Determination (SATCOEF) - Wideband

The SAT PLL attempts to lock onto the incoming signal when it is a coherent signal within ±15 Hz of the SCC center frequency. SAT lock is determined over a 0.1-second interval, during which time there are approximately 600 cycles of the regenerated SAT. The input and output signals are compared, and when they are out of phase an error counter is incremented. When the counter reaches the value defined by SATCOEF (Table 5–23), an invalid SAT is indicated immediately on status bit S1.6 (read address 00). When the counter does not reach the threshold by the end of the 0.1-second period, a valid SAT is indicated.

When the received SAT is different from the SCC, lock cannot not be obtained. The input and reference signals beat in and out of phase. They are out of phase 50 percent of the time, so approximately 300 errors

can be expected. The absence of a signal is also detected. The number of times that the input is held high or low for a whole cycle is counted, halved, and then added to the error counter.

To allow a safety margin, the error counter only goes up to the default error threshold of 255. It should not be necessary to lower the threshold; however, some programmability is provided. The lower nibble of error threshold is hardwired to Fh and the upper nibble can be programmed using the SATCOEF register. It is also possible to enable/disable the counting of the two error types previously discussed.

Table 5–23. SAT Lock Control Definition

SATCOEF BIT	FUNCTION
0 – 3	Errors required to loose lock (most significant nibble)
4	Phase error counting enabled
5	No-signal error counting enabled

5.11.31 Address 2E - Data Processor Test Control 1 (DTEST1)

To facilitate production testing of the data processor, PIO ports 1 and 2 can be used to control and observe internal blocks. Port directions must be set as input or output by writing to the direction control registers PIO C1 and PIO C2 (write addresses 15 and 17).

To select a test mode, set the appropriate bit of the test register to 1 as defined in Table 5–24. When more than one test mode is selected, PIO C1 affects all test modes simultaneously but data can be observed from one test mode only. The selected test mode that is the least significant bit of DTEST1 is the one that is observed on PIO2.

Table 5–24. TCM8030 Data Processor Test Modes

DTEST1 BIT	TEST MODE
0	Reserved
1	Reserved
2	Data recovery observation
3 – 7	Reserved

The detailed description of each test mode is listed in Table 5–25.

Table 5–25. Data Recovery Observation (DTEST1.2 = 1)

PIO2 BIT	INFORMATION OBSERVED ON PIO2 OUTPUTS WHEN DTEST1.2 IS SET TO 1
0	NRZ narrowband data and wideband data before Manchester decoding. (e.g., Manchester-encoded 1 is seen as 0 followed by 1)
1	NRZ clock - 200 Hz (narrowband); 16 kHz (TACS); 20 kHz (AMPS).
2	Decoded Manchester data. (e.g., 01 or 10 input sequences output as 1 or 0)
3	Clock - 100 Hz (narrowband), 8 kHz (TACS), 10 kHz (AMPS)
4 – 7	Reserved

5.11.32 Address 30 - Auxiliary Power Enable (AUXPE) Register

The IFAMP, DACs 1–3, and AMP7 circuit blocks can be individually powered down. These bits are overriden and all circuits power down in total power-down mode.

This register is used to independently enable (bit is set to 1) or power down (bit is set to 0) the DACs, AMP7 (uncommitted op amp), IFAMP, and LS DRIVER blocks as listed in Table 5–26.

Table 5–26. Auxiliary Power Enables (AUXPE) Definition

BIT	NAME	FUNCTION
0	DAC1EN	DAC1 enable
1	DAC2EN	DAC2 enable
2	DAC3EN	DAC3 enable
3	AMP7EN	AMP7 (uncommitted op amp) enable
4	IFAMPEN	IFAMP enable
5	LSDRIVEREN	LSDRIVER enable. The LS driver is powered off independently when both bits C4.3 and C4.4 are low (see write address 3). Differential or single-ended operation is selected by bit RXCFG.7, write address 32.

5.11.33 Address 31 - Clock Source Frequency Select (CLKSRC)

The TCM8030 can be clocked from one of the following frequency sources selected by the first three bits in the CLKSRC register as listed in Table 5–27. Also see Section 5.6 for additional clock source details.

Table 5–27. External Clock and Crystal Frequency Select

BIT	NAME	FREQUENCY
0	CKRT0	CKRT (bits 2–0) = 000: 5.12 MHz, 001: 7.68 MHz, 010: 10.24 MHz, 011: 12.80 MHz 100: 15.36 MHz, 101: 17.92 MHz, 110: not allowed, 111: not allowed
1	CKRT1	
2	CKRT2	
3	CLKOUTSEL	When set to 0 CLKOUT is active; when set to 1 CLKOUT = Hi-Z

5.11.34 Address 32 - Receive-Audio Path Configuration (RXCFG)

The RXCFG register configures the receive audio path switches. The receive audio path is automuted at REC1SW during the reception of wideband data on FVC when automuting is enabled with a 0 to C5.2 (write address 4) as listed in Table 5–28.

Table 5–28. Receive-Audio Path Configuration (RXCFG) Control

BIT	NAME	FUNCTION
0	EBSW	Expandor bypass switch. 0 = Expandor connected, 1 = Expandor bypassed
1	REC1SW0	Receive path switch REC1SW = 00: Mute 01: Expandor (or bypassed expandor) output 10: CTI input 11: Forbidden
2	REC1SW1	
3	RECSUM	Sidetone switch and summing block (RECSUM) = 0: STI switched out 1: STI summed in
4	RECBUF0	REC1 and REC2 configuration (REC2SW) = 00: REC1 mute, REC2 mute 01: REC1 connected, REC2 mute 10: REC1 mute, REC2 connected 11: REC1 and REC2 differential
5	RECBUF1	
6	LSOPBIAS†	Independent loudspeaker VMID output bias control on RECN and RECP terminals. 0 = RECN and RECP outputs must be biased externally. 1 = RECN and RECP outputs are biased to VMID internally.
7	DIFFSIGSEL	LSDRIVER differential/single-ended control 0: Single-ended output (Only RECN output active, RECP output powered down), 1: RECN and RECP form differential outputs

† In power-off mode, the LS output biases are automatically switched off.

5.11.35 Address 33 - Transmit-Audio Path Configuration (TXCFG)

The TXCFG register is six bits wide and configures the transmit-audio path switches as listed in Table 5–29. The audio transmit path is automuted at the TXSUM functional block during the transmission of wideband data on RVC, when automuting is enabled with a 0 written to C5.2 (write address 4).

See Table 5–4 for write address 00 to configure different transmit modes using the last three bits in this register and the control bits in operational control word 1 (C1), write address 0.

Table 5–29. Transmit-Audio Path Configuration (TXCFG) Control

BIT	NAME	FUNCTION	
0	TXSW0	TX audio source. TXSW =	11: DTI 10: AMP2 select 01: AMP1 select 00: Mute
1	TXSW1		
2	CBSW	Compressor bypass	0: Compressor connected 1: Compressor bypassed
3	TXVEN	TX voice enable at TXSUM,	0 = Mute, 1 = enable
4	TXDEN	TX data enable at TXSUM,	0 = Mute, 1 = enable
5	TXSEN	TX SAT enable at TXSUM,	0 = Mute, 1 = enable

5.11.36 Address 34 - Microphone and TX DTMF Trim (VDTRIM)

The VDTRIM register is four bits wide and sets the VDTRIM stage gain for microphone and/or TX DTMF level trim as listed in Table 5–30.

Table 5–30. Microphone and TXDTMF Trim (VDTRIM) Adjust

VD3	VD2	VD1	VD0	NOMINAL GAIN (dB)
0	0	0	0	–4.30
0	0	0	1	–3.74
0	0	1	0	–3.20
0	0	1	1	–2.65
0	1	0	0	–2.12
0	1	0	1	–1.58
0	1	1	0	–1.06
0	1	1	1	–0.53
1	0	0	0	0
1	0	0	1	0.53
1	0	1	0	1.05
1	0	1	1	1.58
1	1	0	0	2.12
1	1	0	1	2.65
1	1	1	0	3.14
1	1	1	1	3.74

5.11.37 Address 35 - Limiter Trim (LIMITER)

The LIMITER register is four bits wide and sets the limiter deviation as listed in Table 5–31.

Table 5–31. Limiter Trim Adjust

LIM3	LIM2	LIM1	LIM0	DIFFERENCE FROM NOMINAL LIMIT LEVEL (dB)
0	0	0	0	−5
0	0	0	1	−4.5
0	0	1	0	−4
0	0	1	1	−3.5
0	1	0	0	−3
0	1	0	1	−2.5
0	1	1	0	−2
0	1	1	1	−1.5
1	0	0	0	−1
1	0	0	1	−0.5
1	0	1	0	0
1	0	1	1	0.5
1	1	0	0	1
1	1	0	1	1.5
1	1	1	0	2
1	1	1	1	2.5

5.11.38 Address 36 - Transmit SAT Trim (SAT TRIM)

The SAT TRIM register is four bits wide and sets the SAT TRIM gain as listed in Table 5–32.

Table 5–32. Transmit SAT TRIM Adjust

SAT3	SAT2	SAT1	SAT0	NOMINAL GAIN (dB)
0	0	0	0	−2.28
0	0	0	1	−1.97
0	0	1	0	−1.67
0	0	1	1	−1.36
0	1	0	0	−1.06
0	1	0	1	−0.76
0	1	1	0	−0.45
0	1	1	1	−0.15
1	0	0	0	0.15
1	0	0	1	0.45
1	0	1	0	0.76
1	0	1	1	1.06
1	1	0	0	1.36
1	1	0	1	1.67
1	1	1	0	1.97
1	1	1	1	2.29

5.11.39 Address 37 - Transmit Data Trim (TXDATRIM)

The TXDATRIM register is three bits wide and sets the TX data trim levels as listed in Table 5–33.

Table 5–33. Transmit Data Trim (TXDATRIM) Adjust

DAT2	DAT1	DAT0	NOMINAL GAIN (dB)
0	0	0	–2.28
0	0	1	–1.82
0	1	0	–1.21
0	1	1	–0.6
1	0	0	0
1	0	1	0.6
1	1	0	1.21
1	1	1	1.82

5.11.40 Address 38 - Transmit Trim (TXTRIM)

The TXTRIM register is five bits wide and sets the TXTRIM stage gain, the final stage in the TX path, as listed in Table 5–34.

Table 5–34. Transmit Trim (TXTRIM) Adjust

TXT4	TXT3	TXT2	TXT1	TXT0	NOMINAL GAIN (dB)
0	0	0	0	0	–4.37
0	0	0	0	1	–4.08
0	0	0	1	0	–3.8
0	0	0	1	1	–3.5
0	0	1	0	0	–3.24
0	0	1	0	1	–2.97
0	0	1	1	0	–2.7
0	0	1	1	1	–2.42
0	1	0	0	0	–2.15
0	1	0	0	1	–1.88
0	1	0	1	0	–1.61
0	1	0	1	1	–1.34
0	1	1	0	0	–1.07
0	1	1	0	1	–0.8
0	1	1	1	0	–0.54
0	1	1	1	1	–0.27
1	0	0	0	0	0
1	0	0	0	1	0.27
1	0	0	1	0	0.53
1	0	0	1	1	0.8
1	0	1	0	0	1.07
1	0	1	0	1	1.34
1	0	1	1	0	1.61
1	0	1	1	1	1.88
1	1	0	0	0	2.15
1	1	0	0	1	2.42
1	1	0	1	0	2.69
1	1	0	1	1	2.97
1	1	1	0	0	3.24
1	1	1	0	1	3.52
1	1	1	1	0	3.8
1	1	1	1	1	4.08

5.11.41 Address 39 - Receive Trim (RXTRIM)

The RXTRIM register is four bits wide and sets the RX TRIM stage gain as listed in Table 5–35.

Table 5–35. Receive Trim (RXTRIM) Adjust

RXT3	RXT2	RXT1	RXT0	NOMINAL GAIN (dB)
0	0	0	0	–4.3
0	0	0	1	–3.74
0	0	1	0	–3.2
0	0	1	1	–2.65
0	1	0	0	–2.12
0	1	0	1	–1.58
0	1	1	0	–1.06
0	1	1	1	–0.53
1	0	0	0	0
1	0	0	1	0.53
1	0	1	0	1.05
1	0	1	1	1.58
1	1	0	0	2.12
1	1	0	1	2.65
1	1	1	0	3.14
1	1	1	1	3.74

5.11.42 Address 3A - Loudspeaker Volume Control (VOL CTRL)

The VOL CTRL register is four bits wide and sets the loudspeaker volume as listed in Table 5–36.

Table 5–36. Loud Speaker Volume Control (VOL CTRL) Adjust

VOL3	VOL2	VOL1	VOL0	NOMINAL GAIN (dB)
0	0	0	0	–20
0	0	0	1	–17.5
0	0	1	0	–15
0	0	1	1	–12.5
0	1	0	0	–10
0	1	0	1	–7.5
0	1	1	0	–5
0	1	1	1	–2.5
1	0	0	0	0
1	0	0	1	2.5
1	0	1	0	5
1	0	1	1	7.5
1	1	0	0	10
1	1	0	1	12.5
1	1	1	0	15
1	1	1	1	17.5

5.11.43 Address 3B - DTMF Control (DTMFCTRL)

The DTMFCTRL register is six bits wide. Bits 0 through 4 select the DTMF generator output as listed in Table 5–37.

Table 5–37. DTMF Tone Output Control

KEY	DTMF4	DTMF3	DTMF2	DTMF1	DTMF0	LOW TONE (Hz)	HIGH TONE (Hz)
	0	0	0	0	0	697	1150
	0	0	0	0	1	770	1150
	0	0	0	1	0	852	1150
	0	0	0	1	1	941	1150
1	0	0	1	0	0	697	1209
4	0	0	1	0	1	770	1209
7	0	0	1	1	0	852	1209
*	0	0	1	1	1	941	1209
2	0	1	0	0	0	697	1336
5	0	1	0	0	1	770	1336
8	0	1	0	1	0	852	1336
0	0	1	0	1	1	941	1336
3	0	1	1	0	0	697	1477
6	0	1	1	0	1	770	1477
9	0	1	1	1	0	852	1477
#	0	1	1	1	1	941	1477
–	1	0	0	0	0	697	Off
–	1	0	0	0	1	770	Off
–	1	0	0	1	0	852	Off
–	1	0	0	1	1	941	Off
–	1	0	1	0	0	Off	1150
–	1	0	1	0	1	Off	1209
–	1	0	1	1	0	Off	1336
–	1	0	1	1	1	Off	1477
–	1	1	0	0	0	Off	1633
–	1	1	0	0	1	Off	2048
–	1	1	0	1	0	Off	Off
–	1	1	0	1	1	Off	Off
–	1	1	1	0	0	Off	Off
–	1	1	1	0	1	Off	Off
–	1	1	1	1	0	Off	Off
–	1	1	1	1	1	Off	Off

Bit 5 of DTMF Control and C1 (write address OOH) bits 0 and 1, select DTMF mode control. The levels of the DTMF tones and a 2-dB level skew between the high tones and low tones are set according to the control bits as listed in Table 5–38.

Table 5–38. DTMF Mode Control

CONTROL WORD 1 (WRITE ADDR 0) BIT 0	CONTROL WORD 1 (WRITE ADDR 0) BIT 1	DTMF CONTROL WORD (WRITE ADDR 3B) BIT 5 MODCTRL	SYSTEM	SIGNAL LEVEL AT DTO (3-V SUPPLY)	SIGNAL LEVEL AT DTO (3-V SUPPLY) BOTH TONES
TACS	WB	0	JTACS levels (skew off)	0.8 Vpp	1.6 Vpp
TACS	WB	1	ETACS levels (skew on)	0.756 Vpp low tones, 0.956 Vpp high tones	1.512-Vpp low tones, 1.912-Vpp high tones
TACS	NB	0	NTACS levels (skew off)	0.867 Vpp	1.734 Vpp
TACS	NB	1	Not allowed	–	–
AMPS	WB	0	AMPS levels (skew off)	1 Vpp	2 Vpp
AMPS	WB	1	Not allowed	–	–
AMPS	NB	0	NAMPS levels (skew off)	1 Vpp	2 Vpp
AMPS	NB	1	Not allowed	–	–

5.11.44 Address 3C - Analog Test Modes (ATEST)

To facilitate testing of the TCM8030, the REC1 and REC2 outputs can be reconfigured to observe internal analog signals. This register is reset to 0000 and should not be written to during normal operation.

5.11.45 Address 40 - DAC Range Select (DACRANGE)

The DACRANGE register is three bits wide and sets the range of each DAC (addresses 41 – 43) as listed in Table 5–39.

Each DAC can be independently set to full or half range. For full range, the step size is TXVDD/256 and for half range the step size is TXVDD/512. Register AUXPE at address 30, is used to independently power each DAC up or down. Each DAC has its own address to which the conversion word is written as described in the following paragraphs.

Table 5–39. DAC Range Select (DACRANGE) Definition

BIT	NAME	FUNCTION
0	DAC1X0	DAC1 range select. 0 = TXVDD/2, 1 = TXVDD
1	DAC2X1	DAC2 range select. 0 = TXVDD/2, 1 = TXVDD
2	DAC3X2	DAC3 range select. 0 = TXVDD/2, 1 = TXVDD

5.11.46 Address 41 - DAC1 Data (DAC1DAT)

This address is the input data register for the first DAC (DAC1).

5.11.47 Address 42 - DAC2 Data (DAC2DAT)

This address is the input data register for the second DAC (DAC2).

5.11.48 Address 43 - DAC3 Data (DAC3DAT)

This address is the input data register for the third DAC (DAC3).

5.11.49 Address 44 - AFC control (AFCCTRL)

The AFCCTRL register is five bits wide. The first four bits set the AFC cycle and the fifth bit, AFCSTART, starts an AFC measurement cycle as listed in Table 5–40.

Table 5–40. AFC Control

BIT	NAME	FUNCTION
0	AFCTERM0	AFCTERM (bits 3–0) = 4 bits set terminal count of AFC cycle
1	AFCTERM1	
2	AFCTERM2	
3	AFCTERM3	
4	AFCSTART	AFC start/stop. When AFCSTART = 1 start AFC count. When AFCSTART = 0 stop AFC count.

The AFC measurement cycle begins when the AFCSTART bit (bit 4) is set. When the TCXO count reaches the terminal value set by the AFCTERM (bits 0–3) bits, the count is stopped, the AFC event bit E2.7 (read address 06) is set, and when the AFC interrupt mask bit IE2.7 (write address 06) is set, an interrupt is generated. The microcontroller can then read the 20-bit terminal count of the IF–2 counter at AFCIF1, AFCIF2, and AFCIF3 (read addresses 43 to 45).

The start bit AFCSTART is reset automatically when the terminal value is reached. When AFCSTART is low, the counter is stopped and not reset. Reading the terminal count when AFCSTART is low resets the counters after the reading of AFCIF3. Reading the counters when AFCSTART is high does not reset the counters but because of the serial reading process the data may not be reliable.

NOTE:

IFAMP must be powered up with bit AUXPE.4 set (write address 30) before the AFC function can start.

5.12 Read Operation

For a read operation (see Figure 5–10), the $\overline{CS}$ transitions to low, data clocks into the DATAIN terminal on each rising edge of DCLK, and data clocks out of the DATAOUT terminal after each falling edge of DCLK. The input sequence is start bit (logic 0) followed by a 7 bit address write operation into DATAIN. After the input sequence, an output sequence follows with eight bits of a data read operation on DATAOUT.

The read address map, Table 5–41, details the TCM8030 read registers and their operation. Data is right justified.

Table 5–41. Read Address Map

HEXA-DECIMAL ADDRESS (7 BITS)	NAME	REGISTER NAME	FUNCTION	NUMBER OF SIGNIFICANT BITS
00	Status word 1	S1	Status word 1	7
01	Status word 2	S2	Status word 2	5
02 – 04	Not used			
05	Event register 1	E1	Event register 1	7
06	Event register 2	E2	Event register 2	8
07 – 0F	Not used			
10	RX data word 0	RXD0	RX bits 27 – 20	8
11	RX data word 1	RXD1	RX bits 19 – 12	8
12	RX data word 2	RXD2	RX bits 11 – 4	8
13	RX data word 3 (Bits 7 – 4)	RXD3	RX bits 3 – 0 and error correction status	8
14, 15	Not used			
16	PIO1 status word	PI1	State of PIO1 terminals	8
17	Not used			
18	PIO2 status word	PI2	State of PIO2 terminals	8
19	Not used			
1A	PIO3 status word	PI3	State of PIO3 terminals	4
1B – 21	Not used			
22	RX repeat count	RXRPT	Number of word repeats used for the majority voting - wideband	4
23, 24	Not used			
25	Narrowband error rate	NBERRS	Number of DSAT and SYNC bit errors in the last 200 received bits - narrowband	8
26 – 42	Not used			
43	AFC term count most significant byte	AFCIF1	Termination count of IF–2, most significant byte	8
44	AFC term count middle byte	AFCIF2	Termination count of IF–2, middle byte	8
45	AFC term count least significant byte	AFCIF3	Termination count of IF–2, least significant nibble	4

In the following descriptions for the read address registers, a bit position within a register is identified by prefixing the bit number with its register name. For example, bit 1 of event register 1 (read address 05) is identified as E1.1.

5.12.1 Address 00 - Status Word 1 Register (S1)

The S1 register is seven bits wide. It contains the status of the TCM8030 data processor. When the processor sets a bit to 1, it is in the state indicated in Table 5–42.

Table 5–42. Status Word 1 (S1) Definition

BIT	STATUS
0	RX data available
1	TX buffer available
2	Most recent TX aborted OR arbitration (wideband) failure
3	TX encoder active
4	RECC busy (not idle)
5	Counter/timer at zero state
6	Received wideband SAT /narrowband DSAT does not match the value defined in register C2. This bit is initially high during the first evaluation.

5.12.2 Address 01 - Status Word 2 Register (S2)

The S2 register is eight bits wide. It contains the status of the TCM8030 data processor. When the processor sets a bit to 1, it is in the state indicated in Table 5–43.

Table 5–43. Status Word 2 (S2) Definition

BIT	STATUS
0	Last two FOCC words differ
1	Not used
2	FVC message being received
3	FOCC in frame sync
4	RXRF idle mode power saving active
5	Not used
6	Not used
7	Not used

5.12.3 Address 05 - Event Register 1 (E1)

The E1 register is seven bits wide. It indicates the data processor status since the previous read of this register, as listed in Table 5–44.

Table 5–44. Event Register 1 (E1) Definition

BIT	STATUS SINCE PREVIOUS READ OF THIS WORD
0	RX data available
1	TX buffer available
2	Arbitration failure
3	TX sequence completed
4	Change of FOCC busy/idle status
5	Counter/timer reaches zero state
6	Wideband SAT/narrowband DSAT status changed. This always changes after the first evaluation.

These flags indicate which event(s) occurred since the previous reading, regardless of the associated interrupt control bits. A reading of this register can be performed independent of an interrupt. Event registers are cleared following a read. Since there are two event registers, the following protocol takes place:

1. The microcontroller addresses E1.
2. The INTRPT terminal transitions to inactive, the contents of both interrupt registers are transferred to buffers, and the registers are cleared and are then ready to catch new events.
3. The serial microcontroller interface clocks out the buffered event information.
4. Any new events are caught in the main interrupt register; however, at this time INTRPT remains inactive.
5. The microcontroller addresses E2.
6. The buffered E2 information, caught in step 2, is clocked out.
7. Once the read is completed, INTRPT becomes active if any interrupts occurred during steps 2 through 6. The event register now contains all the events that occurred during the read process.

NOTE:
Always read both E1 and then E2 in order. Reading only E1 results in the events being queued until E2 is eventually read. Also, see subsection 5.11.3 for INTRPT signal sensing.

5.12.4 Address 06 - Event Register 2 (E2)

The E2 register is eight bits wide. It indicates the data processor status since the previous read of this register, as listed in Table 5–45.

Table 5–45. Event Register 2 (E2) Definition

BIT	STATUS SINCE PREVIOUS READ OF THIS WORD
0	FOCC data changed value
1	FVC dotting detected - wideband
2	FVC frame sync achieved (wideband word sync/narrowband sync word)
3	Change of FOCC frame sync status
4	Change of RXRF idle mode power-saving status
5	NRZ error count register (NBERRS) updated - narrowband
6	PIO3 input port-sensed signal
7	AFC has reached terminal count

These flags indicate which event(s) have occurred since the previous read, regardless of their associated interrupt control bits. E2 can only be read after E1 because of the protocol for queuing and clearing events (see the description for address 05).

No priority for the events in registers E1 and E2, listed in Table 5–44 and Table 5–45, is handled inside the TCM8030. Interrupt priorities are handled in software.

5.12.5 Address 10 - RX Data Word 0 (RXD0)

This register contains the error-corrected received data bits 27 to 20 (bit 27 is MSB).

5.12.6 Address 11 - RX Data Word 1 (RXD1)

This register contains the error-corrected received data bits 19 to 12 (bit 19 is MSB).

5.12.7 Address 12 - RX Data Word 2 (RXD2)

This register contains the error-corrected received data bits 11 to 4 (bit 11 is MSB).

5.12.8 Address 13 - RX Data Word 3 (RXD3)

This register contains the error-corrected received data bits 3 to 0 and the error correction status as listed in Table 5–46.

Table 5–46. RX Data Word 3 (RXD3) Definition

BIT	STATUS
3 – 0	Received data decode status (see Table 5–46)
4	RX data bit 0
5	RX data bit 1
6	RX data bit 2
7	RX data bit 3

The received data error correction status is contained in bits 0 – 3, with 16 possible status conditions as listed in Table 5–47.

Table 5–47. RX Data Word 3 (RXD3) Error Correction Status Definition

RECEIVED DATA WORD 3				DECODE STATUS
BIT 3	BIT 2	BIT 1	BIT 0	
0	0	0	0	No errors detected
0	0	0	1	One error detected in parity bits
0	0	1	0	Two errors detailed in parity bits
0	0	1	1	Not used
0	1	0	0	One error corrected in data
0	1	0	1	One error corrected in data, one error detected in parity bits
0	1	1	0	Not used
0	1	1	1	Not used
1	0	0	0	Two errors corrected in data
1	0	0	1	Not used
1	0	1	0	Not used
1	0	1	1	Not used
1	1	0	0	More than two erasures† occurred - up to two data bits corrected.
1	1	0	1	More than two erasures† occurred - one error detected in parity bits and up to one data bit corrected.
1	1	1	0	More than two erasures† occurred - two errors in parity bits detected.
1	1	1	1	More than two errors detected - data not corrected.

† A bit erasure occurs when, over valid repeats, the bit is detected an equal number of times as a 1 and as a 0.

5.12.9 Addresses 16, 18, 1A - PIO Status Words (PI1, PI2, PI3)

These addresses monitor the states of PIO1, PIO2, and PIO3 terminals.

5.12.10 Address 22 - RX Repeat Count (RXRPT)- Wideband

The received repeat count gives the number of repeats of the received word that were actually used to generate the received data, using the bit-wise majority voting circuit.

5.12.11 Address 25 - Narrowband Error Rate (NBERRS)

This register is provided to assist in implementing the mobile reported interference function required by the NAMPS specification.

5.12.12 Address 43 - AFC Terminal Count MS Byte (AFCIF1)

This register contains the most significant byte (bits 12 –19 stored in locations 0–7) of the IF-2 counter in the AFC block.

5.12.13 Address 44 - AFC Terminal Count Middle Byte (AFCIF2)

This register contains the middle byte (bits 4–11 stored in locations 0 – 7) of the IF-2 counter in the AFC block.

5.12.14 Address 45 - AFC Terminal Count Lower Byte (AFCIF3)

This register contains the lower nibble (bits 0–3 stored in locations 4 –7 respectively) of the IF-2 counter in the AFC block as listed in Table 5–48.

Table 5–48. AFC Terminal Count Lower Byte (AFCIF3) Definition

BIT	STATUS
4	AFC, IF-2 counter bit 0
5	AFC, IF-2 counter bit 1
6	AFC, IF-2 counter bit 2
7	AFC, IF-2 counter bit 3

The AFC terminal counter should be read MS byte first and LS nibble last. After you read the LS nibble, both the TCXO counter and the AFC counter are automatically reset.

5.13 Event Register 1 (E1) Status Definitions

Event register 1 contains events as defined in the following sections.

5.13.1 RX data available (E1 bit 1)

The *RX data available* event status is generated when received data is available within the RX data buffer (RXD0 – RXD3) read addresses 10 – 13, respectively.

5.13.2 TX buffer available (E1 bit 1)

The *TX buffer available* event status is generated after the first repeat of data during the transmission burst on either the RECC or RVC. This signals that the TX data buffer is available to write to (TXD0 – TXD4) write addresses 10 – 14, respectively. This status can be used for multiple word transmission on either the RECC or RVC.

5.13.3 Arbitration failure (E1 bit 2)

The *arbitration failure* event status is generated when an idle-to-busy transition within the FOCC occurs before or after the busy/idle transition window frame. This indicates that the RECC was not seized correctly and therefore the transmission requires termination.

5.13.4 TX sequence complete (E1 bit 3)

The *TX sequence complete* event status is generated upon completion of the transmission burst on either the RECC or RVC.

5.13.5 Change of FOCC busy/idle (E1 bit 4)

The *change of the FOCC busy/idle* event status is generated whenever a busy-to-idle or an idle-to-busy transition occurs on the FOCC.

5.13.6 Counter/timer reaches zero state (E1 bit 5)

The *counter/timer reaches zero state* event status is generated whenever the TCM8030 counter/timer reaches zero.

5.13.7 Wideband SAT/Narrowband DSAT changed (E1 bit 6)

In wideband mode, the *SAT changed* event status is generated whenever the SAT reception block receives an input frequency that is not in the expected band. See subsection 5.11.2.2 for additional details.

In narrowband mode, the *DSAT changed* event status is generated whenever the DSAT reception block receives a DSAT color code that is different than the prior DSCC. In addition, the event status is also generated after the first evaluation. See subsection 5.11.2.4 for additional details.

5.14 Event Register 2 (E2) Status Definitions

Event register 2 contains events as defined in the following sections.

5.14.1 FOCC data changed value (E2 bit 0)

The *FOCC data changed value* event status is generated whenever the RX data received on the FOCC is different from the previous data received.

5.14.2 FVC dotting detected – wideband (E2 bit 1)

The *FVC dotting detected* event status is generated whenever the RX data received on the FVC indicates a dotting sequence.

5.14.3 FVC Frame Sync achieved (E2 bit 2)

The *FVC frame sync achieved* event status is generated when the first word-sync pattern is encountered during a FVC message stream. When this occurs, SYNC (terminal 25) transitions to high in FVC mode (C1.2=1, write address 00) while a message is being received.

5.14.4 Change in Frame Sync (E2 bit 3)

The *change in frame sync* event status is generated after the second consecutive word-sync pattern is encountered during a FOCC message stream. In addition, the event status is also generated if the number of expected word syncs missed (indicated in FRAMEMIS, write address 22) occurs. When this event status is generated, SYNC (terminal 25) transitions to high in FOCC mode (C1.2=0, write address 00) while the data processor syncs with the control channel.

5.14.5 Change of RXRF idle mode power savings (E2 bit 4)

The *change of RXRF idle mode power savings* event status is generated for MCU idle mode processing as indicated in the following paragraphs.

The idle mode processing feature is an addition to the RXRF idle mode. It allows the use of microcontroller power-saving modes. The operation masks out the *RX data available* event by writing 0 to IE1.0 (write address 05) and writing 1 to the *FOCC data changed value* event (IE2.0, write address 06).

The TCM8030 only generates an interrupt when the received word changes from its previous value. This means that no interrupt is generated (after the first word) during the reception of a stream of words that are the same. This extended time between interrupts allows that microcontroller to spend more time in sleep mode.

A typical time to use this message as a power-saving feature is after the reception of a control filler message (CFM). Typically, several control filler messages are received so the microcontroller can start the idle mode process and then go to sleep.

No interpretation of messages is performed, however. The interrupt is generated based on a bit-for-bit comparison of the current word and the previous one. Continuously repeated single words are supported; however, repeated multiword messages are not.

5.14.6 NRZ error count register (NBERRS) updated (E2 bit 5)

The *NRZ error count register updated* event status is generated for the mobile reported interference operation as indicated in the following paragraphs.

In the mobile reported interference operation, the NBERRS contains the total errors detected in the 200 NRZ bits of DSAT and SYNC WORD, received as of the latest NBERRS update. The NBERRS register is updated every 100 received NRZ bits. At the same time as this update, the event status is generated. If the interrupt enable (IE2.5, write address 06) was set, then an external interrupt is generated on INTRPT (terminal 2). The microcontroller then reads the NBERRS register (read address 25) to determine the error rate over the last 200 received NRZ bits.

While SYNC WORD is being received, the DSAT error-checking function produces a large number of errors. These errors are eliminated automatically (subtracted out) once the whole word is successfully received. The error registers are then incremented by the number of SYNC WORD errors. When a data word is completely received, it is assumed that the DSAT signal continues uninterrupted. That is, during data reception, the DSAT generator's phase advances every NRZ clock cycle even though DSAT does not output a signal.

Error counting begins when the TCM8030 receives 24 bits of NRZ data. The total error count in these 24 bits determines the DSAT status; however, the NBERRS error counting mechanism only considers the 24th bit. After this initialization period, the error counting mechanism always functions regardless of DSAT status. For example, if the DSAT status becomes invalid, then the DSAT generator maintains its original phase and continues to perform error accumulation on each bit as it is received. It is only after 670 ms (the time taken to generate a SYNC WORD, DATA WORD, and 24 bits of DSAT) that the DSAT generator phase rotates to find a best fit with the received data. Having found the best fit, the received bit tests itself against the reference bit to see if the error count needs to be incremented.

The rest of the MRI function must occur in the software. This consists of comparing the narrowband error rate with the threshold that is communicated through a control message to the mobile station. If this threshold is exceeded, an MRI order is generated from the mobile station to the base station over the RVC.

This means that the microcontroller must:

1. Read the NBERRS register (after an NBERRS update interrupt).
2. If required, integrate many NBERRS readings over time to get an averaged result.
3. Determine when the error rate goes above the threshold.
4. If the threshold is exceeded, generate an MRI order on the RVC by sending a correct data word to the TCM8030.

The MRI circuit always operates on FVC in narrowband mode. MRI interrupts are enabled or disabled by setting or resetting the interrupt enable bit (IE2.5, write address 06). Therefore, the TCM8030 does not provide an MRI start/stop bit. The NBERRS count reinitializes when the narrowband mode (C1.1, write address 00) and FVC (C1.2, write address 00) bits change from any other state to 11. As a result, no MRI clear bit is provided.

5.14.7 PIO3 input port sensed signal (E2 bit 6)

The *PIO3 input port sensed signal* event status is generated whenever one of the PIO3 ports, configured as an input for interrupt generation, is sensed. See subsection 5.11.23 for additional details.

5.14.8 AFC has reached terminal count (E2 bit 7)

The *AFC has reached terminal count* event status is generated when the AFC counter reaches the AFC terminal count. Following this, the TCM8030 writes the terminal count to the 20–bit AFC terminal registers (AFCIF1, AFCIF2, and AFCIF3; read addresses 43 – 45, respectively).

TCM8030,

Device Status: Preview

Description

The TCM8030 baseband processor for analog cellular telephones provides all the baseband signal processing required for any of the following standards for mobile and hand-portable cellular telephones: advanced mobile telephone service (AMPS); extended advanced mobile telephone service (EAMPS); narrowband advanced mobile telephone service (NAMPS); total access communication system (TACS); extended total access communication system (ETACS); Japanese total access communication system (JTACS), and narrowband total access communications system (NTACS).

The analog section of the TCM8030 performs all filtering required for the speech, data, supervisory audio tone (SAT), and signaling tone (ST) paths. It has an integrated, International Telegraph and Telephone Consultative Committee (CCITT) compatible compandor as well as microphone preamplifiers and a differential, 32-W earpiece driver to complete the full integration of the baseband audio signal paths. The digital section of the device implements the data transceiving, data processing, and SAT functions including data recovery, majority voting, Bose-Chaudhuri-Hocquenghem (BCH) decoding, BCH encoding, transmission (TX) frame assembly, and SAT generation, detection, and regeneration. The TCM8030 supports both narrowband standards, NTACS and NAMPS, with full implementation of the narrowband data, and digital supervisory audio tone (DSAT) and

digital signaling tone (DST) filtering and processing functions.

An on-chip, automatic frequency control (AFC) circuit also facilitates narrowband operation. Communication with the microcontroller is through a simple four-wire serial interface. In addition to these basic signal processing requirements, the TCM8030 integrates many of the ancillary functions required in a typical FM cellular telephone. Included are three 8-bit digital-to-analog converters (DACs), a dual-tone multiple-frequency (DTMF) generator, an 8-bit programmable counter/timer, an independent watchdog timer, two 8-bit microcontroller expansion ports, and a 4-bit keyboard interrupt port. Clock operation is through a pin-selectable on-chip crystal-referenced oscillator, an external clock source, or an external temperature-controlled crystal oscillator (TCXO).

The TCM8030 is designed for ultra low-power applications and is manufactured using a low-power complementary metal-oxide semiconductor (CMOS) process. It operates from a single 2.7-V to 5.5-V supply and has five power-saving modes in addition to normal operation. The TCM8030 also features a total power-down mode in which the TCM8030 waits for the user to press the power-on key located on the telephone keyboard. Also implemented are two features that extend idle mode operation time. One feature enables a reduction in the duty cycle of the microcontroller, and the other periodically shuts down the RF receiver. These features reduce the system power consumption to a minimum during idle mode and significantly increase the telephone standby time.

The gain and signal selection paths are software configurable so that audio trimming functions do not require manual intervention during telephone calibration on the production line. This production time reduction feature, together with its high level of integration and low power design, makes the TCM8030 an ideal solution for FM analog cellular telephones.

Features

- Data Processing Features
  The TCM8030 Provides Data Transceiver, Data Processing, and SAT Functions, and Includes the Following Data Processing Features:
  - Single-Chip Processing for AMPS, NAMPS, TACS, ETACS, NTACS, JTACS, SAT, and DSAT
  - 2.7-V to 5.5-V Operation
  - Serial Interface
  - User-Configurable Interrupt Structure
  - Transmit (TX) and Receive (RX) Data Buffers
  - Integrated RX and TX Data Filters
  - TX Wideband (WB) SAT Filter
  - RX WB and Narrowband (NB) SAT Filters

    - RX WB and NB Data Comparator
    - Programmable Timer
    - Independent Watchdog Timer
    - RX/TX Automatic Mute Functions
    - Arbitration Processing
    - Twenty Programmable Expansion I/O Ports
    - WB and NB-RX Recovery
    - Automatic Frequency Control (AFC)
    - Multiple Power Saving Mode Implementation
    - Separate Encoder for WB-TX and NB-TX
- Audio Processing Features
  The TCM8030 provides the following audio processing features:
  AMPS, NAMPS, TACS, ETACS, NTACS, and JTACS operation
    - Integrated RX and TX Voice Filters
    - Microphone Amplifiers and Loud Speaker Drivers
    - Pre-Emphasis and De-Emphasis Filtering
    - Digitally Controlled Gains and Signal Selection or Muting
    - Adjustable TX Limiter
    - Three 8-Bit Digital-to-Analog Converters (DAC) with Output Buffers
    - Dual-Tone Multifrequency (DTMF) Generator
    - On-Chip Compandor
    - Flexible Clock and Oscillator Operation

To view the following documents, Acrobat Reader 3.x is required.
To download a document to your hard drive, right-click on the link and choose 'Save'.

Datasheets

Full datasheet in Acrobat PDF: slws033a.pdf (568 KB)
Full datasheet in Zipped PostScript: slws033a.psz (417 KB)

Pricing/Samples/Availability

Orderable Device	Package	Pins	Temp (ºC)	Status	Price/unit USD (100-999)	Pack Qty	Availability / Samples
TCM8030		0		PREVIEW			Check stock or order
TCM8030PN	PN	80		PREVIEW			Check stock or order

Application Reports

- MicroStar BGA Packaging Reference Guide (SSYZ015A, 1110 KB - Updated: 07/12/1999)

User Manuals

- Analog Baseband Processor User's Guide (SLWU002 - Updated: 07/16/1997)

Table Data Updated on: 9/14/2000