TL071, TL071A, TL071B, TL071H
TL072, TL072A, TL072B, TL072H, TL072M
TL074, TL074A, TL074B, TL074H, TL074M
SLOS080V – SEPTEMBER 1978 – REVISED APRIL 2023

TL07xx Low-Noise FET-Input Operational Amplifiers

1 Features

- High slew rate: 20 V/µs (TL07xH, typ)
- Low offset voltage: 1 mV (TL07xH, typ)
- Low offset voltage drift: 2 µV/°C
- Low power consumption: 940 µA/ch (TL07xH, typ)
- Wide common-mode and differential voltage ranges
  - Common-mode input voltage range includes V_{CC+}
- Low input bias and offset currents
- Low noise: V_n = 18 nV/√Hz (typ) at f = 1 kHz
- Output short-circuit protection
- Low total harmonic distortion: 0.003% (typ)
- Wide supply voltage: ±2.25 V to ±20 V, 4.5 V to 40 V

2 Applications

- Solar energy: string and central inverter
- Motor drives: AC and servo drive control and power stage modules
- Single phase online UPS
- Three phase UPS
- Pro audio mixers
- Battery test equipment

3 Description

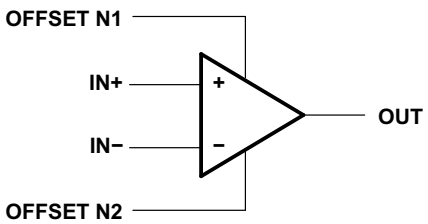
The TL07xH (TL071H, TL072H, and TL074H) family of devices are the next-generation versions of the industry-standard TL07x (TL071, TL072, and TL074) devices. These devices provide outstanding value for cost-sensitive applications, with features including low offset (1 mV, typical), high slew rate (20 V/µs), and common-mode input to the positive supply. High ESD (1.5 kV, HBM), integrated EMI and RF filters, and operation across the full –40°C to 125°C enable the TL07xH devices to be used in the most rugged and demanding applications.

Package Information

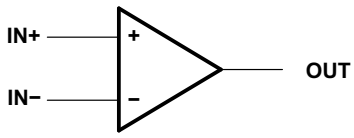
PART NUMBER(1)	PACKAGE	BODY SIZE (NOM)
TL071x	P (PDIP, 8)	9.59 mm × 6.35 mm
	DCK (SC70, 5)	2.00 mm × 1.25 mm
	PS (SO, 8)	6.20 mm × 5.30 mm
	D (SOIC, 8)	4.90 mm × 3.90 mm
	DBV (SOT-23, 5)	1.60 mm × 1.20 mm
TL072x	P (PDIP, 8)	9.59 mm × 6.35 mm
	PS (SO, 8)	6.20 mm × 5.30 mm
	D (SOIC, 8)	4.90 mm × 3.90 mm
	P (SOT-23, 8)	2.90 mm × 1.60 mm
	PW (TSSOP, 8)	4.40 mm × 3.00 mm
TL072M	JG (CDIP , 8)	9.59 mm × 6.67 mm
	W (CFP, 10)	6.12 mm × 3.56 mm
	FK (LCCC, 20)	8.89 mm × 8.89 mm
TL074x	N (PDIP, 14)	19.30 mm × 6.35 mm
	NS (SO, 14)	10.30 mm × 5.30 mm
	D (SOIC, 14)	8.65 mm × 3.91 mm
	DYY (SOT-23, 14)	4.20 mm × 2.00 mm
	DB (SSOP, 14)	6.20 mm × 5.30 mm
	PW (TSSOP, 14)	5.00 mm × 4.40 mm
TL074M	J (CDIP, 14)	19.56 mm × 6.92 mm
	W (CFP, 14)	9.21 mm × 6.29 mm
	FK (LCCC, 20)	8.89 mm × 8.89 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

TL071



TL072 (each amplifier)
TL074 (each amplifier)



Logic Symbols

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision U (December 2022) to Revision V (April 2023)	Page
• Updated *Overview*, *Functional Block Diagram*, and *Feature Description* sections	32

Changes from Revision T (December 2021) to Revision U (December 2022)	Page
• Changed *Absolute Maximum Ratings, ESD Ratings, Recommended Operating Conditions, and Thermal Information* sections by merging TL07xH and TL07xx specifications	12
• Changed *Electrical Characteristics* tables by merging TL07xC, TL07xAC, TL07xBC, TL07xI, and TL07xM specifications	17
• Changed gain bandwidth value of all non-NS/non-PS packages and non-TL07xM devices from 3 MHz to 5.25 MHz	17
• Changed TL07xC, TL07xAC, TL07xBC, TL07xI, and TL07xM *Switching Characteristics* tables by renaming to *Electrical Characteristics (AC)*	19
• Changed input voltage noise density at 1 kHz for all non-PS/non-NS packages and all non-TL07xM devices to 37 nV/$\sqrt{\text{Hz}}$	19
• Changed THD+N for all non-PS/non-NS packages and all non-TL07xM devices to 0.00012%	19

Changes from Revision S (July 2021) to Revision T (December 2021)	Page
• Corrected DCK pinout diagram and table in *Pin Configurations and Functions* section	5

Changes from Revision R (June 2021) to Revision S (July 2021)	Page
• Deleted preview note from TL071H SOIC (8), SOT-23 (5) and SC70 (5) packages throughout the data sheet	1

Changes from Revision Q (June 2021) to Revision R (June 2021)	Page
• Deleted preview note from TL072H SOIC (8), SOT-23 (8) and TSSOP (8) packages throughout the data sheet	1

- Added ESD information for TL072H 12
- Added I_Q spec for TL072H 15

Changes from Revision P (November 2020) to Revision Q (June 2021) **Page**

- Deleted VSSOP (8) package from the *Device Information* section 1
- Added DBV, DCK, and D Package,s to TL071H in *Pin Configuration and Functions* section 5
- Deleted DGK Package, from TL072x in *Pin Configuration and Functions* section 5
- Deleted tables with duplicate information from the *Specifications* section 12
- Added D, DCK, and DBV package thermal information in Thermal Information for Single Channel: TL071H section 13
- Added D, DDF, and PW package thermal information in Thermal Information for Dual Channel: TL072H section 13
- Added I_B and I_{OS} specification for single channel DCK and DBV package 15
- Added I_Q spec for TL071H 15
- Deleted *Related Links* section from the *Device and Documentation Support* section 38

Changes from Revision O (October 2020) to Revision P (November 2020) **Page**

- Added SOIC and TSSOP package thermal information in *Thermal Information for Quad Channel: TL074H section* 14
- Added *Typical Characteristics:TL07xH* section in *Specifications* section 20

Changes from Revision N (July 2017) to Revision O (October 2020) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document 1
- Features of TL07xH added to the *Features* section 1
- Added link to applications in the *Applications* section 1
- Added TL07xH in the *Description* section 1
- Added TL07xH device in the *Device Information* section 1
- Added SOT-23 (14), VSSOP (8), SOT-23 (8), SC70 (5), and SOT-23 (5) packages to the *Device Information* section 1
- Added TSSOP, VSSOP and DDF Package,s to TL072x in *Pin Configuration and Functions* section 5
- Added DYY Package, to TL074x in *Pin Configuration and Functions* section 5
- Removed Table of Graphs from the *Typical Characteistics* section 27
- Deleted reference to obsolete documentation in *Layout Guidelines* section 36
- Removed *Related Documentation* section 38

Changes from Revision M (February 2014) to Revision N (July 2017) **Page**

- Updated data sheet text to latest documentation and translation standards 1
- Added TL072M and TL074M devices to data sheet 1
- Rewrote text in *Description* section 1
- Changed TL07x 8-pin PDIP package to 8-pin CDIP package in *Device Information* table 1
- Deleted 20-pin LCCC package from *Device Information* table 1
- Added 2017 copyright statement to front page schematic 1
- Deleted TL071x FK (LCCC) pinout drawing and pinout table in *Pin Configurations and Functions* section 5
- Updated pinout diagrams and pinout tables in *Pin Configurations and Functions* section 5
- Added Figure 6-59 to *Typical Characteristics* section 27
- Added second *Typical Application* section application curves 34
- Changed document references in *Layout Guidelines* section 36

Changes from Revision L (February 2014) to Revision M (February 2014) **Page**

- Added *Device Information* table, *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section..... 1

5 Pin Configuration and Functions

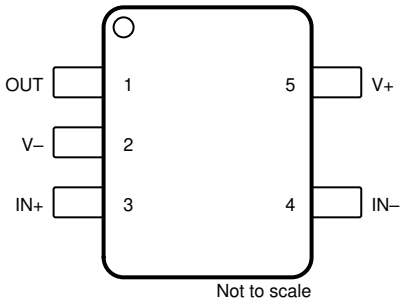


Figure 5-1. TL071H DBV Package, 5-Pin SOT-23 (Top View)

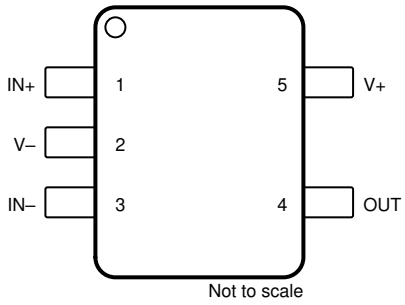
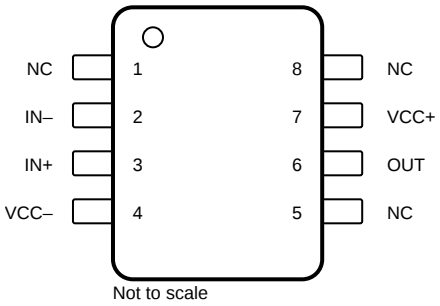


Figure 5-2. TL071H DCK Package, 5-Pin SC70 (Top View)

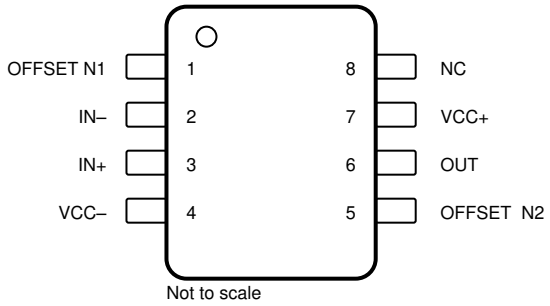


NC- no internal connection

Figure 5-3. TL071H D Package, 8-Pin SOIC (Top View)

Table 5-1. Pin Functions: TL071H

PIN				I/O	DESCRIPTION
NAME	DBV	DCK	D		
IN–	4	3	2	I	Inverting input
IN+	3	1	3	I	Noninverting input
NC	—	—	8	—	Do not connect
NC	—	—	1	—	Do not connect
NC	—	—	5	—	Do not connect
OUT	1	4	6	O	Output
VCC–	2	2	4	—	Power supply
VCC+	5	5	7	—	Power supply



NC- no internal connection

Figure 5-4. TL071x D, P, and PS Package, 8-Pin SOIC, PDIP, and SO (Top View)

Table 5-2. Pin Functions: TL071x

PIN		I/O	DESCRIPTION
NAME	NO.		
IN–	2	I	Inverting input
IN+	3	I	Noninverting input
NC	8	—	Do not connect
OFFSET N1	1	—	Input offset adjustment
OFFSET N2	5	—	Input offset adjustment
OUT	6	O	Output
VCC–	4	—	Power supply
VCC+	7	—	Power supply

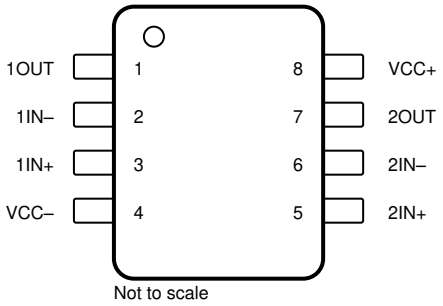
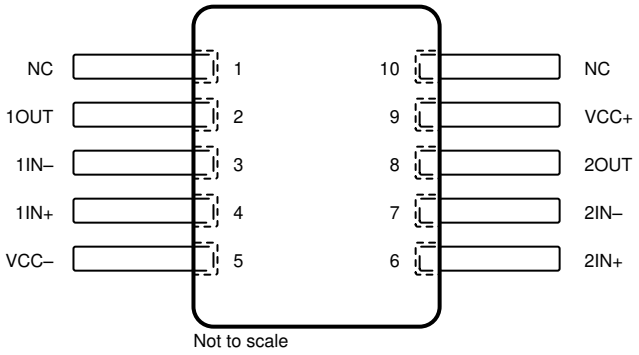


Figure 5-5. TL072x D, DDF, JG, P, PS, and PW Package, 8-Pin SOIC, SOT-23, CDIP, PDIP, SO, and TSSOP (Top View)

Table 5-3. Pin Functions: TL072x

PIN		I/O	DESCRIPTION
NAME	NO.		
1IN–	2	I	Inverting input
1IN+	3	I	Noninverting input
1OUT	1	O	Output
2IN–	6	I	Inverting input
2IN+	5	I	Noninverting input
2OUT	7	O	Output
VCC–	4	—	Power supply
VCC+	8	—	Power supply

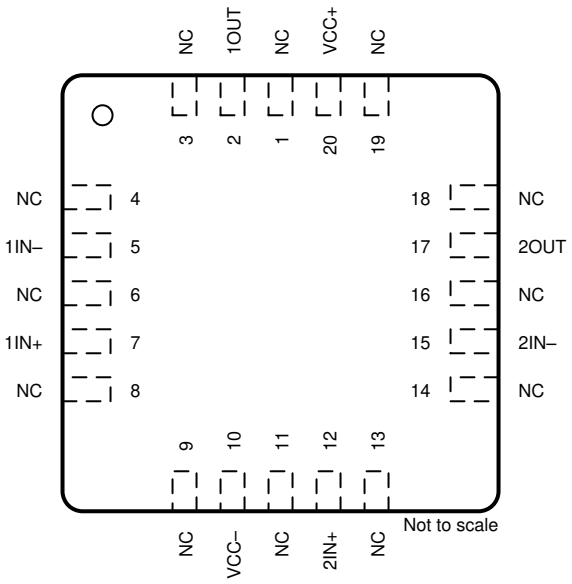


NC- no internal connection

Figure 5-6. TL072x U Package, 10-Pin CFP (Top View)

Table 5-4. Pin Functions: TL072x

PIN		I/O	DESCRIPTION
NAME	NO.		
1IN–	3	I	Inverting input
1IN+	4	I	Noninverting input
1OUT	2	O	Output
2IN–	7	I	Inverting input
2IN+	6	I	Noninverting input
2OUT	8	O	Output
NC	1, 10	—	Do not connect
VCC–	5	—	Power supply
VCC+	9	—	Power supply



NC- no internal connection

Figure 5-7. TL072 FK Package, 20-Pin LCCC (Top View)

Table 5-5. Pin Functions: TL072x

PIN		I/O	DESCRIPTION
NAME	NO.		
1IN–	5	I	Inverting input
1IN+	7	I	Noninverting input
1OUT	2	O	Output
2IN–	15	I	Inverting input
2IN+	12	I	Noninverting input
2OUT	17	O	Output
NC	1, 3, 4, 6, 8, 9, 11, 13, 14, 16, 18, 19	—	Do not connect
VCC–	10	—	Power supply
VCC+	20	—	Power supply

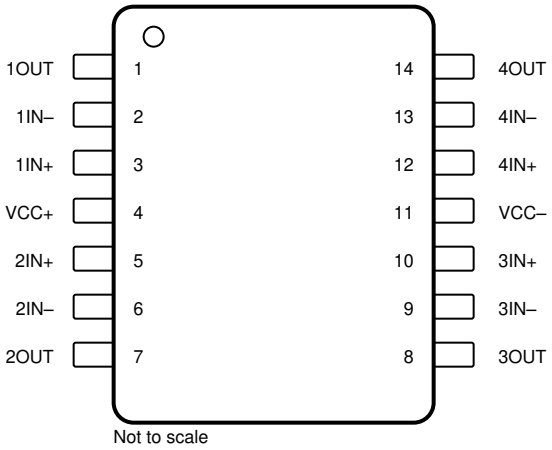
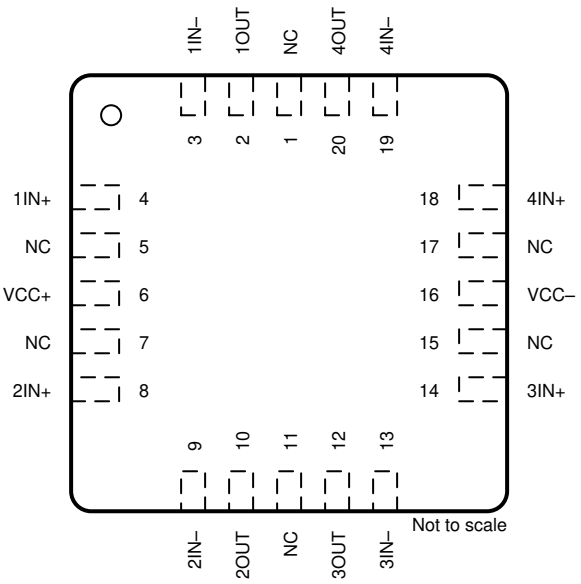


Figure 5-8. TL074x D, N, NS, PW, J, DYY, and W Package, 14-Pin SOIC, PDIP, SO, TSSOP, CDIP, SOT-23, and CFP (Top View)

Table 5-6. Pin Functions: TL074x

PIN		I/O	DESCRIPTION
NAME	NO.		
1IN–	2	I	Inverting input
1IN+	3	I	Noninverting input
1OUT	1	O	Output
2IN–	6	I	Inverting input
2IN+	5	I	Noninverting input
2OUT	7	O	Output
3IN–	9	I	Inverting input
3IN+	10	I	Noninverting input
3OUT	8	O	Output
4IN–	13	I	Inverting input
4IN+	12	I	Noninverting input
4OUT	14	O	Output
$V_{CC–}$	11	—	Power supply
V_{CC+}	4	—	Power supply



NC- no internal connection

Figure 5-9. TL074 FK Package, 20-Pin LCCC (Top View)

Table 5-7. Pin Functions: TL074x

PIN		I/O	DESCRIPTION
NAME	NO.		
1IN–	3	I	Inverting input
1IN+	4	I	Noninverting input
1OUT	2	O	Output
2IN–	9	I	Inverting input
2IN+	8	I	Noninverting input
2OUT	10	O	Output
3IN–	13	I	Inverting input
3IN+	14	I	Noninverting input
3OUT	12	O	Output
4IN–	19	I	Inverting input
4IN+	18	I	Noninverting input
4OUT	20	O	Output
NC	1, 5, 7, 11, 15, 17	—	Do not connect
VCC–	16	—	Power supply
VCC+	6	—	Power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)		All NS and PS packages; All TL07xM devices	–0.3	36	V
		All other devices	0	42	V
Signal input pins	Common-mode voltage (3)	All NS and PS packages; All TL07xM devices	(V–) – 0.3	(V–) + 36	V
		All other devices	(V–) – 0.5	(V+) + 0.5	V
	Differential voltage (3)	All NS and PS packages; All TL07xM devices (4)	(V–) – 0.3	(V–) + 36	V
		All other devices		V_S + 0.2	V
	Current (3)	All NS and PS packages; All TL07xM devices		50	mA
		All other devices	–10	10	mA
Output short-circuit (2)			Continuous		
Operating ambient temperature, T_A			–55	150	°C
Junction temperature, T_J				150	°C
Case temperature for 60 seconds - FK package				260	°C
Lead temperature 1.8 mm (1/16 inch) from case for 10 seconds				300	°C
Storage temperature, T_{stg}			–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to ground, one amplifier per package.
(3) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
(4) Differential voltage only limited by input voltage.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_S	Supply voltage, (V+) – (V–)	All NS and PS packages; All TL07xM devices(1)	10	30	V
		All other devices	4.5	40	V
V_I	Input voltage range	All NS and PS packages; All TL07xM devices	(V–) + 2	(V+) + 0.1	V
		All other devices	(V–) + 4	(V+) + 0.1	V
T_A	Specified temperature	TL07xM	–55	125	°C
		TL07xH	–40	125	°C
		TL07xI	–40	85	°C
		TL07xC	0	70	°C

(1) V+ and V– are not required to be of equal magnitude, provided that the total V_S (V+ – V–) is between 10 V and 30 V.

6.4 Thermal Information for Single Channel

THERMAL METRIC (1)		TL071xx					UNIT
		D (SOIC)	DCK (SC70)	DBV (SOT-23)	P (PDIP)	PS (SO)	
		8 PINS	5 PINS	5 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	158.8	217.5	212.2	85	95	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	98.6	113.1	111.1	–	–	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	102.3	63.8	79.4	–	–	°C/W
ψ_{JT}	Junction-to-top characterization parameter	45.8	34.8	51.8	–	–	°C/W
ψ_{JB}	Junction-to-board characterization parameter	101.5	63.5	79.0	–	–	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Thermal Information for Dual Channel

THERMAL METRIC (1)		TL072xx								UNIT
		D (SOIC)	DDF (SOT-23)	FK (LCCC)	JG (CDIP)	P (PDIP)	PS (SO)	PW (TSSOP)	U (CFP)	
		8 PINS	8 PINS	20 PINS	8 PINS	8 PINS	8 PINS	8 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	147.8	181.5	–	–	85	95	200.3	169.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	88.2	112.5	5.61	15.05	–	–	89.4	62.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	91.4	98.2	–	–	–	–	131.0	176.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	36.8	17.2	–	–	–	–	22.2	48.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	90.6	97.6	–	–	–	–	129.3	144.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	–	–	–	–	N/A	5.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.6 Thermal Information for Quad Channel

THERMAL METRIC (1)		TL074xx								UNIT
		D (SOIC)	DYY (SOT-23)	FK (TSSOP)	J (TSSOP)	N (TSSOP)	NS (TSSOP)	PW (TSSOP)	W (TSSOP)	
		14 PINS	14 PINS	20 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	114.2	153.2	–	–	80	76	–	128.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	70.3	88.7	5.61	14.5	–	–	14.5	56.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	70.2	65.4	–	–	–	–	–	127.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	28.8	9.5	–	–	–	–	–	29	°C/W
ψ_{JB}	Junction-to-board characterization parameter	69.8	65.0	–	–	–	–	–	106.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	–	–	–	–	–	0.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.7 Electrical Characteristics: TL07xH

For $V_S = (V_{CC+}) – (V_{CC–}) = 4.5$ V to 40 V (±2.25 V to ±20 V) at $T_A = 25°C$, $R_L = 10$ kΩ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{O\ UT} = V_S / 2$, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±1	±4	mV
			T_A = –40°C to 125°C			±5	
dV_{OS}/dT	Input offset voltage drift		T_A = –40°C to 125°C		±2		µV/°C
PSRR	Input offset voltage versus power supply	V_S = 5 V to 40 V, $V_{CM} = V_S / 2$	T_A = –40°C to 125°C		±1	±10	µV/V
	Channel separation	f = 0 Hz			10		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±1	±120	pA
			DCK and DBV packages		±1	±300	pA
			T_A = –40°C to 125°C (1)			±5	nA
I_{OS}	Input offset current				±0.5	±120	pA
			DCK and DBV packages		±0.5	±250	pA
			T_A = –40°C to 125°C (1)			±5	nA
NOISE							
E_N	Input voltage noise	f = 0.1 Hz to 10 Hz			9.2		μV_{PP}
					1.4		μV_{RMS}
e_N	Input voltage noise density	f = 1 kHz			37		$nV/\sqrt{Hz}$
		f = 10 kHz			21		
i_N	Input current noise	f = 1 kHz			80		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range			$(V_{CC–}) + 1.5$		(V_{CC+})	V
CMRR	Common-mode rejection ratio	V_S = 40 V, $(V_{CC–}) + 2.5$ V < V_{CM} < $(V_{CC+}) – 1.5$ V		100	105		dB
			T_A = –40°C to 125°C	95			dB
		V_S = 40 V, $(V_{CC–}) + 2.5$ V < V_{CM} < (V_{CC+})		90	105		dB
			T_A = –40°C to 125°C	80			dB
INPUT CAPACITANCE							
Z_{ID}	Differential				100 || 2		MΩ || pF
Z_{ICM}	Common-mode				6 || 1		TΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = 40 V, $V_{CM} = V_S / 2$, $(V_{CC–}) + 0.3$ V < V_O < $(V_{CC+}) – 0.3$ V	T_A = –40°C to 125°C	118	125		dB
A_{OL}	Open-loop voltage gain	V_S = 40 V, $V_{CM} = V_S / 2$, R_L = 2 kΩ, $(V_{CC–}) + 1.2$ V < V_O < $(V_{CC+}) – 1.2$ V	T_A = –40°C to 125°C	115	120		dB
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product				5.25		MHz
SR	Slew rate	V_S = 40 V, G = +1, C_L = 20 pF			20		V/µs
t_S	Settling time	To 0.1%, V_S = 40 V, V_{STEP} = 10 V , G = +1, CL = 20 pF			0.63		µs
		To 0.1%, V_S = 40 V, V_{STEP} = 2 V , G = +1, CL = 20 pF			0.56		
		To 0.01%, V_S = 40 V, V_{STEP} = 10 V , G = +1, CL = 20 pF			0.91		
		To 0.01%, V_S = 40 V, V_{STEP} = 2 V , G = +1, CL = 20 pF			0.48		
	Phase margin	G = +1, R_L = 10 kΩ, C_L = 20 pF			56		°
	Overload recovery time	V_{IN} × gain > V_S			300		ns
THD+N	Total harmonic distortion + noise	V_S = 40 V, V_O = 6 V_{RMS}, G = +1, f = 1 kHz			0.00012		%
EMIRR	EMI rejection ratio	f = 1 GHz			53		dB
OUTPUT							

6.7 Electrical Characteristics: TL07xH (continued)

For $V_S = (V_{CC+}) – (V_{CC–}) = 4.5$ V to 40 V (±2.25 V to ±20 V) at $T_A = 25°C$, $R_L = 10$ kΩ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{O\ UT} = V_S / 2$, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Voltage output swing from rail	Positive rail headroom	V_S = 40 V, R_L = 10 kΩ		115	210	mV
			V_S = 40 V, R_L = 2 kΩ		520	965	
		Negative rail headroom	V_S = 40 V, R_L = 10 kΩ		105	215	
			V_S = 40 V, R_L = 2 kΩ		500	1030	
I_{SC}	Short-circuit current				±26		mA
C_{LOAD}	Capacitive load drive				300		pF
Z_O	Open-loop output impedance	f = 1 MHz, I_O = 0 A			125		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 A			937.5	1125	µA
		I_O = 0 A, (TL071H)			960	1156	
		I_O = 0 A	T_A = –40°C to 125°C			1130	
		I_O = 0 A, (TL072H)				1143	
		I_O = 0 A, (TL071H)				1160	
	Turn-On Time	At $T_A = 25°C$, V_S = 40 V, V_S ramp rate > 0.3 V/µs			60		µs

(1) Max I_B and I_{os} data is specified based on characterization results.

6.8 Electrical Characteristics (DC): TL07xC, TL07xAC, TL07xBC, TL07xI, TL07xM

For $V_S = (V_{CC+}) – (V_{CC–}) = ±15$ V at $T_A = 25°C$, unless otherwise noted

PARAMETER		TEST CONDITIONS(1) (2)			MIN	TYP	MAX	UNIT
V_{OS}	Input offset voltage	$V_O = 0$ V, $R_S = 50$ Ω	TL07xC			3	10	mV
				T_A = Full range			13	
			TL07xAC			3	6	
				T_A = Full range			7.5	
			TL07xBC			2	3	
				T_A = Full range			5	
			TL07xI			3	6	
				T_A = Full range			8	
			TL071M, TL072M			3	6	
				T_A = Full range			9	
			TL074M			3	9	
				T_A = Full range			15	
dV_{OS}/dT	Input offset voltage drift	$V_O = 0$ V, $R_S = 50$ Ω	T_A = Full range			±18		μV/°C
I_{OS}	Input offset current	$V_O = 0$ V	TL07xC			5	100	pA
				T_A = Full range			10	nA
			TL07xAC, TL07xBC, TL07xI			5	100	pA
				T_A = Full range			2	nA
			TL07xM			5	100	pA
				T_A = Full range			20	nA
I_B	Input bias current	$V_O = 0$ V	TL07xC, TL07xAC, TL07xBC, TL07xI			65	200	pA
				T_A = Full range			7	nA
			TL071M, TL072M			65	200	pA
				T_A = Full range			50	nA
			TL074M			65	200	pA
				T_A = Full range			20	nA
V_{CM}	Common-mode voltage range				±11	–12 to 15		V
VOM	Maximum peak output voltage swing	$R_L = 10$ kΩ			±12	±13.5		V
		$R_L ≥ 10$ kΩ	T_A = Full range		±12			
		$R_L ≥ 2$ kΩ			±10			
A_{OL}	Open-loop voltage gain	$V_O = 0$ V	TL07xC		25	200		V/mV
				T_A = Full range	15			
			TL07xAC, TL07xBC, TL07xI		50	200		
				T_A = Full range	25			
			TL07xM		35	200		
				T_A = Full range	15			
GBW	Gain-bandwidth product	All NS and PS packages; All TL07xM devices				3		MHz
		All other devices				5.25		
R_{ID}	Common-mode input resistance					1		TΩ
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR(min)}$, $V_O = 0$ V, $R_S = 50$ Ω	TL07xC		70	100		dB
			TL07xAC, TL07xBC, TL07xI		75	100		
			TL07xM		80	86		
PSRR	Input offset voltage versus power supply	$V_S = ±9$ V to ± 18 V, $V_O = 0$ V, $R_S = 50$ Ω	TL07xC		70	100		dB
			TL07xAC, TL07xBC, TL07xI		80	100		
			TL07xM		80	86		
I_Q	Quiescent current per amplifier	$V_O = 0$ V; no load				1.4	2.5	mA

6.8 Electrical Characteristics (DC): TL07xC, TL07xAC, TL07xBC, TL07xI, TL07xM (continued)

For $V_S = (V_{CC+}) – (V_{CC–}) = ±15$ V at $T_A = 25°C$, unless otherwise noted

PARAMETER		TEST CONDITIONS(1) (2)	MIN	TYP	MAX	UNIT
	Channel separation	f = 0 Hz		1		µV/V

(1) All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified.
(2) Full range is $T_A = 0°C$ to 70°C for the TL07xC, TL07xAC, and TL07xBC; $T_A = –40°C$ to 85°C for the TL07xI; and $T_A = –55°C$ to 125°C for the TL07xM.

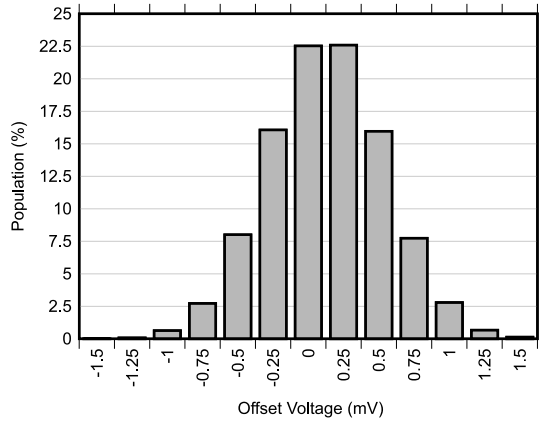
6.9 Electrical Characteristics (AC): TL07xC, TL07xAC, TL07xBC, TL07xI, TL07xM

For $V_S = (V_{CC+}) – (V_{CC–}) = ±15$ V at $T_A = 25°C$, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate	V_I = 10 V, C_L = 100 pF, R_L = 2 kΩ	TL07xM	5	20		V/µs
			TL07xC, TL07xAC, TL07xBC, TL07xI	8	20		V/µs
t_S	Settling time	V_I = 20 V, C_L = 100 pF, R_L = 2 kΩ			0.1		µs
					20%		
e_N	Input voltage noise density	All PS and NS packages; All TL07xM devices	R_S = 20 Ω, f = 1 kHz		18		nV/√Hz
		All other devices	f = 1 kHz		37		nV/√Hz
			f = 10 kHz		21		
E_N	Input voltage noise	All PS and NS packages; All TL07xM devices	R_S = 20 Ω, f = 10 Hz to 10 kHz		4		$µV_{RMS}$
		All other devices	f = 0.1 Hz to 10 Hz		1.4		$µV_{RMS}$
i_N	Input current noise	R_S = 20 Ω, f = 1 kHz			10		fA/√Hz
	Phase margin	TL07xC, TL07xAC, TL07xBC, TL07xI	G = +1, R_L = 10 kΩ, C_L = 20 pF		56		°
	Overload recovery time	V_{IN} × gain > V_S			300		ns
THD+N	Total harmonic distortion + noise	All PS and NS packages; All TL07xM devices	V_O = 6 V_{RMS}, R_L ≥ 2 kΩ, f = 1 kHz, G = +1, R_S ≤ 1 kΩ		0.003		%
		All other devices	V_S = 40 V, V_O = 6 V_{RMS}, G = +1, f = 1 kHz		0.00012		%
EMIRR	EMI rejection ratio	TL07xC, TL07xAC, TL07xBC, TL07xI	f = 1 GHz		53		dB
Z_O	Open-loop output impedance	TL07xC, TL07xAC, TL07xBC, TL07xI	f = 1 MHz, I_O = 0 A		125		Ω

6.10 Typical Characteristics: TL07xH

at T_A = 25°C, V_S = 40 V (±20 V), V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 20 pF (unless otherwise noted)



T_A = 25°C

Figure 6-1. Offset Voltage Production Distribution

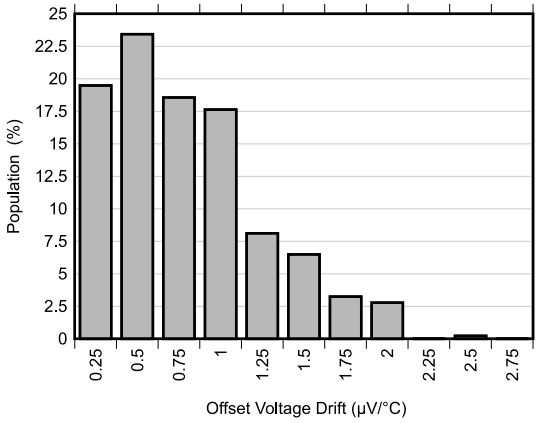
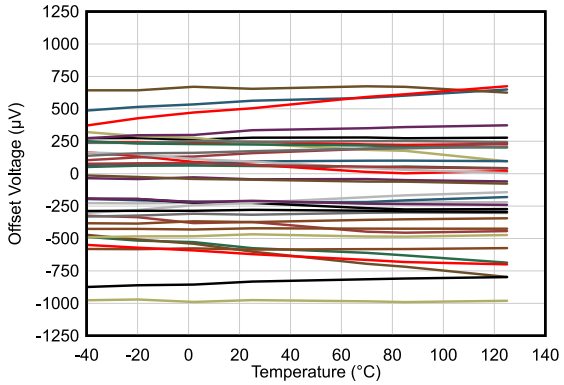
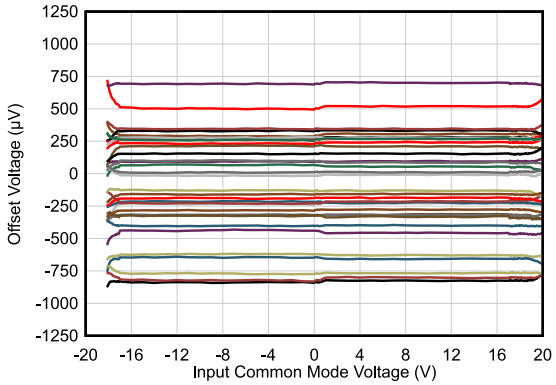


Figure 6-2. Offset Voltage Drift Distribution



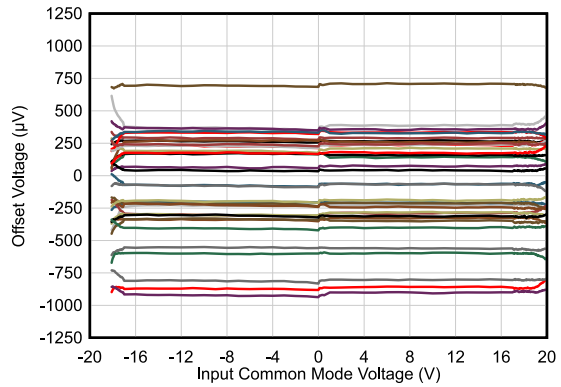
V_{CM} = V_S / 2

Figure 6-3. Offset Voltage vs Temperature



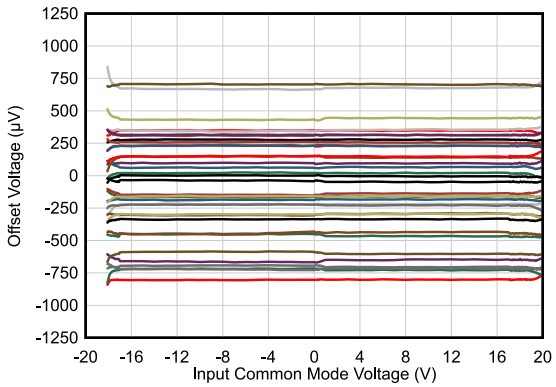
T_A = 25°C

Figure 6-4. Offset Voltage vs Common-Mode Voltage



T_A = 125°C

Figure 6-5. Offset Voltage vs Common-Mode Voltage



T_A = –40°C

Figure 6-6. Offset Voltage vs Common-Mode Voltage

6.10 Typical Characteristics: TL07xH (continued)

at T_A = 25°C, V_S = 40 V (±20 V), V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 20 pF (unless otherwise noted)

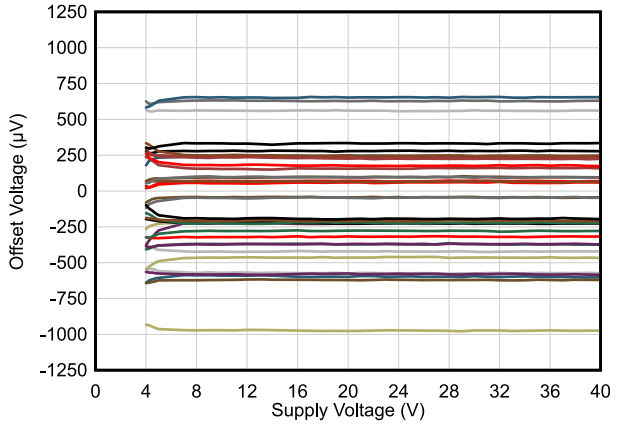


Figure 6-7. Offset Voltage vs Power Supply

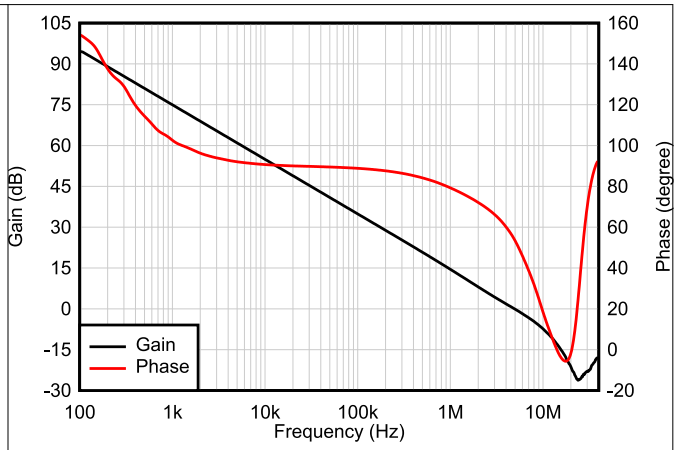


Figure 6-8. Open-Loop Gain and Phase vs Frequency

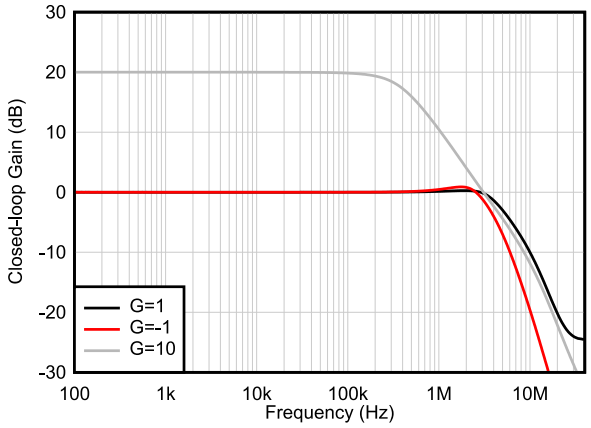


Figure 6-9. Closed-Loop Gain vs Frequency

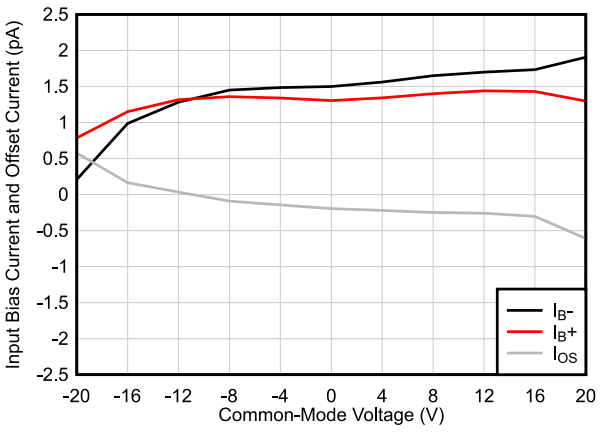


Figure 6-10. Input Bias Current vs Common-Mode Voltage

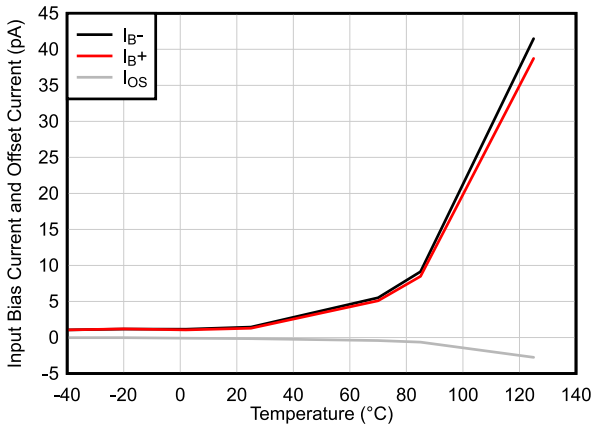


Figure 6-11. Input Bias Current vs Temperature

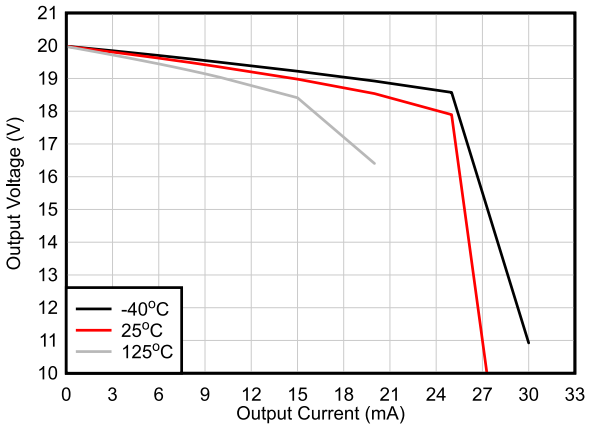


Figure 6-12. Output Voltage Swing vs Output Current (Sourcing)

6.10 Typical Characteristics: TL07xH (continued)

at T_A = 25°C, V_S = 40 V (±20 V), V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 20 pF (unless otherwise noted)

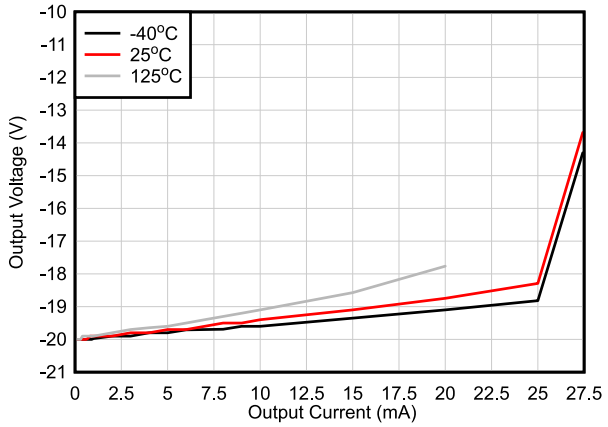


Figure 6-13. Output Voltage Swing vs Output Current (Sinking)

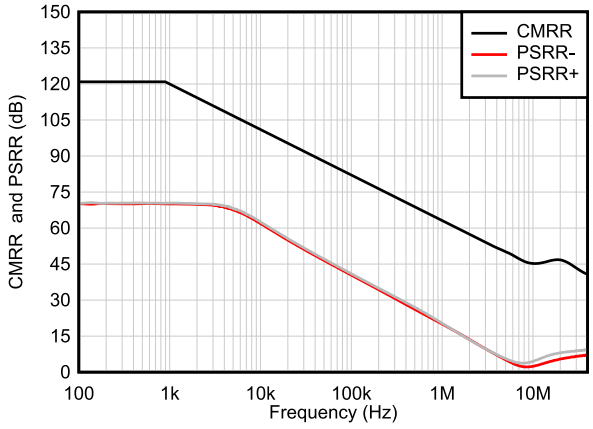
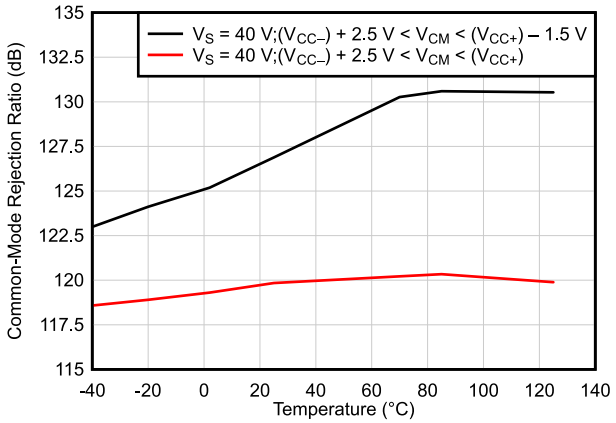
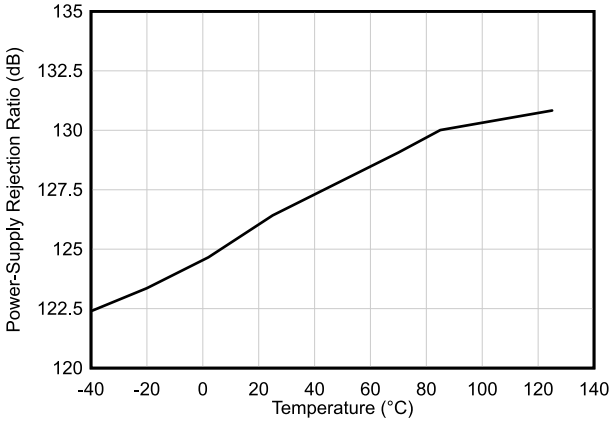


Figure 6-14. CMRR and PSRR vs Frequency



f = 0 Hz

Figure 6-15. CMRR vs Temperature (dB)



f = 0 Hz

Figure 6-16. PSRR vs Temperature (dB)

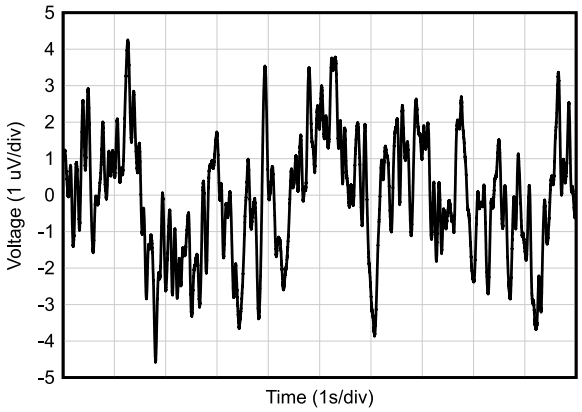


Figure 6-17. 0.1-Hz to 10-Hz Noise

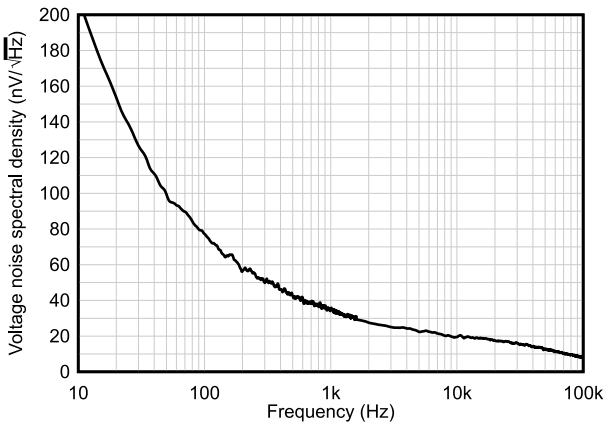
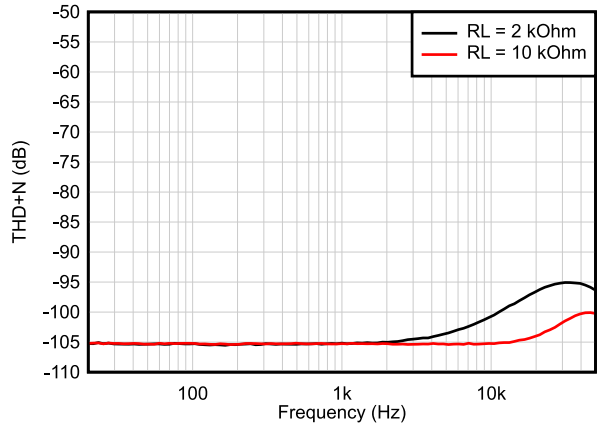


Figure 6-18. Input Voltage Noise Spectral Density vs Frequency

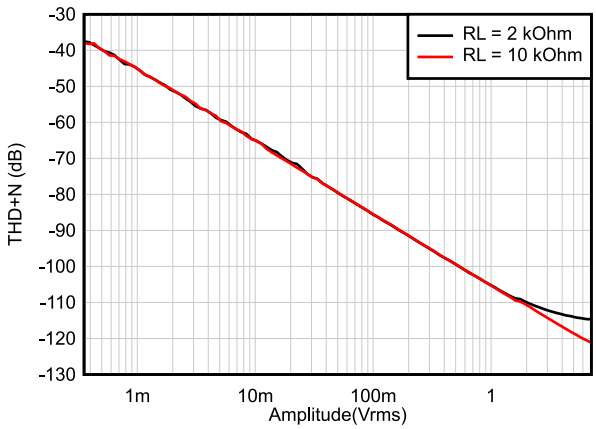
6.10 Typical Characteristics: TL07xH (continued)

at T_A = 25°C, V_S = 40 V (±20 V), V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 20 pF (unless otherwise noted)



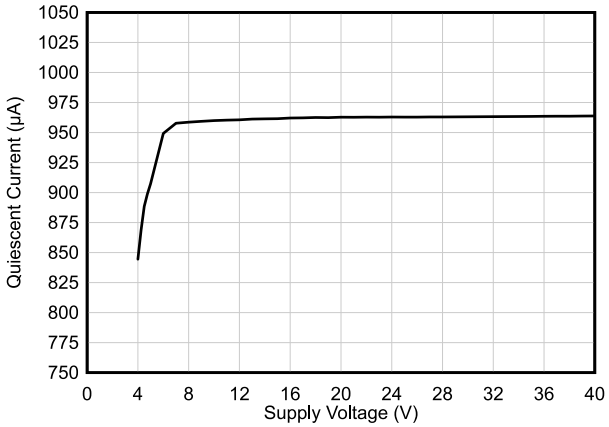
BW = 80 kHz, V_{OUT} = 1 V_{RMS}

Figure 6-19. THD+N Ratio vs Frequency



BW = 80 kHz, f = 1 kHz

Figure 6-20. THD+N vs Output Amplitude



V_{CM} = V_S / 2

Figure 6-21. Quiescent Current vs Supply Voltage

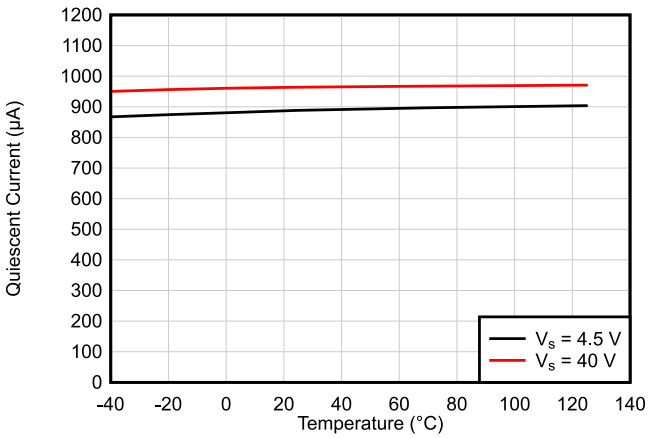


Figure 6-22. Quiescent Current vs Temperature

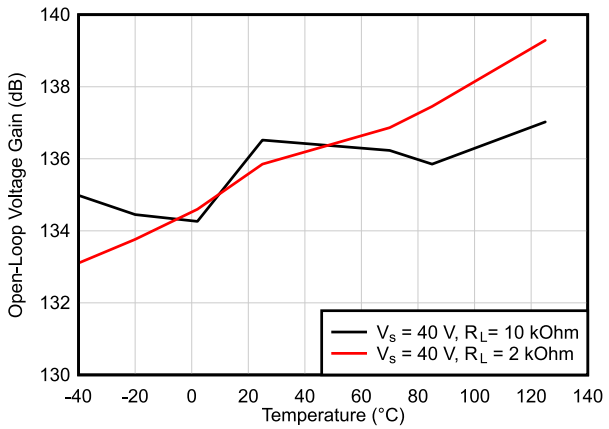


Figure 6-23. Open-Loop Voltage Gain vs Temperature (dB)

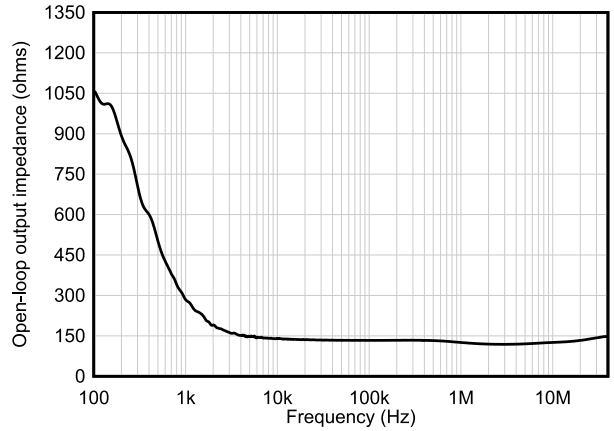
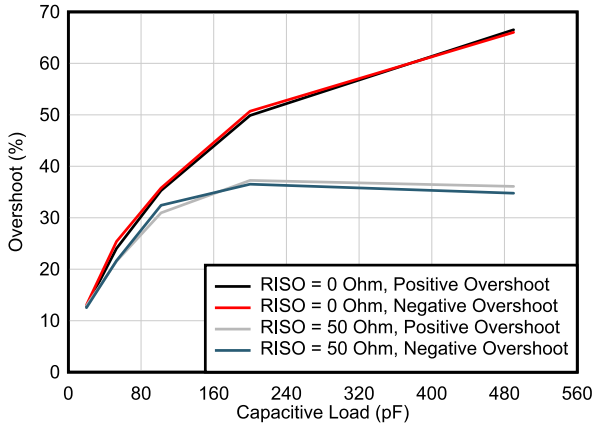


Figure 6-24. Open-Loop Output Impedance vs Frequency

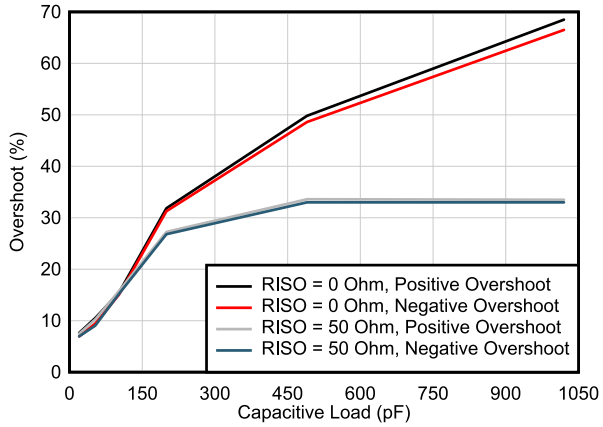
6.10 Typical Characteristics: TL07xH (continued)

at T_A = 25°C, V_S = 40 V (±20 V), V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 20 pF (unless otherwise noted)



G = –1, 25-mV output step

Figure 6-25. Small-Signal Overshoot vs Capacitive Load



G = 1, 10-mV output step

Figure 6-26. Small-Signal Overshoot vs Capacitive Load

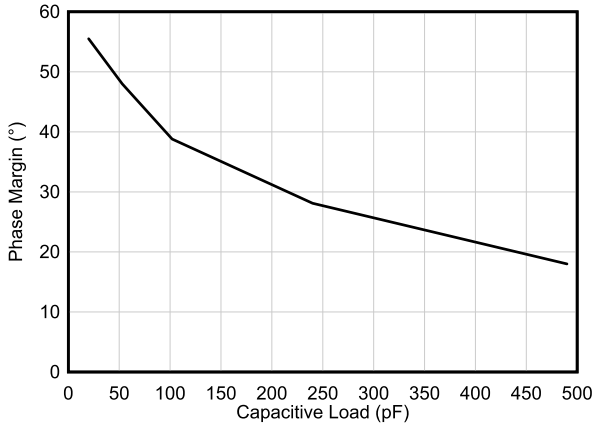
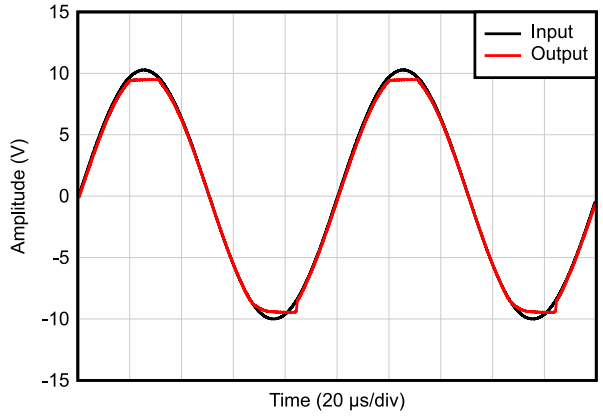
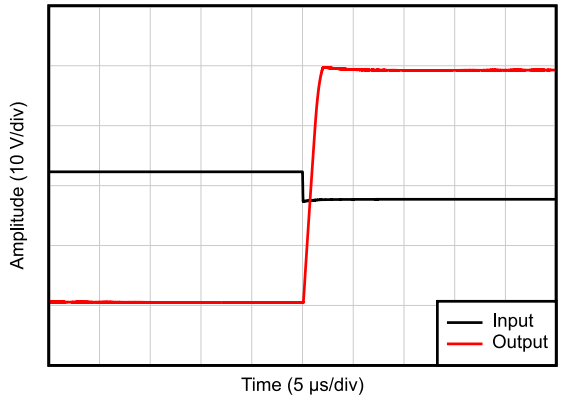


Figure 6-27. Phase Margin vs Capacitive Load



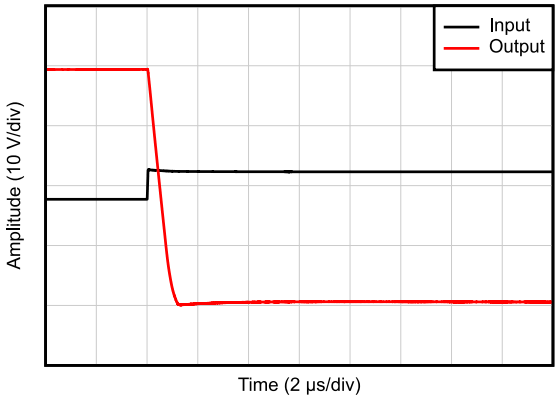
V_S = ±10 V, V_{IN} = V_{OUT}

Figure 6-28. No Phase Reversal



G = –10

Figure 6-29. Positive Overload Recovery

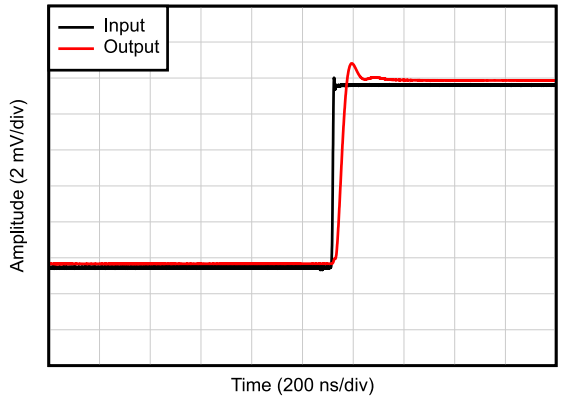


G = –10

Figure 6-30. Negative Overload Recovery

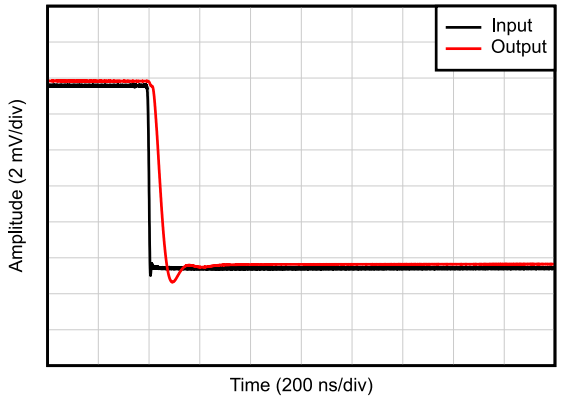
6.10 Typical Characteristics: TL07xH (continued)

at T_A = 25°C, V_S = 40 V (±20 V), V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 20 pF (unless otherwise noted)



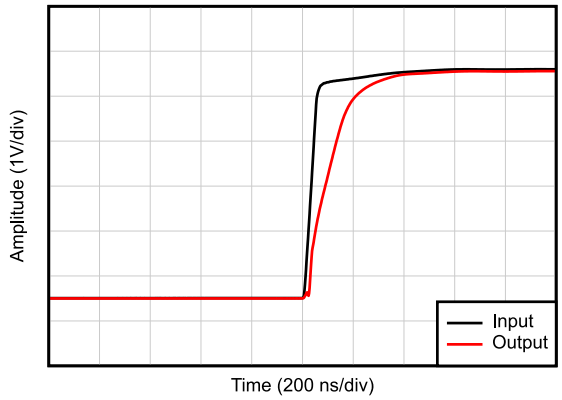
C_L = 20 pF, G = 1, 10-mV step response

Figure 6-31. Small-Signal Step Response, Rising



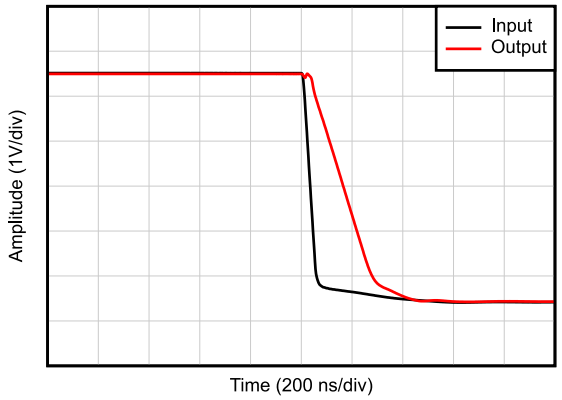
C_L = 20 pF, G = 1, 10-mV step response

Figure 6-32. Small-Signal Step Response, Falling



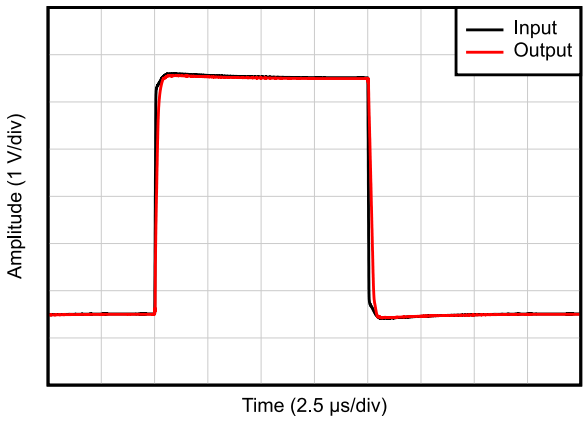
C_L = 20 pF, G = 1

Figure 6-33. Large-Signal Step Response (Rising)



C_L = 20 pF, G = 1

Figure 6-34. Large-Signal Step Response (Falling)



C_L = 20 pF, G = 1

Figure 6-35. Large-Signal Step Response

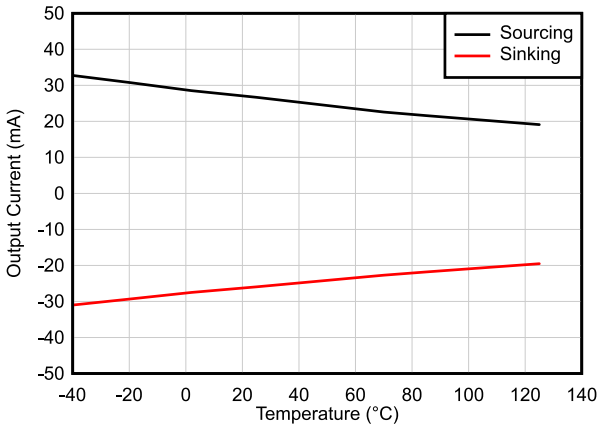


Figure 6-36. Short-Circuit Current vs Temperature

6.10 Typical Characteristics: TL07xH (continued)

at T_A = 25°C, V_S = 40 V (±20 V), V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 20 pF (unless otherwise noted)

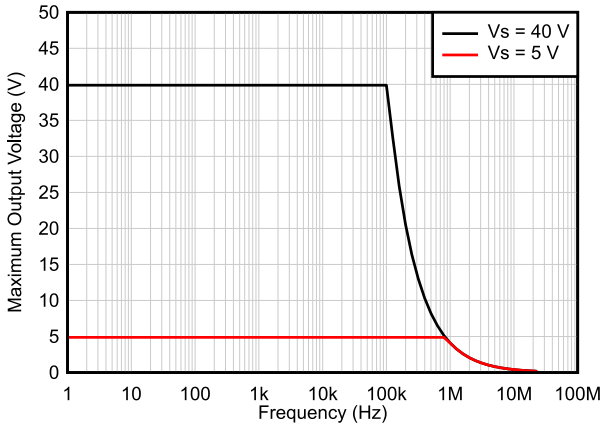


Figure 6-37. Maximum Output Voltage vs Frequency

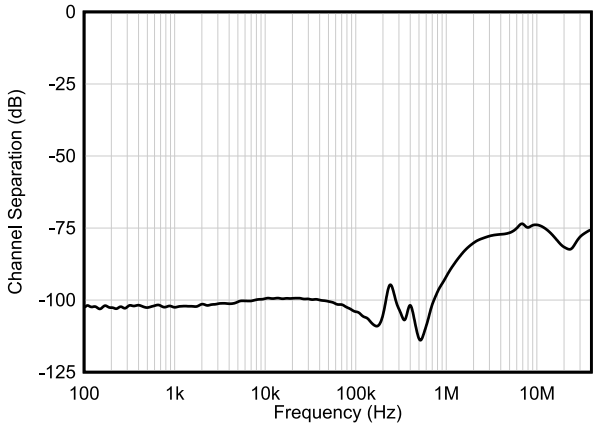


Figure 6-38. Channel Separation vs Frequency

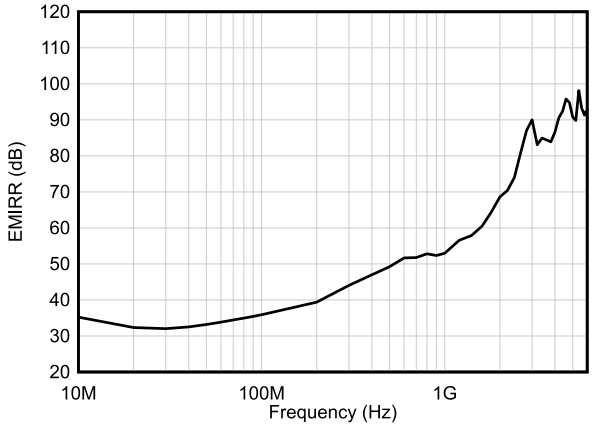


Figure 6-39. EMIRR (Electromagnetic Interference Rejection Ratio) vs Frequency

6.11 Typical Characteristics: All Devices Except TL07xH

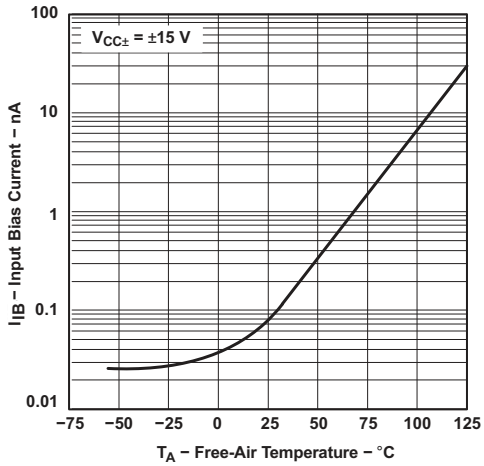


Figure 6-40. Input Bias Current vs Free-Air Temperature

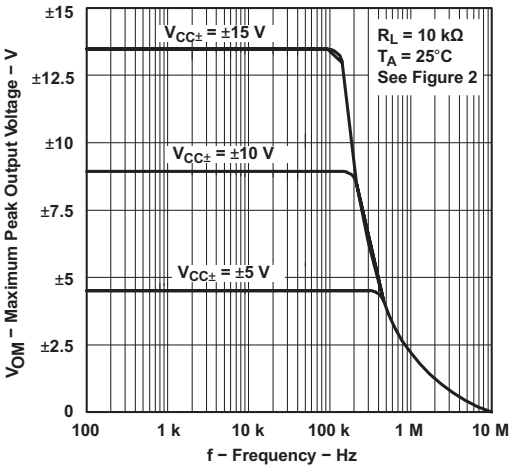


Figure 6-41. Maximum Peak Output Voltage vs Frequency

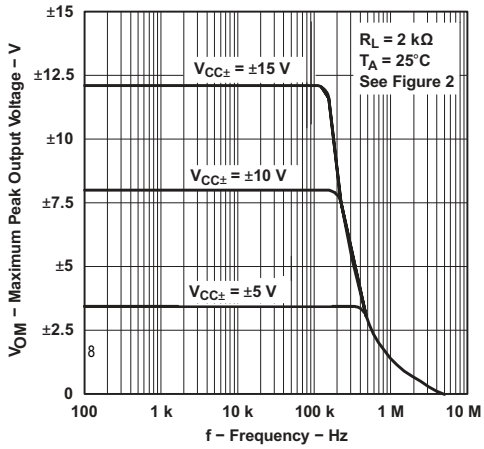


Figure 6-42. Maximum Peak Output Voltage vs Frequency

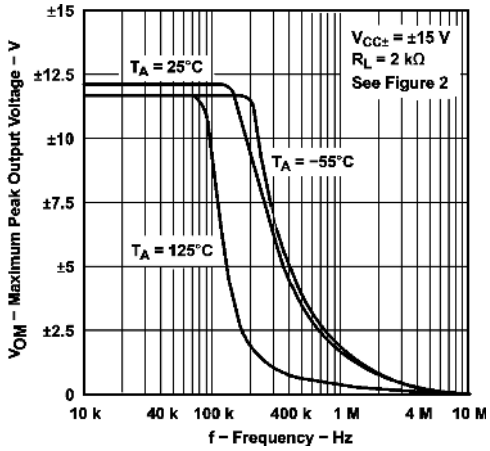


Figure 6-43. Maximum Peak Output Voltage vs Frequency

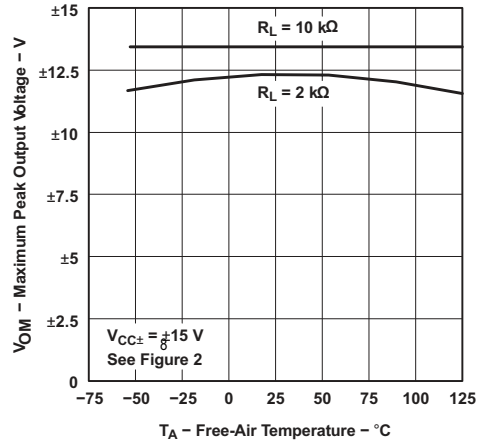


Figure 6-44. Maximum Peak Output Voltage vs Free-Air Temperature

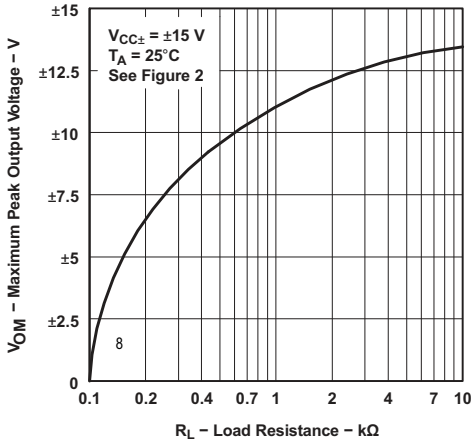


Figure 6-45. Maximum Peak Output Voltage vs Load Resistance

6.11 Typical Characteristics: All Devices Except TL07xH (continued)

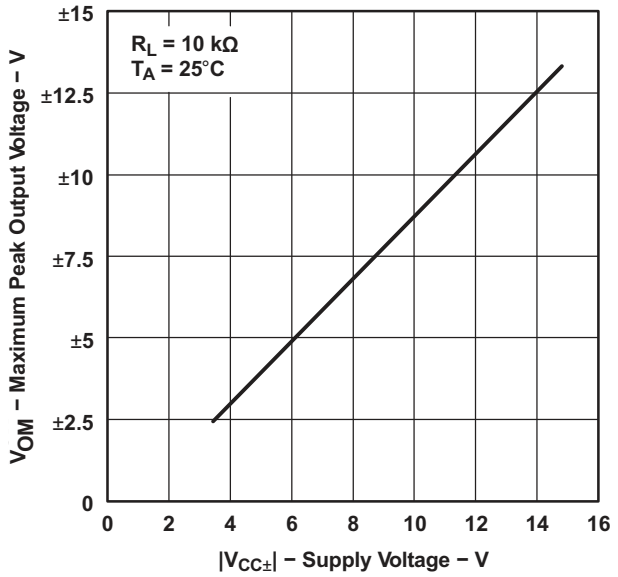


Figure 6-46. Maximum Peak Output Voltage vs Supply Voltage

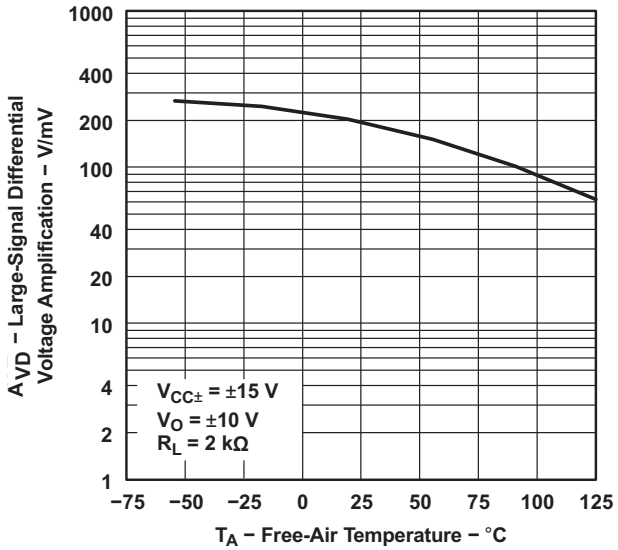


Figure 6-47. Large-Signal Differential Voltage Amplification vs Free-Air Temperature

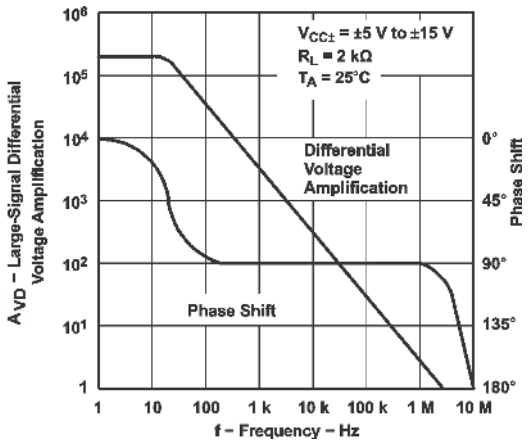


Figure 6-48. Large-Signal Differential Voltage Amplification and Phase Shift vs Frequency

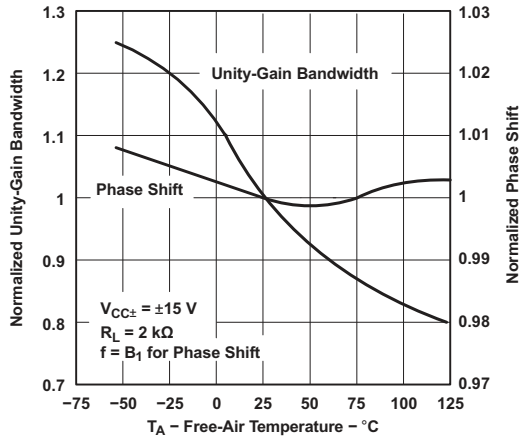


Figure 6-49. Normalized Unity-Gain Bandwidth and Phase Shift vs Free-Air Temperature

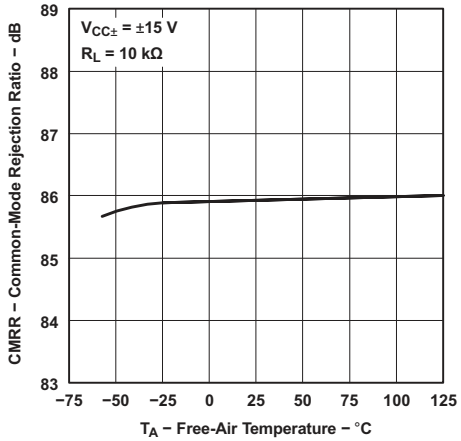


Figure 6-50. Common-Mode Rejection Ratio vs Free-Air Temperature

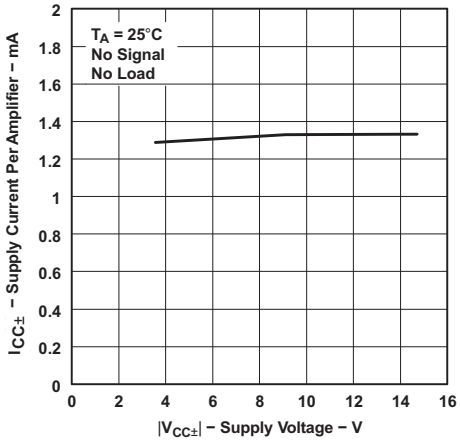


Figure 6-51. Supply Current Per Amplifier vs Supply Voltage

6.11 Typical Characteristics: All Devices Except TL07xH (continued)

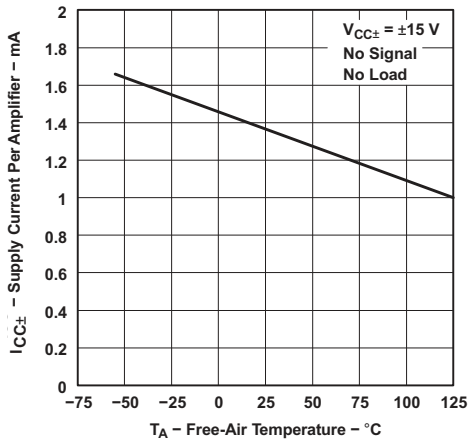


Figure 6-52. Supply Current Per Amplifier vs Free-Air Temperature

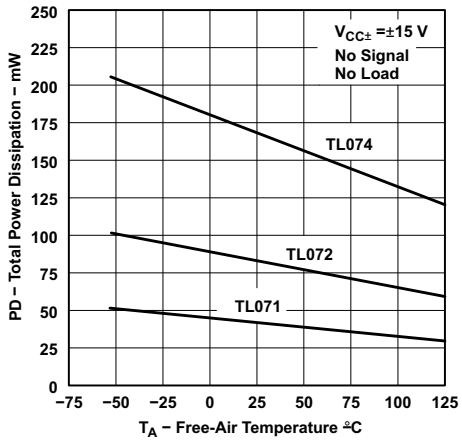


Figure 6-53. Total Power Dissipation vs Free-Air Temperature

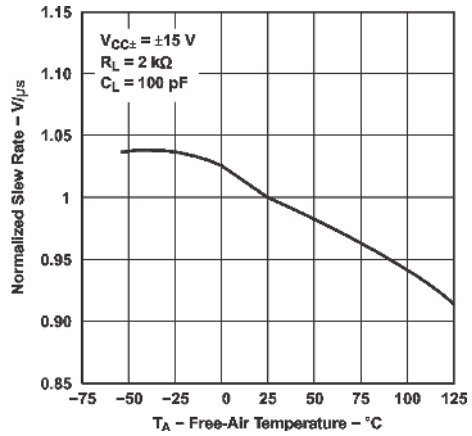


Figure 6-54. Normalized Slew Rate vs Free-Air Temperature

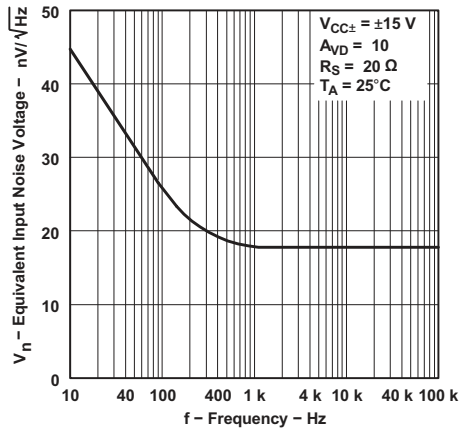


Figure 6-55. Equivalent Input Noise Voltage vs Frequency

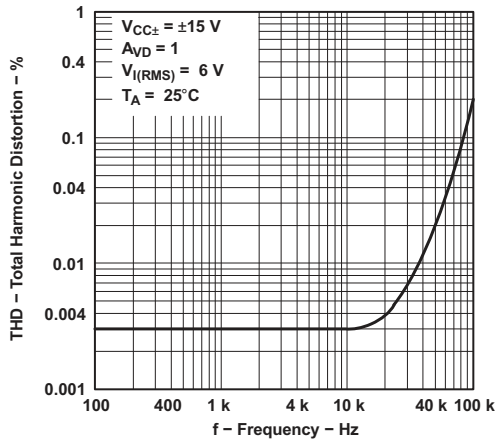


Figure 6-56. Total Harmonic Distortion vs Frequency

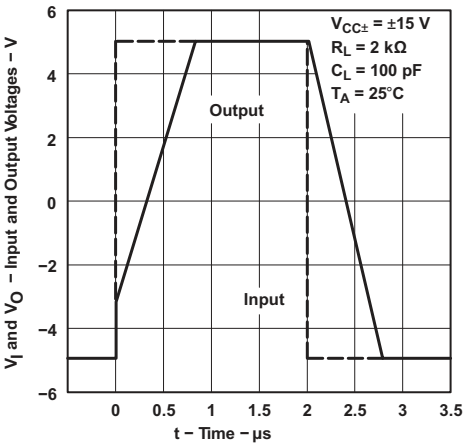


Figure 6-57. Voltage-Follower Large-Signal Pulse Response

6.11 Typical Characteristics: All Devices Except TL07xH (continued)

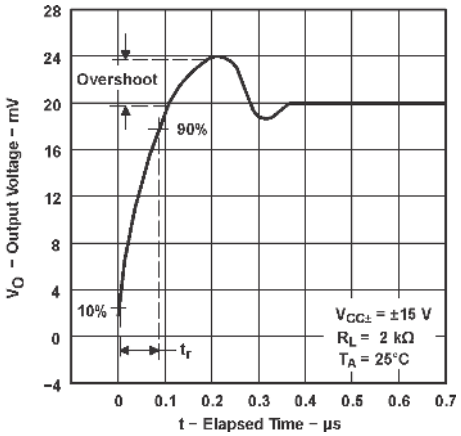


Figure 6-58. Output Voltage vs Elapsed Time

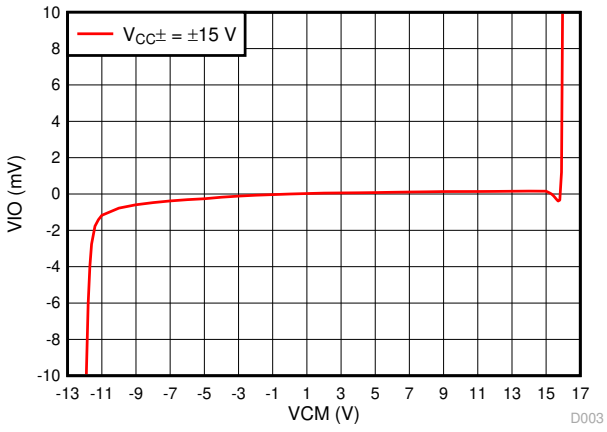


Figure 6-59. V_{IO} vs V_{CM}

7 Parameter Measurement Information

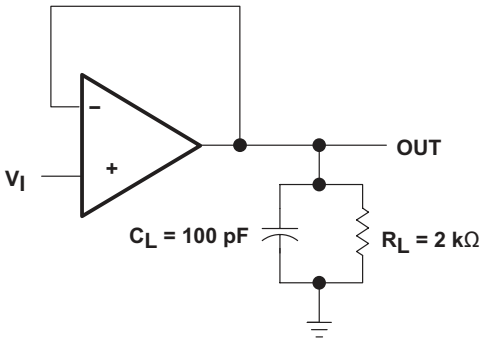


Figure 7-1. Unity-Gain Amplifier

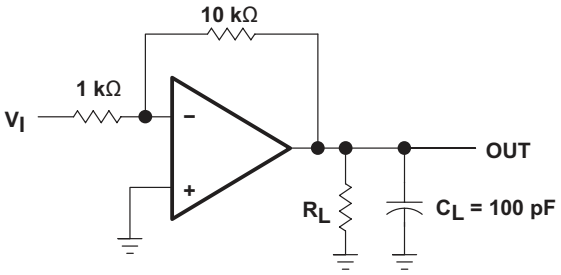


Figure 7-2. Gain-of-10 Inverting Amplifier

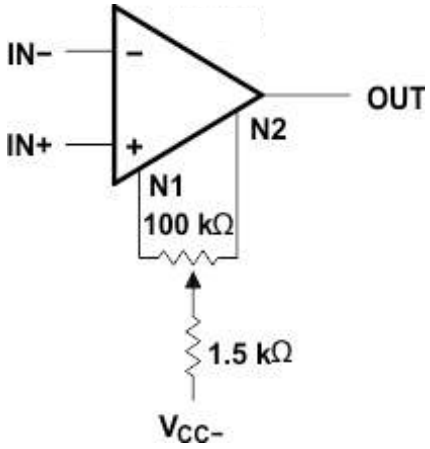


Figure 7-3. Input Offset-Voltage Null Circuit

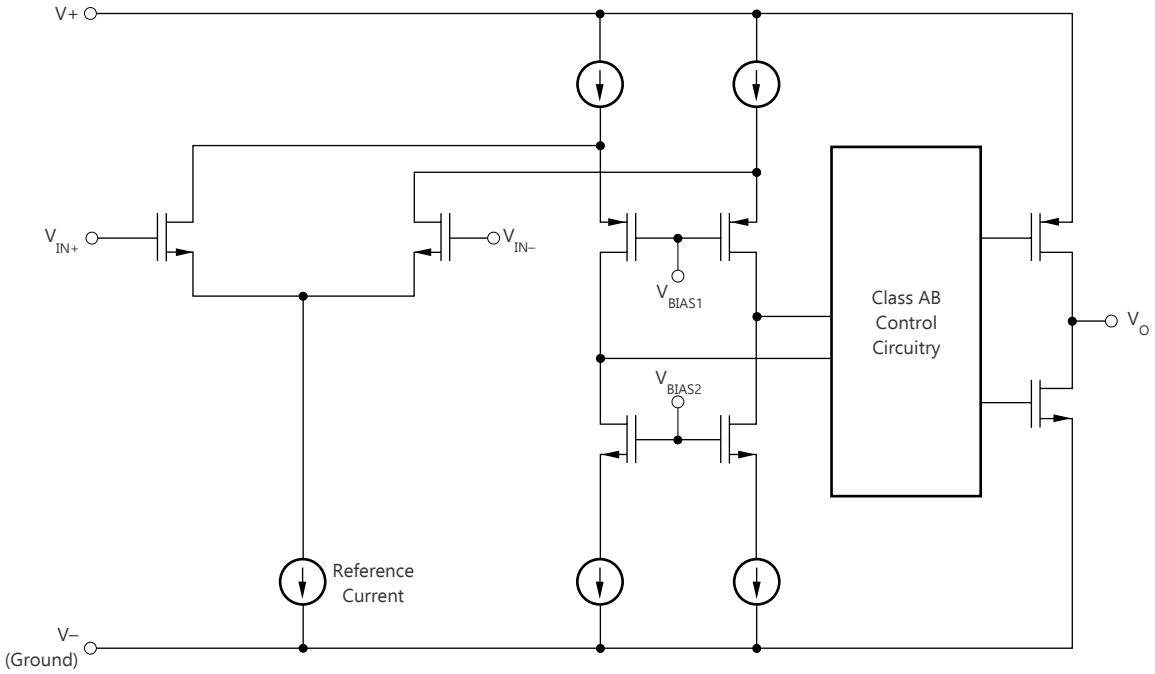
8 Detailed Description

8.1 Overview

The TL07xH (TL071H, TL072H, and TL074H) family of devices are the next-generation versions of the industry-standard TL07x (TL071, TL072, and TL074) devices. These devices provide outstanding value for cost-sensitive applications, with features including low offset (1 mV, typical), high slew rate (20 V/µs, typical), and common-mode input to the positive supply. High ESD (2 kV, HBM), integrated EMI and RF filters, and operation across the full –40°C to 125°C enable the TL07xH devices to be used in the most rugged and demanding applications.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from −40°C to +85°C. The M-suffix devices are characterized for operation over the full military temperature range of −55°C to +125°C.

8.2 Functional Block Diagram



8.3 Feature Description

The TL07xH family of devices improve many specifications as compared to the industry-standard TL07x family. Several comparisons of key specifications between these families are included in the following sections to show the advantages of the TL07xH family.

8.3.1 Total Harmonic Distortion

Harmonic distortions to an audio signal are created by electronic components in a circuit. Total harmonic distortion (THD) is a measure of harmonic distortions accumulated by a signal in an audio system. These devices have a very low THD of 0.003% meaning that the TL07x device adds little harmonic distortion when used in audio signal applications.

8.3.2 Slew Rate

The slew rate is the rate at which an operational amplifier can change the output when there is a change on the input. These devices have a 20-V/µs slew rate.

8.4 Device Functional Modes

These devices are powered on when the supply is connected. These devices can be operated as a single-supply operational amplifier or dual-supply amplifier depending on the application.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

A typical application for an operational amplifier is an inverting amplifier. This amplifier takes a positive voltage on the input, and makes the voltage a negative voltage. In the same manner, the amplifier makes negative voltages positive.

9.2 Typical Application

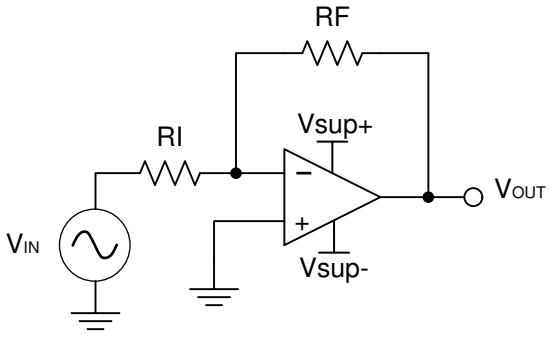


Figure 9-1. Inverting Amplifier

9.2.1 Design Requirements

The supply voltage must be selected so the supply voltage is larger than the input voltage range and output range. For instance, this application scales a signal of ±0.5 V to ±1.8 V. Setting the supply at ±12 V is sufficient to accommodate this application.

9.2.2 Detailed Design Procedure

$$V_o = (V_i + V_{io}) \times \left(1 + \frac{1M\Omega}{1k\Omega}\right) \quad (1)$$

Determine the gain required by the inverting amplifier:

$$A_V = \frac{VOUT}{VIN} \quad (2)$$

$$A_V = \frac{1.8}{-0.5} = -3.6 \quad (3)$$

Once the desired gain is determined, select a value for RI or RF. Selecting a value in the kilohm range is desirable because the amplifier circuit uses currents in the milliamp range. This ensures the part does not draw too much current. This example uses 10 kΩ for RI which means 36 kΩ is used for RF. This is determined by Equation 4.

$$A_V = -\frac{RF}{RI} \quad (4)$$

9.2.3 Application Curve

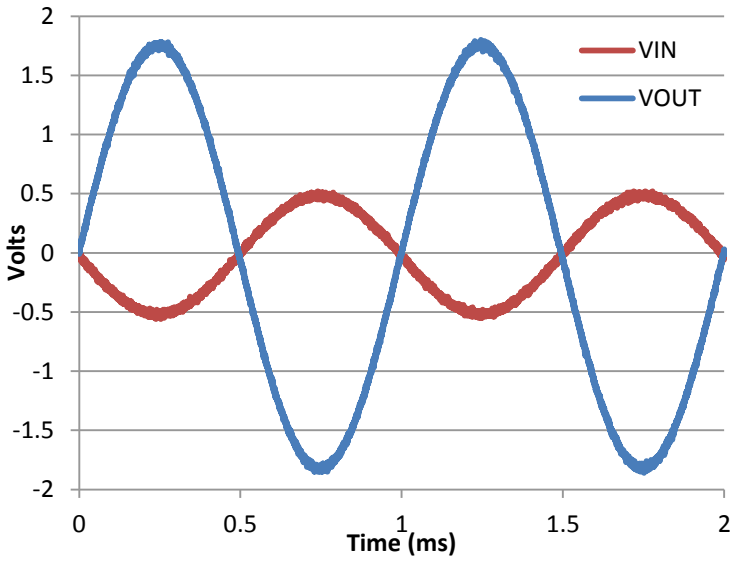


Figure 9-2. Input and Output Voltages of the Inverting Amplifier

9.3 Unity Gain Buffer

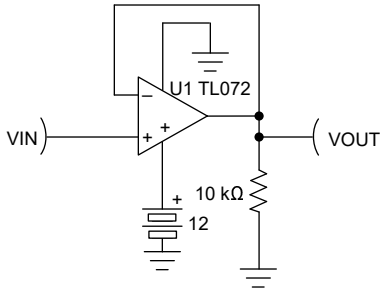


Figure 9-3. Single-Supply Unity Gain Amplifier

9.3.1 Design Requirements

- V_{CC} must be within valid range per *Recommended Operating Conditions*. This example uses a value of 12 V for V_{CC}.
- Input voltage must be within the recommended common-mode range, as shown in *Recommended Operating Conditions*. The valid common-mode range is 4 V to 12 V ($V_{CC–}$ + 4 V to V_{CC+}).
- Output is limited by output range, which is typically 1.5 V to 10.5 V, or $V_{CC–}$ + 1.5 V to V_{CC+} – 1.5 V.

9.3.2 Detailed Design Procedure

- Avoid input voltage values below 1 V to prevent phase reversal where output goes high.
- Avoid input values below 4 V to prevent degraded V_{IO} that results in an apparent gain greater than 1. This may cause instability in some second-order filter designs.

9.3.3 Application Curves

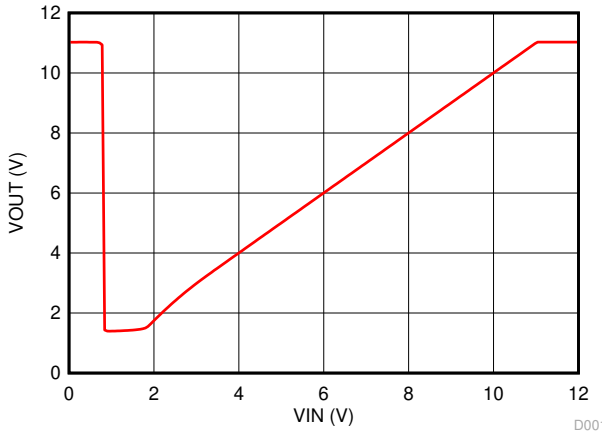


Figure 9-4. Output Voltage vs Input Voltage

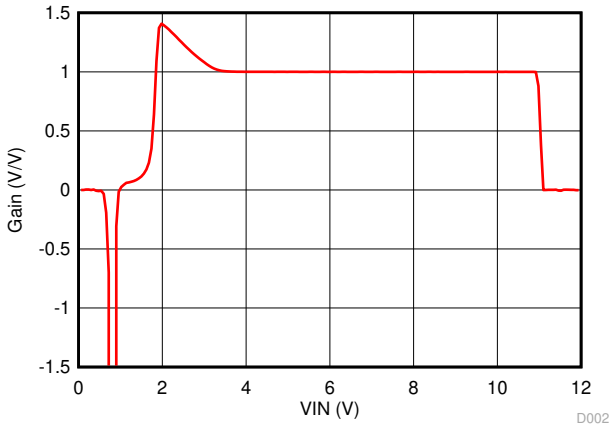


Figure 9-5. Gain vs Input Voltage

9.4 System Examples

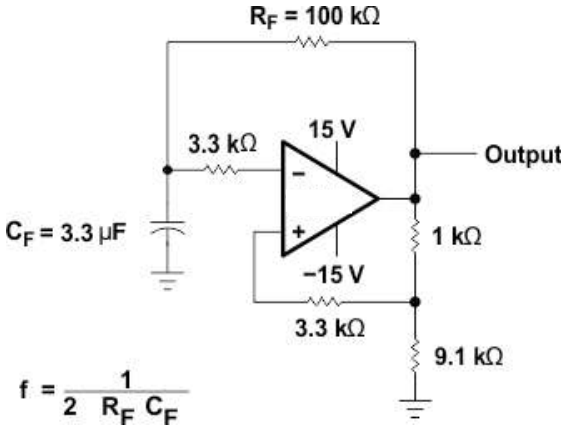


Figure 9-6. 0.5-Hz Square-Wave Oscillator

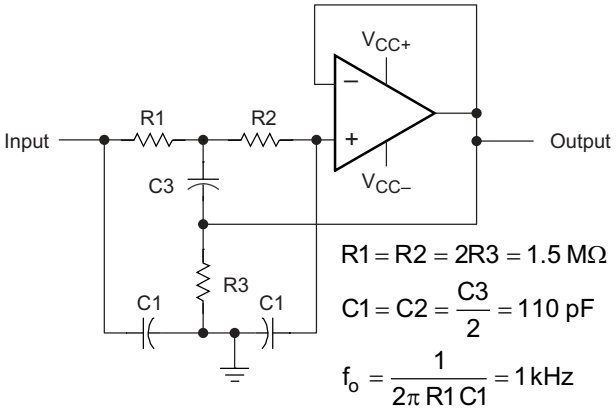


Figure 9-7. High-Q Notch Filter

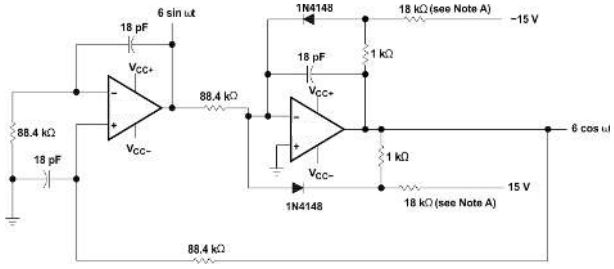


Figure 9-8. 100-kHz Quadrature Oscillator

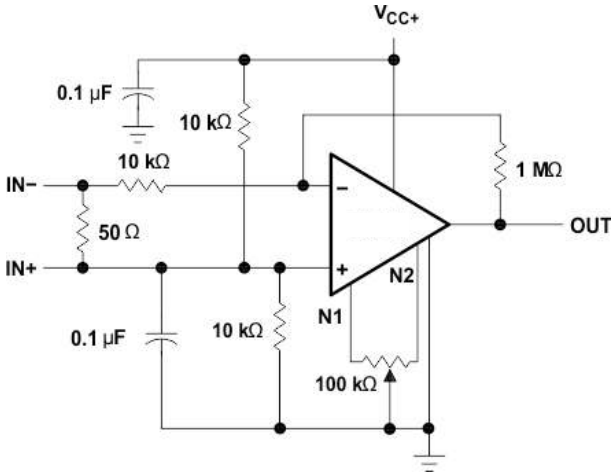


Figure 9-9. AC Amplifier

9.5 Power Supply Recommendations

CAUTION

Supply voltages larger than 36 V for a single-supply or outside the range of ±18 V for a dual-supply can permanently damage the device (see Section 6.1).

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see Section 9.6.

9.6 Layout

9.6.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V_{CC+} to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance. For more information, see Section 9.6.2.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

9.6.2 Layout Example

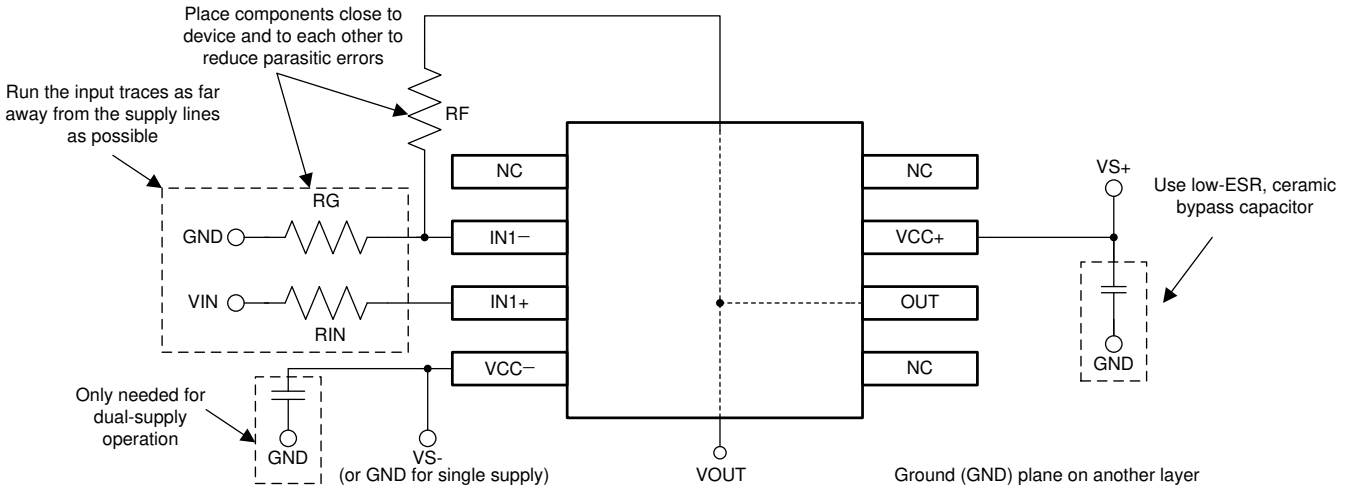


Figure 9-10. Operational Amplifier Board Layout for Noninverting Configuration

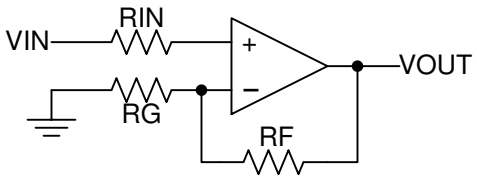


Figure 9-11. Operational Amplifier Schematic for Noninverting Configuration

10 Device and Documentation Support

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
81023052A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	81023052A TL072MFKB	Samples
8102305HA	ACTIVE	CFP	U	10	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8102305HA TL072M	Samples
8102305PA	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8102305PA TL072M	Samples
81023062A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	81023062A TL074MFKB	Samples
8102306CA	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8102306CA TL074MJB	Samples
8102306DA	ACTIVE	CFP	W	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8102306DA TL074MWB	Samples
JM38510/11905BPA	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510 /11905BPA	Samples
M38510/11905BPA	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510 /11905BPA	Samples
TL071ACDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	071AC	Samples
TL071ACP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL071ACP	Samples
TL071BCDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	071BC	Samples
TL071BCP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL071BCP	Samples
TL071CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL071C	Samples
TL071CDRE4	LIFEBUY	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL071C	
TL071CDRG4	LIFEBUY	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL071C	
TL071CP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL071CP	Samples
TL071CPE4	LIFEBUY	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL071CP	
TL071CPSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T071	Samples
TL071HIDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T71V	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL071HIDCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1IO	Samples
TL071HIDR	ACTIVE	SOIC	D	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL071D	Samples
TL071IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL071I	Samples
TL071IDRG4	LIFEBUY	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL071I	
TL071IP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TL071IP	Samples
TL072ACDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	072AC	Samples
TL072ACDRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	072AC	Samples
TL072ACDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	072AC	Samples
TL072ACP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL072ACP	Samples
TL072ACPE4	LIFEBUY	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL072ACP	
TL072BCD	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	072BC	
TL072BCDE4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	072BC	
TL072BCDG4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	072BC	
TL072BCDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	072BC	Samples
TL072BCP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL072BCP	Samples
TL072CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL072C	Samples
TL072CDRE4	LIFEBUY	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL072C	
TL072CDRG4	LIFEBUY	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL072C	
TL072CP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL072CP	Samples
TL072CPE4	LIFEBUY	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL072CP	
TL072CPS	ACTIVE	SO	PS	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T072	Samples
TL072CPSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T072	Samples
TL072CPSRG4	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T072	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL072CPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T072	Samples
TL072CPWRE4	LIFEBUY	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T072	
TL072CPWRG4	LIFEBUY	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T072	
TL072HIDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O72F	Samples
TL072HIDR	ACTIVE	SOIC	D	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL072D	Samples
TL072HIPWR	ACTIVE	TSSOP	PW	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	072HPW	Samples
TL072IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL072I	Samples
TL072IDRE4	LIFEBUY	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL072I	
TL072IDRG4	LIFEBUY	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL072I	
TL072IP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TL072IP	Samples
TL072IPE4	LIFEBUY	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TL072IP	
TL072MFKB	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	81023052A TL072MFKB	Samples
TL072MJG	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	TL072MJG	Samples
TL072MJGB	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8102305PA TL072M	Samples
TL072MUB	ACTIVE	CFP	U	10	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8102305HA TL072M	Samples
TL074ACD	LIFEBUY	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074AC	
TL074ACDE4	LIFEBUY	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074AC	
TL074ACDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074AC	Samples
TL074ACDRE4	LIFEBUY	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074AC	
TL074ACN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL074ACN	Samples
TL074ACNE4	LIFEBUY	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL074ACN	
TL074ACNSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074A	Samples
TL074BCD	LIFEBUY	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074BC	
TL074BCDE4	LIFEBUY	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074BC	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL074BCDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074BC	Samples
TL074BCDRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074BC	Samples
TL074BCDRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074BC	Samples
TL074BCN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL074BCN	Samples
TL074BCNE4	LIFEBUY	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL074BCN	
TL074CD	LIFEBUY	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074C	
TL074CDBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T074	Samples
TL074CDG4	LIFEBUY	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074C	
TL074CDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	TL074C	Samples
TL074CDRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074C	Samples
TL074CN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL074CN	Samples
TL074CNE4	LIFEBUY	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL074CN	
TL074CNSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074	Samples
TL074CPW	LIFEBUY	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T074	
TL074CPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T074	Samples
TL074CPWRE4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T074	Samples
TL074CPWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T074	Samples
TL074HIDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL074HID	Samples
TL074HIDYYR	ACTIVE	SOT-23-THIN	DYY	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T074HDYY	Samples
TL074HIPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL074PW	Samples
TL074ID	LIFEBUY	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I	
TL074IDE4	LIFEBUY	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I	
TL074IDG4	LIFEBUY	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL074IDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I	Samples
TL074IDRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I	Samples
TL074IDRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I	Samples
TL074IN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TL074IN	Samples
TL074MFK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	TL074MFK	Samples
TL074MFKB	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	81023062A TL074MFKB	Samples
TL074MJ	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	TL074MJ	Samples
TL074MJB	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8102306CA TL074MJB	Samples
TL074MWB	ACTIVE	CFP	W	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8102306DA TL074MWB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TL072, TL072M, TL074, TL074M :

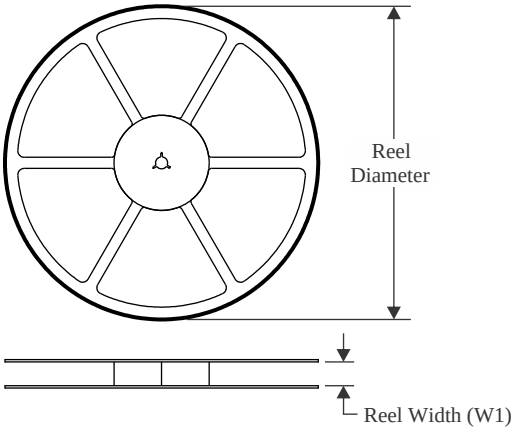
- Catalog : TL072, TL074
- Enhanced Product : TL072-EP, TL072-EP, TL074-EP, TL074-EP
- Military : TL072M, TL074M

NOTE: Qualified Version Definitions:

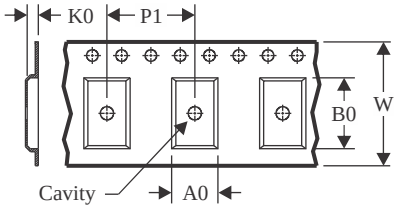
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

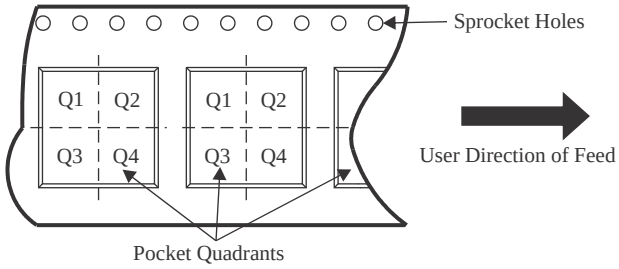


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

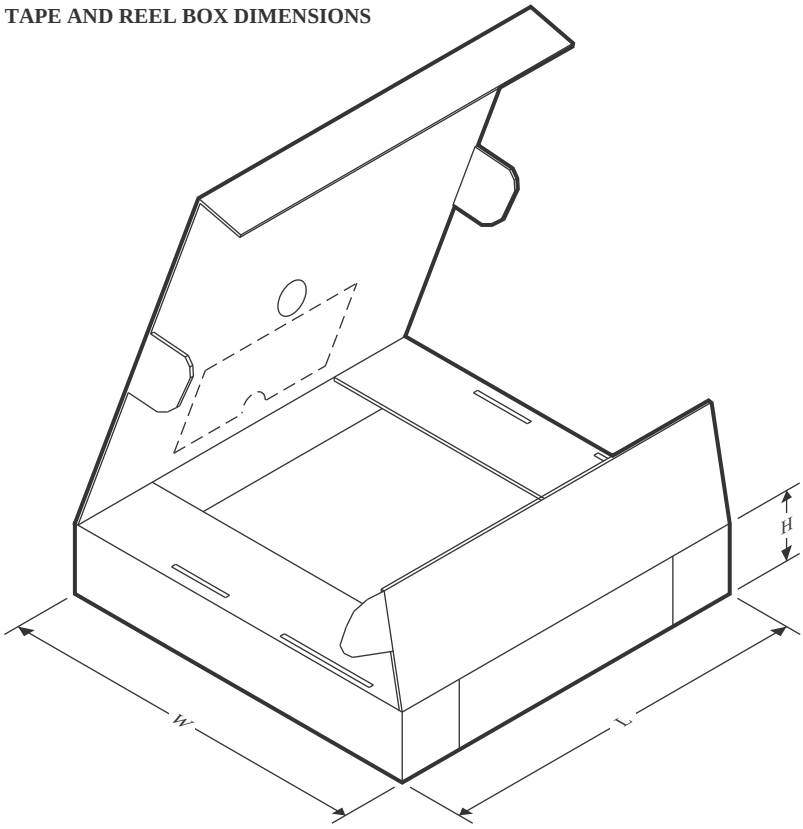


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL071ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL071ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL071BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL071BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL071CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL071CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL071CPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TL071HIDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TL071HIDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TL071HIDR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL071IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL072CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072CPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TL072CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL072CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL072HIDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TL072HIDR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072HIPWR	TSSOP	PW	8	3000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL072IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL074ACDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074ACNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TL074BCDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074CDBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TL074CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074CDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074CNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TL074CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL074HIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074HIDYYR	SOT-23-THIN	DYY	14	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
TL074HIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL074IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

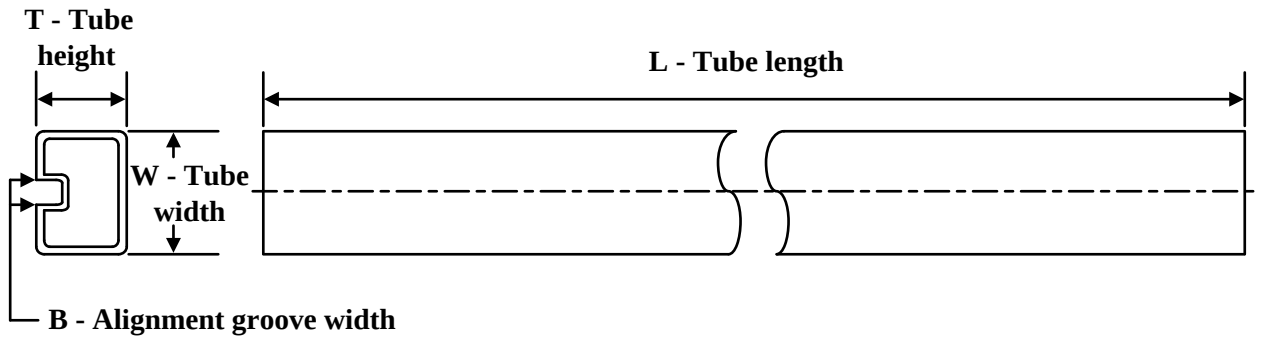


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL071ACDR	SOIC	D	8	2500	356.0	356.0	35.0
TL071ACDR	SOIC	D	8	2500	340.5	336.1	25.0
TL071BCDR	SOIC	D	8	2500	340.5	336.1	25.0
TL071BCDR	SOIC	D	8	2500	356.0	356.0	35.0
TL071CDR	SOIC	D	8	2500	356.0	356.0	35.0
TL071CDR	SOIC	D	8	2500	340.5	336.1	25.0
TL071CPSR	SO	PS	8	2000	356.0	356.0	35.0
TL071HIDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TL071HIDCKR	SC70	DCK	5	3000	190.0	190.0	30.0
TL071HIDR	SOIC	D	8	3000	356.0	356.0	35.0
TL071IDR	SOIC	D	8	2500	340.5	336.1	25.0
TL072ACDR	SOIC	D	8	2500	340.5	336.1	25.0
TL072ACDR	SOIC	D	8	2500	356.0	356.0	35.0
TL072BCDR	SOIC	D	8	2500	340.5	336.1	25.0
TL072CDR	SOIC	D	8	2500	340.5	336.1	25.0
TL072CDR	SOIC	D	8	2500	356.0	356.0	35.0
TL072CDR	SOIC	D	8	2500	356.0	356.0	35.0
TL072CPSR	SO	PS	8	2000	356.0	356.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL072CPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
TL072CPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
TL072HIDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TL072HIDR	SOIC	D	8	3000	356.0	356.0	35.0
TL072HIPWR	TSSOP	PW	8	3000	356.0	356.0	35.0
TL072IDR	SOIC	D	8	2500	340.5	336.1	25.0
TL072IDR	SOIC	D	8	2500	356.0	356.0	35.0
TL072IDR	SOIC	D	8	2500	356.0	356.0	35.0
TL074ACDR	SOIC	D	14	2500	340.5	336.1	32.0
TL074ACNSR	SO	NS	14	2000	356.0	356.0	35.0
TL074BCDR	SOIC	D	14	2500	340.5	336.1	32.0
TL074CDBR	SSOP	DB	14	2000	356.0	356.0	35.0
TL074CDR	SOIC	D	14	2500	340.5	336.1	32.0
TL074CDRG4	SOIC	D	14	2500	340.5	336.1	32.0
TL074CNSR	SO	NS	14	2000	356.0	356.0	35.0
TL074CPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TL074HIDR	SOIC	D	14	2500	356.0	356.0	35.0
TL074HIDYYR	SOT-23-THIN	DYY	14	3000	336.6	336.6	31.8
TL074HIPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TL074IDR	SOIC	D	14	2500	340.5	336.1	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
81023052A	FK	LCCC	20	1	506.98	12.06	2030	NA
8102305HA	U	CFP	10	1	506.98	26.16	6220	NA
81023062A	FK	LCCC	20	1	506.98	12.06	2030	NA
8102306DA	W	CFP	14	1	506.98	26.16	6220	NA
TL071ACP	P	PDIP	8	50	506	13.97	11230	4.32
TL071BCP	P	PDIP	8	50	506	13.97	11230	4.32
TL071CP	P	PDIP	8	50	506	13.97	11230	4.32
TL071CPE4	P	PDIP	8	50	506	13.97	11230	4.32
TL071IP	P	PDIP	8	50	506	13.97	11230	4.32
TL072ACP	P	PDIP	8	50	506	13.97	11230	4.32
TL072ACPE4	P	PDIP	8	50	506	13.97	11230	4.32
TL072BCD	D	SOIC	8	75	507	8	3940	4.32
TL072BCDE4	D	SOIC	8	75	507	8	3940	4.32
TL072BCDG4	D	SOIC	8	75	507	8	3940	4.32
TL072BCP	P	PDIP	8	50	506	13.97	11230	4.32
TL072CP	P	PDIP	8	50	506	13.97	11230	4.32
TL072CPE4	P	PDIP	8	50	506	13.97	11230	4.32
TL072CPS	PS	SOP	8	80	530	10.5	4000	4.1
TL072IP	P	PDIP	8	50	506	13.97	11230	4.32
TL072IPE4	P	PDIP	8	50	506	13.97	11230	4.32
TL072MFKB	FK	LCCC	20	1	506.98	12.06	2030	NA
TL072MUB	U	CFP	10	1	506.98	26.16	6220	NA
TL074ACD	D	SOIC	14	50	507	8	3940	4.32
TL074ACDE4	D	SOIC	14	50	507	8	3940	4.32
TL074ACN	N	PDIP	14	25	506	13.97	11230	4.32
TL074ACNE4	N	PDIP	14	25	506	13.97	11230	4.32
TL074BCD	D	SOIC	14	50	507	8	3940	4.32
TL074BCDE4	D	SOIC	14	50	507	8	3940	4.32
TL074BCN	N	PDIP	14	25	506	13.97	11230	4.32

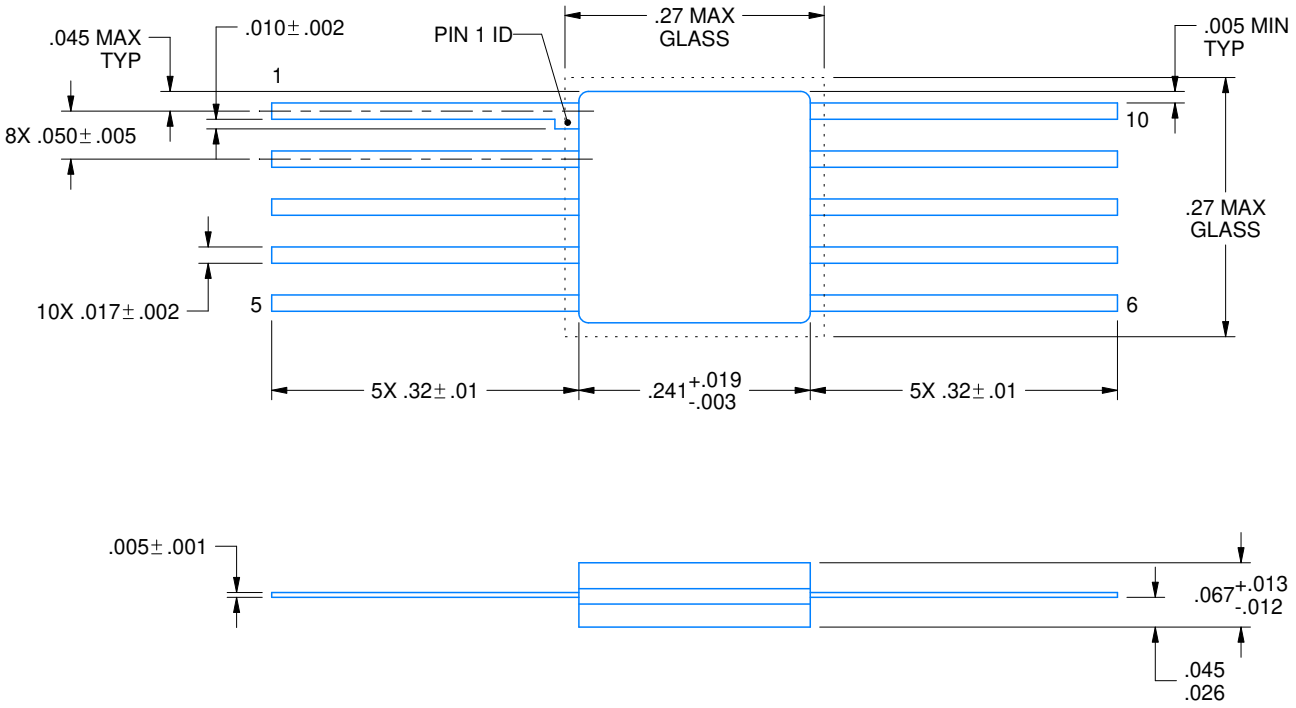
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TL074BCNE4	N	PDIP	14	25	506	13.97	11230	4.32
TL074CD	D	SOIC	14	50	507	8	3940	4.32
TL074CDG4	D	SOIC	14	50	507	8	3940	4.32
TL074CN	N	PDIP	14	25	506	13.97	11230	4.32
TL074CN	N	PDIP	14	25	506	13.97	11230	4.32
TL074CNE4	N	PDIP	14	25	506	13.97	11230	4.32
TL074CNE4	N	PDIP	14	25	506	13.97	11230	4.32
TL074CPW	PW	TSSOP	14	90	530	10.2	3600	3.5
TL074ID	D	SOIC	14	50	507	8	3940	4.32
TL074IDE4	D	SOIC	14	50	507	8	3940	4.32
TL074IDG4	D	SOIC	14	50	507	8	3940	4.32
TL074IN	N	PDIP	14	25	506	13.97	11230	4.32
TL074MFK	FK	LCCC	20	1	506.98	12.06	2030	NA
TL074MFKB	FK	LCCC	20	1	506.98	12.06	2030	NA
TL074MWB	W	CFP	14	1	506.98	26.16	6220	NA

U0010A

PACKAGE OUTLINE

CFP - 2.03 mm max height

CERAMIC FLATPACK



4225582/A 01/2020

NOTES:

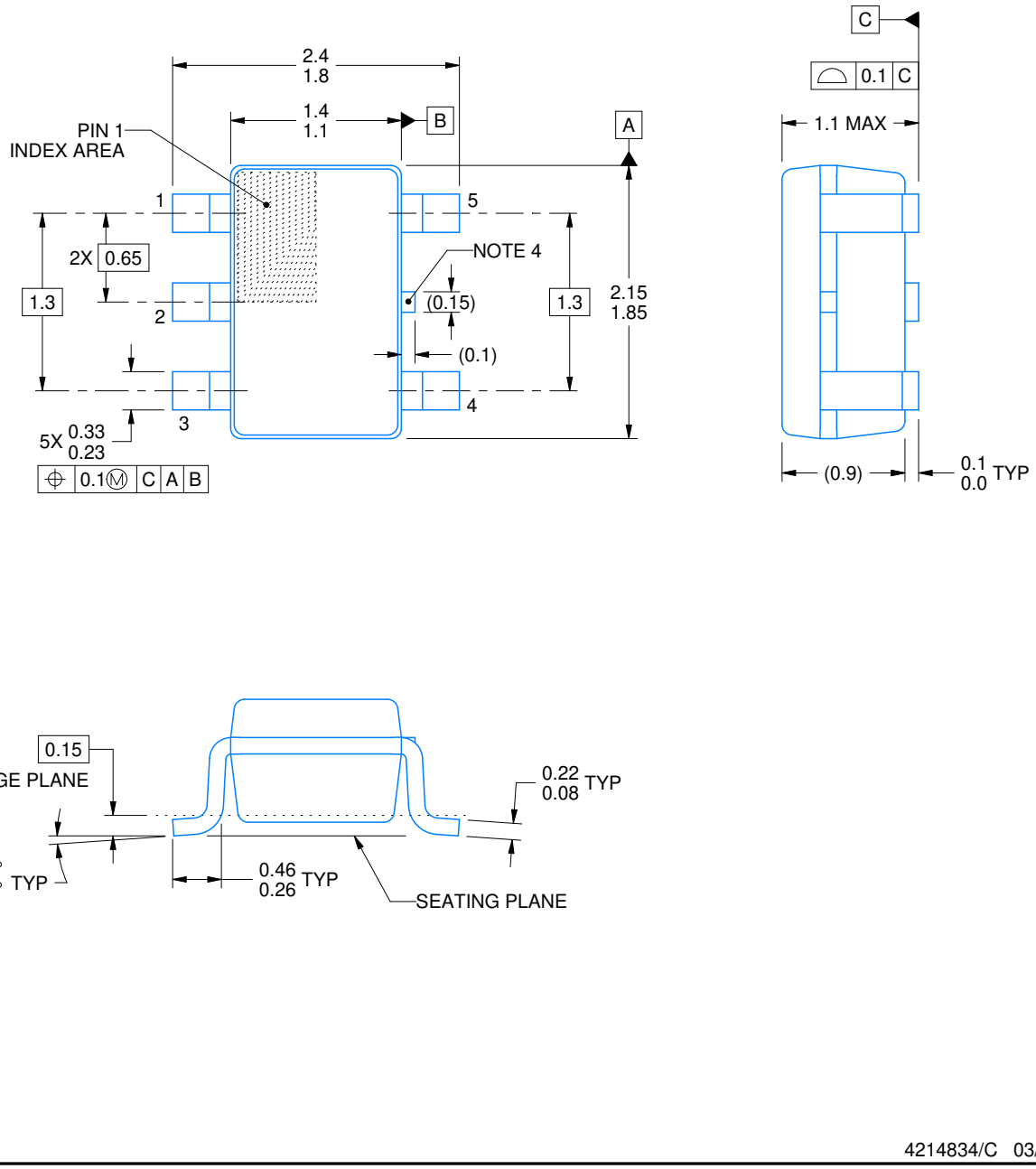
1. All linear dimensions are in inches. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

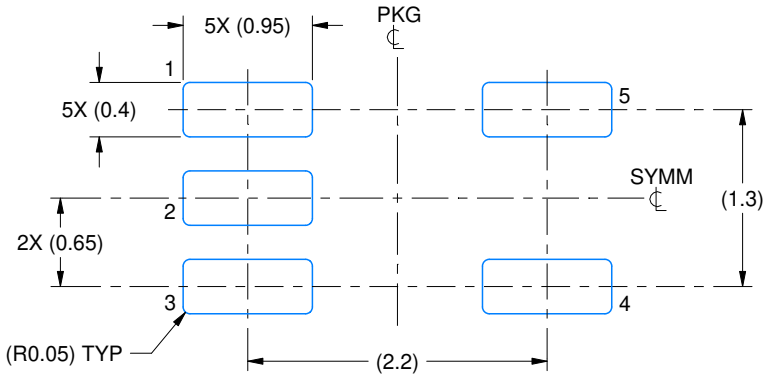
SMALL OUTLINE TRANSISTOR



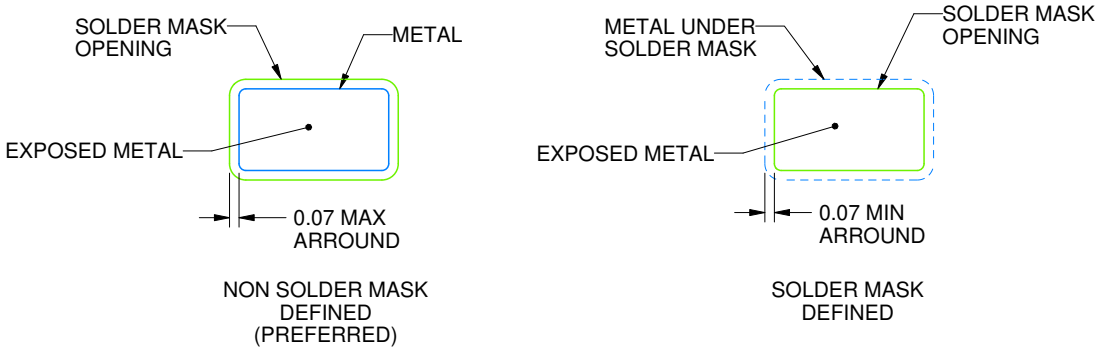
4214834/C 03/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

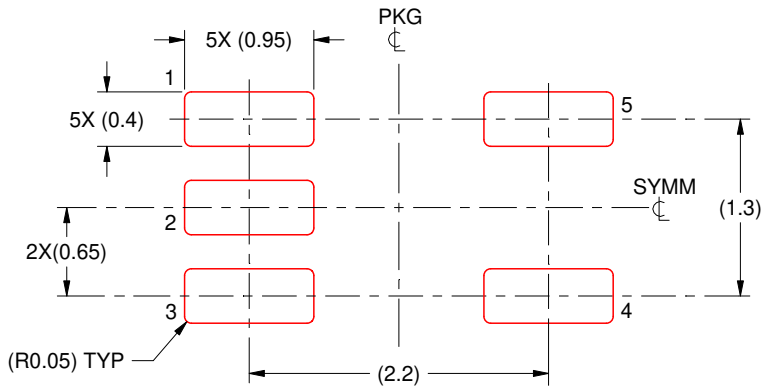


SOLDER MASK DETAILS

4214834/C 03/2023

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/C 03/2023

NOTES: (continued)

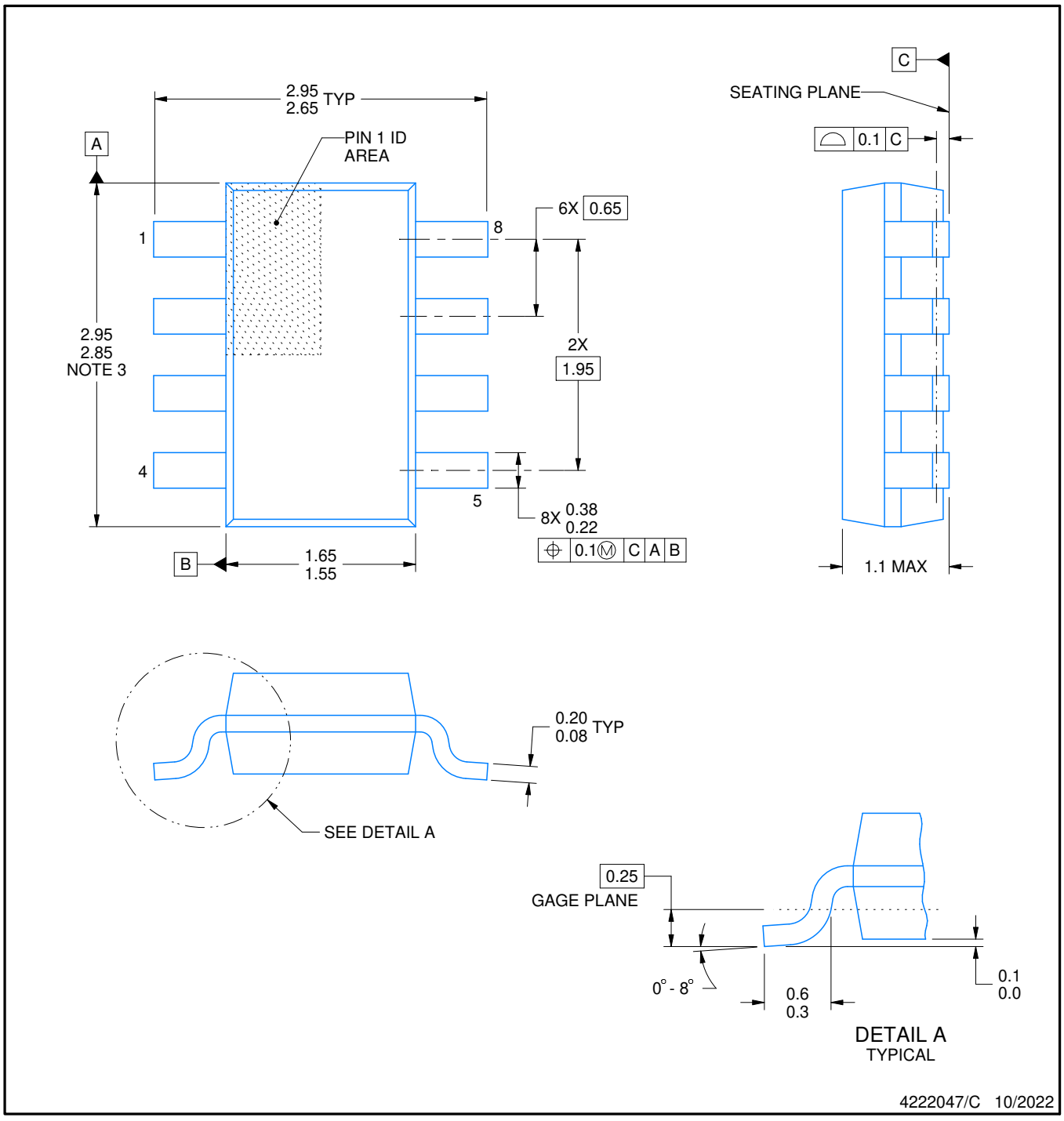
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DDF0008A

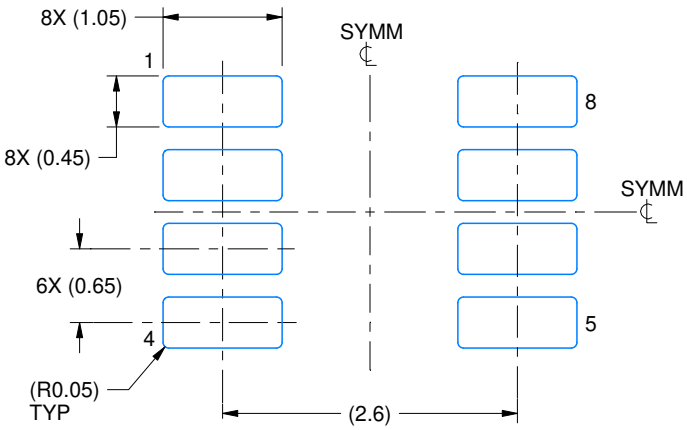
SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE

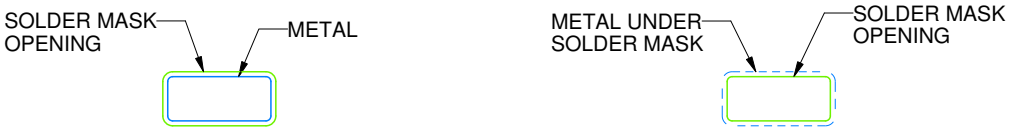


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
SCALE:15X



NON SOLDER MASK
DEFINED

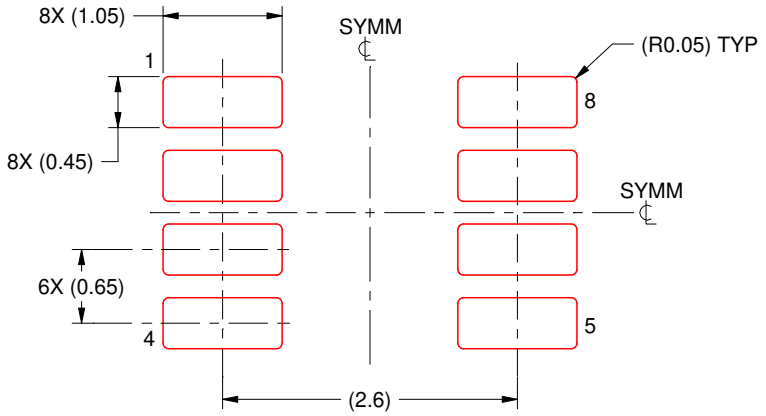
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4222047/C 10/2022

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/C 10/2022

NOTES: (continued)

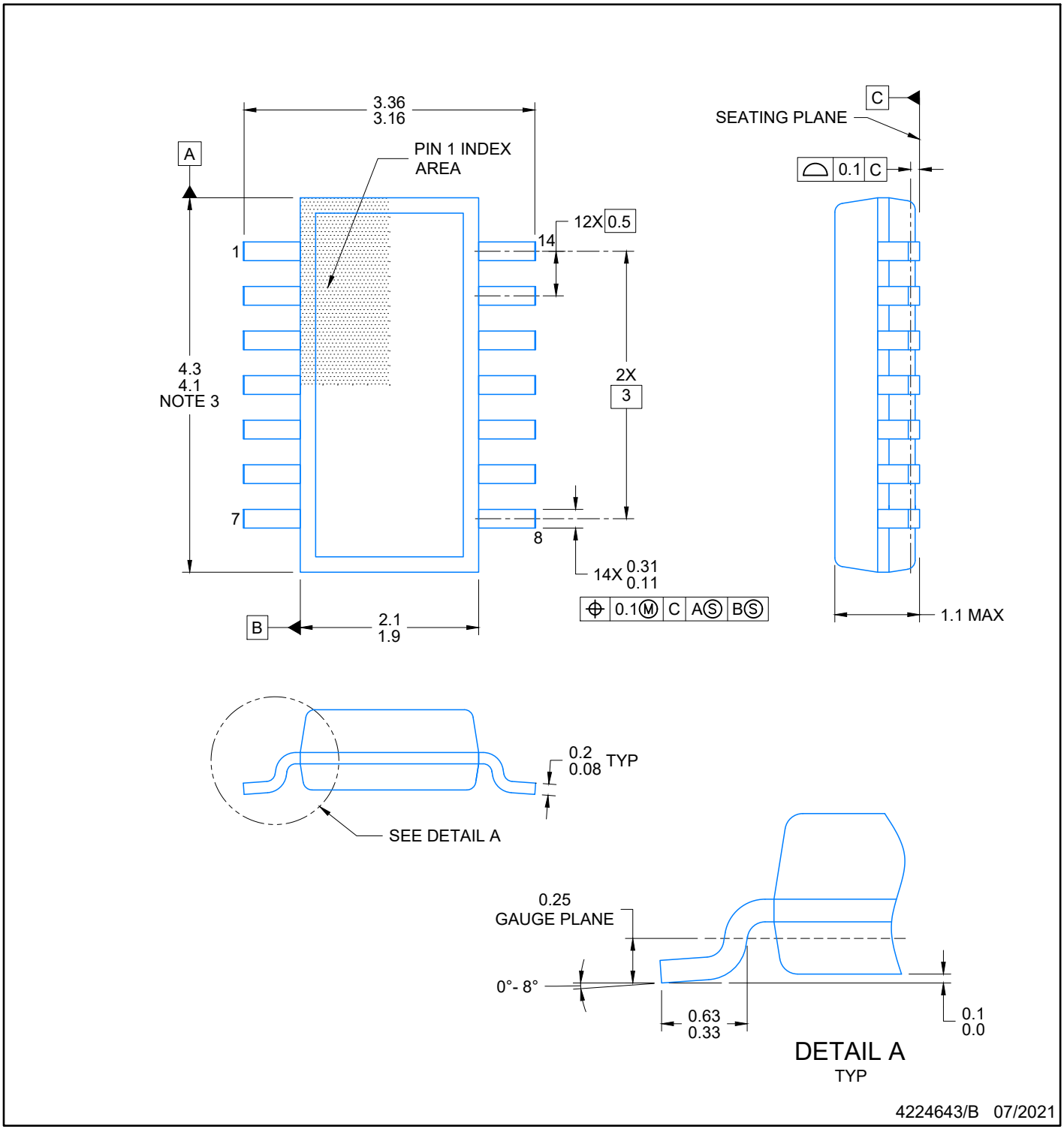
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DYY0014A

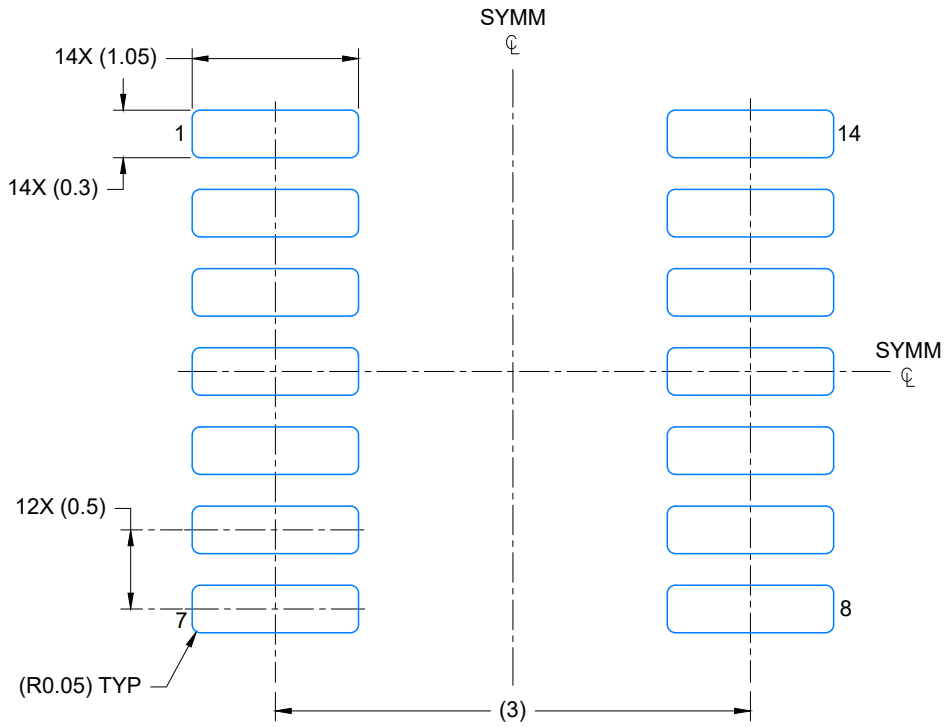
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

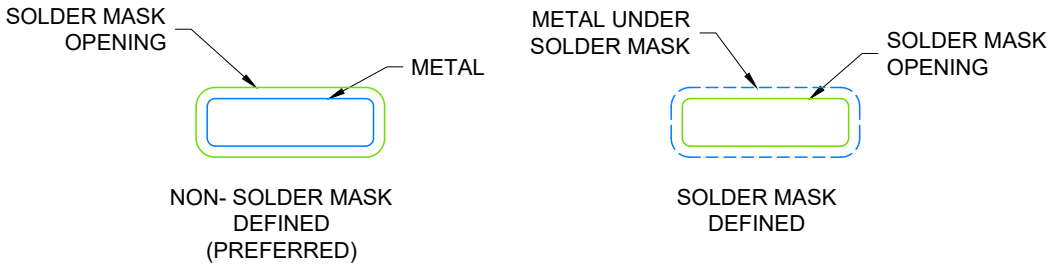


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

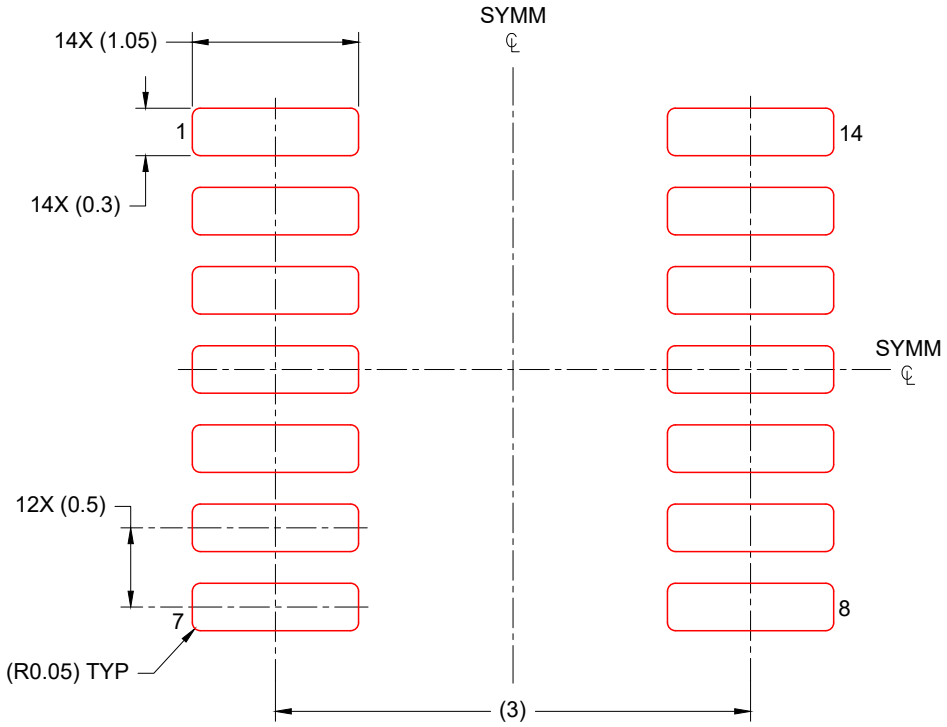


SOLDER MASK DETAILS

4224643/B 07/2021

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224643/B 07/2021

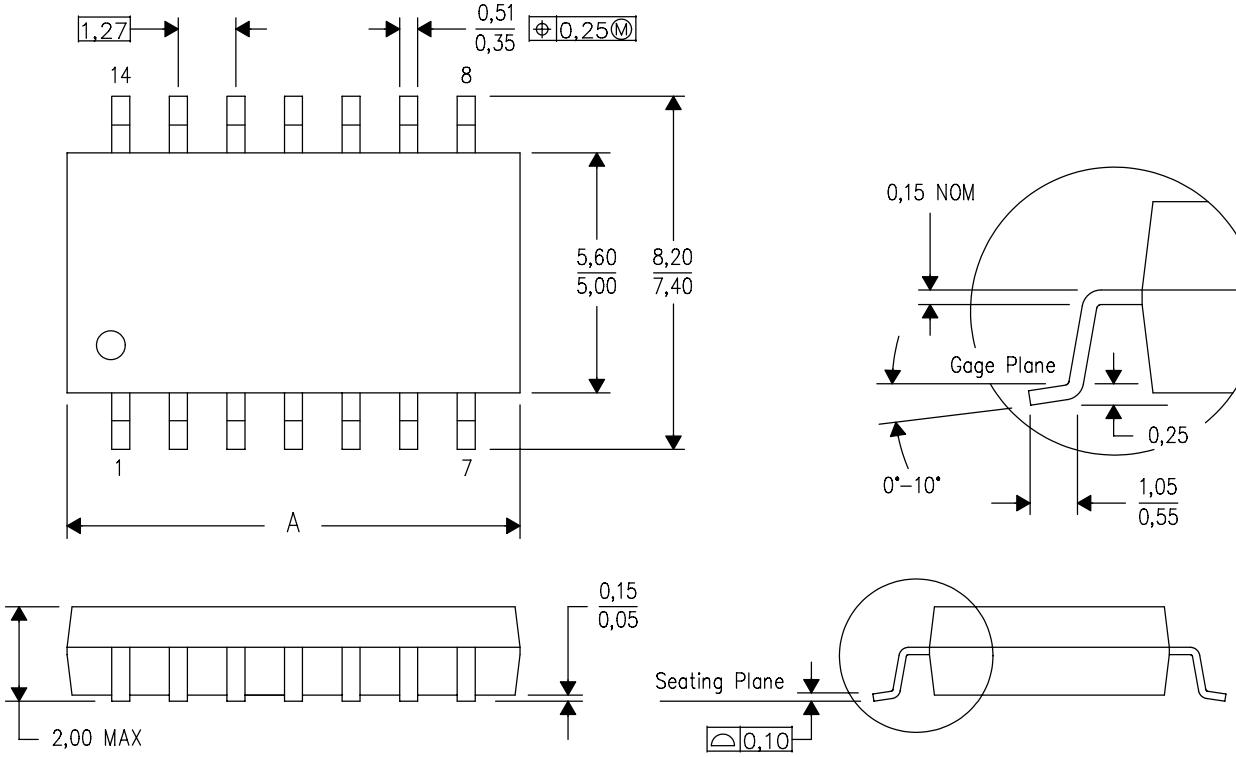
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

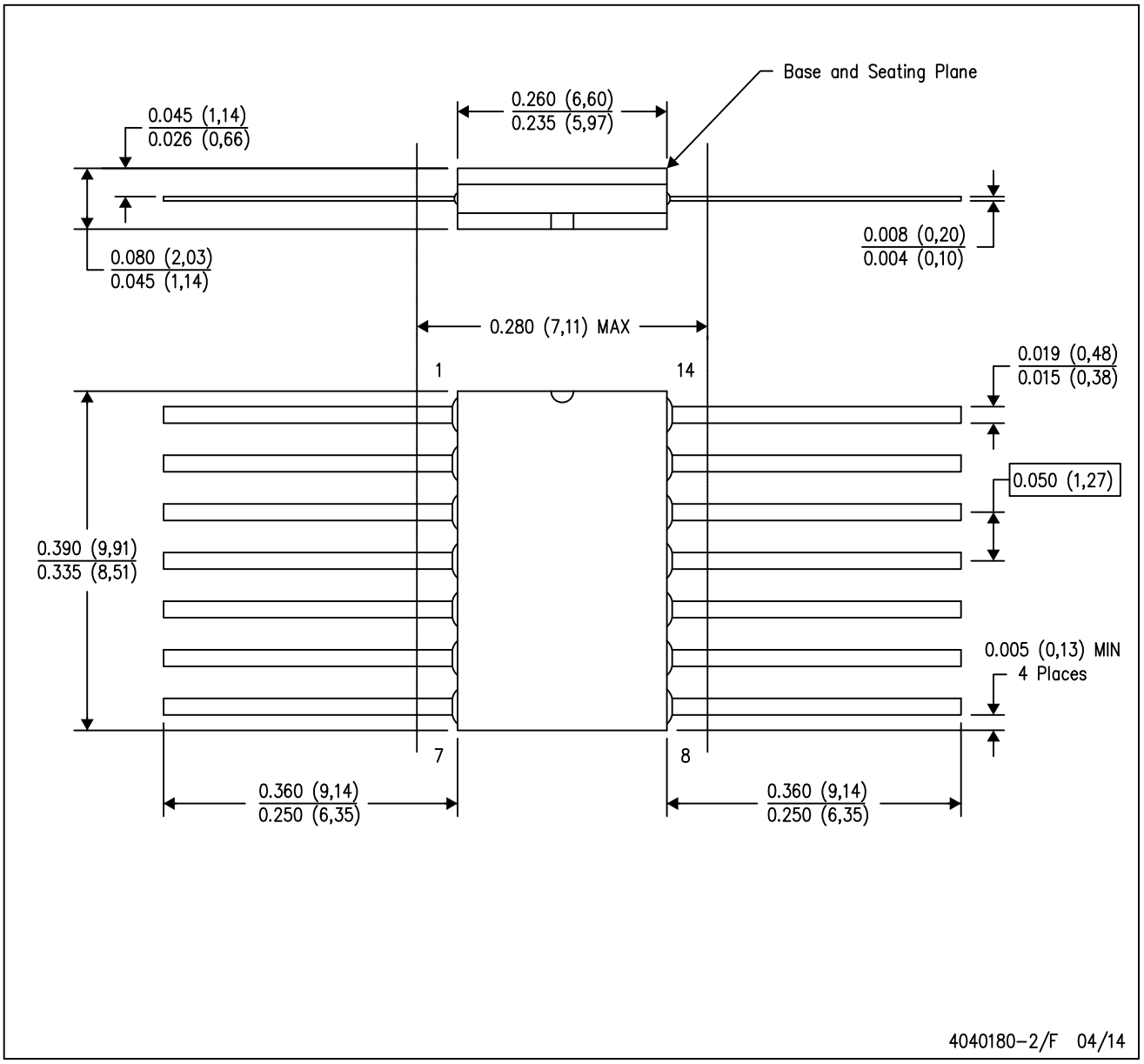


DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R–GDFP–F14) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

GENERIC PACKAGE VIEW

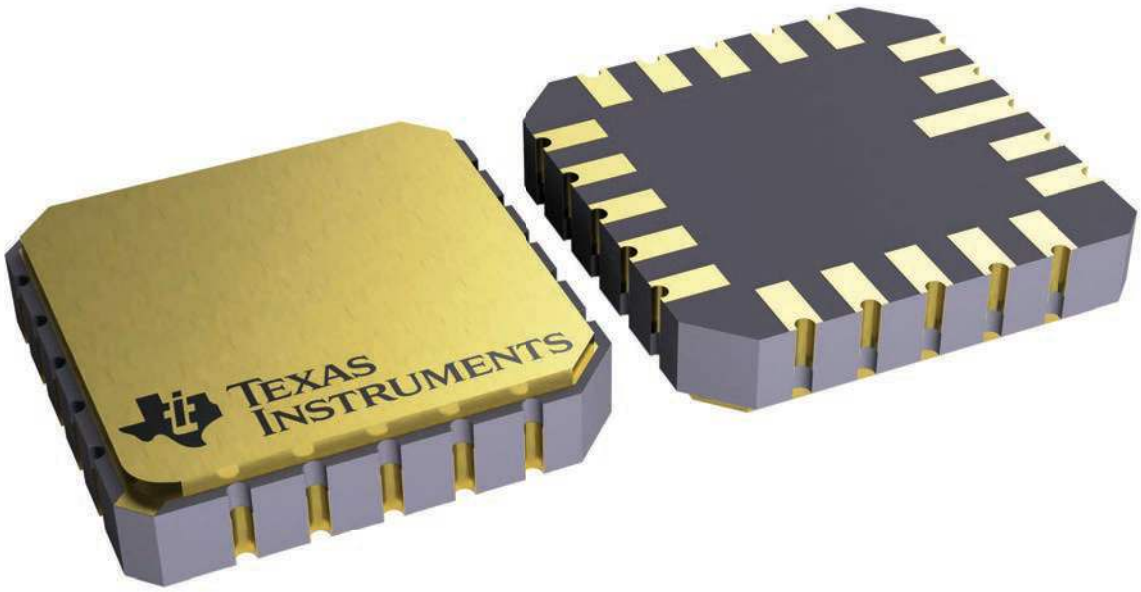
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

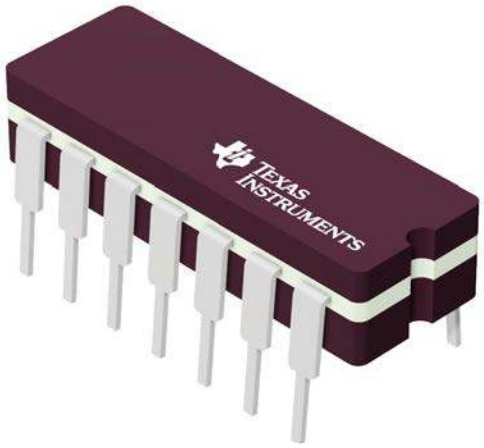


4229370\VA\

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

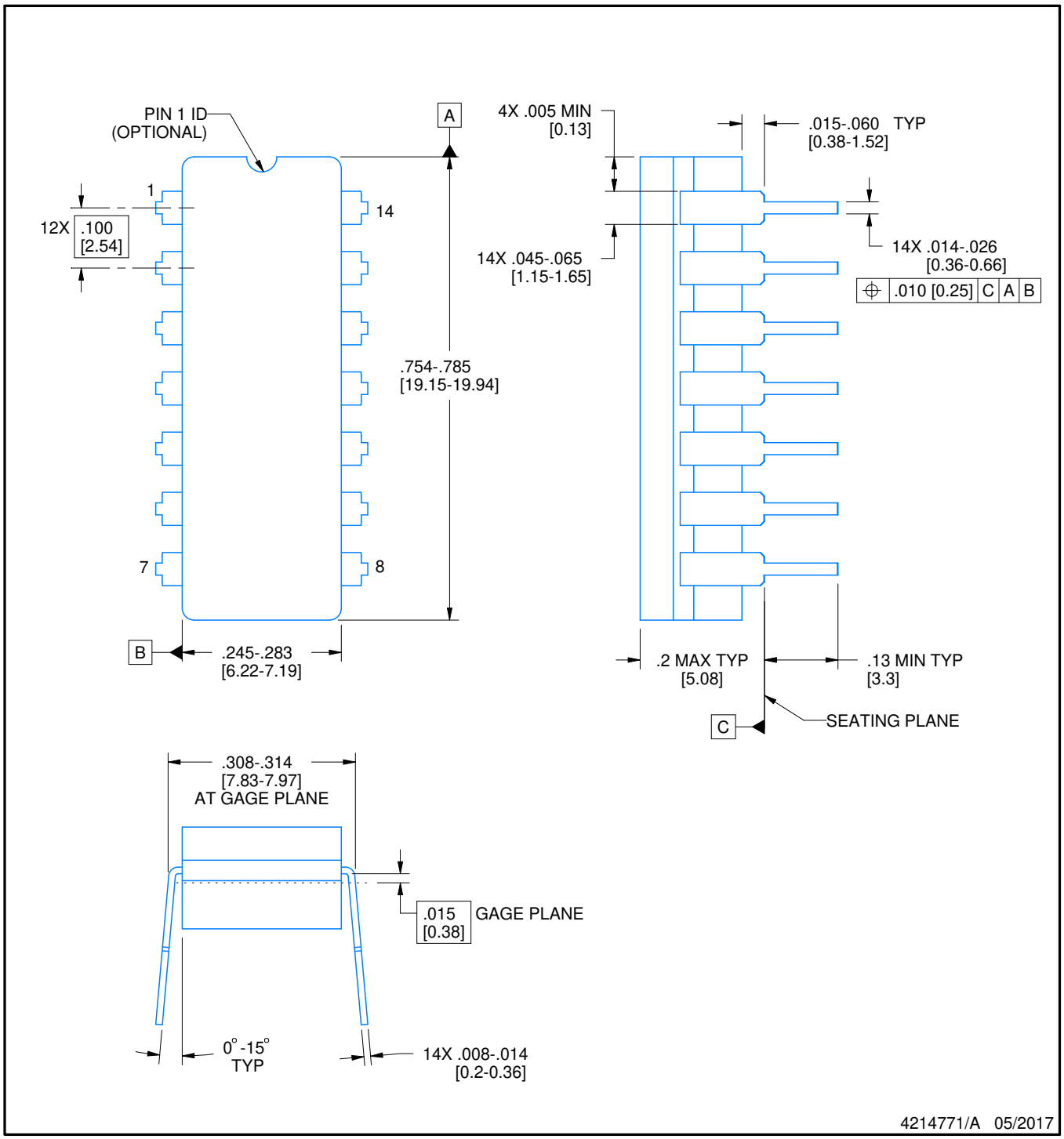
4040083-5/G

PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

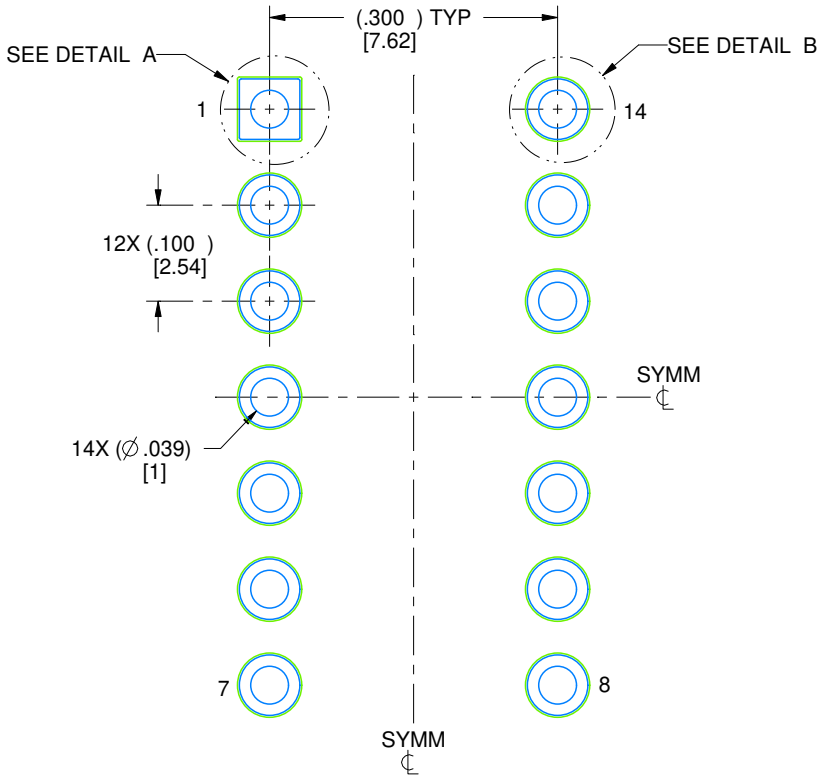
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

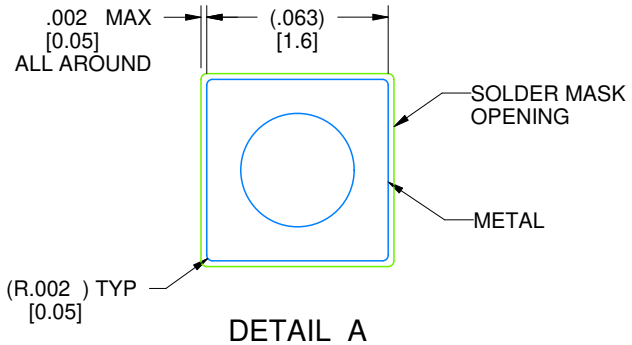
J0014A

CDIP - 5.08 mm max height

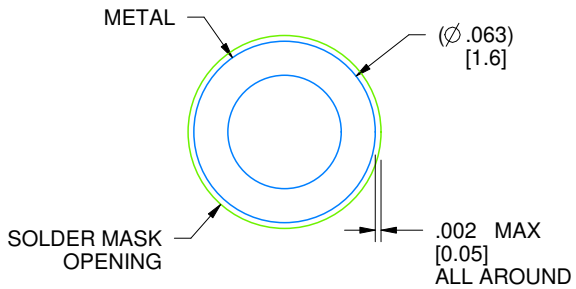
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

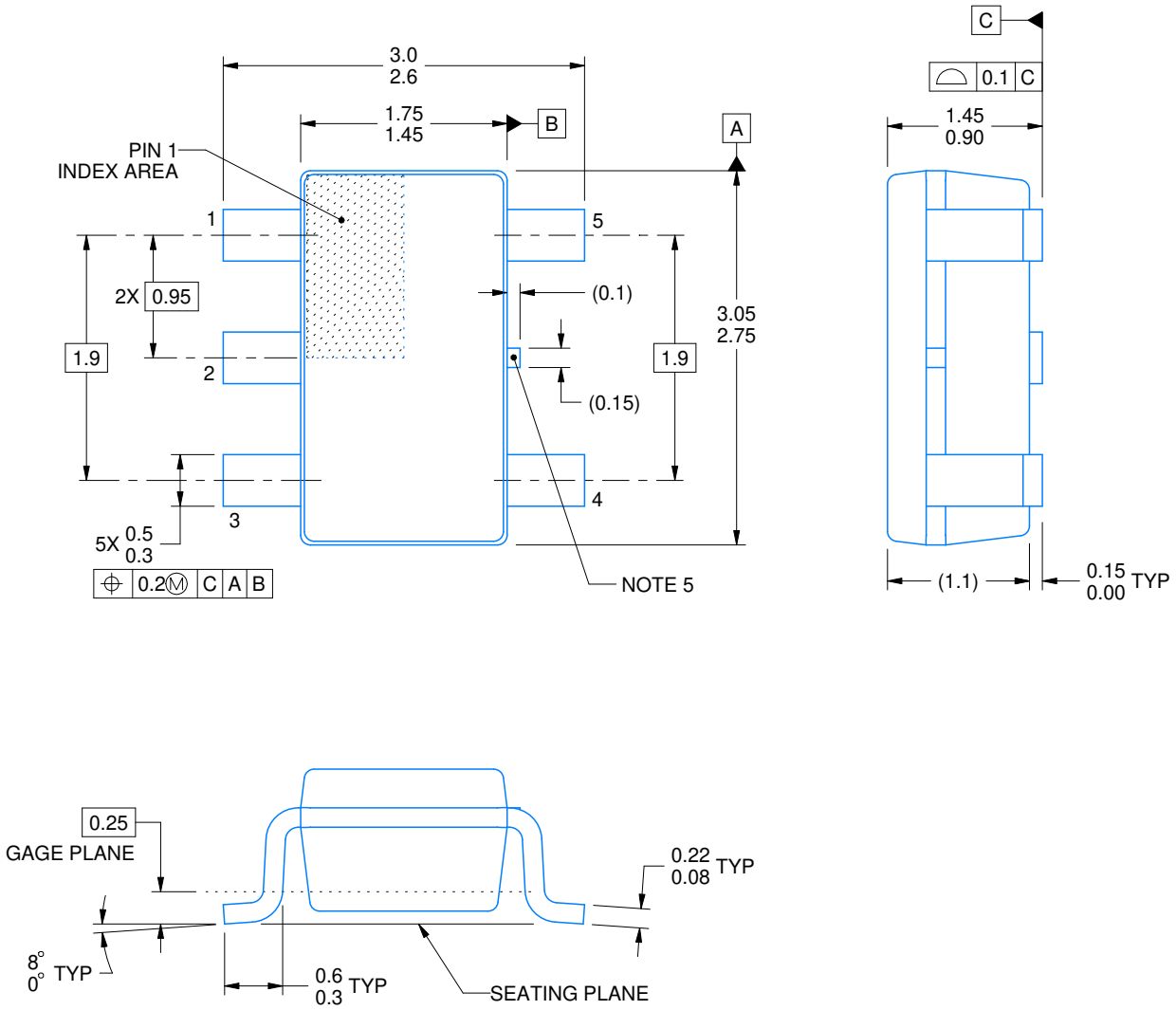
4214771/A 05/2017

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

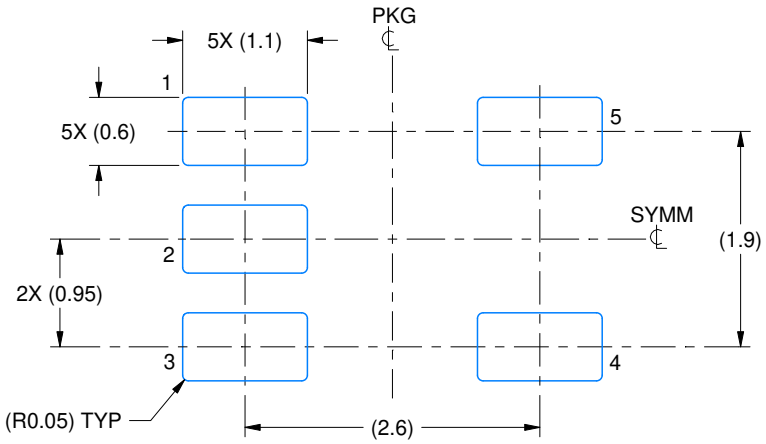
SMALL OUTLINE TRANSISTOR



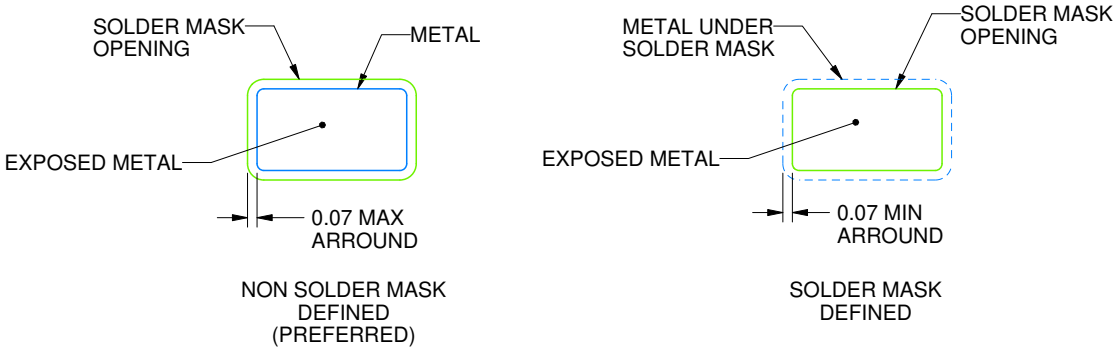
4214839/G 03/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

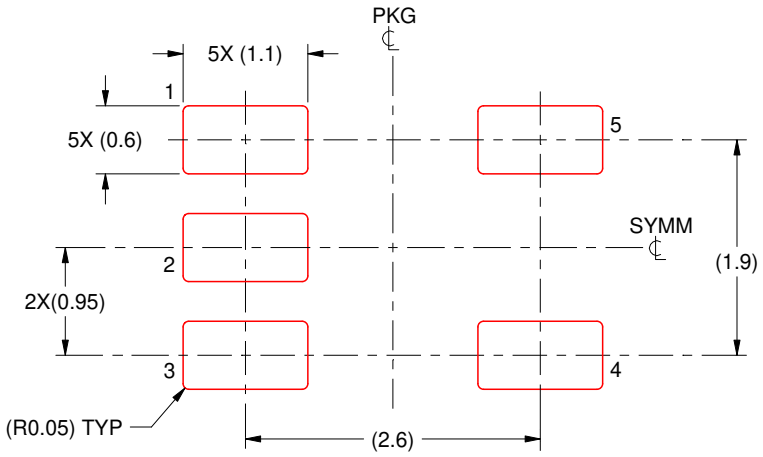


SOLDER MASK DETAILS

4214839/G 03/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



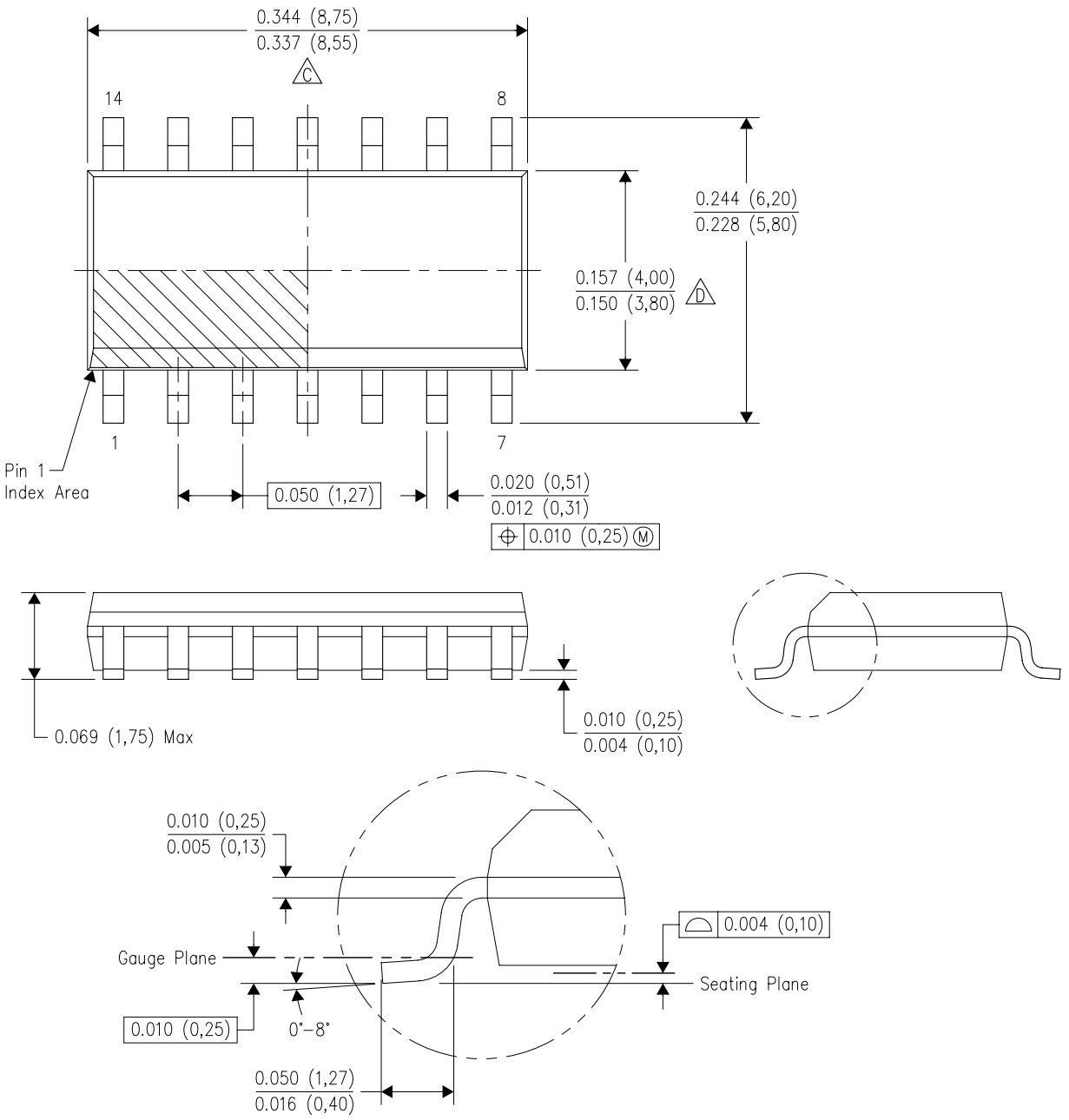
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/G 03/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

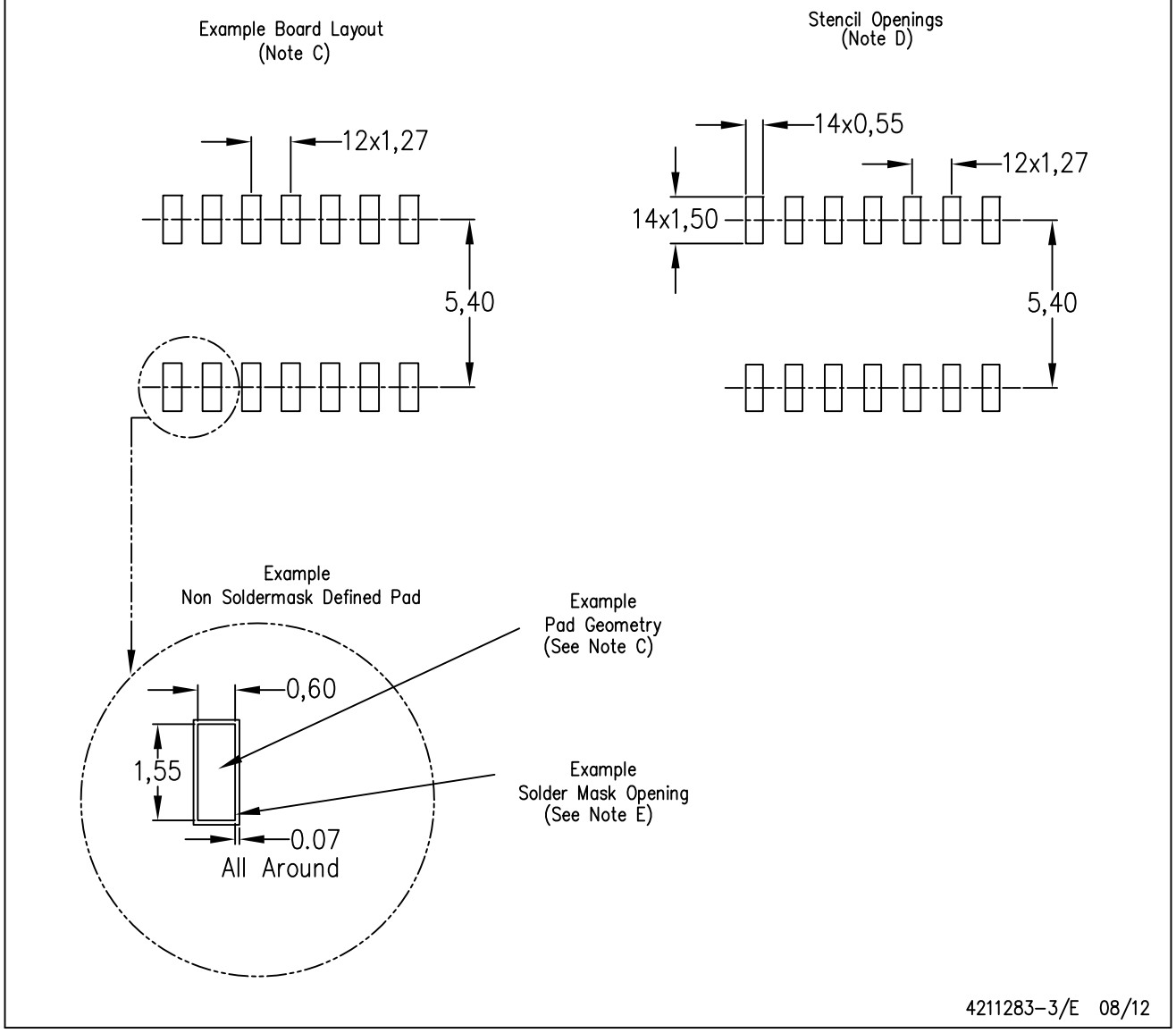
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

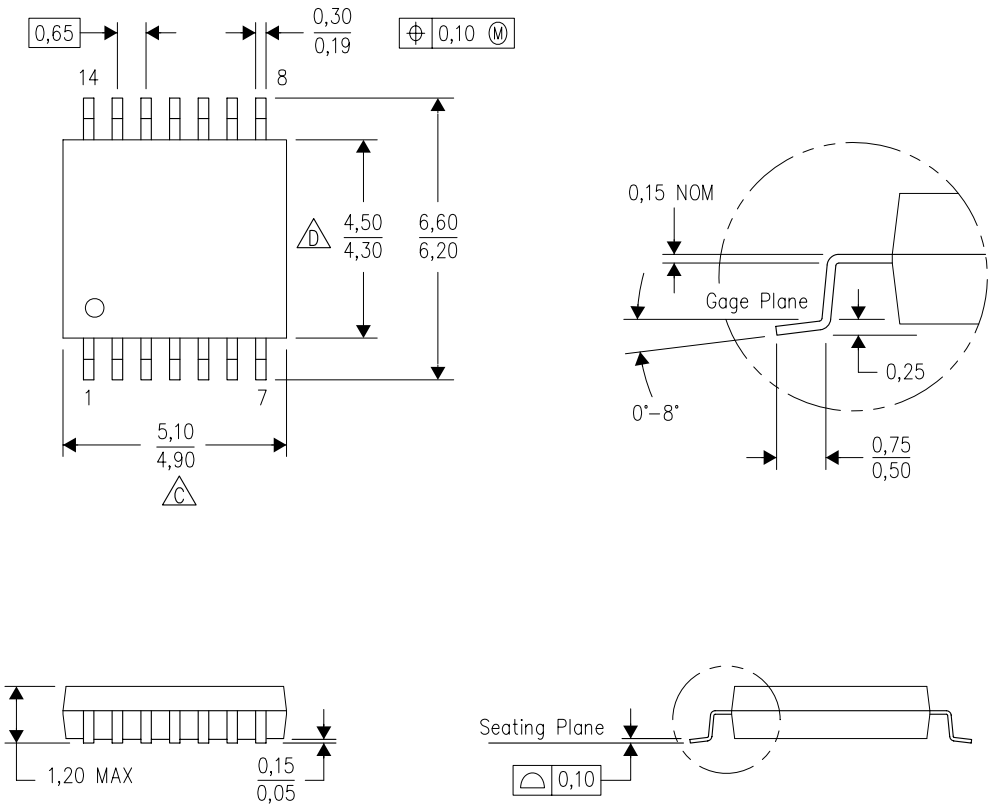
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



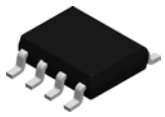
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

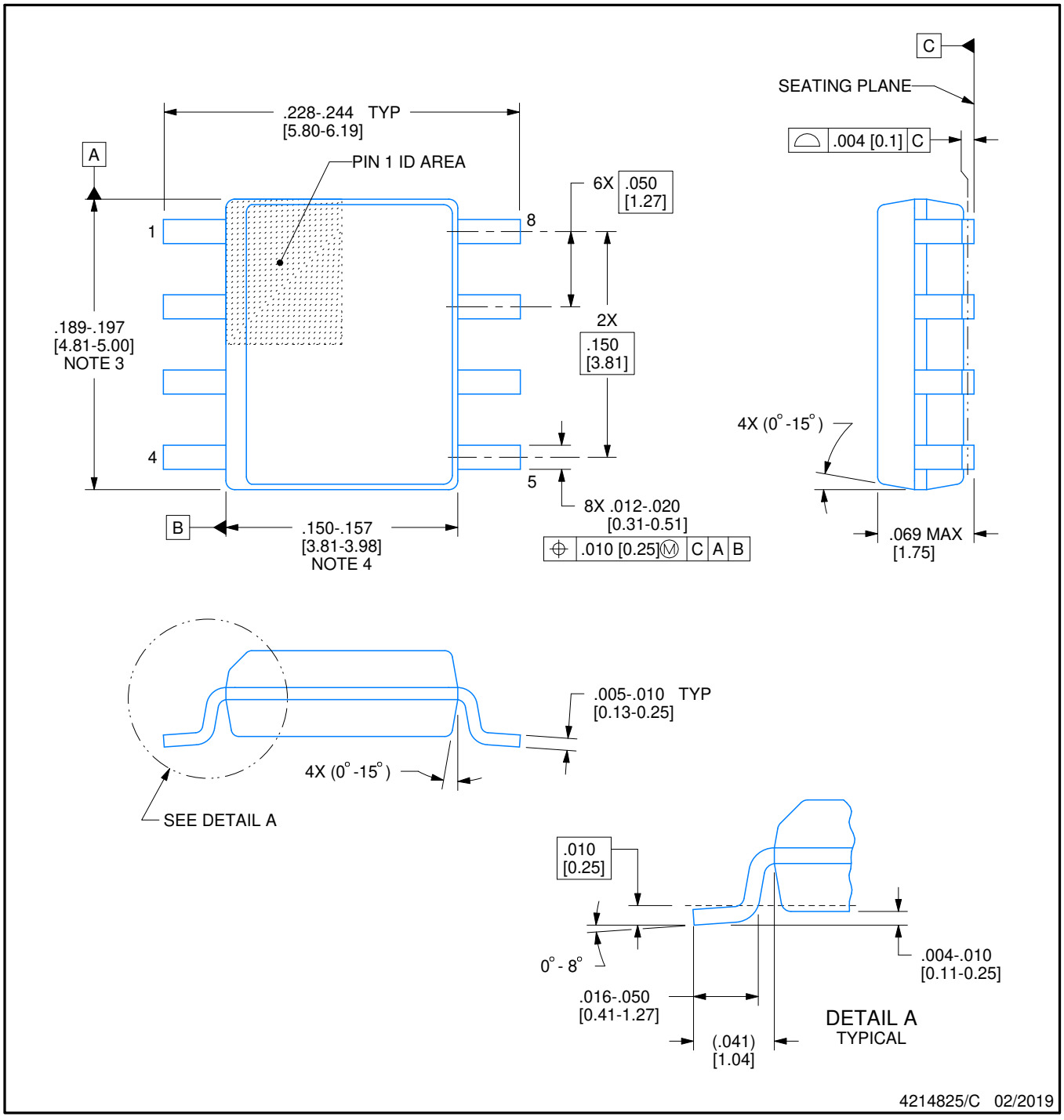


PACKAGE OUTLINE

D0008A

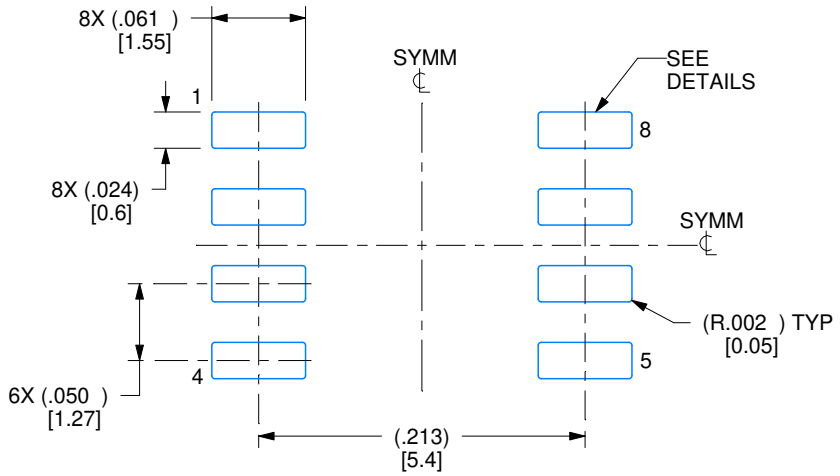
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

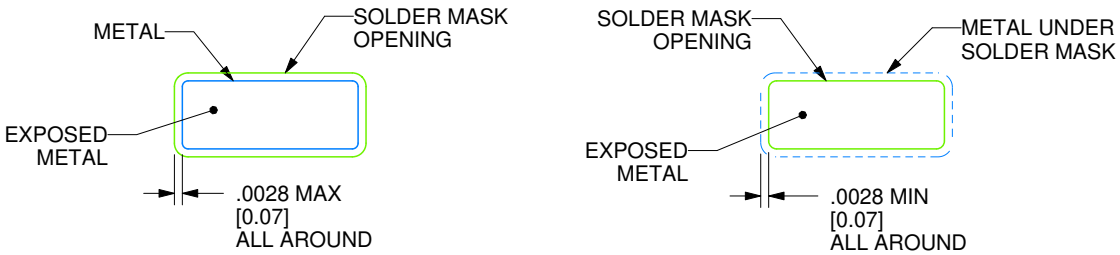


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

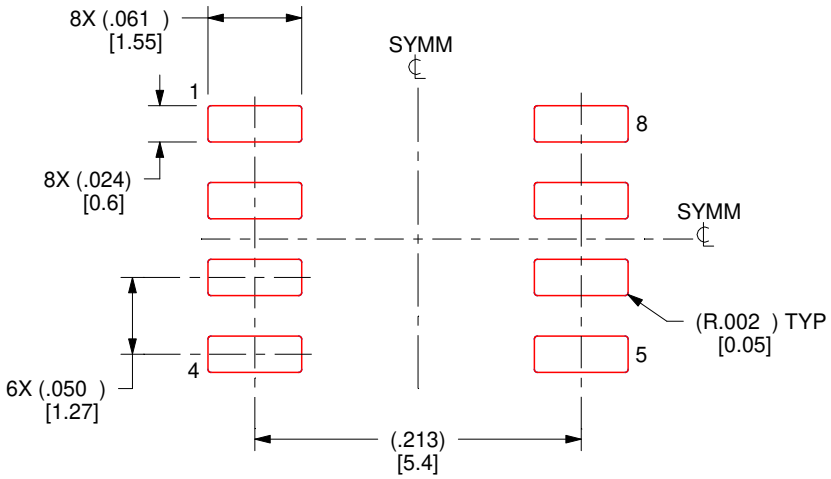
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

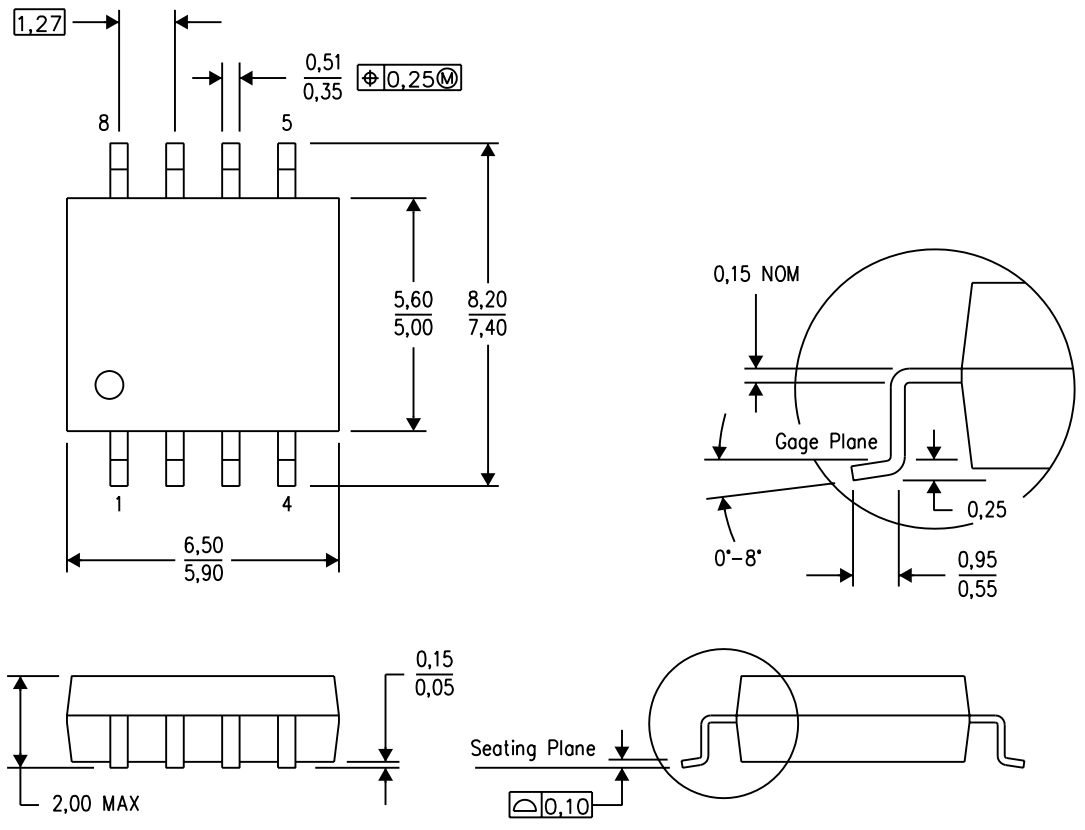
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

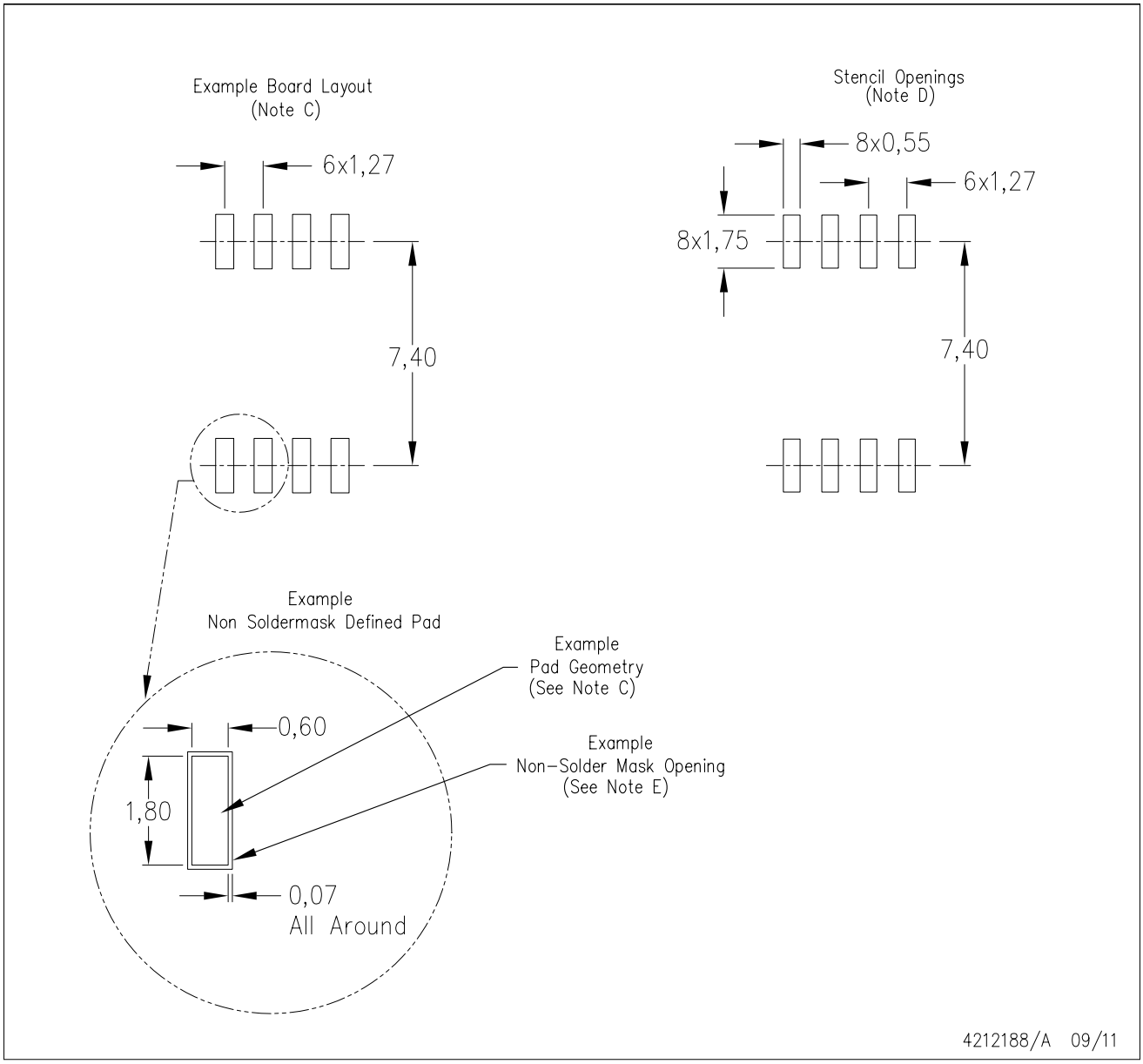
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

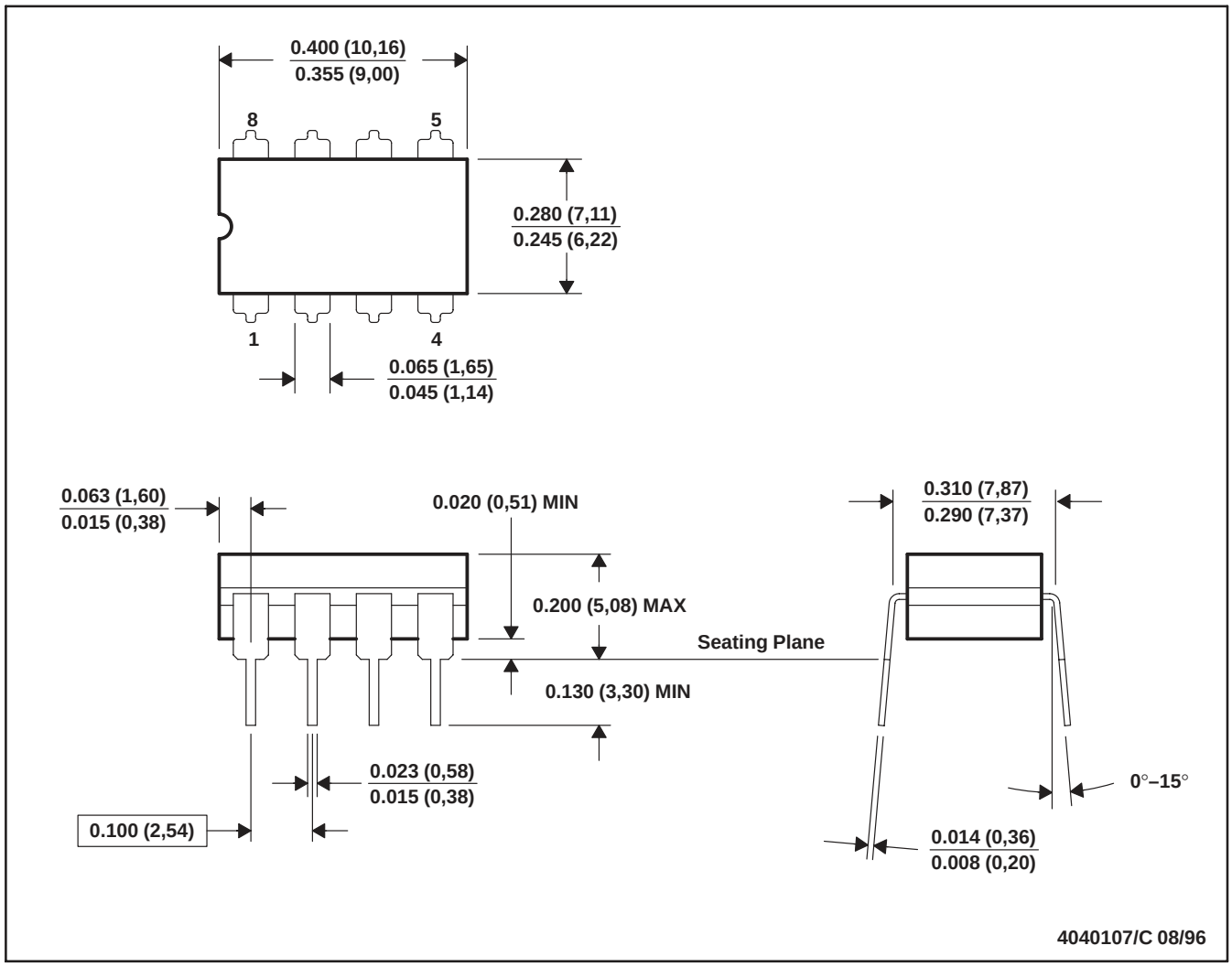
PS (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

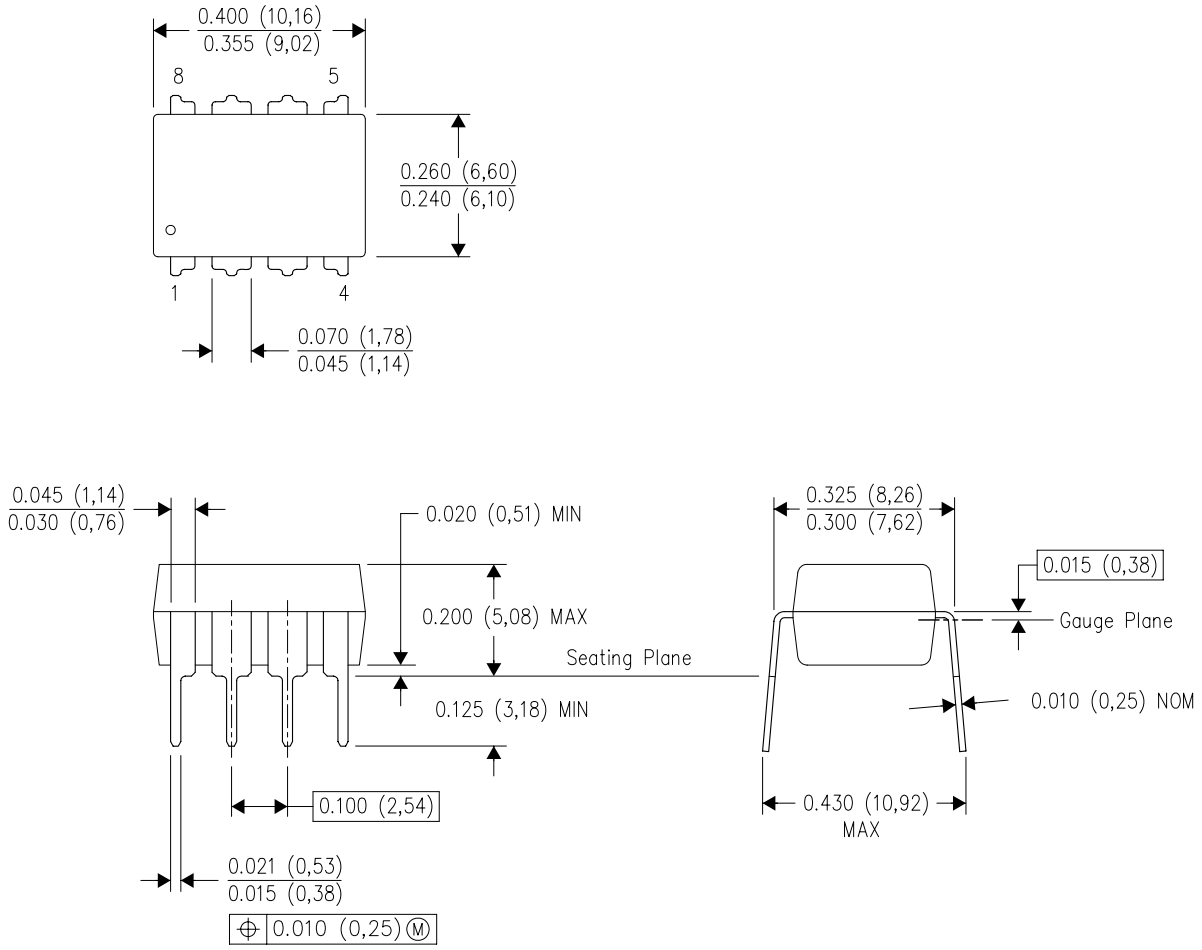
MCER001A – JANUARY 1995 – REVISED JANUARY 1997

JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE

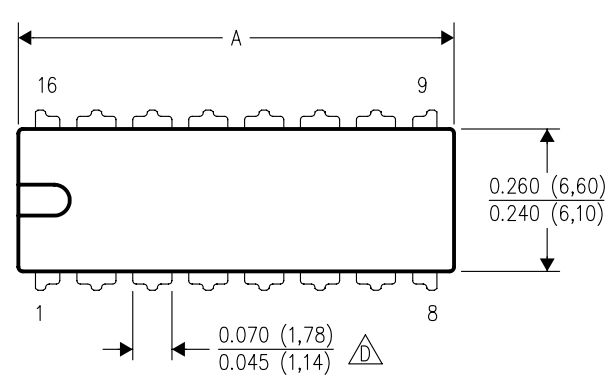


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

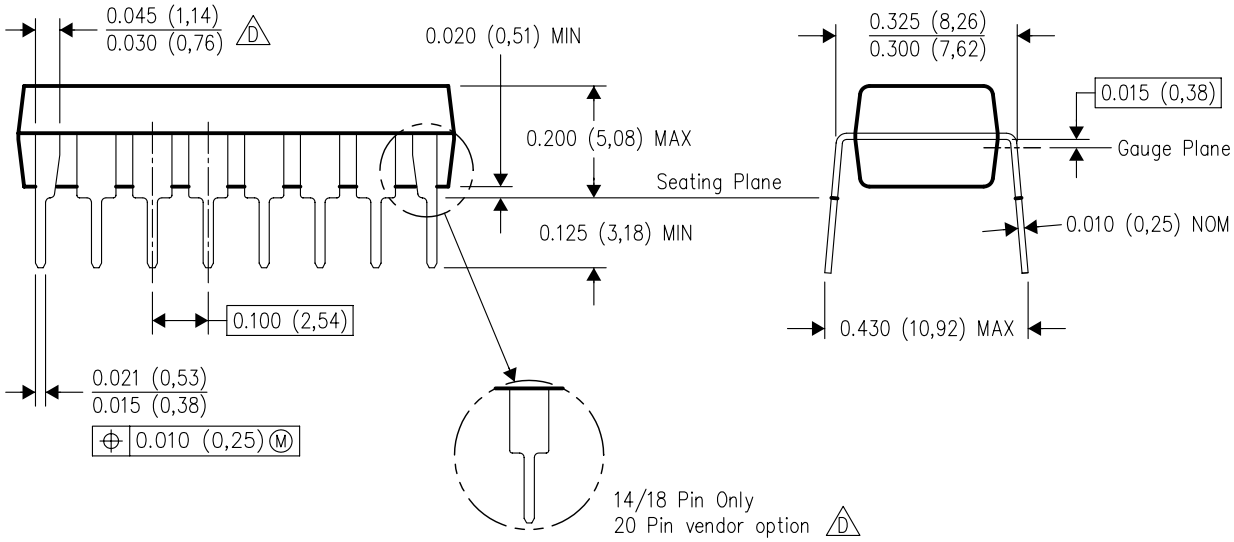
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

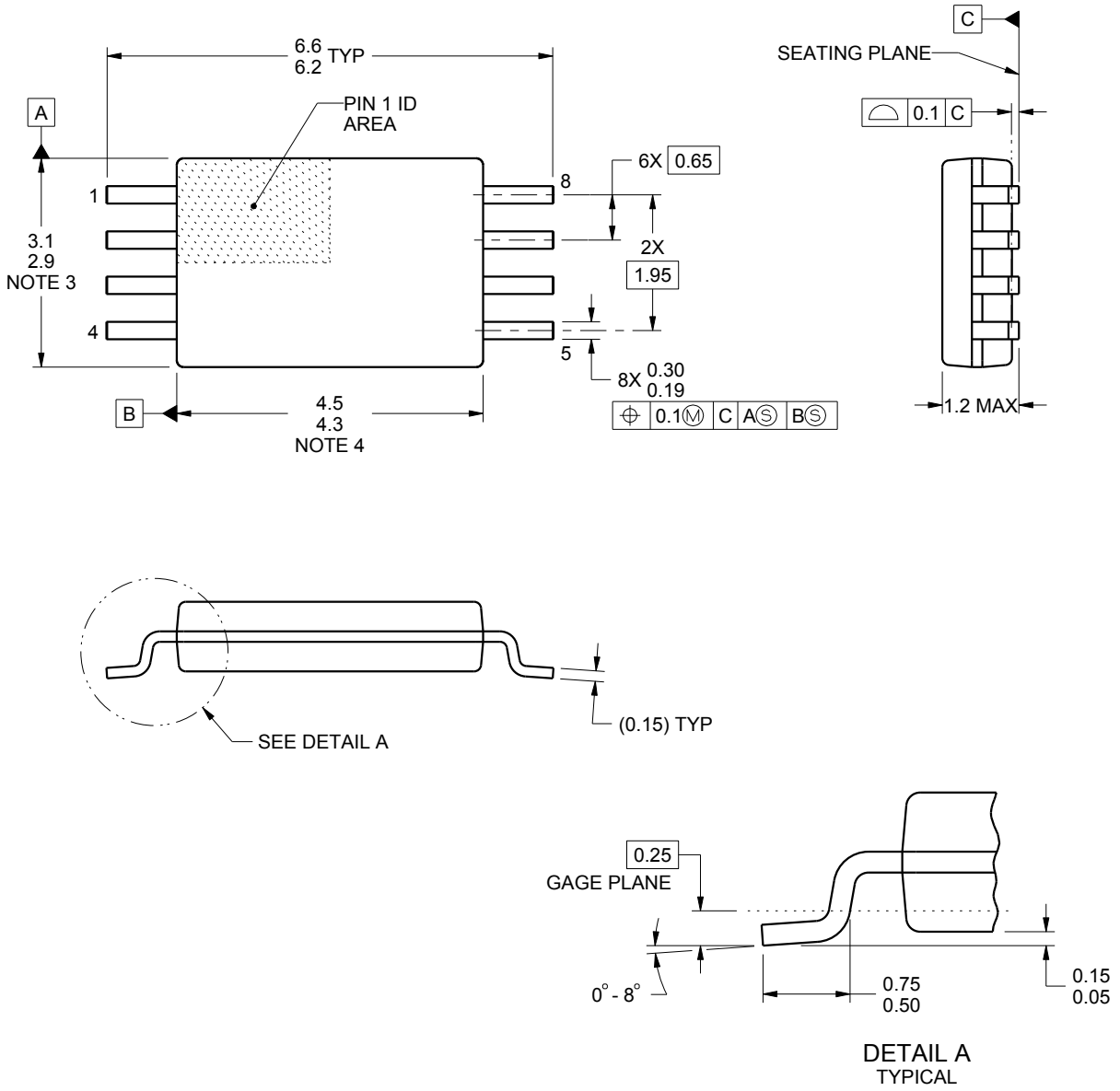
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

PACKAGE OUTLINE

PW0008A

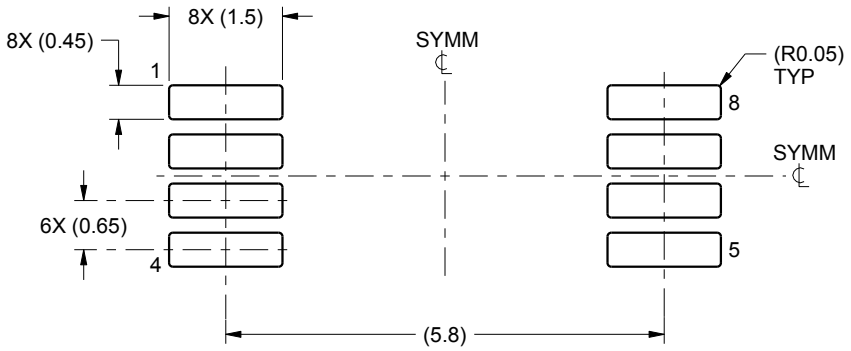
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

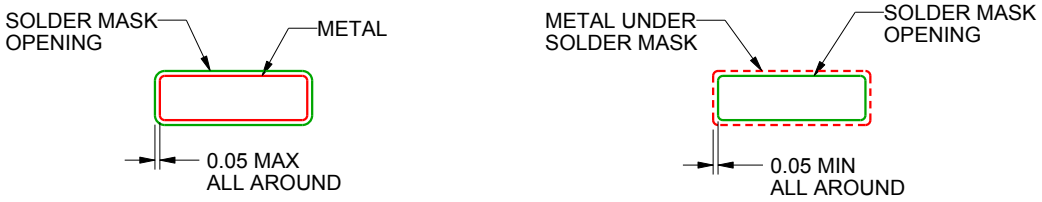


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

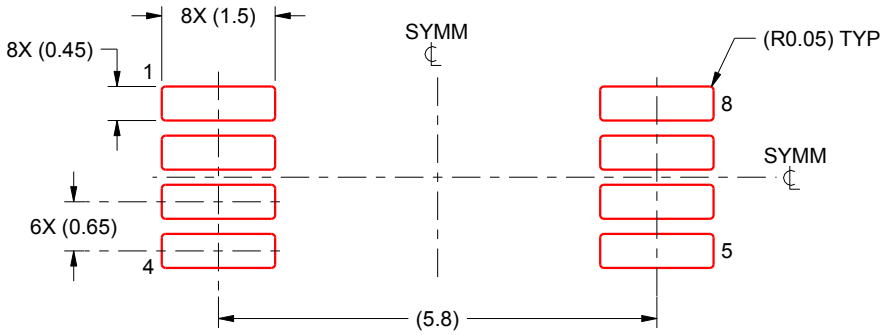


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

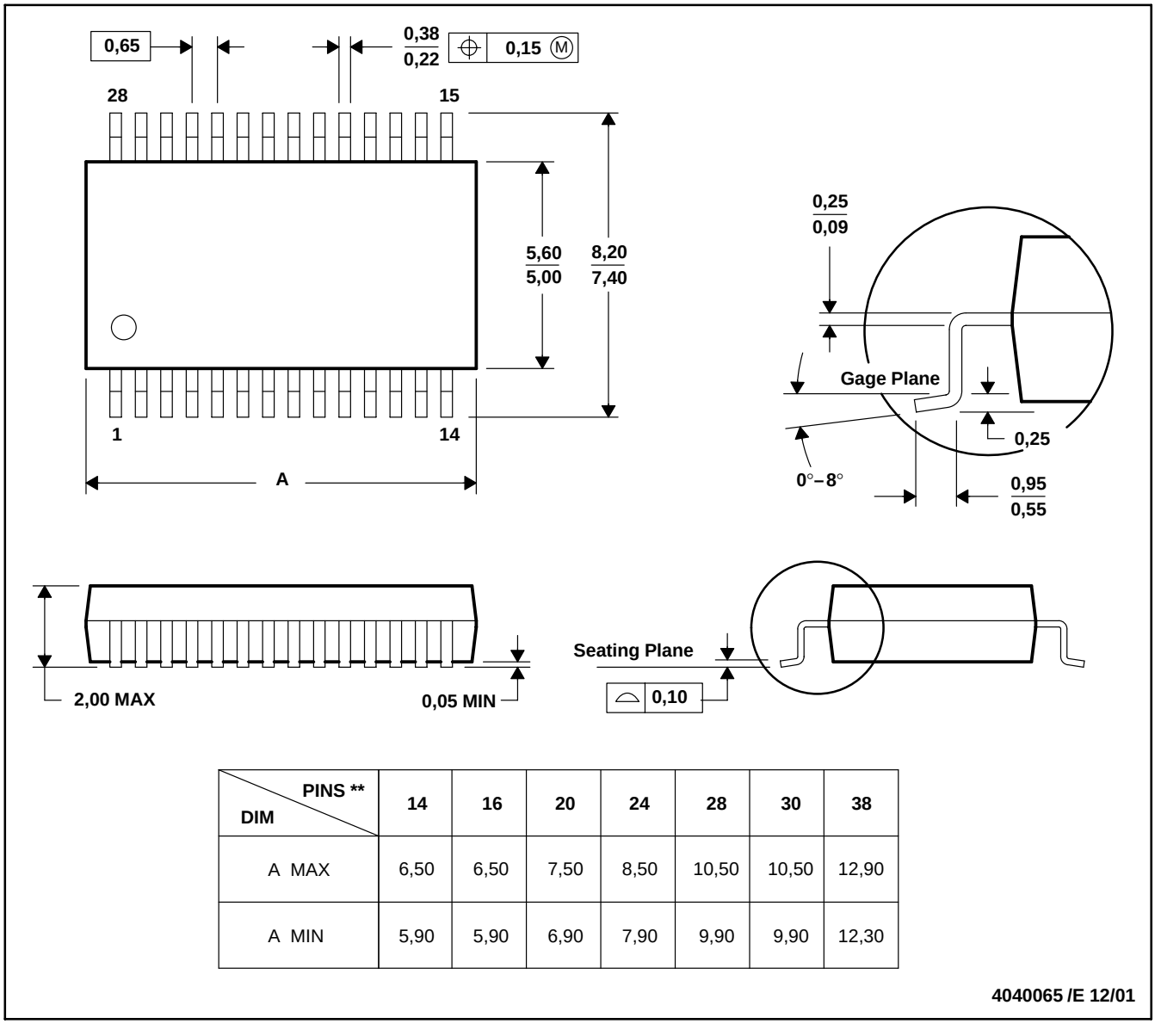
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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