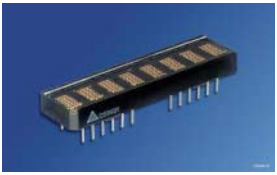
5.10 mm (0.200") 8-Character 5x7 Dot Matrix Parallel Input Alphanumeric Intelligent Display® Devices

Lead (Pb) Free Product - RoHS Compliant



Red	**PDSP2110**
Yellow	**PDSP2111**
Super-red	**PDSP2112**
Green	**PDSP2113**
High Efficiency Green	**PDSP2114**

DESCRIPTION

The PDSP2110 (Red), PDSP2111 (Yellow), PDSP2112 (Super-red), PDSP2113 (Green), and PDSP2114 (High Efficiency Green) are eight digit, 5 x 7 dot matrix, parallel input, alphanumeric Intelligent Display devices. The 5.10 mm (0.200”) high digits are packaged in a rugged, high quality, optically transparent, 15.24 mm (0.6”) lead spacing, 28 pin plastic DIP.

The on-board CMOS has a built-in 256 character ROM. Both pages are mask programmable for 256 custom characters.The first page of ROM of a standard product contains 128 characters including ASCII, selected European and Scientific symbols. The second page contains Katakana Japanese characters, more European characters, Avionics, and other graphic symbols.

The PDSP211X is designed for standard microprocessor interface techniques, and is fully TTL compatible. The Clock I/O and Clock Select pins allow the user to cascade multiple display modules.

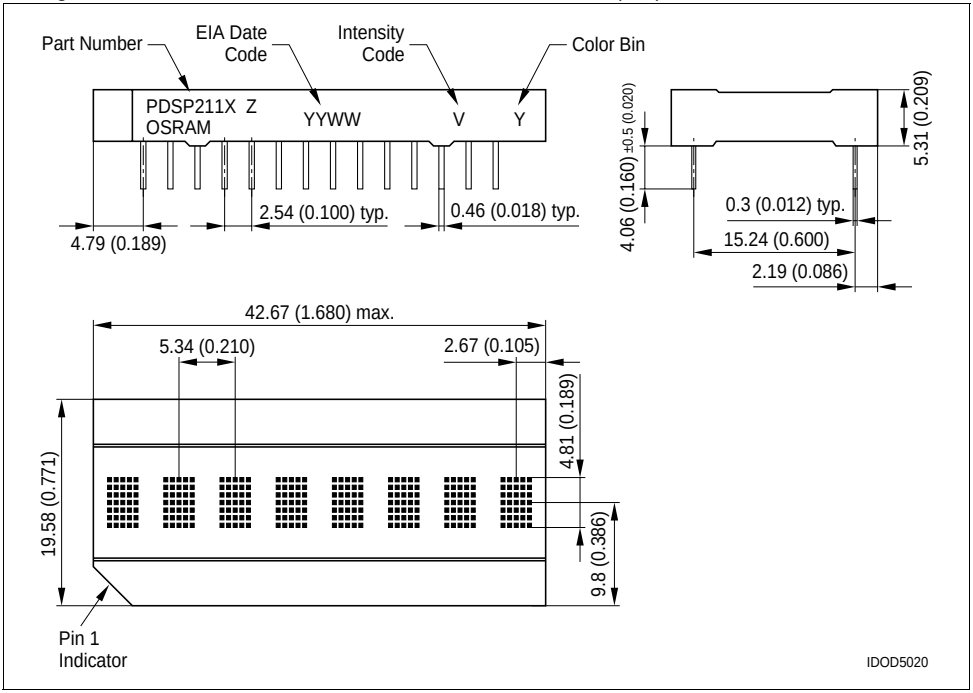
FEATURES

- Eight 5.10 mm (0.200”) Dot Matrix Characters in Red, Yellow, Super-red, Green, High Efficiency Green
- Built-in 2 Page, 256 Character ROM, Both pages are Mask Programmable for Custom Fonts
- Readable from 2.5 meters (8 feet)
- Built-in Decoders, Multiplexers and Drivers
- Wide Viewing Angle, X Axis ± 55°, Y Axis ± 65°
- Programmable Features:
  - Individual Flashing Character
  - Full Display Blinking
  - Multi-Level Dimming and Blanking
  - Clear Function
  - Lamp Test
- Internal or External Clock
- End Stackable Dual-In-Line Plastic Package

Ordering Information

Type	Color of Emission	Character Height mm (inch)	Ordering Code
PDSP2110	red	5.10 (0.200)	Q68000A8474
PDSP2111	yellow		Q68000A8503
PDSP2112	super-red		Q68000A8504
PDSP2113	green		Q68000A8505
PDSP2114	high efficiency green		Q68000A8533

Package Outlines Dimensions in mm (inch)



Maximum Ratings (T_A=25°C)

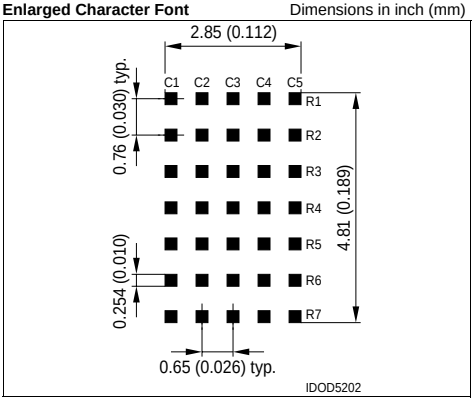
Parameter	Symbol	Value	Unit
Operating temperature range	T_{op}	– 40 … + 85	°C
Storage temperature range	T_{stg}	– 40 … + 100	°C
DC Supply Voltage, V_{CC} to GND (max. voltage with no LEDs on)	V_{CC}	-0.5 to + 7.0	V
Input Voltage Levels Relative to GND		-0.5 to V_{CC} + 0.5	V
Solder Temperature 1.59 mm (0.063") below seating plane, t < 5.0 s	T_S	260	°C
Relative Humidity (non-condensing)		85	%

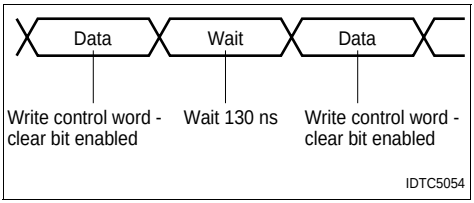
Optical Characteristics at 25°C
(V_{CC}=5.0 V at 100% brightness level)

Description		Symbol	Values					Unit
			Red PDSP2110	Yellow PDSP2111	Super-red PDSP2112	Green PDSP2113	High Efficiency Green PDSP2114	
Peak Luminous Intensity[1)]	(min.) (typ.)	I_{Vpeak}	70 90	130 210	150 330	150 260	200 510	µcd/dot µcd/dot
Peak Wavelength	(typ.)	λ_{peak}	660	583	630	565	568	nm
Dominant Wavelength	(typ.)	λ_{dom}	639	585	626	570	574	nm

Note:
1) Peak luminous intensity is measured at T_A=T_J=25°C. No time is allowed for the device to warm up prior to measurement.

Enlarged Character Font Dimensions in inch (mm)



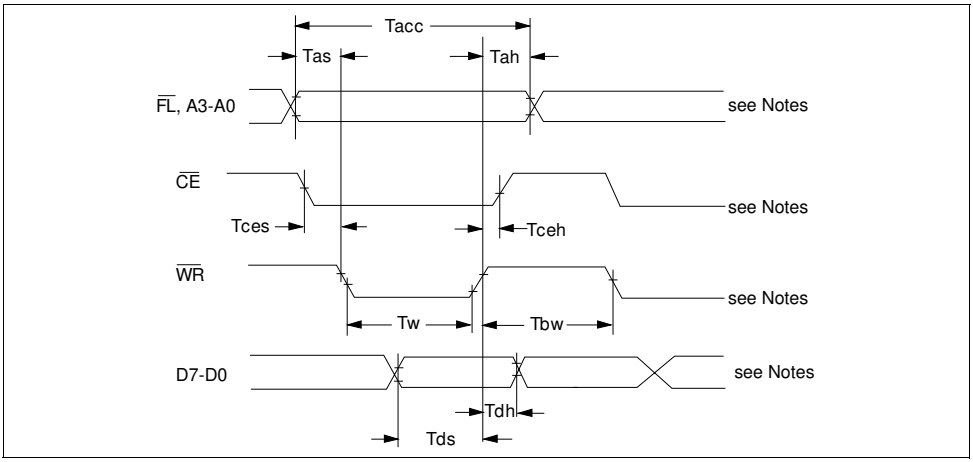


Switching Specifications
(over operating temperature range and V_{CC}=4.5 V)

Symbol	Description	Min.	Units
T_{bw}	Time Between Writes	30	ns
T_{acc} (2)	Display Access Time	130	ns
T_{as}	Address Setup Time	10	ns
T_{ces}	Chip Enable Setup Time	0	ns
T_{ah}	Address Hold Time	20	ns
T_{ceh}	Chip Enable Hold Time	0	ns
T_{w}	Write Active Time	100	ns
T_{ds}	Data Valid Prior to Rising Edge of Write	50	ns
T_{dh}	Data Hold Time	20	ns
T_{ic} (1)	Reset Active Time	300	ns
T_{clr} (3)	Clear Cycle Time	3.0	µs

Notes:
1) Wait 300 ns min. after the reset function is turned off.
2) $T_{acc}=T_{as}+T_{w}+T_{ah}$
3) The Clear Cycle Time may be shortened by writing a second Control Word with the Clear Bit disabled, 160 ns after the first control word that enabled the Clear Bit.
The Flash RAM and Character RAM may not be accessed until the Clear Cycle is complete.

Write Cycle Timing Diagram



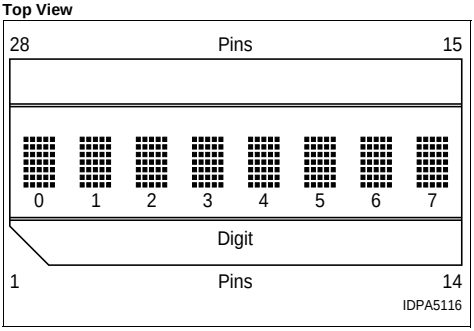
Notes:
1. All input voltages are V_{IL}=0.8 V, V_{IH}=2.0 V.
2. These wave forms are not edge triggered.
3. $T_{bw}=T_{as}+T_{ah}$

Electrical Characteristics at 25°C

Parameters	Limits				Conditions
	Min.	Typ.	Max.	Units	
V_{CC}	4.5	5.0	5.5	V	—
I_{CC} Blank	—	0.5	1.0	mA	V_{CC}=5.0 V, V_{IN}=5.0 V
I_{CC} 8 digits[1)] 12 dots/character	—	200	255	mA	V_{CC}=5.0 V, "V" displayed in all eight digits
I_{CC} 8 digits[1)] 20 dots/character	—	300	370	mA	V_{CC}=5.0 V, "#" displayed in all eight digits
I_{IP} Current (with pull-up)	—	11	18	µA	V_{CC}=5.0 V, V_{IN}=0 V to V_{CC} ($\overline{WR}$, $\overline{CE}$, $\overline{FL}$, $\overline{RST}$, $\overline{CLKSEL}$)
I, Input Leakage Current (no pull-up)	—	—	±1.0	µA	V_{CC}=5.0 V,V_{IN}=0 V to V_{CC} (Clk I/O, A0–A3, D0–D7)
V_{IH} Input Voltage High	2.0	—	V_{CC} +0.3	V	V_{CC}=4.5 V to 5.5 V
V_{IL} Input Voltage Low	GND –0.3	—	0.8	V	V_{CC}=4.5 V to 5.5 V
V_{OL} Output Voltage Low (Clock Pin)	—	—	0.4	V	V_{CC}=4.5 V to 5.5 V I_{OL}=1.6 mA
V_{OH} Output Voltage High (Clock Pin)	2.4	—	—	V	V_{CC}=4.5 V to 5.5 V I_{OH}=40 mA
I_{OH} Output Current High (Clock I/O)	–0.9	—	—	mA	V_{CC}=4.5 V, V_{OH}=–2.4 V
I_{OL} Output Current Low (Clock I/O)	1.6	2.0	—	mA	V_{CC}=4.5 V, V_{OL}=–0.4 V
θ_{JC} Thermal Resistance Junction to Case	—	25	—	°C/W	—
F_{EXT} External Clock Input Frequency[2)]	28	—	81.14	kHz	V_{CC}=5.0 V, $\overline{CLKSEL}$=0
F_{OSC} Internal Clock Output Frequency[2)]	28	—	81.14	kHz	V_{CC}=5.0 V, $\overline{CLKSEL}$=1
Clock I/O Buss Loading	—	—	240	pF	—
Clock Out Rise Time	—	—	500	ns	V_{CC}=4.5 V, V_{OH}=2.4 V
Clock Out Fall Time	—	—	500	ns	V_{CC}=4.5 V, V_{OL}=0.4 V
FM, Digit Multiplex Frequency	125	256	362.5	Hz	—
Blinking Rate	0.98	2.0	2.83	Hz	—

Notes:
1) Average I_{CC} measured at full brightness. Peak I_{CC}=2 x I_{AVG} I_{CC} (# displayed).
2) Internal/external frequency duty factor is 50%.

Top View



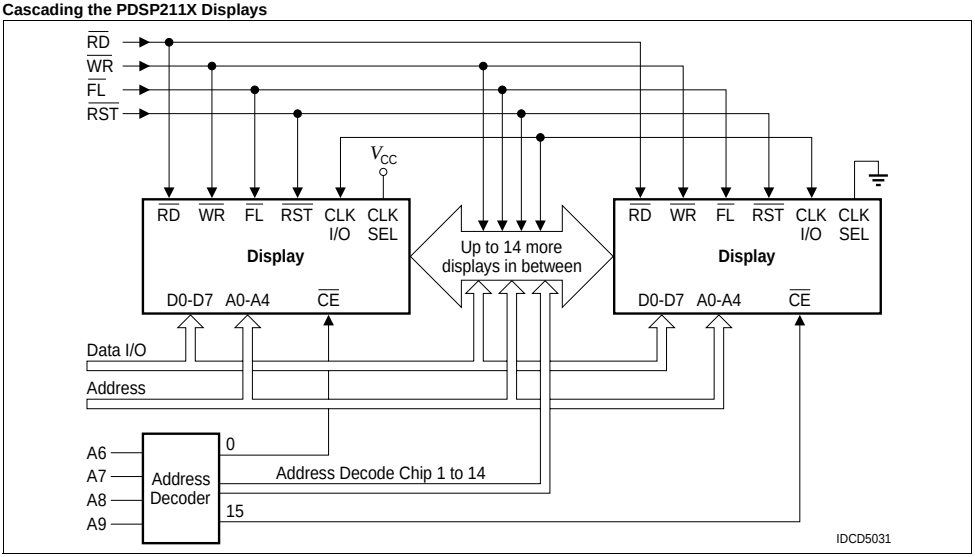
Pin Assignments

Pin	Function	Pin	Function
1	$\overline{\text{RST}}$	28	D7
2	$\overline{\text{FL}}$	27	D6
3	A0	26	D5
4	A1	25	D4
5	A2	24	D3
6	A3	23	D2
7	Substr. bias	22	No Pin
8		21	
9		20	D1
10	No Connect	19	D0
11	$\overline{\text{CLKSEL}}$	18	No Connect
12	CLK I/O	17	$\overline{\text{CE}}$
13	$\overline{\text{WR}}$	16	GND (logic)
14	V_{CC}	15	GND (supply)

Pin Definitions

Pin	Function	Definition
1	$\overline{\text{RST}}$	Used for initialization of a display and sychronization of blinking for multiple displays
2	$\overline{\text{FL}}$	Low input accesses the Flash RAM
3	A0	Address input LSB
4	A1	Address input
5	A2	Address input MSB
6	A3	Mode selector
7-9	Substr. bias	Used to bias IC substrate, must be connected to V_{CC}. Can't be used to supply power to display.
10	No connect	—
11	$\overline{\text{CLKSEL}}$	Selects internal/external clock source
12	CLK I/O	Outputs master clock or inputs external clock
13	$\overline{\text{WR}}$	A low will write data into the display if $\overline{\text{CE}}$ is low
14	V_{CC}	Positive power supply input
15	GND	Analog Ground for LED drivers
16	GND	Digital Ground for internal logic
17	$\overline{\text{CE}}$	Enables access to the display
18	No Connect	—
19	D0	Data input LSB
20	D1	Data input
21	No pin	—
22		
23	D2	Data input
24	D3	
25	D4	
26	D5	
27	D6	
28	D7	Data input MSB, selects ROM, page 1 or 2

Cascading the PDSP211X Displays



Character Set

ROM Page 1 (D7= 0)

ASCII CODE																			
			D0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
			D1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
			D2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
			D3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
D6	D5	D4	HEX	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0	0	0																
0	0	1	1																
0	1	0	2																
0	1	1	3																
1	0	0	4																
1	0	1	5																
1	1	0	6																
1	1	1	7																

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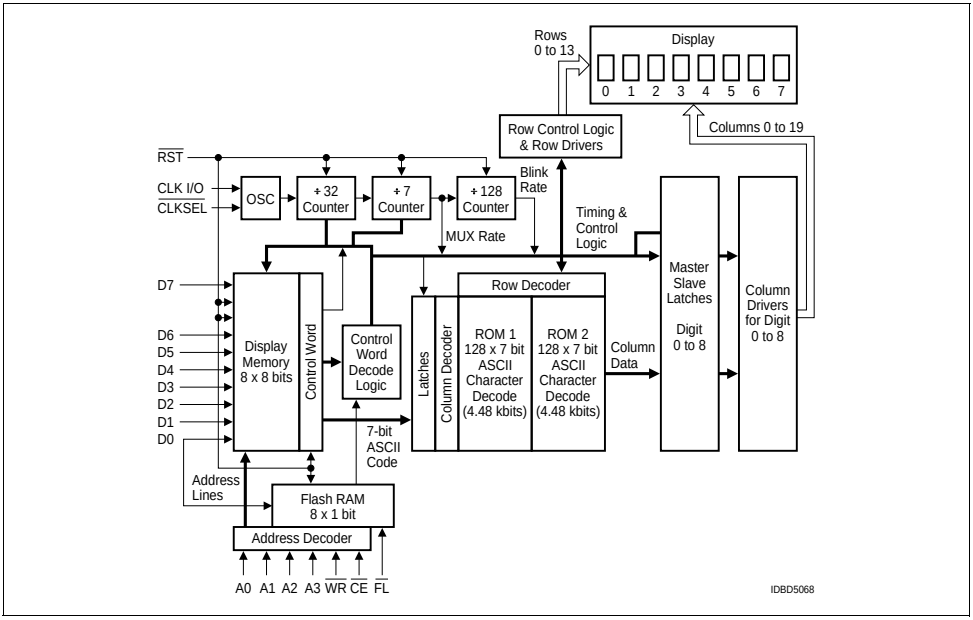
ROM Page 2 (D7=1)

ASC|| CODE																			
			D0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
			D1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
			D2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
			D3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
D6	D5	D4	HEX	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0	0	0																
0	0	1	1																
0	1	0	2																
0	1	1	3																
1	0	0	4																
1	0	1	5																
1	1	0	6																
1	1	1	7																

IDCS5094

Block Diagram



Functional Description

The PDSP211X block diagram is comprised of the following major blocks and registers.

Display Memory consists of a 8 x 8 bit RAM block. Each of the eight 8-bit words holds the 7-bit ASCII data (bit D0-D6). The 8th bit, D7 selects 1 of the 2 pages of character ROM. D7=0 selects Page 1 of the ROM and D7=1 selects Page 2 of the ROM. A3=1.

$\overline{RST}$ can be used to initialize display operation upon power up or during normal operation. When activated, $\overline{RST}$ will clear the Flash RAM and Control Word Register (00H) and reset the internal counter. All eight display memory locations will be set to 20H to show blanks in all digits.

$\overline{FL}$ pin enables access to the **Flash RAM**. The **Flash RAM** will set (D0=0) or reset (D0=0) flashing of the character addressed by A0-A2.

The 1 x 8 bit **Control Word RAM** is loaded with attribute data if A3=0.

The **Control Word Logic** decodes attribute data for proper implementation.

Character ROM is designed for two pages of 128 characters each. Both pages of the ROM are Mask Programmable for custom fonts. On the standard product page one contains standard ASCII, selected European characters and some scientific symbols. Page two contains Katakana characters, more European characters, avionics, and other graphic symbols.

The **Clock Source** could either be the internal oscillator ($\overline{CLKSEL}$=1) of the device or an external clock ($\overline{CLKSEL}$=0) could be an input from another PDSP211X display for the synchronization of blinking for multiple displays.

The **Display Multiplexer** controls the Row Drivers so no additional logic is required for a display system.

The **Display** has eight digits. Each digit has 35 LEDs clustered into a 5 x 7 dot matrix.

Theory of Operation

The PDSP211X Programmable display is designed to work with all major microprocessors. Data entry is via an eight bit parallel bus. Three bits of address route the data to the proper digit location in the RAM. Standard control signals like $\overline{WR}$ and $\overline{CE}$ allow the data to be written into the display.

D0- D7 data bits are used for both ASCII and control word data input. A3 acts as the mode selector. If A3=0, D0-D7 load the RAM with control word data. If A3=1, D0-D7 will load the RAM with ASCII and page select data. In the later mode, D7=0 selects Page 1 of Character ROM and D7=1 selects Page 2 of Character ROM.

For normal operation $\overline{FL}$ pin should be held high. When $\overline{FL}$ is held low, Flash RAM is accessed to set character blinking.

The seven bit ASCII code is decoded by the Character ROM to generate Column data. Twenty columns worth of data is sent out each display cycle and it takes fourteen display cycles to write into eight digits.

The rows are being multiplexed in two sets of seven rows each. The internal timing and control logic synchronizes the turning on of rows and presentation of column data to assure proper display operation.

Data Input Commands

Signals								
$\overline{CE}$	$\overline{WR}$	$\overline{FL}$	A3	A2	A1	A0	Operation	
1	X	X	X	X	X	X	No operation	
X	1	X	X	X	X	X	No operation	
0	0	1	0	0	0	0	Write Control Register	
0	0	1	1	0	0	0	Digit 0 (left)	Write display data to
0	0	1	1	0	0	1	Digit 1	user RAM and Page
0	0	1	1	0	1	0	Digit 2	Select Register
0	0	1	1	0	1	1	Digit 3	
0	0	1	1	1	0	0	Digit 4	
0	0	1	1	1	0	1	Digit 5	D0–D6=ASCII Data
0	1	1	1	1	0	0	Digit 6	D7=0 Select ROM 1
0	0	1	1	1	1	1	Digit 7 (right)	D7=1 Select ROM 2
0	0	0	X	0	0	0	Digit 0 (left)	Write Flash RAM Register
0	0	0	X	0	0	1	Digit 1	
0	0	0	X	0	1	0	Digit 2	
0	0	0	X	1	1	1	Digit 3	
0	0	0	X	1	0	0	Digit 4	
0	0	0	X	1	0	1	Digit 5	D0=0 Flashing Charac. off
0	0	0	X	1	1	0	Digit 6	D0=1 Flashing Charac. on
0	0	0	X	1	1	1	Digit 7 (right)	D1–D7=X

X=Don't care

Power up Sequence

Upon power up display will come on at random. Thus the display should be reset on power-up. The reset will clear the Flash RAM, Control Word Register and reset the internal counter. All the digits will show blanks and display brightness level will be 100%.

Microprocessor Interface

The interface to a microprocessor is through the 8-bit data bus (D0-D7), the 4-bit address bus (A0-A3) and control lines $\overline{FL}$, $\overline{CE}$ and $\overline{WR}$.

To write data (ASCII/Control Word) into the display $\overline{CE}$ should be held low, address and data signals stable and $\overline{WR}$ should be brought low.

The Control Word is decoded by the Control Word Decode Logic. Each code has a different function. The code for display brightness changes the duty cycle for the column drivers. The peak LED current stays the same but the average LED current diminishes depending on the intensity level.

The character Flash Enable causes 2.0 Hz coming out of the counter to be ANDED with column drive signal and makes the column driver to cycle at 2.0 Hz. Thus the character flashes at 2.0 Hz.

The display Blink works the same way as the Flash Enable but causes all twenty column drivers to cycle at 2.0 Hz thereby making all eight digits to blink at 2.0 Hz.

The Lamp Test causes the column drivers to run at 1/2 duty cycle thus all the LEDs in all eight digits turn on at 50% intensity.

Clear bit clears the character RAM and writes a blank into the display memory. It however does not clear the control word.

ASCII Data or Control Word Data can be written into the display at this point. For multiple display operation, CLK I/O must be properly selected. CLK I/O will output the internal clock if $\overline{CLKSEL}$=1, or will allow input from an external clock if $\overline{CLKSEL}$=0.

Control Word Format

Display Brightness

The display can be programmed to vary between blank, 13%, 20%, 27%, 40%, 53%, 80% and full brightness.
Bits D0, D1 and D2 control the display brightness.

$\overline{CE}$	$\overline{WR}$	$\overline{FL}$	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	Display Brightness
0	0	1	0	X	X	X	0	0	X	X	X	0	0	0	100% Brightness
0	0	1	0	X	X	X	0	0	X	X	X	0	0	1	80% Brightness
0	0	1	0	X	X	X	0	0	X	X	X	0	1	0	53% Brightness
0	0	1	0	X	X	X	0	0	X	X	X	0	1	1	40% Brightness
0	0	1	0	X	X	X	0	0	X	X	X	1	0	0	27% Brightness
0	0	1	0	X	X	X	0	0	X	X	X	1	0	1	20% Brightness
0	0	1	0	X	X	X	0	0	X	X	X	1	1	0	13% Brightness
0	0	1	0	X	X	X	0	0	X	X	X	1	1	1	Blank Display

X=Don't Care

Flash RAM Function

Character Flash is controlled by $\overline{FL}$ pin, bit D0 and control word bit D3. Combination of $\overline{FL}$ being low, proper digit address and D0 being high will write a flash bit into the Flash RAM Register. In the control word mode when D3 is brought high, the above mentioned character will flash.

Setting the Flash Bit

$\overline{CE}$	$\overline{WR}$	$\overline{FL}$	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	Operation
0	0	0	X	A	A	A	X	X	X	X	X	X	X	0	Flash RAM Disabled
0	0	0	X	A	A	A	X	X	X	X	X	X	X	1	Flash RAM Enabled

X=Don't Care A=Selected Address

Character Flash Control Word

$\overline{CE}$	$\overline{WR}$	$\overline{FL}$	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	Operation
0	0	1	0	X	X	X	0	0	X	0	0	B	B	B	Disable Flashing Character
0	0	1	0	X	X	X	0	0	X	0	1	B	B	B	Enable Flashing Character

X=Don't Care B=Selected Brightness

Display Blinking

Blinking Function is independent of Flash function. When D4 is held high, entire display blinks at 2.0 Hz.

$\overline{CE}$	$\overline{WR}$	$\overline{FL}$	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	Operation
0	0	1	0	X	X	X	0	0	X	0	0	B	B	B	Display Blinking Disabled
0	0	1	0	X	X	X	0	0	X	1	0	B	B	B	Display Blinking Enabled

X=Don't Care B=Selected Brightness

Lamp Test

Bit D6 when brought high will cause all the LEDs in all eight digits to light up at 53% brightness.
Selecting or de-selecting Lamp Test bit has no effect on the display memory.

$\overline{CE}$	$\overline{WR}$	$\overline{FL}$	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	Operation
0	0	1	0	X	X	X	0	0	X	0	X	X	X	X	Lamp Test Disabled
0	0	1	0	X	X	X	0	1	X	0	0	X	X	X	Lamp Test Enabled

X=Don't Care

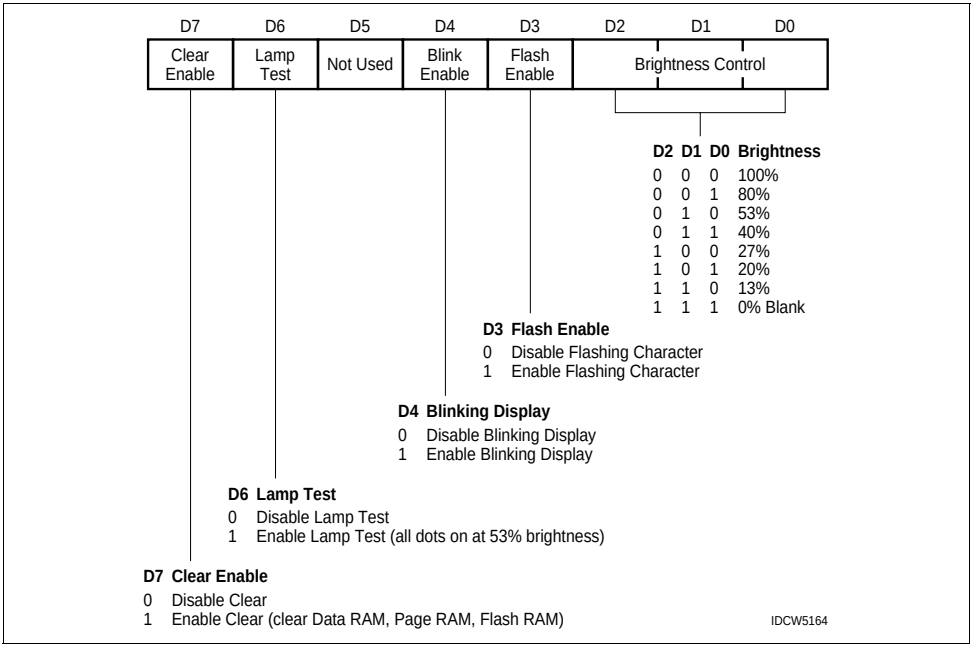
Clear Function

Clear function will clear the display. The Flash RAM will be set to all zeros. An ASCII blank code (20H) will be written into the display memory. The user must wait 3.0 ms or write a new control word to the display with control word bit D7 = 0 to disable clear before writing any data to the display memory, otherwise all new data to the display memory will remain cleared. See Switching Specifications for clear function timing.

$\overline{CE}$	$\overline{WR}$	$\overline{FL}$	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	Operation
0	0	1	0	X	X	X	0	X	X	X	X	X	X	X	Clear Disabled
0	0	1	0	X	X	X	1	X	X	X	X	X	X	X	Clear User RAM, Page RAM, Flash RAM and Display

X=Don't Care

Control Word Format



Electrical and Mechanical Considerations

Voltage Transient Suppression

For best results power the display and the components that interface with the display to avoid logic inputs higher than V_{CC}. Additionally, the LEDs may cause transients in the power supply line while they change display states. The common practice is to place a parallel combination of a 0.01 µF and a 22 µF capacitor between V_{CC} and GND for all display packages.

ESD Protection

The input protection structure of the PDSP2110/1/2/3/4 provides significant protection against ESD damage. It is capable of withstanding discharges greater than 2.0 kV. Take all the standard precautions, normal for CMOS components. These include properly grounding personnel, tools, tables, and transport carriers that come in contact with unshielded parts. If these conditions are not, or cannot be met, keep the leads of the device shorted together or the parts in anti-static packaging.

Soldering Considerations

The PDSP2110/1/2/3/4 can be hand soldered with SN63 solder using a grounded iron set to 260°C.

Wave soldering is also possible following these conditions: Preheat that does not exceed 93°C on the solder side of the PC board or a package surface temperature of 85°C. Water soluble organic acid flux (except carboxylic acid) or rosin-based RMA flux without alcohol can be used.

Wave temperature of 245°C ± 5°C with a dwell between 1.5 sec. to 3.0 sec. Exposure to the wave should not exceed temperatures above 260°C for five seconds at 1.59 mm (0.063") below the seating plane. The packages should not be immersed in the wave.

Post Solder Cleaning Procedures

The least offensive cleaning solution is hot D.I. water (60°C) for less than 15 minutes. Addition of mild saponifiers is acceptable. Do not use commercial dishwasher detergents.

For faster cleaning, solvents may be used. Exercise care in choosing solvents as some may chemically attack the nylon package. Maximum exposure should not exceed two minutes at elevated temperatures. Acceptable solvents are TF (trichorotrifluorethane), TA, 111 Trichloroethane, and unheated acetone.[1)]

Note:

1) Acceptable commercial solvents are: Basic TF, Arklone, P. Genesolv, D. Genesolv DA, Blaco-Tron TF and Blaco-Tron TA.

Unacceptable solvents contain alcohol, methanol, methylene chloride, ethanol, TP35, TCM, TMC, TMS+, TE, or TES. Since many commercial mixtures exist, contact a solvent vendor for chemical composition information. Some major solvent manufacturers are: Allied Chemical Corporation, Specialty Chemical Division, Morristown, NJ; Baron-Blakeslee, Chicago, IL; Dow Chemical, Midland, MI; E.I. DuPont de Nemours & Co., Wilmington, DE.

For further information refer to Appnotes 18 and 19 at www.osram-os.com

An alternative to soldering and cleaning the display modules is to use sockets. Naturally, 28 pin DIP sockets 15.24 mm (0.600") wide with 2.54 mm (0.100") centers work well for single displays.

Multiple display assemblies are best handled by longer SIP sockets or DIP sockets when available for uniform package alignment. Socket manufacturers are Aries Electronics, Inc., Frenchtown, NJ; Garry Manufacturing, New Brunswick, NJ; Robinson-Nugent, New Albany, IN; and Samtec Electronic Hardward, New Albany, IN.

For further information refer to Appnote 22 at www.osram-os.com

Optical Considerations

The 5.10 mm (0.200") high character of the PDSP211X gives readability up to eight feet. Proper filter selection enhances readability over this distance.

Using filters emphasizes the contrast ratio between a lit LED and the character background. This will increase the discrimination of different characters. The only limitation is cost. Take into consideration the ambient lighting environment for the best cost/benefit ratio for filters.

Incandescent (with almost no green) or fluorescent (with almost no red) lights do not have the flat spectral response of sunlight. Plastic band-pass filters are an inexpensive and effective way to strengthen contrast ratios. The PDSP2110/2112 are red/super-red displays and should be matched with long wavelength pass filter in the 570 nm to 590 nm range. The PDSP2111/2113/2114 should be matched with a yellow-green band-pass filter that peaks at 565 nm. For displays of multiple colors, neutral density grey filters offer the best compromise.

Additional contrast enhancement is gained by shading the displays. Plastic band-pass filters with built-in louvers offer the next step up in contrast improvement. Plastic filters can be improved further with anti-reflective coatings to reduce glare. The trade-off is fuzzy characters. Mounting the filters close to the display reduces this effect. Take care not to overheat the plastic filter by allowing for proper air flow.

Optimal filter enhancements are gained by using circular polarized, anti-reflective, band-pass filters. The circular polarizing further enhances contrast by reducing the light that travels through the filter and reflects back off the display to less than 1%.

Several filter manufacturers supply quality filter materials. Some of them are: Panelgraphic Corporation, W. Caldwell, NJ; SGL Homalite, Wilmington, DE; 3M Company, Visual Products Division, St. Paul, MN; Polaroid Corporation, Polarizer Division, Cambridge, MA; Marks Polarized Corporation, Deer Park, NY, Hoya Optics, Inc., Fremont, CA.

One last note on mounting filters: recessing displays and bezel assemblies is an inexpensive way to provide a shading effect in overhead lighting situations. Several bezel manufacturers are: R.M.F. Products, Batavia, IL; Nobex Components, Griffith Plastic Corp., Burlingame, CA; Photo Chemical Products of California, Santa Monica, CA; I.E.E.–Atlas, Van Nuys, CA.

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all	Lead free device	2006-01-23

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