ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
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Offices: 310-530-9400 / Fax: 310-530-9402
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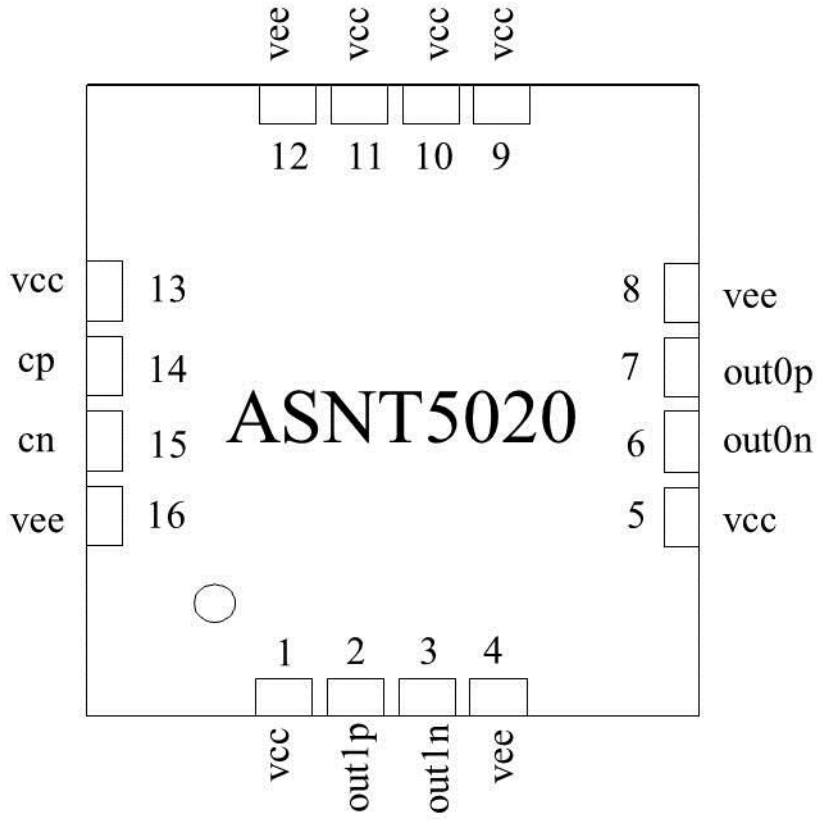
ASNT5020-PQD
DC-26*Gbps*/13*GHz* Signal Distributor 1-to-2

- High-speed broadband Data/Clock Amplifier and Distributor
- Exhibits low jitter and limited temperature variation over industrial temperature range
- One input differential signal port and two differential amplified output signal ports
- Matched phase delays for all outputs
- Fully differential CML input interface
- Fully differential CML output interfaces with 600*mV* single-ended swing
- Single +3.3*V* or -3.3*V* power supply
- Power consumption: 560*mW*
- Fabricated in SiGe for high performance, yield, and reliability
- Standard MLF/QFN 16-pin package



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DESCRIPTION

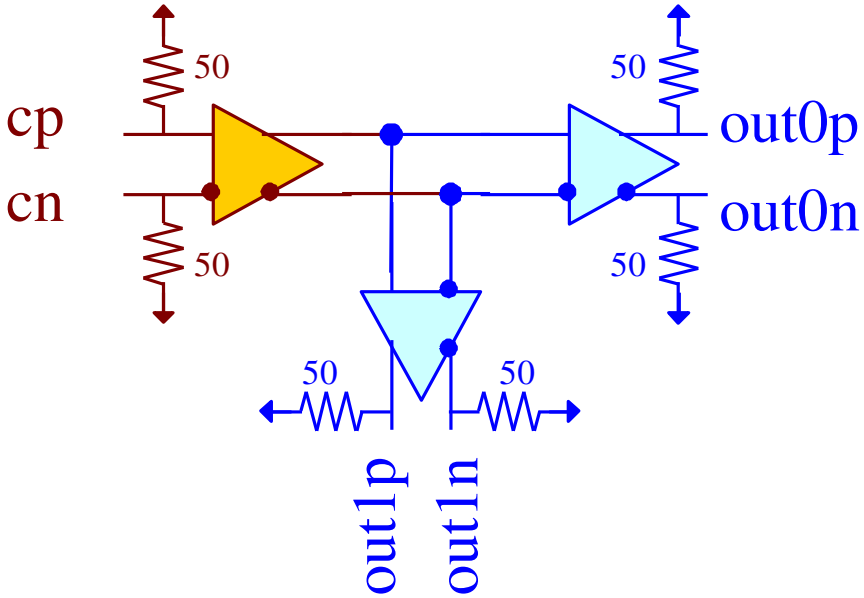

Fig. 1. Functional Block Diagram

The temperature stable ASNT5020-PQD SiGe IC provides active broadband data/clock signal splitting, and is intended for use in high-speed measurement / test equipment. The IC shown in Fig. 1 can deliver two phase-matched copies of the broadband data/clock input signal cp/cn to two high-speed differential outputs out0p/out0n, out1p/out1n.

The part's I/O's support the CML logic interface with on chip 50*Ohm* termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination (see also POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

POWER SUPPLY CONFIGURATION

The part can operate with either negative supply (vcc = 0.0*V* = ground and vee = −3.3*V*), or positive supply (vcc = +3.3*V* and vee = 0.0*V* = ground). In case of the positive supply, all I/Os need AC termination when connected to any devices with 50*Ohm* termination to ground. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume vcc = 0.0*V* and vee = -3.3*V*.

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ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 1 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground.

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)		-3.6	*V*
Power Consumption		0.62	*W*
RF Input Voltage Swing (SE)		1.0	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
High-Speed I/Os			
cp	14	CML input	Differential high speed data/clock inputs with internal SE 50*Ohm* termination to vcc
cn	15		
out0p	7	CML output	Differential high speed data/clock outputs with internal SE 50*Ohm* termination to vcc. Require external SE 50*Ohm* termination to vcc
out0n	6		
out1p	2	CML output	Differential high speed data/clock outputs with internal SE 50*Ohm* termination to vcc. Require external SE 50*Ohm* termination to vcc
out1n	3		
Supply and Termination Voltages			
Name	**Description**		**Pin Number**
vcc	Positive power supply. (+3.3*V* or 0)		1, 5, 9, 10, 11, 13
vee	Negative power supply. (0*V* or -3.3*V*)		4, 8, 12, 16

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee	-3.1	-3.3	-3.5	*V*	±6%
vcc		0.0		*V*	External ground
*I*vee		170		*mA*	
Power consumption		560		*mW*	
Junction temperature	-40	25	125	*°C*	
HS Input Data/Clock (cp/cn)					
Data Rate	DC		26	*Gbps*	
Frequency	DC		13	*GHz*	
Swing	0.05		1.0	*V*	Differential or SE, p-p
CM Voltage Level	vcc-0.8		vcc	*V*	Must match for both inputs
HS Output Data/Clock (out0p/out0n, out1p/out1n)					
Data Rate	DC		26	*Gbps*	
Frequency	DC		13	*GHz*	
Phase mismatch			2	*ps*	Between any two SE outputs
Logic "1" level		vcc		*V*	
Logic "0" level		vcc-0.6		*V*	With external 50*Ohm* DC termination
Rise/Fall times	13		17	*ps*	20%-80%
Additive Jitter			5	*ps*	Peak-to-peak
Duty cycle	45	50	55	*%*	For clock signal

PACKAGE INFORMATION

The chip die is housed in a standard 16-pin QFN package shown in Fig. 2. It is recommended that the center heat slug located on the back side of the package is soldered to the vee plain that is ground for the positive supply or power for the negative supply.

The part's identification label is ASNT5020-PQD. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.

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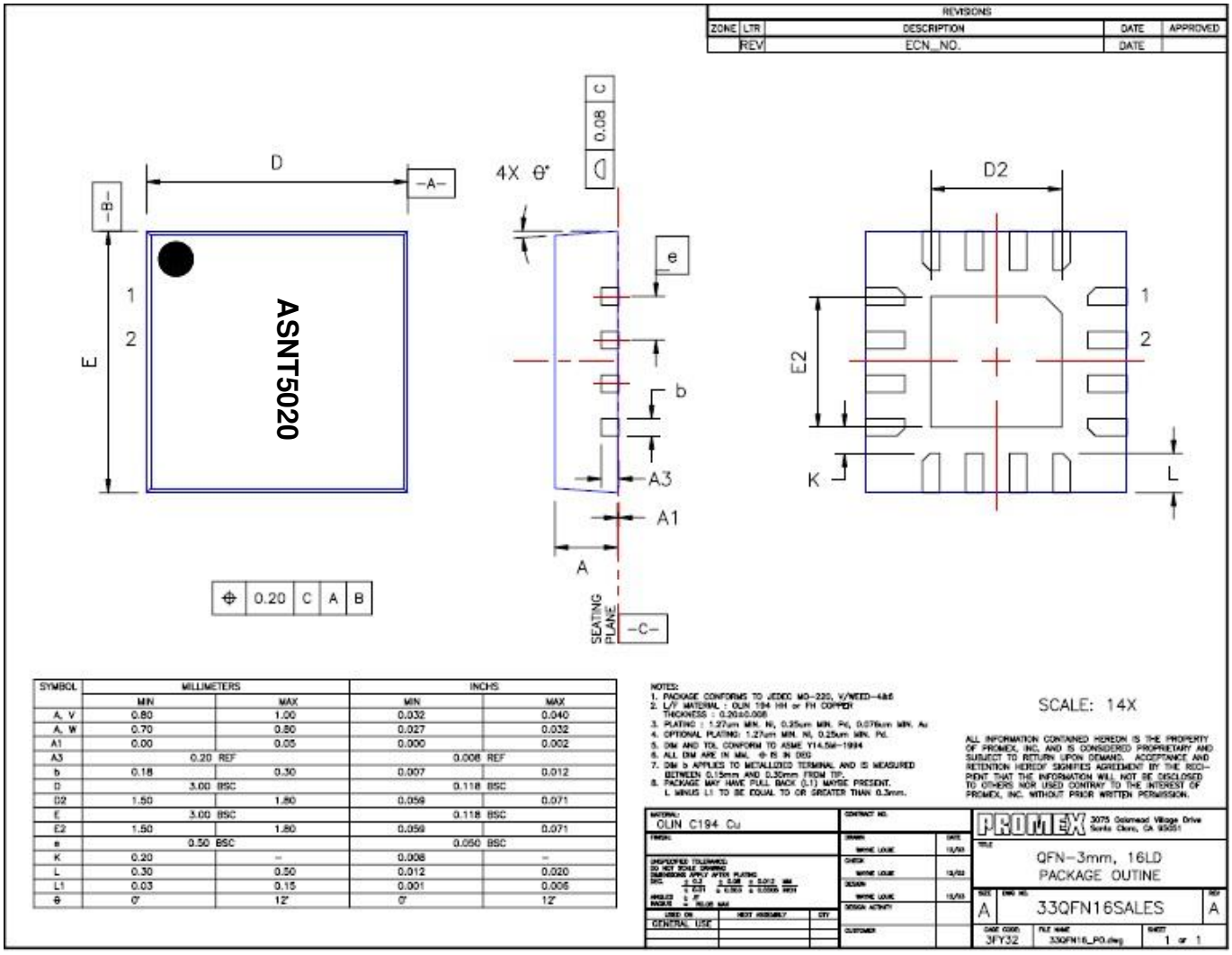

SYMBOL	MILLIMETERS		INCHS	
	MIN	MAX	MIN	MAX
A, V	0.80	1.00	0.032	0.040
A, W	0.70	0.80	0.027	0.032
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	3.00 BSC		0.118 BSC	
D2	1.50	1.80	0.059	0.071
E	3.00 BSC		0.118 BSC	
E2	1.50	1.80	0.059	0.071
e	0.50 BSC		0.050 BSC	
K	0.20	–	0.008	–
L	0.30	0.50	0.012	0.020
L1	0.03	0.15	0.001	0.006
θ	0°	12°	0°	12°

Fig. 2. QFN 16-Pin Package Drawing (All Dimensions in mm)

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REVISION HISTORY

Revision	Date	Changes
2.2.2	05-2020	Updated Package Information
2.1.2	07-2019	Updated Letterhead
2.1.1	03-2013	Added phase mismatch specifications Updated description
2.0.1	02-2013	Revised title Revised pin out diagram Revised functional block diagram Revised description Added power supply configuration Added absolute maximum ratings Revised terminal functions Revised electrical characteristics Revised package information Added mechanical drawing Format correction
1.0	10-2008	Initial release