Si52147

PCI-Express Gen 1, Gen 2, & Gen 3 Nine-Output Clock Generator

Features

- PCI-Express Gen 1, Gen 2, Gen 3, and Gen 4 common clock compliant
- Gen 3 SRNS Compliant
- Supports Serial-ATA (SATA) at 100 MHz
- Low power push-pull HCSL compatible differential outputs
- No termination resistors required
- Output enable pins for all clocks
- Spread enable pin
- 25 MHz crystal input or clock input
- Up to nine PCI-Express clock outputs
- I^2C support with readback capabilities
- Triangular spread spectrum profile for maximum electromagnetic interference (EMI) reduction
- Industrial temperature: –40 to 85 °C
- 3.3 V power supply
- 48-pin QFN package

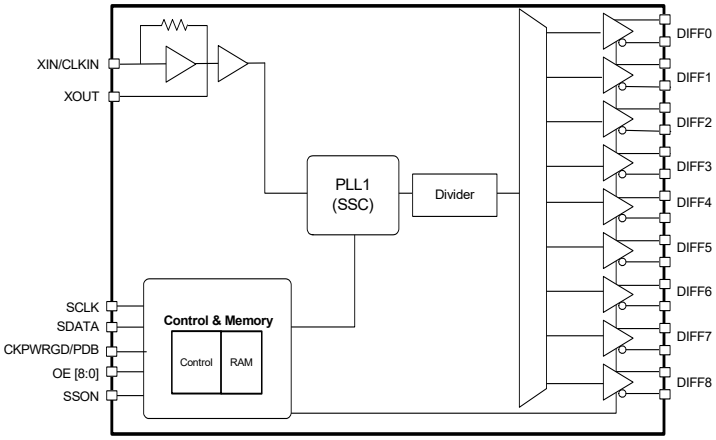
Applications

- Network attached storage
- Multi-function printer
- Wireless access point
- Servers

Description

The Si52147 is a high-performance, PCIe clock generator that can source nine PCIe clocks from a 25 MHz crystal or clock input. The clock outputs are compliant to PCIe Gen 1, Gen 2, Gen 3, Gen 3 SRNS and Gen 4 common clock specifications. The device has six hardware output enable control pins for enabling and disabling differential outputs. A spread spectrum control pin for EMI reduction is also available. The small footprint and low power consumption makes the Si52147 the ideal clock solution for consumer and embedded applications. Measuring PCIe clock jitter is quick and easy with the Skyworks Solutions PCIe Clock Jitter Tool. Download it for free at https://www.skyworksinc.com/en/application-pages/pci-express-learning-center.

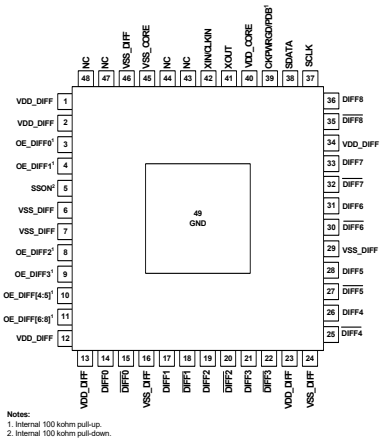
Functional Block Diagram



Ordering Information:

See page 20.

Pin Assignments



Patents pending

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1. Electrical Specifications

Table 1. DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
3.3 V Operating Voltage	VDD core	3.3 ±5%	3.135	3.3	3.465	V
3.3 V Input High Voltage	V_{IH}	Control input pins	2.0	—	V_{DD} + 0.3	V
3.3 V Input Low Voltage	V_{IL}	Control input pins	V_{SS} – 0.3	—	0.8	V
Input High Voltage	V_{IHI2C}	SDATA, SCLK	2.2	—	—	V
Input Low Voltage	V_{ILI2C}	SDATA, SCLK	—	—	1.0	V
Input High Leakage Current	I_{IH}	Except internal pull-down resistors, $0 < V_{IN} < V_{DD}$	—	—	5	µA
Input Low Leakage Current	I_{IL}	Except internal pull-up resistors, $0 < V_{IN} < V_{DD}$	–5	—	—	µA
High-impedance Output Current	I_{OZ}		–10	—	10	µA
Input Pin Capacitance	C_{IN}		1.5	—	5	pF
Output Pin Capacitance	C_{OUT}		—	—	6	pF
Pin Inductance	L_{IN}		—	—	7	nH
Power Down Current	I_{DD_PD}		—	—	1	mA
Dynamic Supply Current	$I_{DD\_3.3V}$	All outputs enabled. Differential clocks with 5” traces and 2 pF load.	—	—	85	mA

Table 2. AC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal						
Long-term Accuracy	L_{ACC}	Measured at $V_{DD}/2$ differential	—	—	250	ppm
Clock Input						
CLKIN Duty Cycle	T_{DC}	Measured at $V_{DD}/2$	47	—	53	%
CLKIN Rise and Fall Times	T_R/T_F	Measured between 0.2 V_{DD} and 0.8 V_{DD}	0.5	—	4.0	V/ns
CLKIN Cycle to Cycle Jitter	T_{CCJ}	Measured at VDD/2	—	—	250	ps
CLKIN Long Term Jitter	T_{LTJ}	Measured at VDD/2	—	—	350	ps
Input High Voltage	V_{IH}	XIN/CLKIN pin	2	—	VDD+0.3	V
Input Low Voltage	V_{IL}	XIN/CLKIN pin	—	—	0.8	V
Input High Current	I_{IH}	XIN/CLKIN pin, VIN = VDD	—	—	35	uA
Input Low Current	I_{IL}	XIN/CLKIN pin, 0 < VIN <0.8	–35	—	—	uA
DIFF at 0.7 V						
Duty Cycle	T_{DC}	Measured at 0 V differential	45	—	55	%
Output-to-Output skew	T_{SKEW}	Measured at 0 V differential	—	—	800	ps
Cycle to Cycle Jitter	T_{CCJ}	Measured at 0 V differential	—	35	50	ps
PCIe Gen 1 Pk-Pk Jitter, Common Clock	Pk-Pk	PCIe Gen 1	0	40	50	ps
PCIe Gen 2 Phase Jitter, Common Clock	RMS_{GEN2}	10 kHz < F < 1.5 MHz	0	1.8	2.0	ps
		1.5 MHz < F < Nyquist	0	1.8	2.1	ps
PCIe Gen 3 Phase Jitter, Common Clock	RMS_{GEN3}	PLL BW of 2–4 or 2–5 MHz, CDR = 10 MHz	0	0.5	0.6	ps
PCIe Gen 3 Phase Jitter, Separate Reference No Spread, SRNS	RMS_{GEN3_SRNS}	PLL BW of 2–4 or 2–5 MHz, CDR = 10 MHz	—	0.35	0.42	ps
PCIe Gen 4 Phase Jitter, Common Clock	RMS_{GEN4}	PLL BW of 2–4 or 2–5 MHz, CDR = 10 MHz	—	0.5	0.6	ps
Long Term Accuracy	L_{ACC}	Measured at 0 V differential	—	—	100	ppm
Rising/Falling Slew Rate	T_R/T_F	Measured differentially from ±150 mV	1	—	8	V/ns
Voltage High	V_{HIGH}		—	—	1.15	V
Voltage Low	V_{LOW}		–0.3	—	—	V
Crossing Point Voltage at 0.7 V Swing	V_{OX}		300	—	550	mV
Spread Range	SPR-2	Down spread	—	–0.5	—	%
Modulation Frequency	F_{MOD}		30	31.5	33	kHz

Notes:
1. Visit https://pcisig.com/ for complete PCIe specifications.
2. Gen 4 specifications based on the PCI-Express Base Specification 4.0 rev. 0.5.
3. Download the Skyworks Solutions PCIe Clock Jitter Tool at https://www.skyworksinc.com/en/application-pages/pci-express-learning-center.

Table 2. AC Electrical Specifications (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Enable/Disable and Setup						
Clock Stabilization from Power-up	T_{STABLE}	Measured from the point both V_{DD} and clock input are valid	—	—	1.8	ms
Stopclock Set-up Time	T_{SS}		10.0	—	—	ns

Notes:
1. Visit https://pcisig.com/ for complete PCIe specifications.
2. Gen 4 specifications based on the PCI-Express Base Specification 4.0 rev. 0.5.
3. Download the Skyworks Solutions PCIe Clock Jitter Tool at https://www.skyworksinc.com/en/application-pages/pci-express-learning-center.

Table 3. Absolute Maximum Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Main Supply Voltage	$V_{DD\_3.3V}$	Functional	—	—	4.6	V
Input Voltage	V_{IN}	Relative to V_{SS}	–0.5	—	4.6	V_{DC}
Temperature, Storage	T_S	Non-functional	–65	—	150	°C
Temperature, Operating Ambient	T_A	Functional	–40	—	85	°C
Temperature, Junction	T_J	Functional	—	—	150	°C
Dissipation, Junction to Case	$Ø_{JC}$	JEDEC (JESD 51)	—	—	22	°C/W
Dissipation, Junction to Ambient	$Ø_{JA}$	JEDEC (JESD 51)	—	—	30	°C/W
ESD Protection (Human Body Model)	ESD_{HBM}	JEDEC (JESD 22-A114)	2000	—	—	V
Flammability Rating	UL-94	UL (Class)	V–0			

Note: While using multiple power supplies, the voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is not required.

2. Functional Description

2.1. Crystal Recommendations

If using crystal input, the device requires a parallel resonance 25 MHz crystal.

Table 4. Crystal Recommendations

Frequency (Fund)	Cut	Loading	Load Cap	Shunt Cap (max)	Motional (max)	Tolerance (max)	Stability (max)	Aging (max)
25 MHz	AT	Parallel	12–15 pF	5 pF	0.016 pF	35 ppm	30 ppm	5 ppm

2.1.1. Crystal Loading

Crystal loading is critical in achieving low ppm performance. In order to achieve low/zero ppm error, use the calculations in section 2.1.2 to estimate the appropriate capacitive loading (CL).

Figure 1 shows a typical crystal configuration using the two trim capacitors. It is important that the trim capacitors are in series with the crystal.

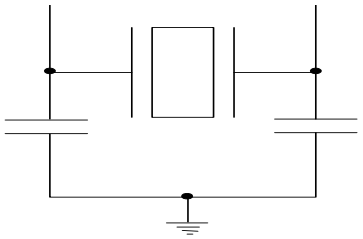


Figure 1. Crystal Capacitive Clarification

2.1.2. Calculating Load Capacitors

In addition to the standard external trim capacitors, consider the trace capacitance and pin capacitance to calculate the crystal loading correctly. The capacitance on each side is in series with the crystal. The total capacitance on both sides is twice the specified crystal load capacitance (CL). Trim capacitors are calculated to provide equal capacitive loading on both sides.

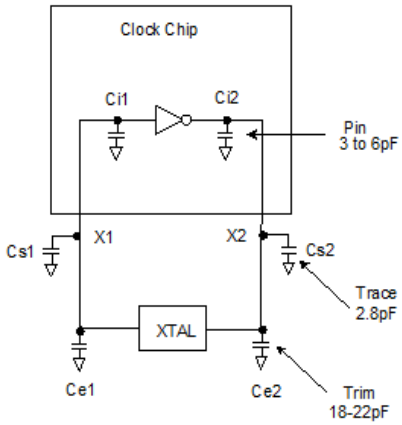


Figure 2. Crystal Loading Example

Use the following formulas to calculate the trim capacitor values for Ce1 and Ce2.

Load Capacitance (each side)

$$Ce = 2 \times CL - (Cs + Ci)$$

Total Capacitance (as seen by the crystal)

$$CLe = \frac{1}{\left(\frac{1}{Ce1 + Cs1 + Ci1} + \frac{1}{Ce2 + Cs2 + Ci2}\right)}$$

- CL: Crystal load capacitance
- CLe: Actual loading seen by crystal using standard value trim capacitors
- Ce: External trim capacitors
- Cs: Stray capacitance (terraced)
- Ci : Internal capacitance (lead frame, bond wires, etc.)

2.2. CKPWRGD/PDB (Power Down) Pin

The CKPWRGD/PDB pin is a dual-function pin. During initial power up, the pin functions as the CKPWRGD pin. Upon the first power up, if the CKPWRGD pin is low, the outputs will be disabled, but the crystal oscillator and I^2C logics will be active. Once the CKPWRGD pin has been sampled high by the clock chip, the pin assumes a PDB functionality. When the pin has assumed a PDB functionality and is pulled low, the device will be placed in power down mode. The CKPWRGD/PDB pin is required to be driven at all times even though it has an internal 100 kΩ resistor.

2.3. PDB (Power Down) Assertion

The PDB pin is an asynchronous active low input used to disable all output clocks in a glitch-free manner. All outputs will be driven low in power down mode. In power down mode, all outputs, the crystal oscillator, and the I^2C logic are disabled.

2.4. PDB Deassertion

When a valid rising edge on CKPWRGD/PDB pin is applied, all outputs are enabled in a glitch-free manner within two to six output clock cycles.

2.5. OE Pin

The OE pin is an active high input used to enable and disable the output clock. To enable the output clock, the OE pin and the I^2C OE bit need to be a logic high. By default, the OE pin and the I^2C OE bit are set to a logic high. There are two methods to disable the output clock: the OE pin is pulled to a logic low, or the I^2C OE bit is set to a logic low. The OE pin is required to be driven at all times even though it has an internal 100 kΩ resistor.

2.6. OE Assertion

The OE pin is an active high input used for synchronous stopping and starting the respective output clock while the rest of the clock generator continues to function. The assertion of the OE function is achieved by pulling the OE pin and the I^2C OE bit high which causes the respective stopped output to resume normal operation. No short or stretched clock pulses are produced when the clocks resume. The maximum latency from the assertion to active outputs is no more than two to six output clock cycles.

2.7. OE Deassertion

The OE function is deasserted by pulling the pin or the I^2C OE bit to a logic low. The corresponding output is stopped cleanly and the final output state is driven low.

2.8. SSON Pin

The SSON pin is an active input used to enable –0.5% spread spectrum on the outputs. When sampled high, –0.5% spread is enabled on the output clocks. When sampled low, the output clocks are non-spread.

3. Test and Measurement Setup

Figure 3 shows the test load configuration for the HCSL compatible output clocks.

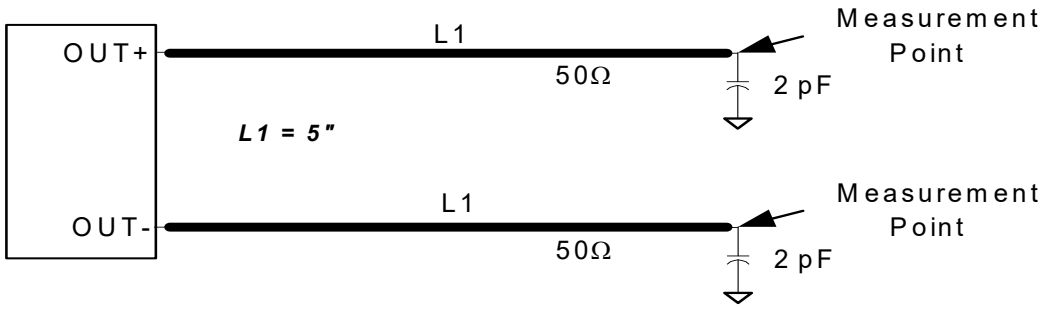


Figure 3. 0.7 V Differential Load Configuration

Please reference application note AN781 for recommendations on how to terminate the differential outputs for LVDS, LVPECL, or CML signalling levels.

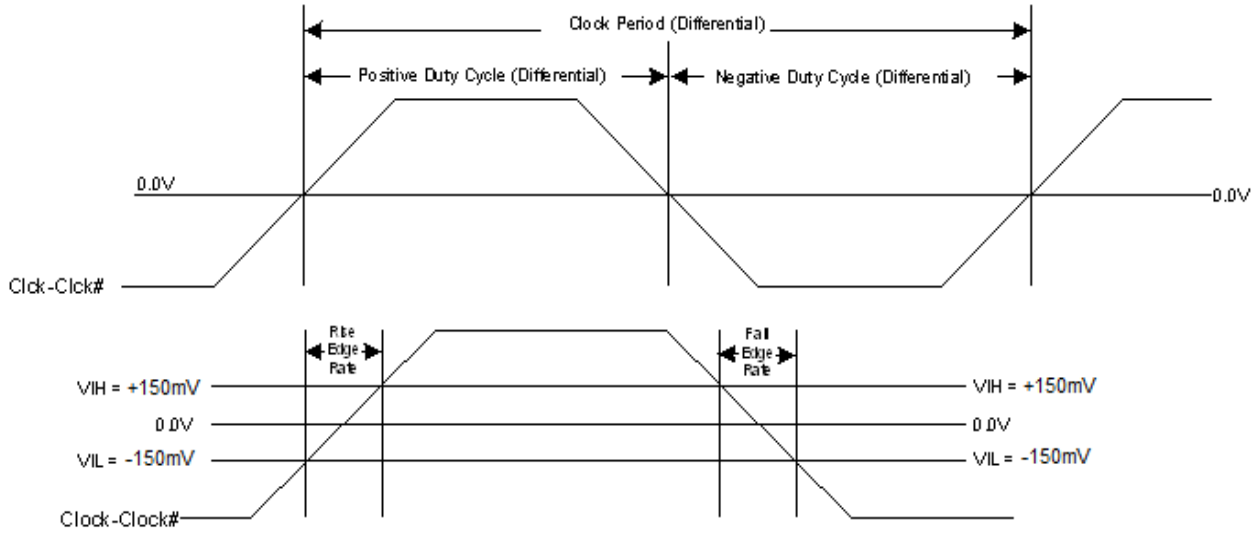


Figure 4. Differential Output Signals (for AC Parameters Measurement)

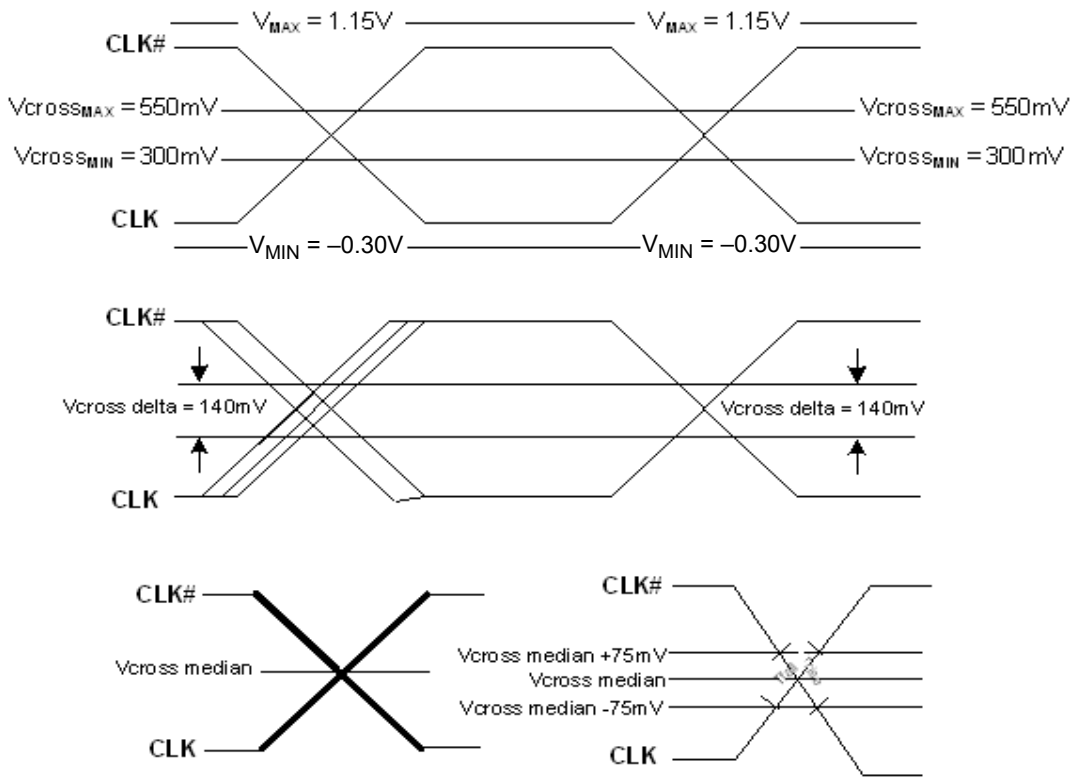


Figure 5. Single-ended Measurement for Differential Output Signals (for AC Parameters Measurement)

4. Control Registers

4.1. I²C Interface

To enhance the flexibility and function of the clock synthesizer, an I²C interface is provided. Through the I²C interface, various device functions are available, such as individual clock output enablement. The registers associated with the I²C interface initialize to their default setting at power-up. The use of this interface is optional. Clock device register changes are normally made at system initialization, if any are required.

4.2. Data Protocol

The clock driver I²C protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, access the bytes in sequential order from lowest to highest (most significant bit first) with the ability to stop after any complete byte is transferred. For byte write and byte read operations, the system controller can access individually indexed bytes.

The block write and block read protocol is outlined in Table 5 while Table 6 outlines byte write and byte read protocol. The slave receiver address is 11010110 (D6h).

Table 5. Block Read and Block Write Protocol

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
8:2	Slave address—7 bits	8:2	Slave address–7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code—8 bits	18:11	Command Code–8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Byte Count—8 bits	20	Repeat start
28	Acknowledge from slave	27:21	Slave address–7 bits
36:29	Data byte 1–8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
45:38	Data byte 2–8 bits	37:30	Byte Count from slave–8 bits
46	Acknowledge from slave	38	Acknowledge
....	Data Byte/Slave Acknowledges	46:39	Data byte 1 from slave–8 bits
....	Data Byte N–8 bits	47	Acknowledge
....	Acknowledge from slave	55:48	Data byte 2 from slave–8 bits
....	Stop	56	Acknowledge
		....	Data bytes from slave/Acknowledge
		....	Data Byte N from slave–8 bits
		....	NOT Acknowledge
		....	Stop

Table 6. Byte Read and Byte Write Protocol

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
8:2	Slave address–7 bits	8:2	Slave address–7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code–8 bits	18:11	Command Code–8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Data byte–8 bits	20	Repeated start
28	Acknowledge from slave	27:21	Slave address–7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		37:30	Data from slave–8 bits
		38	NOT Acknowledge
		39	Stop

Control Register 0. Byte 0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 00000000

Bit	Name	Function
7:0	Reserved	

Control Register 1. Byte 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				DIFF0_OE		DIFF1_OE	DIFF2_OE	DIFF3_OE
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 00010111

Bit	Name	Function
7:5	Reserved	
4	DIFF0_OE	**Output Enable for DIFF0.** 0: Output disabled. 1: Output enabled.
3	Reserved	
2	DIFF1_OE	**Output Enable for DIFF1.** 0: Output disabled. 1: Output enabled.
1	DIFF2_OE	**Output Enable for DIFF2.** 0: Output disabled. 1: Output enabled.
0	DIFF3_OE	**Output Enable for DIFF3.** 0: Output disabled. 1: Output enabled.

Control Register 2. Byte 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DIFF4_OE	DIFF5_OE	DIFF6_OE	DIFF7_OE	DIFF8_OE			
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 11111000

Bit	Name	Function
7	DIFF4_OE	**Output Enable for DIFF4.** 0: Output disabled. 1: Output enabled.
6	DIFF5_OE	**Output Enable for DIFF5.** 0: Output disabled. 1: Output enabled.
5	DIFF6_OE	**Output Enable for DIFF6.** 0: Output disabled. 1: Output enabled.
4	DIFF7_OE	**Output Enable for DIFF7.** 0: Output disabled. 1: Output enabled.
3	DIFF8_OE	**Output Enable for DIFF8.** 0: Output disabled. 1: Output enabled.
2:0	Reserved	

Control Register 3. Byte 3

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Rev Code[3:0]				Vendor ID[3:0]			
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 00001000

Bit	Name	Function
7:4	Rev Code[3:0]	**Program Revision Code.**
3:0	Vendor ID[3:0]	**Vendor Identification Code.**

Control Register 4. Byte 4

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	BC[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 00000110

Bit	Name	Function
7:0	BC[7:0]	**Byte Count Register.**

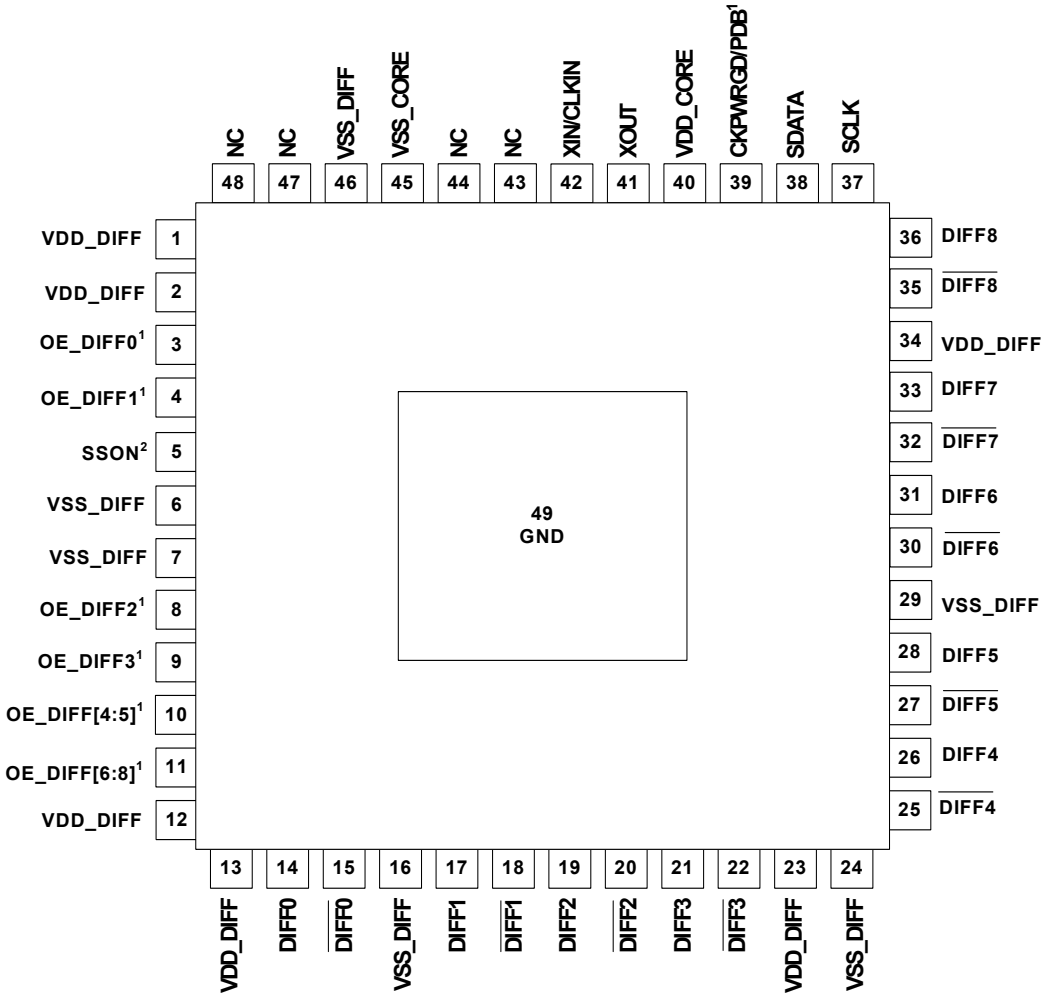
Control Register 5. Byte 5

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DIFF_Amp_Sel	DIFF_Amp_Cntl[2]	DIFF_Amp_Cntl[1]	DIFF_Amp_Cntl[0]				
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 11011000

Bit	Name	Function
7	DIFF_Amp_Sel	**Amplitude Control for DIFF Differential Outputs.** 0: Differential outputs with Default amplitude. 1: Differential outputs amplitude is set by Byte 5[6:4].
6	DIFF_Amp_Cntl[2]	**DIFF Differential Outputs Amplitude Adjustment.** 000: 300 mV 001: 400 mV 010: 500 mV 011: 600 mV 100: 700 mV 101: 800 mV 110: 900 mV 111: 1000 mV
5	DIFF_Amp_Cntl[1]	
4	DIFF_Amp_Cntl[0]	
3:0	Reserved	

5. Pin Descriptions: 48-Pin QFN



Notes:
1. Internal 100 kohm pull-up.
2. Internal 100 kohm pull-down.

Table 7. Si 52147 48-Pin QFN Descriptions

Pin #	Name	Type	Description
1	VDD_DIFF	PWR	3.3 V Power Supply
2	VDD_DIFF	PWR	3.3 V Power Supply
3	OE_DIFF0	I,PU	Active high input pin enables DIFF0 (internal 100 kΩ pull-up).
4	OE_DIFF1	I,PU	Active high input pin enables DIFF1 (internal 100 kΩ pull-up).
5	SSON	I, PD	Active high input pin enables –0.5% spread on DIFF clocks (internal 100 kΩ pull-down)
6	VSS_DIFF	GND	Ground
7	VSS_DIFF	GND	Ground

Table 7. Si 52147 48-Pin QFN Descriptions (Continued)

Pin #	Name	Type	Description
8	OE_DIFF2	I,PU	Active high input pin enables DIFF2 (internal 100 kΩ pull-up).
9	OE_DIFF3	I,PU	Active high input pin enables DIFF3 (internal 100 kΩ pull-up).
10	OE_DIFF[4:5]	I,PU	Active high input pin enables DIFF[4:5] (internal 100 kΩ pull-up).
11	OE_DIFF[6:8]	I,PU	Active high input pin enables DIFF[6:8] (internal 100 kΩ pull-up).
12	VDD_DIFF	PWR	3.3 V Power Supply
13	VDD_DIFF	PWR	3.3 V Power Supply
14	DIFF0	O, DIF	0.7 V, 100 MHz differential clock output
15	$\overline{\text{DIFF0}}$	O, DIF	0.7 V, 100 MHz differential clock output
16	VSS_DIFF	GND	Ground
17	DIFF1	O, DIF	0.7 V, 100 MHz differential clock output
18	$\overline{\text{DIFF1}}$	O, DIF	0.7 V, 100 MHz differential clock output
19	DIFF2	O, DIF	0.7 V, 100 MHz differential clock output
20	$\overline{\text{DIFF2}}$	O, DIF	0.7 V, 100 MHz differential clock output
21	DIFF3	O, DIF	0.7 V, 100 MHz differential clock output
22	$\overline{\text{DIFF3}}$	O, DIF	0.7 V, 100 MHz differential clock output
23	VDD_DIFF	PWR	3.3V Power Supply
24	VSS_DIFF	GND	Ground
25	$\overline{\text{DIFF4}}$	O, DIF	0.7 V, 100 MHz differential clock output
26	DIFF4	O, DIF	0.7 V, 100 MHz differential clock output
27	$\overline{\text{DIFF5}}$	O, DIF	0.7 V, 100 MHz differential clock output
28	DIFF5	O, DIF	0.7 V, 100 MHz differential clock output
29	VSS_DIFF	GND	Ground
30	$\overline{\text{DIFF6}}$	O, DIF	0.7 V, 100 MHz differential clock output
31	DIFF6	O, DIF	0.7 V, 100 MHz differential clock output
32	$\overline{\text{DIFF7}}$	O, DIF	0.7 V, 100 MHz differential clock output
33	DIFF7	O, DIF	0.7 V, 100 MHz differential clock output
34	VDD_DIFF	PWR	3.3 V Power Supply
35	$\overline{\text{DIFF8}}$	O, DIF	0.7 V, 100 MHz differential clock output
36	DIFF8	O, DIF	0.7 V, 100 MHz differential clock output

Table 7. Si 52147 48-Pin QFN Descriptions (Continued)

Pin #	Name	Type	Description
37	SCLK	I	I^2C compatible SCLOCK
38	SDATA	I/O	I^2C compatible SDATA
39	CKPWRGD/PDB	I, PU	Active low input pin asserts power down (PDB) and disables all outputs (internal 100 kΩ pull-up).
40	VDD_CORE	PWR	3.3 V Power Supply
41	XOUT	O	25.00 MHz crystal output, Float XOUT if using only CLKIN (Clock input).
42	XIN/CLKIN	I	25.00 MHz crystal input or 3.3 V, 25 MHz Clock Input.
43	NC	NC	No Connect
44	NC	NC	No Connect
45	VSS_CORE	GND	Ground
46	VSS_DIFF	GND	Ground
47	NC	NC	No Connect
48	NC	NC	No Connect
49	GND	GND	Ground for bottom pad of the IC.

6. Ordering Guide

Part Number	Package Type	Temperature
Lead-free		
Si52147-A01AGM	48-pin QFN	Industrial, –40 to 85 °C
Si52147-A01AGMR	48-pin QFN—Tape and Reel	Industrial, –40 to 85 °C

7. Package Outline

Figure 6 illustrates the package details for the Si52147. Table 8 lists the values for the dimensions shown in the illustration.

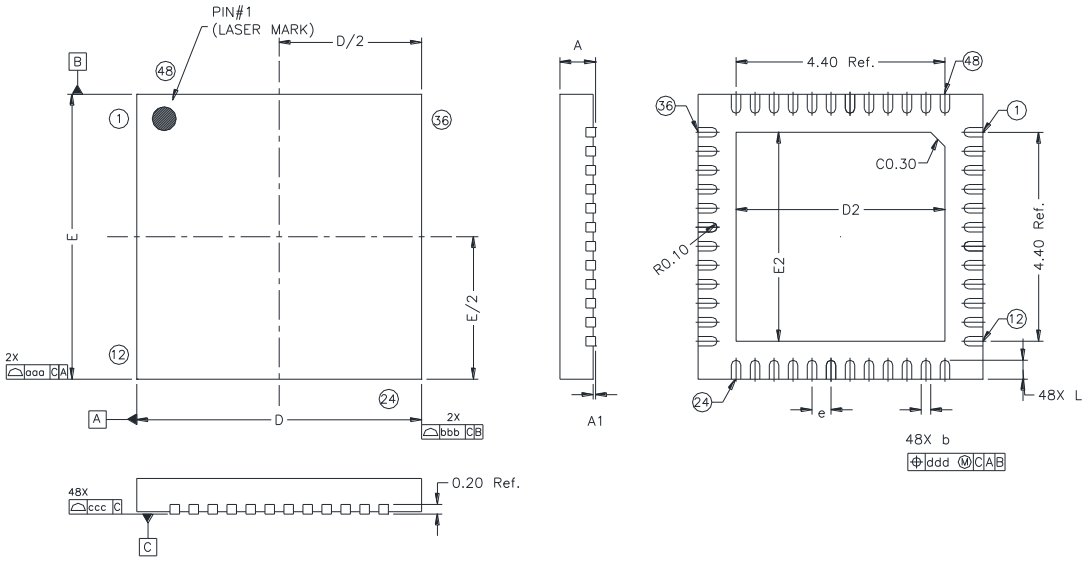


Figure 6. 48-Pin Quad Flat No Lead (QFN) Package

Table 8. Package Diagram Dimensions

Symbol	Millimeters		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	0.025	0.05
b	0.15	0.20	0.25
D		6.00 BSC	
D2	4.30	4.40	4.50
e		0.40 BSC	
E		6.00 BSC	
E2	4.30	4.40	4.50
L	0.30	0.40	0.50
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.07	

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-220, variation VGGD-8.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8. Land Pattern

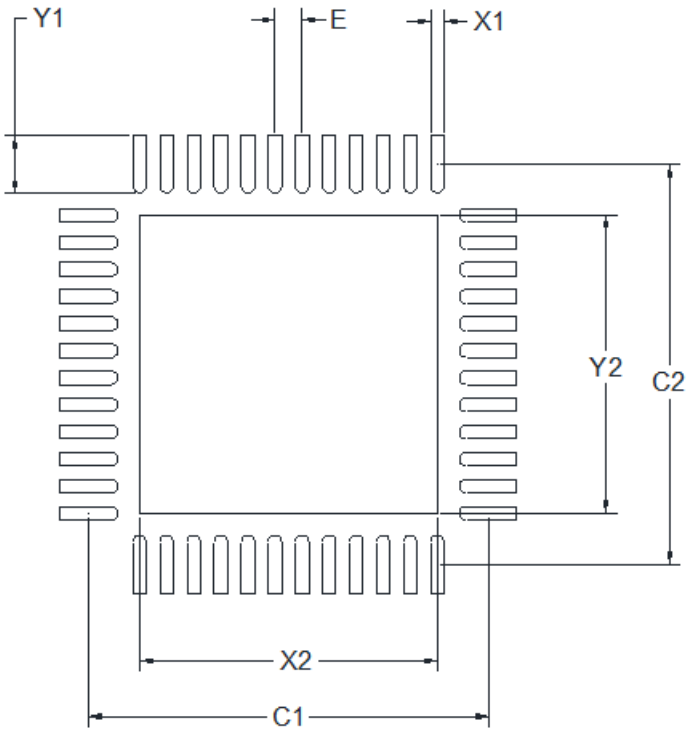


Figure 7. QFN Land Pattern

Table 9. Land Pattern Dimensions

Dimension	Min	Max
C1	5.85	5.95
C2	5.85	5.95
X1	0.15	0.25
Y1	0.80	0.90
E	0.40 BSC	
X2	4.35	4.45

Table 9. Land Pattern Dimensions (Continued)

Y2	4.35	4.45

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.

Solder Mask Design

3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.

Stencil Design

4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter
7. pads.
8. A 4x4 array of 0.80 mm square openings on 1.05 mm pitch should be used for the center ground pad to achieve between 50-60% solder coverage.

Card Assembly

9. A No-Clean, Type-3 solder paste is recommended.
10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Document Change List

Revision 0.1 to Revision 1.0

- Updated pinout.
- Updated Table 2.
- Updated section 2.1.
- Updated section 2.1.1.
- Updated sections 2.2 through 2.8.
- Updated section 4.2.
- Updated Table 7.

Revision 1.0 to Revision 1.1

- Removed Moisture Sensitivity Level specification from Table 3.

Revision 1.1 to Revision 1.2

- Updated Table 2.
- Updated Section 3.

Revision 1.2 to Revision 1.3

- Updated Features on page 1.
- Updated Description on page 1.
- Updated specs in Table 2, “AC Electrical Specifications,” on page 5.

Revision 1.3 to Revision 1.4

- Added test condition for Tstable in Table 2.

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