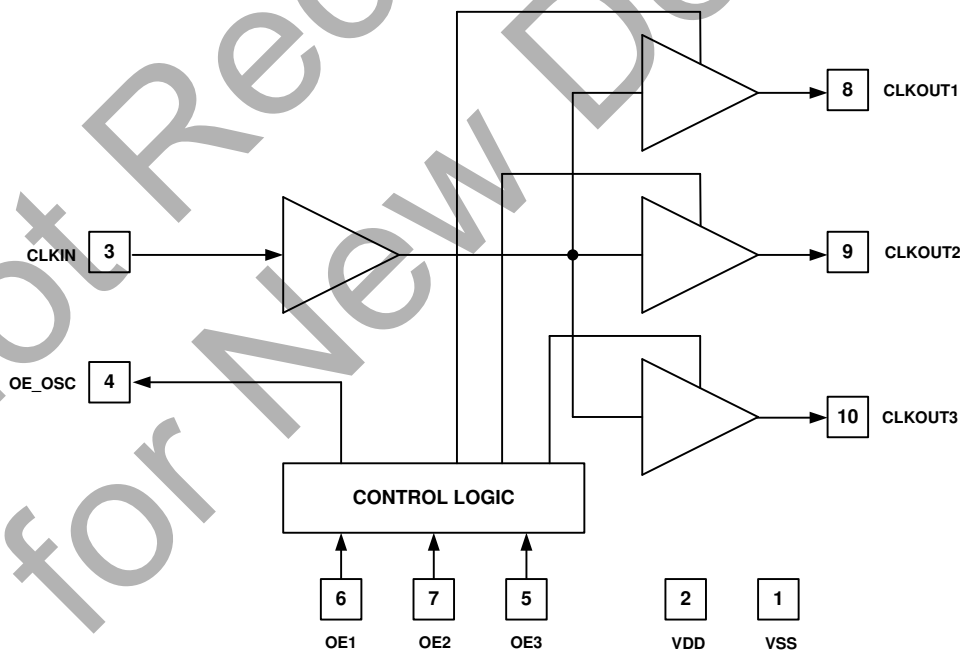


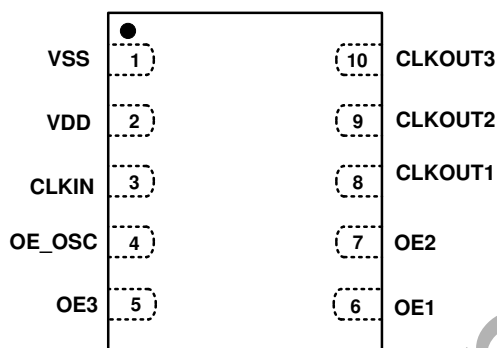
3-Channel Clock Distribution Buffer

| Key Features | Description |
|---|---|
| <ul style="list-style-type: none"> • Low current consumption - 2.7mA-typ (VDD=1.8V and CL=0) • 1.7V to 3.65V power supply operation • 10MHz to 52MHz CLKIN • Supports LVCMOS and clipped sine wave inputs • Supports 3 single-ended LVCMOS square wave outputs • OE1/2/3 functions for each CLKOUT1/2/3 outputs • OE_OSC control pin to enable external TCXO/XO • Ultra-Low phase noise • Ultra low standby current • 10-pin TDFN package (1.4x2.0x0.75 mm) • Industrial -40 °C to 85 °C temperature range | <p>The SL18860DC product is a high performance 3 output clock distribution buffer and provides 3 outputs from a single input clock by using SLI proprietary low phase noise and low power dissipation circuit design.</p> <p>The SL18860DC can be used in baseband mobile RF applications including WLAN, Bluetooth and DVB-H as an input clock reference. The product designed to isolate each device driven by their clock outputs to minimize interference between these devices.</p> <p>Each of the clock buffer outputs can be individually disabled by using OE1/2/3 control pins to reduce the power consumption if the connected device does not need the clock. The device operates from single power supply from 1.7V to 3.65V and from -40 °C to 85 °C.</p> <p>Benefits</p> <ul style="list-style-type: none"> • Fast Time-to-market • Cost Reduction • Low Power Dissipation • Low Phase Noise |
| <p>Application</p> <ul style="list-style-type: none"> • Smart Mobile Handsets • Multi-mode RF Clock Distribution • Baseband Peripheral Clock Distribution | |

Block Diagram



Pin Configuration



10-Pin TDFN Package Pinout

Pin Description

| Pin Number | Pin Name | Pin Type | Pin Description |
|------------|----------|----------|---|
| 1 | VSS | Power | Power supply ground. |
| 2 | VDD | Power | 2.25 to 3.65V or 1.8V +/-5% positive power supply |
| 3 | CLKIN | Input | External clock input pin. VSS to VDD CMOS level. |
| 4 | OE_osc | Output | Crystal oscillator enable pin. If OE1=OE2=OE3=0 then OE_osc=0. OE_osc=1 for all the other OE1/2/3 logic states. |
| 5 | OE3 | Input | Output enable pin for CLKOUT3. The input has 150kΩ-typ on-chip pull-down resistor. |
| 6 | OE1 | Input | Output enable pin for CLKOUT1. The input has 150kΩ-typ on-chip pull-down resistor. |
| 7 | OE2 | Input | Output enable pin for CLKOUT2. The input has 150kΩ-typ on-chip pull-down resistor. |
| 8 | CLKOUT1 | Output | Clock output-1. Clock frequency is the same as CLKIN. |
| 9 | CLKOUT2 | Output | Clock output-2. Clock frequency is the same as CLKIN. |
| 10 | CLKOUT3 | Output | Clock output-3. Clock frequency is the same as CLKIN. |

| OE1 (Input) | OE2 (Input) | OE3 (Input) | OE_osc (Output) | CLKOUT1 | CLKOUT2 | CLKOUT3 |
|-------------|-------------|-------------|-----------------|---------|---------|---------|
| 0 | 0 | 0 | 0 | Hi-Z | Hi-Z | Hi-Z |
| 1 | 0 | 0 | 1 | CLOCK | Hi-Z | Hi-Z |
| 1 | 1 | 0 | 1 | CLOCK | CLOCK | Hi-Z |
| ... | ... | ... | ... | ... | ... | ... |
| 1 | 1 | 1 | 1 | CLOCK | CLOCK | CLOCK |

Table 1. Truth Table for OE1/2/3, OE_osc and CLKOUT1/2/3

Absolute Maximum Ratings

| Description | Condition | Min | Max | Unit |
|----------------------------------|--------------------------------|--------|---------|------|
| Supply voltage, VDD (Absolute) | | -0.5 | 4.6 | V |
| Supply voltage, VDD (Operation) | | 1.70 | 3.65 | V |
| All Inputs and Outputs | | -0.5 | VDD+0.5 | V |
| Ambient Operating Temperature | In operation, C-Grade | -40 | 85 | °C |
| Storage Temperature | No power is applied | -65 | 150 | °C |
| Junction Temperature | In operation, power is applied | - | 125 | °C |
| Soldering Temperature | | - | 260 | °C |
| ESD Rating (Human Body Model) | JEDEC22-A114D | -4,000 | 4,000 | V |
| ESD Rating (Charge Device Model) | JEDEC22-C101C | -1,500 | 1,500 | V |
| ESD Rating (Machine Model) | JEDEC22-A115D | -200 | 200 | V |

DC Electrical Characteristics (I-Grade)

Unless otherwise stated VDD= 1.8V+/- 5% and Operation Temperature Range -40 to +85°C

| Description | Symbol | Condition | Min | Typ | Max | Unit |
|--------------------------|--------|------------------------------------|---------|------|--------|------|
| Operating Voltage | VDD | Operation range, 1.8V+/-5% | 1.70 | 1.80 | 1.90 | V |
| Operating Temperature | TA | I-Grade | -40 | 25 | 85 | °C |
| Input Low Voltage | VIL | CMOS Level, Pins 3,5, 6 and 7 | VSS | - | 0.3VDD | V |
| Input High Voltage | VIH | CMOS Level, Pins 3,5, 6 and 7 | 0.7VDD | - | VDD | V |
| Output High Voltage | VOH | IOH=-4mA, Pins 4, 8, 9 and 10 | VDD-0.4 | - | - | V |
| Output Low Voltage | VOL | IOL=-4mA, Pins 4, 8, 9 and 10 | - | - | 0.4 | V |
| Input Leakage Current | ILH | VIN=VDD, Pins 5, 6 and 7 | -25 | - | 25 | µA |
| Input Leakage Current | ILL | VIN=GND, Pins 5, 6 and 7 | -10 | - | 10 | µA |
| Pull-Down Resistor | RPD | Pins 5, 6 and 7 | 100 | 150 | 250 | kΩ |
| Operating Supply Current | IDD1 | CLKIN=26MHz, OE1=OE2=OE3=1 | - | 2.7 | - | mA |
| Operating Supply Current | IDD2 | OE1=OE2=OE3=0 CLKIN=Low or High | - | - | 1.0 | µA |
| Input Capacitance | CIN | Pins 5, 6 and 7 | - | 3 | 5 | pF |
| Load Capacitance | CL | CLKOUT1/2/3, Pins 8, 9 and 10 | - | 10 | 20 | pF |

AC Electrical Characteristics (I-Grade)

Unless otherwise stated VDD= 1.8V +/- 5% and Operation Temperature Range -40 to +85°C

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---------------------------------|--------|--|------|--------|------|--------|
| Input Clock Range | CLKIN | External Clock, CMOS square wave | 10 | 26.000 | 52 | MHz |
| Output Clock Range | CLKOUT | External Clock, CMOS square wave CLKOUT1/2/3 | 10 | 26.000 | 52 | MHz |
| Input Clock Voltage Swing Level | VINpp | VDD=1.8V | 0.72 | 1 | - | Vpp |
| Input Duty Cycle | DCIN | CLKIN, Pin 3 | 30 | 50 | 70 | % |
| Output Clock Rise Time | tr | VDD=1.8, CL=10pF, measured from 10 to 90% of VDD, Pins 4, 8, 9 and 10 | - | 2.0 | 4.00 | ns |
| Output Clock Fall Time | tf | VDD=1.8, CL=10pF, measured from 10 to 90% of VDD, Pins 4, 8, 9 and 10 | - | 2.0 | 4.00 | ns |
| Additive Phase Noise | APN-1 | CLKIN=26MHz and 1 kHz offset CLKOUT1/2/3 | - | -140 | - | dBc/Hz |
| Additive Phase Noise | APN-2 | CLKIN=26MHz and 10 kHz offset CLKOUT1/2/3 | - | -150 | - | dBc/Hz |
| Additive Phase Noise | APN-3 | CLKIN=26MHz and 100 kHz offset CLKOUT1/2/3 | - | -159 | - | dBc/Hz |
| Power-up Time | tPU | Time duration until CLKOUT1/2/3 frequency reaches valid frequency after power supply reaches 0.9xVDD value | - | 100 | 200 | Ns |
| Output Enable Time | tOE1 | Time from OE raising edge to active at outputs CLKOUT1/2/3 (Asynchronous) | - | 25 | - | ns |
| Output Disable Time | tOD | Time from OE falling edge to Hi-Z at outputs CLKOUT1/2/3 (Asynchronous) | - | 25 | - | ns |
| Output Enable Time | tOE2 | Active recovery time from standby (CLKIN=0 or 1) to active at outputs CLKOUT1/2/3 | - | 100 | - | Ns |

DC Electrical Characteristics (I-Grade)

Unless otherwise stated VDD= 2.5V+/- 10% and Operation Temperature Range -40 to +85°C

| Description | Symbol | Condition | Min | Typ | Max | Unit |
|--------------------------|--------|------------------------------------|---------|------|--------|------|
| Operating Voltage | VDD | Operation range, 2.5V+/-10% | 2.25 | 2.50 | 2.75 | V |
| Operating Temperature | TA | I-Grade | -40 | 25 | 85 | °C |
| Input Low Voltage | VIL | CMOS Level, Pins 3,5, 6 and 7 | VSS | - | 0.3VDD | V |
| Input High Voltage | VIH | CMOS Level, Pins 3,5, 6 and 7 | 0.7VDD | - | VDD | V |
| Output High Voltage | VOH | IOH=-4mA , Pins 4, 8, 9 and 10 | VDD-0.4 | - | - | V |
| Output Low Voltage | VOL | IOL=-4mA, Pins 4, 8, 9 and 10 | - | - | 0.4 | V |
| Input Leakage Current | ILH | VIN=VDD, Pins 5, 6 and 7 | -30 | - | 30 | µA |
| Input Leakage Current | ILL | VIN=GND, Pins 5, 6 and 7 | -15 | - | 15 | µA |
| Pull-Down Resistor | RPD | Pins 5, 6 and 7 | 100 | 150 | 250 | kΩ |
| Operating Supply Current | IDD1 | CLKIN=26MHz, OE1=OE2=OE3=1 | - | 3.0 | - | mA |
| Operating Supply Current | IDD2 | OE1=OE2=OE3=0 CLKIN=Low or High | - | - | 1.5 | µA |
| Input Capacitance | CIN | Pins 5, 6 and 7 | - | 3 | 5 | pF |
| Load Capacitance | CL | CLKOUT1/2/3, Pins 8, 9 and 10 | - | 10 | 20 | pF |

AC Electrical Characteristics (I-Grade)

Unless otherwise stated VDD= 2.5V+/- 10% and Operation Temperature Range -40 to +85°C

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---------------------------------|--------|---|-----|--------|------|--------|
| Input Clock Range | CLKIN | External Clock, CMOS square wave | 10 | 26.000 | 52 | MHz |
| Output Clock Range | CLKOUT | External Clock, CMOS square wave CLKOUT1/2/3 | 10 | 26.000 | 52 | MHz |
| Input Clock Voltage Swing Level | VINpp | VDD=2.5V, connect to CLKIN directly | 1.0 | 1.2 | - | V |
| | | VDD=2.5V, connect to CLKIN through AC coupling and bias circuit | 0.6 | - | - | V |
| Input Duty Cycle | DCIN | CLKIN, Pin 3 | 30 | 50 | 70 | % |
| Output Clock Rise Time | tr | VDD=1.8, CL=10pF, measured from 10 to 90% of VDD, Pins 4, 8, 9 and 10 | - | 2.0 | 4.00 | ns |
| Output Clock Fall Time | tf | VDD=1.8, CL=10pF, measured from 10 to 90% of VDD, Pins 4, 8, 9 and 10 | - | 2.0 | 4.00 | ns |
| Additive Phase Noise | APN-1 | CLKIN=26MHz and 1 kHz offset CLKOUT1/2/3 | - | -142 | - | dBc/Hz |

| | | | | | | |
|-----------------------------|-------|---|---|------|-----|--------|
| Additive Phase Noise | APN-2 | CLKIN=26MHz and 10 kHz offset CLKOUT1/2/3 | - | -156 | - | dBc/Hz |
| Additive Phase Noise | APN-3 | CLKIN=26MHz and 100 kHz offset CLKOUT1/2/3 | - | -164 | - | dBc/Hz |
| Power-up Time | tPU | Time for CLKOUT1/2/3 frequency to reach valid frequency after power supply reaches 0.9xVDDvalue | - | 100 | 200 | ns |
| Output Enable Time | tOE1 | Time from OE raising edge to active at outputs CLKOUT1/2/3 (Asynchronous) | - | 25 | - | ns |
| Output Disable Time | tOD | Time from OE falling edge to Hi-Z at outputs CLKOUT1/2/3 (Asynchronous) | - | 25 | - | ns |
| Output Enable Time | tOE2 | Active recovery time from standby (CLKIN=0 or 1) to active at outputs CLKOUT1/2/3 | - | 100 | - | ns |

DC Electrical Characteristics (I-Grade)

Unless otherwise stated VDD= 3.3V+/- 10% and Operation Temperature Range -40 to +85°C

| Description | Symbol | Condition | Min | Typ | Max | Unit |
|---------------------------------|--------|------------------------------------|---------|-----|--------|------|
| Operating Voltage | VDD | Operation range , 3.3V+/-10% | 2.95 | 3.3 | 3.65 | V |
| Operating Temperature | TA | I-Grade | -40 | 25 | 85 | °C |
| Input Low Voltage | VIL | CMOS Level, Pins 3.5, 6 and 7 | VSS | - | 0.3VDD | V |
| Input High Voltage | VIH | CMOS Level, Pins 3.5, 6 and 7 | 0.7VDD | - | VDD | V |
| Output High Voltage | VOH | IOH=-4mA , Pins 4, 8, 9 and 10 | VDD-0.4 | - | - | V |
| Output Low Voltage | VOL | IOL=-4mA, Pins 4, 8, 9 and 10 | - | - | 0.5 | V |
| Input Leakage Current | ILH | VIN=VDD, Pins 5, 6 and 7 | -35 | - | 35 | µA |
| Input Leakage Current | ILL | VIN=GND, Pins 5, 6 and 7 | -20 | - | 20 | µA |
| Pull-Down Resistor | RPD | Pins 5, 6 and 7 | 100 | 150 | 250 | kΩ |
| Operating Supply Current | IDD1 | CLKIN=26MHz, OE1=OE2=OE3=1 | - | 3.4 | - | mA |
| Operating Supply Current | IDD2 | OE1=OE2=OE3=0 CLKIN=Low or High | - | - | 2.0 | µA |
| Input Capacitance | CIN | Pins 5, 6 and 7 | - | 3 | 5 | pF |
| Load Capacitance | CL | CLKOUT1/2/3, Pins 8, 9 and 10 | - | 10 | 25 | pF |

AC Electrical Characteristics (I-Grade)

Unless otherwise stated VDD= 3.3V+/- 10% and Operation Temperature Range -40 to +85°C

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|--|--------|--|------|--------|-----|--------|
| Input Clock Range | CLKIN | External Clock, CMOS square wave | 10 | 26.000 | 52 | MHz |
| Output Clock Range | CLKOUT | External Clock, CMOS square wave CLKOUT1/2/3 | 10 | 26.000 | 52 | MHz |
| Input Clock Voltage Swing Level | VINpp | VDD=3.3V, connect to CLKIN directly | 1.32 | 1.4 | - | V |
| | | VDD=3.3V, connect to CLKIN through AC coupling and bias circuit | 0.6 | - | - | V |
| Input Duty Cycle | DCIN | CLKIN, Pin 3 | 30 | 50 | 70 | % |
| Output Clock Rise Time | tr | VDD=1.8, CL=10pF, measured from 10 to 90% of VDD, Pins 4, 8, 9 and 10 | - | 1.2 | 2.2 | ns |
| Output Clock Fall Time | tf | VDD=1.8, CL=10pF, measured from 10 to 90% of VDD, Pins 4, 8, 9 and 10 | - | 1.2 | 2.2 | ns |
| Additive Phase Noise | APN-1 | CLKIN=26MHz and 1 kHz offset CLKOUT1/2/3 | - | -138 | - | dBc/Hz |
| Additive Phase Noise | APN-2 | CLKIN=26MHz and 10 kHz offset CLKOUT1/2/3 | - | -157 | - | dBc/Hz |
| Additive Phase Noise | APN-3 | CLKIN=26MHz and 100 kHz offset CLKOUT1/2/3 | - | -165 | - | dBc/Hz |
| Power-up Time | tPU | Time duration until CLKOUT1/2/3 frequency reaches valid frequency after power supply reaches 0.9xVDD value | - | 100 | 200 | ns |
| Output Enable Time | tOE1 | Time from OE raising edge to active at outputs CLKOUT1/2/3 (Asynchronous) | - | 25 | - | ns |
| Output Disable Time | tOD | Time from OE falling edge to Hi-Z at outputs CLKOUT1/2/3 (Asynchronous) | - | 25 | - | ns |
| Output Enable Time | tOE2 | Active recovery time from standby (CLKIN=0 or 1) to active at outputs CLKOUT1/2/3 | - | 100 | - | ns |

| SL18860DC CLKOUT1/2/3 | | | | | | | |
|-------------------------------|---------|---------|---------|---------|---------|---------|-------|
| Phase Noise (dBc/Hz) CL=15pF. | | | | | | | |
| VDD(V) | 100hz | 1Khz | 10Khz | 100Khz | 1Mhz | 5Mhz | Fig # |
| 1.8 | -115.52 | -139.85 | -150.79 | -159.31 | -160.52 | -162.52 | 1 |
| 2.5 | -125.16 | -142.67 | -156.37 | -164.02 | -166.45 | -167.02 | 2 |
| 3.3 | -116.60 | -138.06 | 157.41 | -164.88 | -167.21 | -168.57 | 3 |

Table 2. Output Phase Noise Summary Table

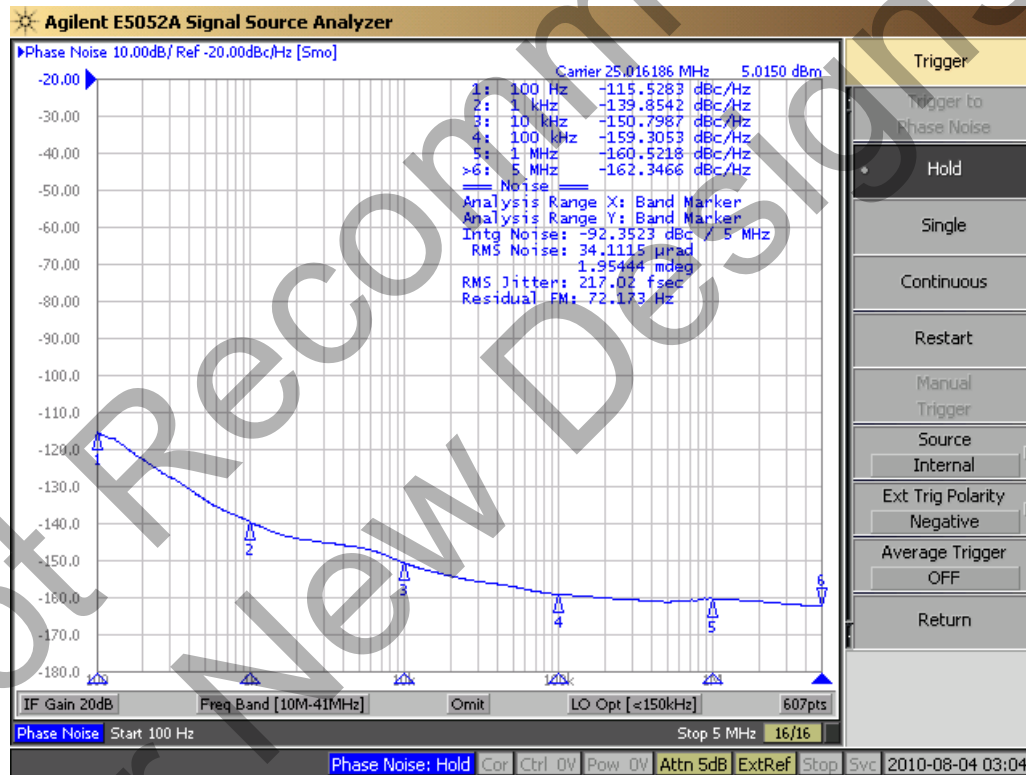


Figure 1. Output Phase Noise VDD=1.8V, CL=15pF

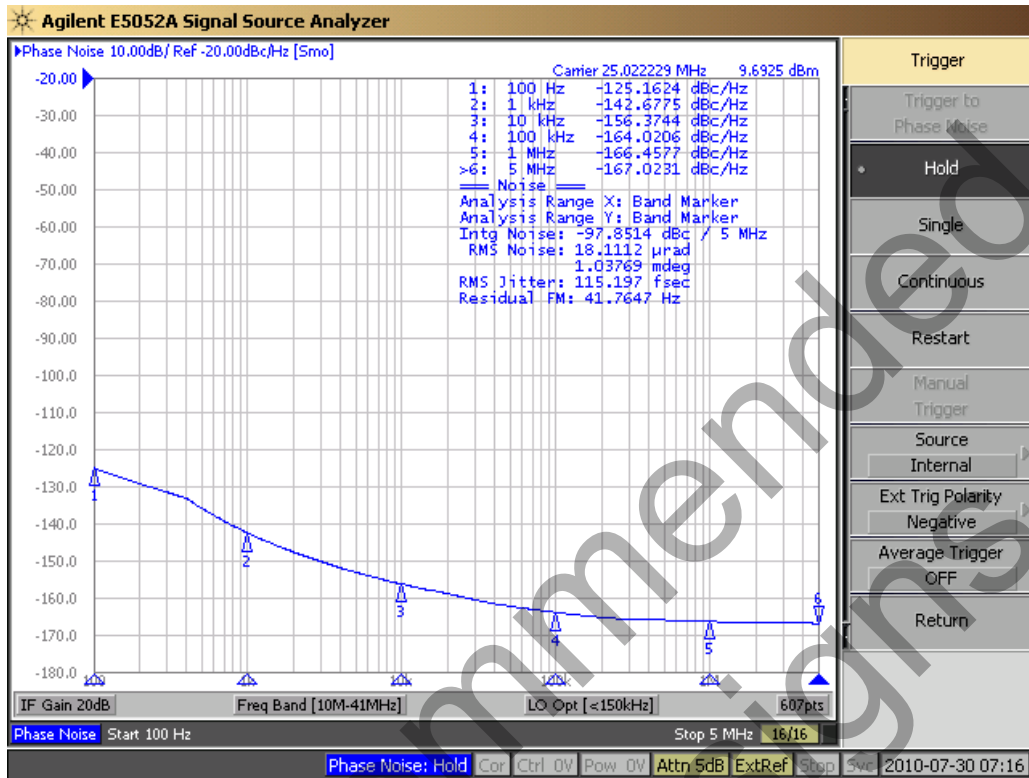


Figure 2. Output Phase Noise VDD=2.5V, CL=15pF

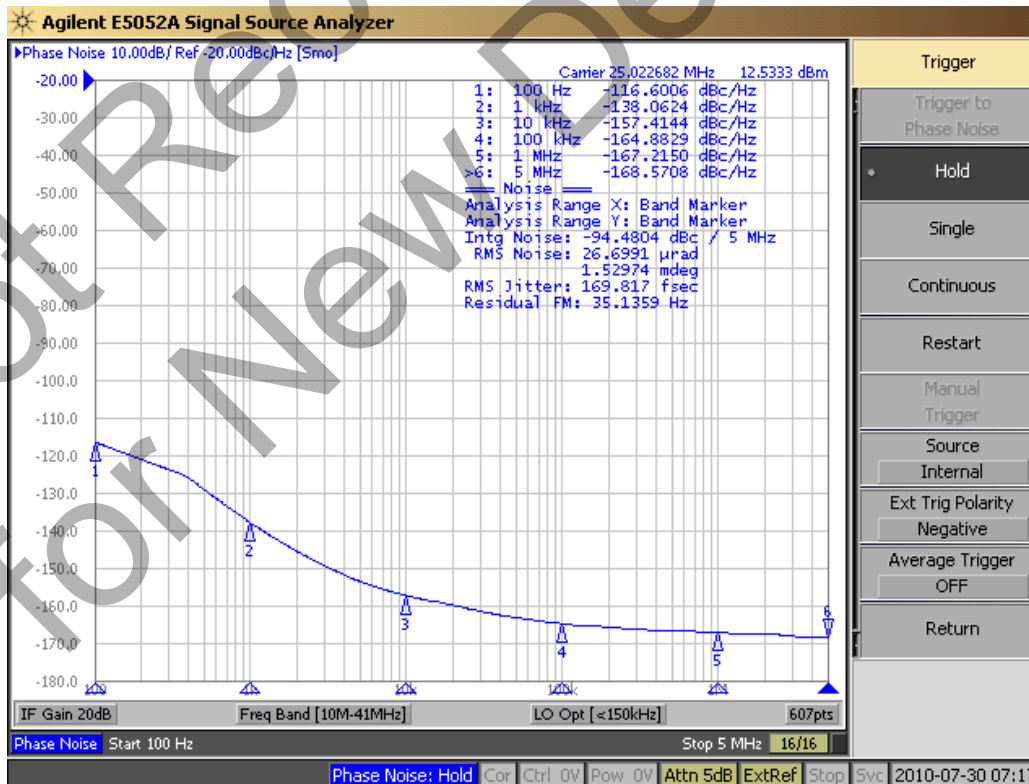
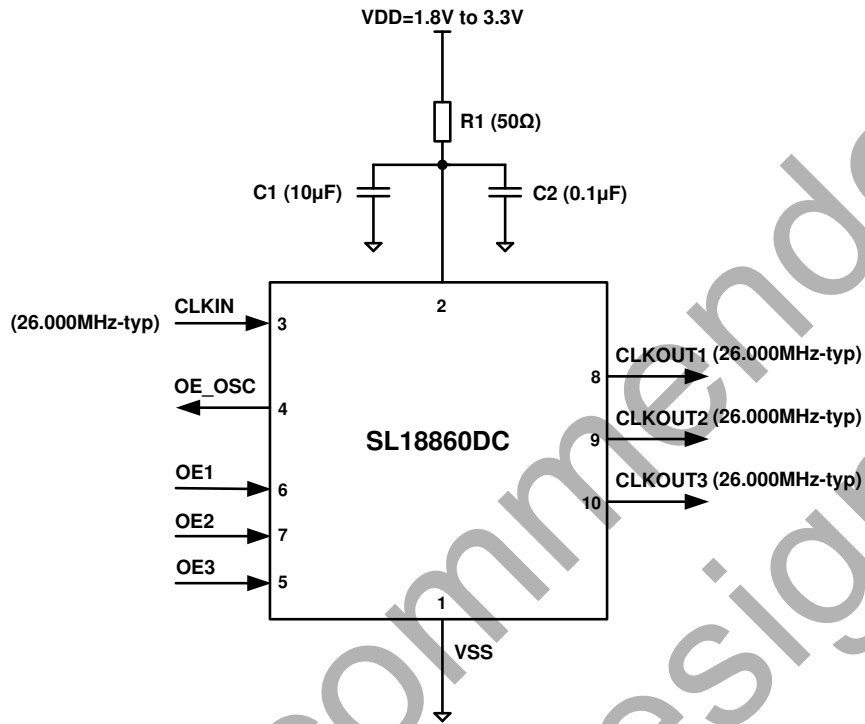
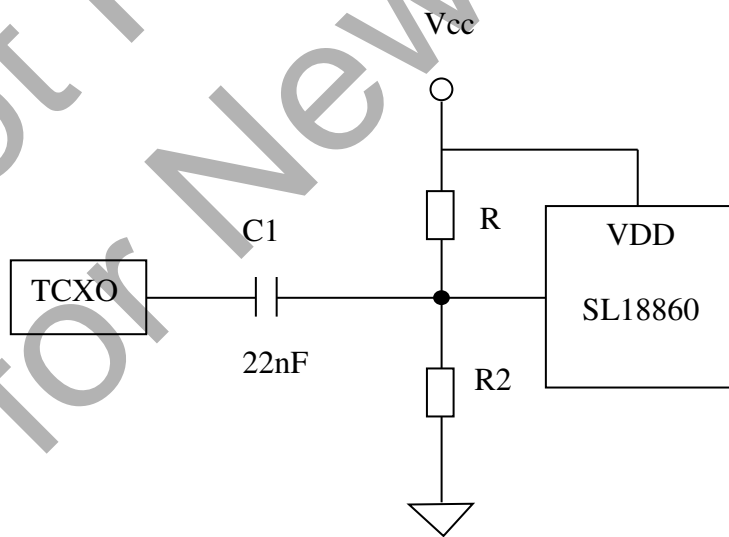


Figure 3. Output Phase Noise VDD=3.3V, CL=15pF

Typical Application Circuit

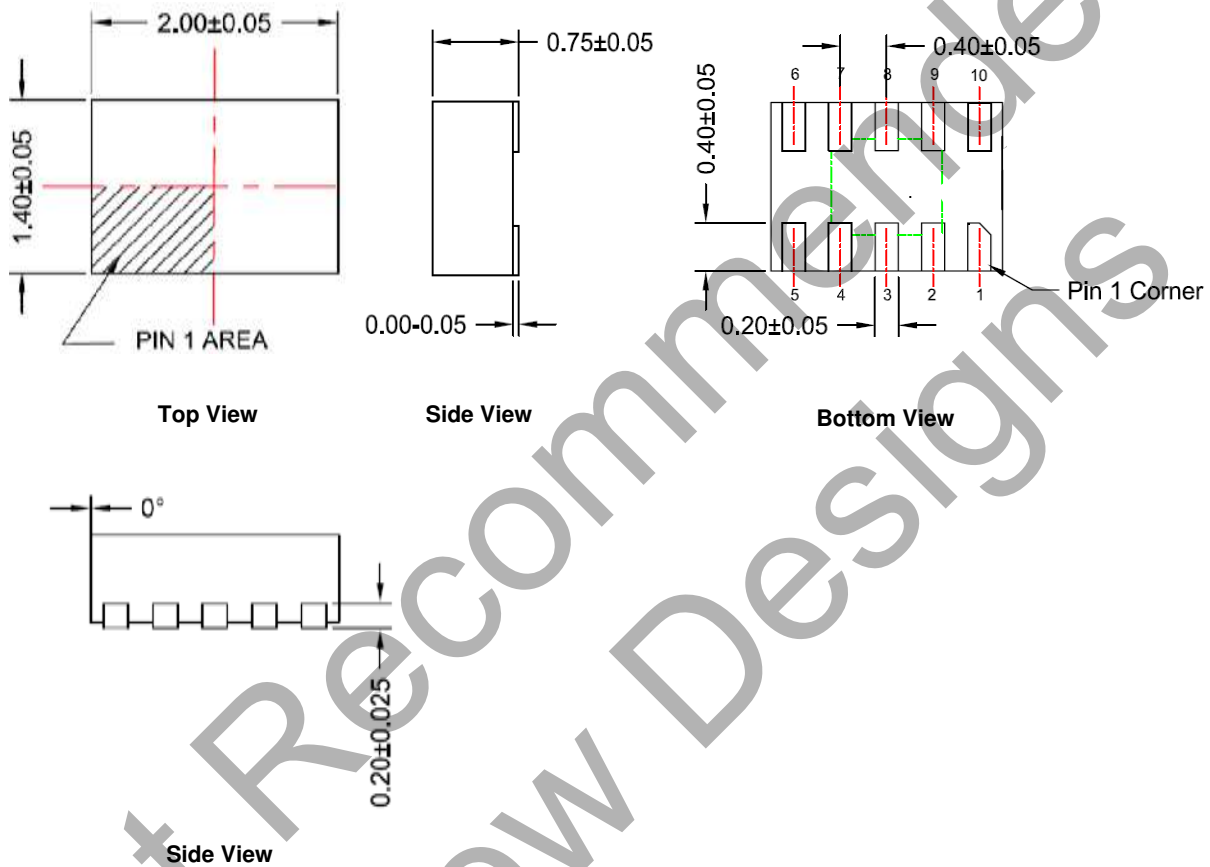


AC coupling and bias circuit



Package Outline and Package Dimensions

10-Pin TDFN Package (1.4x2.0x0.75 mm)



Ordering Information

| Ordering Number | Shipping Package | Package | Temperature |
|-----------------|------------------|-------------|-------------|
| SL18860DC | Tube | 10-pin TDFN | -40 to 85°C |
| SL18860DCT | Tape and Reel | 10-pin TDFN | -40 to 85°C |

Note:

The SL18860 is RoHS compliant



Pin 1

| Line | Characters | Description |
|------|------------|---|
| 1 | TTTT | Manufacturing Trace Code |
| 2 | YWW | Characters corresponding to the last digit of year (Y) and work week (WW) of package assembly |



ClockBuilder Pro

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Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
USA

<http://www.silabs.com>