

# CD74FCT646T, CD74FCT648T, CD74FCT651T, CD74FCT652T, CD74FCT2646T, CD74FCT2652T

December 1996

## Fast CMOS Octal Registered Transceivers

### Features

- Advanced 0.8 micron CMOS Technology
- These Devices are Pin Compatible with Bipolar FAST™ Series at a Higher Speed, Lower Power Consumption
- 25Ω Series Resistor on All Outputs (FCT2XXX Only)
- TTL Input and Output Levels
- Low Ground Bounce Outputs
- Extremely Low Static Power
- Hysteresis on All Inputs

### Description

These devices are designed with a bus transceiver with three-state D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. The CD74FCT651T, CD74FCT652T and CD74FCT2652T utilize GAB and  $\bar{G}B\bar{A}$  signals to control the transceiver functions. The CD74FCT646T, CD74FCT2646T and CD74FCT648T utilize the enable control ( $\bar{G}$ ) and direction pins (DIR) to control the transceiver functions. SAB and SBA control pins are used to select either real-time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between real-time and stored data. A low input level selects real-time data and a high selects stored data.

The CD74FCT646T is a non-inverting option of the CD74FCT648T. The CD74FCT652T is a non-inverting option of the CD74FCT651T.

The CD74FCT2646T and CD74FCT2652T devices have a built-in 25Ω series resistor on all outputs to reduce noise due to reflections, thus eliminating the need for an external terminating resistor.

### Ordering Information

| PART NUMBER     | TEMP. RANGE (°C) | PACKAGE    | PKG. NO. |
|-----------------|------------------|------------|----------|
| CD74FCT646ATM   | -40 to 85        | 24 Ld SOIC | M24.3-P  |
| CD74FCT646ATQM  | -40 to 85        | 24 Ld QSOP | M24.15-P |
| CD74FCT646CTM   | -40 to 85        | 24 Ld SOIC | M24.3-P  |
| CD74FCT646CTQM  | -40 to 85        | 24 Ld QSOP | M24.15-P |
| CD74FCT646DTM   | -40 to 85        | 24 Ld SOIC | M24.3-P  |
| CD74FCT646DTQM  | -40 to 85        | 24 Ld QSOP | M24.15-P |
| CD74FCT646TM    | -40 to 85        | 24 Ld SOIC | M24.3-P  |
| CD74FCT646TQM   | -40 to 85        | 24 Ld QSOP | M24.15-P |
| CD74FCT648ATM   | -40 to 85        | 24 Ld SOIC | M24.3-P  |
| CD74FCT648ATQM  | -40 to 85        | 24 Ld QSOP | M24.15-P |
| CD74FCT648CTM   | -40 to 85        | 24 Ld SOIC | M24.3-P  |
| CD74FCT648CTQM  | -40 to 85        | 24 Ld QSOP | M24.15-P |
| CD74FCT648TM    | -40 to 85        | 24 Ld SOIC | M24.3-P  |
| CD74FCT648TQM   | -40 to 85        | 24 Ld QSOP | M24.15-P |
| CD74FCT651ATM   | -40 to 85        | 24 Ld SOIC | M24.3-P  |
| CD74FCT651ATQM  | -40 to 85        | 24 Ld QSOP | M24.15-P |
| CD74FCT651CTM   | -40 to 85        | 24 Ld SOIC | M24.3-P  |
| CD74FCT651CTQM  | -40 to 85        | 24 Ld QSOP | M24.15-P |
| CD74FCT651TM    | -40 to 85        | 24 Ld SOIC | M24.3-P  |
| CD74FCT651TQM   | -40 to 85        | 24 Ld QSOP | M24.15-P |
| CD74FCT652ATM   | -40 to 85        | 24 Ld SOIC | M24.3-P  |
| CD74FCT652ATQM  | -40 to 85        | 24 Ld QSOP | M24.15-P |
| CD74FCT652CTM   | -40 to 85        | 24 Ld SOIC | M24.3-P  |
| CD74FCT652CTQM  | -40 to 85        | 24 Ld QSOP | M24.15-P |
| CD74FCT652DTM   | -40 to 85        | 24 Ld SOIC | M24.3-P  |
| CD74FCT652DTQM  | -40 to 85        | 24 Ld QSOP | M24.15-P |
| CD74FCT652TM    | -40 to 85        | 24 Ld SOIC | M24.3-P  |
| CD74FCT652TQM   | -40 to 85        | 24 Ld QSOP | M24.15-P |
| CD74FCT2646ATM  | -40 to 85        | 24 Ld SOIC | M24.3-P  |
| CD74FCT2646ATQM | -40 to 85        | 24 Ld QSOP | M24.15-P |
| CD74FCT2646TM   | -40 to 85        | 24 Ld SOIC | M24.3-P  |
| CD74FCT2646TQM  | -40 to 85        | 24 Ld QSOP | M24.15-P |
| CD74FCT2652ATM  | -40 to 85        | 24 Ld SOIC | M24.3-P  |
| CD74FCT2652ATQM | -40 to 85        | 24 Ld QSOP | M24.15-P |
| CD74FCT2652CTM  | -40 to 85        | 24 Ld SOIC | M24.3-P  |
| CD74FCT2652CTQM | -40 to 85        | 24 Ld QSOP | M24.15-P |
| CD74FCT2652TM   | -40 to 85        | 24 Ld SOIC | M24.3-P  |
| CD74FCT2652TQM  | -40 to 85        | 24 Ld QSOP | M24.15-P |

NOTE: QSOP is commonly known as SSOP.

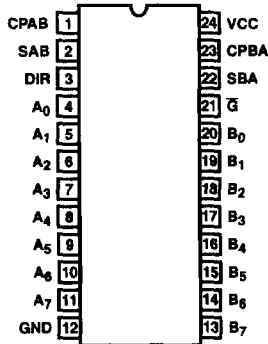
When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

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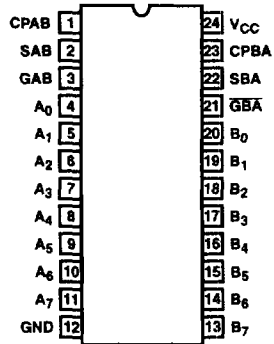
OCTAL 5V FCT  
5V FCT 25Ω

**Pinouts**

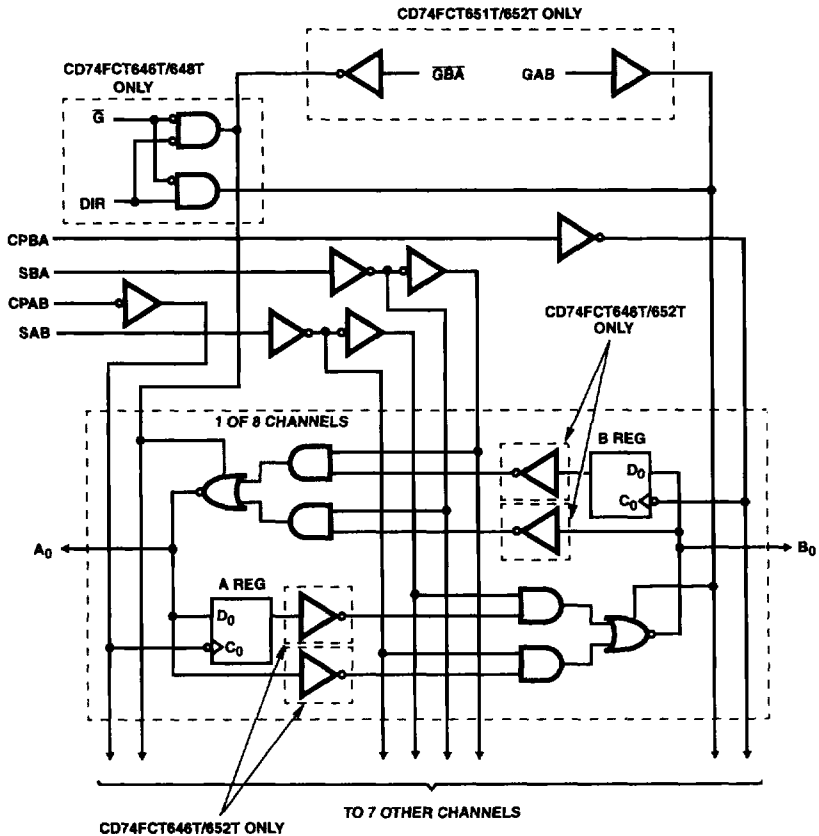
CD74FCT646T, CD74FCT648T, CD74FCT2646T  
(QSOP, SOIC)  
TOP VIEW



CD74FCT651T, CD74FCT652T, CD74FCT2652T  
(QSOP, SOIC)  
TOP VIEW



**Functional Block Diagram**



**CD74FCT646T, CD74FCT648T, CD74FCT651T, CD74FCT652T, CD74FCT2646T, CD74FCT2652T**

**CD74FCT646T, CD74FCT2646T, CD74FCT648T TRUTH TABLE**

| CD74FCT646T,<br>CD74FCT2646T | CD74FCT648T                       | INPUTS    |     |        |        |     |     | (NOTE 2)<br>DATA I/O           |                                |
|------------------------------|-----------------------------------|-----------|-----|--------|--------|-----|-----|--------------------------------|--------------------------------|
|                              |                                   | $\bar{G}$ | DIR | CPAB   | CPBA   | SAB | SBA | A <sub>0</sub> -A <sub>7</sub> | B <sub>0</sub> -B <sub>7</sub> |
| Isolation                    | Isolation                         | H         | X   | H or L | H or L | X   | X   | Input                          | Input                          |
| Store A and B Data           | Store A and B Data                | H         | X   | ↑      | ↑      | X   | X   | Input                          | Input                          |
| Real Time B Data to A Bus    | Real Time $\bar{B}$ Data to A Bus | L         | L   | X      | X      | X   | L   | Output                         | Input                          |
| Stored B Data to A Bus       | Stored $\bar{B}$ Data to A Bus    | L         | L   | X      | H or L | X   | H   | Output                         | Input                          |
| Real Time A Data to B Bus    | Real Time $\bar{A}$ Data to B Bus | L         | H   | X      | X      | L   | X   | Input                          | Output                         |
| Stored A Data to B Bus       | Stored $\bar{A}$ Data to B Bus    | L         | H   | H or L | X      | H   | X   | Input                          | Output                         |

**CD74FCT651T, CD74FCT652T, CD74FCT2652T TRUTH TABLE**

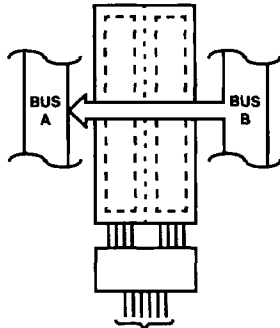
| CD74FCT651T  | CD74FCT652T,<br>CD74FCT2652T                         | INPUTS |                         |        |        |               |               | (NOTE 2)<br>DATA I/O           |                                |
|--|--|--------|-------------------------|--------|--------|---------------|---------------|--------------------------------|--------------------------------|
|  |  | GAB    | $\bar{G}\bar{B}\bar{A}$ | CPAB   | CPBA   | SAB           | SBA           | A <sub>0</sub> -A <sub>7</sub> | B <sub>0</sub> -B <sub>7</sub> |
| Isolation  | Isolation  | L      | H                       | H or L | H or L | X             | X             | Input                          | Input                          |
| Store A and B Data   | Store A and B Data                                   | L      | H                       | ↑      | ↑      | X             | X             | Input                          | Input                          |
| Store A, Hold B  | Store A, Hold B                                      | X      | H                       | ↑      | H or L | X             | X             | Input                          | Unspecified<br>(Note 1)        |
| Store A in Both Registers<br>(Note 3)                                | Store A in Both Registers                            | H      | H                       | ↑      | ↑      | X<br>(Note 2) | X             | Input                          | Output                         |
| Hold A, Store B  | Hold A, Store B                                      | L      | X                       | H or L | ↑      | X             | X             | Unspecified<br>(Note 1)        | Input                          |
| Store B in Both Registers<br>(Note 4)                                | Store B in Both Registers                            | L      | L                       | ↑      | ↑      | X             | X<br>(Note 2) | Output                         | Input                          |
| Real Time $\bar{B}$ Data to A Bus                                    | Real Time B Data to A Bus                            | L      | L                       | X      | X      | X             | L             | Output                         | Input                          |
| Stored $\bar{B}$ Data to A Bus                                       | Stored B Data to A Bus                               | L      | L                       | X      | H or L | X             | H             | Output                         | Input                          |
| Real Time $\bar{A}$ Data to B Bus                                    | Real Time A Data to B Bus                            | H      | H                       | X      | X      | L             | X             | Input                          | Output                         |
| Stored $\bar{A}$ Data to B Bus                                       | Stored A Data to B Bus                               | H      | H                       | H or L | X      | H             | X             | Input                          | Output                         |
| Stored $\bar{A}$ Data to B Bus and<br>Stored $\bar{B}$ Data to A Bus | Stored A Data to B Bus and<br>Stored B Data to A Bus | H      | L                       | H or L | H or L | H             | H             | Output                         | Output                         |

**NOTES:**

- The data output functions may be enabled or disabled by various signals at the GAB or  $\bar{G}\bar{B}\bar{A}$  inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.
- Select control = L: clocks can occur simultaneously.  
Select control = H: clocks must be staggered in order to load both registers.  
H = High Voltage Level; L = Low Voltage Level; X = Don't Care; ↑ = LOW-to-HIGH transition
- $\bar{A}$  in B Register.
- $\bar{B}$  in A Register.

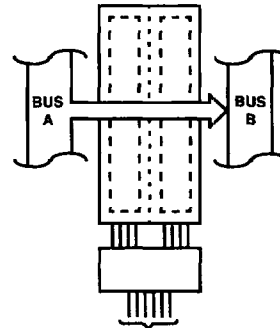
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**OCTAL 5V FCT  
5V FCT 25Ω**



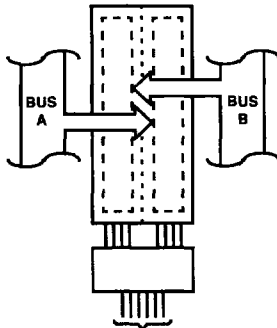
|                 |     |                  |      |      |     |     |
|-----------------|-----|------------------|------|------|-----|-----|
| 646T/648T/2646T | DIR | $\bar{G}$        | CPAB | CPBA | SAB | SBA |
|                 | L   | L                | X    | X    | X   | L   |
| 651T/652T/2652T | GAB | $\bar{G}\bar{A}$ | CPAB | CPBA | SAB | SBA |
|                 | L   | L                | X    | X    | X   | L   |

FIGURE 1. REAL-TIME TRANSFER BUS B TO A



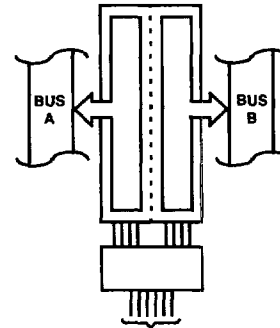
|                 |     |                  |      |      |     |     |
|-----------------|-----|------------------|------|------|-----|-----|
| 646T/648T/2646T | DIR | $\bar{G}$        | CPAB | CPBA | SAB | SBA |
|                 | H   | L                | X    | X    | L   | X   |
| 651T/652T/2652T | GAB | $\bar{G}\bar{A}$ | CPAB | CPBA | SAB | SBA |
|                 | H   | H                | X    | X    | L   | X   |

FIGURE 2. REAL-TIME TRANSFER BUS A TO B



|                 |     |                  |      |      |     |     |
|-----------------|-----|------------------|------|------|-----|-----|
| 646T/648T/2646T | DIR | $\bar{G}$        | CPAB | CPBA | SAB | SBA |
|                 | H   | L                | ↑    | X    | X   | X   |
|                 | L   | L                | X    | ↑    | X   | X   |
| 651T/652T/2652T | GAB | $\bar{G}\bar{A}$ | CPAB | CPBA | SAB | SBA |
|                 | X   | H                | ↑    | X    | X   | X   |
|                 | L   | X                | X    | ↑    | X   | X   |
|                 | L   | H                | ↑    | ↑    | X   | X   |

FIGURE 3. STORAGE FROM A AND/OR B



|                             |     |                  |      |      |     |     |
|-----------------------------|-----|------------------|------|------|-----|-----|
| 646T/648T/2646T<br>(NOTE 5) | DIR | $\bar{G}$        | CPAB | CPBA | SAB | SBA |
|                             | L   | L                | X    | HorL | X   | H   |
| 651T/652T/2652T             | GAB | $\bar{G}\bar{A}$ | CPAB | CPBA | SAB | SBA |
|                             | H   | L                | HorL | HorL | H   | H   |

FIGURE 4. TRANSFER STORES DATA TO A AND/OR B

NOTE:

- The CD74FCT646T and CD74FCT2646T cannot transfer data to A bus and B bus simultaneously.

**Pin Descriptions**

| PIN NAME                       | DESCRIPTION   |
|--------------------------------|---|
| A <sub>0</sub> -A <sub>7</sub> | Data Register A Inputs<br>Data Register B Outputs                   |
| B <sub>0</sub> -B <sub>7</sub> | Data Register B Inputs<br>Data Register A Outputs                   |
| CPAB, CPBA                     | Clock Pulse Inputs  |
| SAB, SBA                       | Output Data Source Select Inputs                                    |
| DIR, $\bar{G}$                 | Output Enable Inputs<br>(CD74FCT646T, CD74FCT648T,<br>CD74FCT2646T) |
| GAB, $\bar{G}A$                | Output Enable Inputs<br>(CD74FCT651T, CD74FCT652T,<br>CD74FCT2652T) |
| GND                            | Ground  |
| V <sub>CC</sub>                | Power   |

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OCTAL 5V FCT  
5V FCT 25Ω

**CD74FCT646T, CD74FCT648T, CD74FCT651T, CD74FCT652T, CD74FCT2646T, CD74FCT2652T**

**Absolute Maximum Ratings**

DC Input Voltage ..... -0.5V to 7.0V  
 DC Output Current ..... 120mA

**Operating Conditions**

Operating Temperature Range ..... -40°C to 85°C  
 Supply Voltage to Ground Potential  
 Inputs and V<sub>CC</sub> Only ..... -0.5V to 7.0V  
 Supply Voltage to Ground Potential  
 Outputs and D/O Only ..... -0.5V to 7.0V

**Thermal Information**

Thermal Resistance (Typical, Note 6)  $\theta_{JA}$  (°C/W)  
 SOIC Package ..... 75  
 QSOP Package ..... 100  
 Maximum Junction Temperature ..... 150°C  
 Maximum Storage Temperature Range ..... -65°C to 150°C  
 Maximum Lead Temperature (Soldering 10s) ..... 300°C  
 (Lead Tips Only)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

**NOTE**

6.  $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

**Electrical Specifications**

| PARAMETER  | SYMBOL                                 | (NOTE 7)<br>TEST CONDITIONS   | MIN                                      | (NOTE 8)<br>TYP | MAX  | UNITS |    |
|--|--|---|--|-----------------|------|-------|----|
| <b>DC ELECTRICAL SPECIFICATIONS</b> Over the Operating Range, T <sub>A</sub> = -40°C to 85°C, V <sub>CC</sub> = 5.0V ±5% |  |   |  |                 |      |       |    |
| Output HIGH Voltage  | V <sub>OH</sub>                        | V <sub>CC</sub> = Min, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> | I <sub>OH</sub> = -15.0mA                | 2.4             | 3.0  | -     | V  |
| Output LOW Voltage   | V <sub>OL</sub>                        | V <sub>CC</sub> = Min, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> | I <sub>OL</sub> = 64mA                   | -               | 0.3  | 0.55  | V  |
| Output LOW Voltage   | V <sub>OL</sub>                        | V <sub>CC</sub> = Min, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> | I <sub>OL</sub> = 12mA<br>(25Ω series)   | -               | 0.3  | 0.55  | V  |
| Input HIGH Voltage   | V <sub>IH</sub>                        | Guaranteed Logic HIGH Level   |  | 2.0             | -    | -     | V  |
| Input LOW Voltage  | V <sub>IL</sub>                        | Guaranteed Logic LOW Level  |  | -               | -    | 0.8   | V  |
| Input HIGH Current   | I <sub>IH</sub>                        | V <sub>CC</sub> = Max   | V <sub>IN</sub> = V <sub>CC</sub>        | -               | -    | 1     | μA |
| Input LOW Current  | I <sub>IL</sub>                        | V <sub>CC</sub> = Max   | V <sub>IN</sub> = GND                    | -               | -    | -1    | μA |
| High impedance<br>Output Current   | I <sub>OZH</sub> ,<br>I <sub>OZL</sub> | V <sub>CC</sub> = Max   | V <sub>OUT</sub> = 2.7V                  |                 |      | 1     | μA |
|  |  |   | V <sub>OUT</sub> = 0.5V                  |                 |      | -1    | μA |
| Clamp Diode Voltage  | V <sub>IK</sub>                        | V <sub>CC</sub> = Min, I <sub>IN</sub> = -18mA                              |  | -               | -0.7 | -1.2  | V  |
| Short Circuit Current  | I <sub>OS</sub>                        | V <sub>CC</sub> = Max (Note 9),<br>V <sub>OUT</sub> = GND                   |  | -60             | -120 | -     | mA |
| Power Down Disable   | I <sub>OFF</sub>                       | V <sub>CC</sub> = GND, V <sub>OUT</sub> = 4.5V                              |  | -               | -    | 100   | μA |
| Input Hysteresis   | V <sub>H</sub>                         |   |  | -               | 200  | -     | mV |
| <b>CAPACITANCE</b> T <sub>A</sub> = 25°C, f = 1MHz   |  |   |  |                 |      |       |    |
| Input Capacitance<br>(Note 10)   | C <sub>IN</sub>                        | V <sub>IN</sub> = 0V  |  | -               | 6    | 10    | pF |
| Output<br>Capacitance (Note 10)  | C <sub>OUT</sub>                       | V <sub>OUT</sub> = 0V   |  | -               | 8    | 12    | pF |
| <b>POWER SUPPLY SPECIFICATIONS</b>   |  |   |  |                 |      |       |    |
| Quiescent Power<br>Supply Current  | I <sub>CC</sub>                        | V <sub>CC</sub> = Max   | V <sub>IN</sub> = GND or V <sub>CC</sub> | -               | 0.1  | 500   | μA |
| Supply Current per<br>Input at TTL HIGH  | ΔI <sub>CC</sub>                       | V <sub>CC</sub> = Max   | V <sub>IN</sub> = 3.4V<br>(Note 11)      | -               | 0.5  | 2     | mA |

**Electrical Specifications (Continued)**

| PARAMETER                                  | SYMBOL           | (NOTE 7)<br>TEST CONDITIONS  |  | MIN | (NOTE 8)<br>TYP | MAX              | UNITS      |
|--|------------------|--|--|-----|-----------------|------------------|------------|
| Supply Current per Input per MHz (Note 12) | I <sub>CCD</sub> | V <sub>CC</sub> = Max, Outputs Open<br>G̅ or DIR = GND or<br>GAB = G̅B̅A = GND<br>One Input Toggling<br>50% Duty Cycle   | V <sub>IN</sub> = V <sub>CC</sub><br>V <sub>IN</sub> = GND | -   | 0.15            | 0.25             | mA/<br>MHz |
| Total Power Supply Current (Note 14)       | I <sub>C</sub>   | V <sub>CC</sub> = Max, Outputs Open<br>f <sub>CP</sub> = 10MHz, 50% Duty Cycle<br>G̅ = DIR = GND or<br>GAB = G̅B̅A = GND<br>f <sub>I</sub> = 5MHz<br>One Bit Toggling                      | V <sub>IN</sub> = V <sub>CC</sub><br>V <sub>IN</sub> = GND | -   | 1.5             | 3.5<br>(Note 13) | mA         |
|  |                  |  | V <sub>IN</sub> = 3.4V<br>V <sub>IN</sub> = GND            | -   | 2.0             | 5.5<br>(Note 13) | mA         |
|  |                  | V <sub>CC</sub> = Max, Outputs Open<br>f <sub>CP</sub> = 10MHz, 50% Duty Cycle<br>G̅ = DIR = GND or<br>GAB = G̅B̅A = GND<br>f <sub>I</sub> = 2.5MHz, 50% Duty Cycle<br>Eight Bits Toggling | V <sub>IN</sub> = V <sub>CC</sub><br>V <sub>IN</sub> = GND | -   | 3.8             | 7.3              | mA         |
|  |                  |  | V <sub>IN</sub> = 3.4V<br>V <sub>IN</sub> = GND            | -   | 6.0             | 16.3             | mA         |

**Switching Specifications Over Operating Range**

| PARAMETER                                     | SYMBOL                                 | (NOTE 15)<br>TEST<br>CONDITIONS                | T   |      | AT               |     | (NOTE 18)<br>CT  |     | (NOTE 18, 19)<br>DT |     | UNIT |
|---|--|--|---|------|------------------|-----|------------------|-----|---------------------|-----|------|
|   |  |  | (NOTE 16)<br>MIN                              | MAX  | (NOTE 16)<br>MIN | MAX | (NOTE 16)<br>MIN | MAX | (NOTE 16)<br>MIN    | MAX |      |
|   |  |  | <b>CD74FCT646T, CD74FCT2646T, CD74FCT648T</b> |      |                  |     |                  |     |                     |     |      |
| Propagation Delay Bus to Bus                  | t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | C <sub>L</sub> = 50pF<br>R <sub>L</sub> = 500Ω | 2.0   | 7.5  | 2.0              | 6.3 | 1.5              | 5.4 | 1.5                 | 4.8 | ns   |
| Output Enable Time G̅, DIR to Bus             | t <sub>PZH</sub> ,<br>t <sub>PZL</sub> | C <sub>L</sub> = 50pF<br>R <sub>L</sub> = 500Ω | 2.0   | 14.0 | 2.0              | 9.8 | 1.5              | 7.8 | 1.5                 | 7.3 | ns   |
| Output Disable Time G̅, DIR to Bus (Note 17)  | t <sub>PHZ</sub> ,<br>t <sub>PLZ</sub> | C <sub>L</sub> = 50pF<br>R <sub>L</sub> = 500Ω | 2.0   | 9.0  | 2.0              | 6.3 | 1.5              | 6.3 | 1.5                 | 6.3 | ns   |
| Propagation Delay Clock to Bus                | t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | C <sub>L</sub> = 50pF<br>R <sub>L</sub> = 500Ω | 2.0   | 9.0  | 2.0              | 6.3 | 1.5              | 5.7 | 1.5                 | 5.2 | ns   |
| Propagation Delay SBA or SAB to Bus           | t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | C <sub>L</sub> = 50pF<br>R <sub>L</sub> = 500Ω | 2.0   | 9.5  | 2.0              | 7.7 | 1.5              | 6.2 | 1.5                 | 5.8 | ns   |
| Setup Time HIGH or LOW, Bus to Clock          | t <sub>SU</sub>                        | C <sub>L</sub> = 50pF<br>R <sub>L</sub> = 500Ω | 4.0   | -    | 2.0              | -   | 2.0              | -   | 2.0                 | -   | ns   |
| Hold Time HIGH or LOW, Bus to Clock           | t <sub>H</sub>                         | C <sub>L</sub> = 50pF<br>R <sub>L</sub> = 500Ω | 2.0   | -    | 1.5              | -   | 1.5              | -   | 1.5                 | -   | ns   |
| Clock Pulse Width HIGH or LOW (Note 17)       | t <sub>W</sub>                         | C <sub>L</sub> = 50pF<br>R <sub>L</sub> = 500Ω | 6.0   | -    | 5.0              | -   | 5.0              | -   | 5.0                 | -   | ns   |
| <b>CD74FCT651T, CD74FCT652T, CD74FCT2652T</b> |  |  |   |      |                  |     |                  |     |                     |     |      |
| Propagation Delay Bus to Bus                  | t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | C <sub>L</sub> = 50pF<br>R <sub>L</sub> = 500Ω | 2.0   | 9.0  | 2.0              | 6.3 | 1.5              | 5.4 | 1.5                 | 4.8 | ns   |
| Output Enable Time G̅B̅A, GAB to Bus          | t <sub>PZH</sub> ,<br>t <sub>PZL</sub> | C <sub>L</sub> = 50pF<br>R <sub>L</sub> = 500Ω | 2.0   | 12.5 | 2.0              | 9.8 | 1.5              | 7.8 | 1.5                 | 7.3 | ns   |

**4**  
 OCTAL 5V FCT  
 5V FCT 25Ω

Switching Specifications Over Operating Range (Continued)

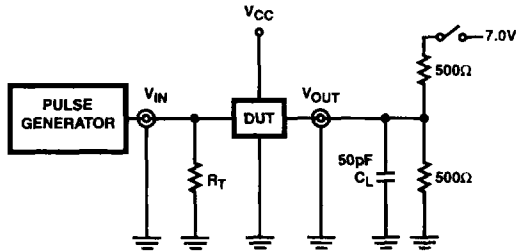
| PARAMETER   | SYMBOL                                 | (NOTE 15)<br>TEST<br>CONDITIONS                | T                |     | AT               |     | (NOTE 18)<br>CT  |     | (NOTE 18, 19)<br>DT |     | UNIT |
|---|--|--|------------------|-----|------------------|-----|------------------|-----|---------------------|-----|------|
|   |  |  | (NOTE 16)<br>MIN | MAX | (NOTE 16)<br>MIN | MAX | (NOTE 16)<br>MIN | MAX | (NOTE 16)<br>MIN    | MAX |      |
| Output Disable Time<br>GBA, GAB to Bus<br>(Note 17) | t <sub>PHZ</sub> ,<br>t <sub>PLZ</sub> | C <sub>L</sub> = 50pF<br>R <sub>L</sub> = 500Ω | 2.0              | 9.0 | 2.0              | 6.3 | 1.5              | 6.3 | 1.5                 | 6.0 | ns   |
| Propagation Delay<br>Clock to Bus                   | t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | C <sub>L</sub> = 50pF<br>R <sub>L</sub> = 500Ω | 2.0              | 9.0 | 2.0              | 6.3 | 1.5              | 5.7 | 1.5                 | 5.2 | ns   |
| Propagation Delay<br>SBA or SAB to Bus              | t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | C <sub>L</sub> = 50pF<br>R <sub>L</sub> = 500Ω | 2.0              | 9.5 | 2.0              | 7.7 | 1.5              | 6.2 | 1.5                 | 5.8 | ns   |
| Setup Time HIGH or<br>LOW, Bus to Clock             | t <sub>SU</sub>                        | C <sub>L</sub> = 50pF<br>R <sub>L</sub> = 500Ω | 4.0              | -   | 2.0              | -   | 2.0              | -   | 2.0                 | -   | ns   |
| Hold Time HIGH or<br>LOW, Bus to Clock              | t <sub>H</sub>                         | C <sub>L</sub> = 50pF<br>R <sub>L</sub> = 500Ω | 2.0              | -   | 1.5              | -   | 1.5              | -   | 1.5                 | -   | ns   |
| Clock Pulse Width<br>HIGH or LOW<br>(Note 17)       | t <sub>W</sub>                         | C <sub>L</sub> = 50pF<br>R <sub>L</sub> = 500Ω | 6.0              | -   | 5.0              | -   | 5.0              | -   | 5.0                 | -   | ns   |

NOTES:

7. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
8. Typical values are at V<sub>CC</sub> = 5.0V, 25°C ambient and maximum loading.
9. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
10. This parameter is determined by device characterization but is not production tested.
11. Per TTL driven input (V<sub>IN</sub> = 3.4V); all other inputs at V<sub>CC</sub> or GND.
12. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
13. Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.
14. I<sub>C</sub> = I<sub>QUIESCENT</sub> + I<sub>INPUTS</sub> + I<sub>DYNAMIC</sub>  
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$   
 I<sub>CC</sub> = Quiescent Current  
 ΔI<sub>CC</sub> = Power Supply Current for a TTL High Input (V<sub>IN</sub> = 3.4V)  
 D<sub>H</sub> = Duty Cycle for TTL Inputs High  
 N<sub>T</sub> = Number of TTL Inputs at D<sub>H</sub>  
 I<sub>CCD</sub> = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)  
 f<sub>CP</sub> = Clock Frequency for Register Devices (Zero for Non-Register Devices)  
 f<sub>I</sub> = Input Frequency  
 N<sub>I</sub> = Number of Inputs at f<sub>I</sub>  
 All currents are in milliamps and all frequencies are in megahertz.
15. See test circuit and wave forms.
16. Minimum limits are guaranteed but not tested on Propagation Delays.
17. This parameter is guaranteed but not production tested.
18. Not applicable to CD74FCT2646T, CD74FCT2652T.
19. Not applicable to CD74FCT648T.
20. Not applicable to CD74FCT651T or CD74FCT652T.



Test Circuits and Waveforms



21. Pulse Generator for All Pulses: Rate  $\leq 1.0\text{MHz}$ ;  $Z_{OUT} \leq 50\Omega$ ;  $t_f, t_r \leq 2.5\text{ns}$ .

FIGURE 5. TEST CIRCUIT

| SWITCH POSITION                      |        |
|--------------------------------------|--------|
| TEST                                 | SWITCH |
| $t_{PLZ}, t_{PZL}$                   | Closed |
| $t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}$ | Open   |

DEFINITIONS:

$C_L$  = Load capacitance, includes jig and probe capacitance.  
 $R_T$  = Termination resistance, should be equal to  $Z_{OUT}$  of the Pulse Generator.

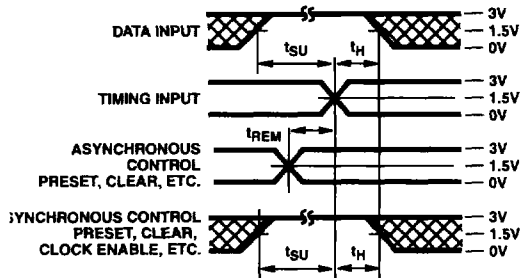


FIGURE 6. SETUP, HOLD, AND RELEASE TIMING

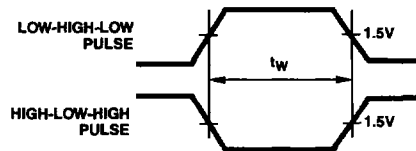


FIGURE 7. PULSE WIDTH

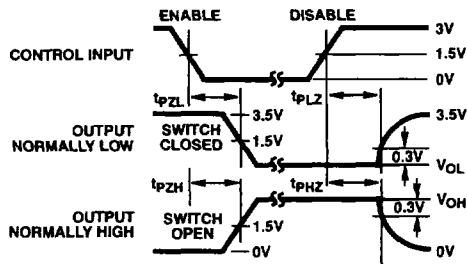


FIGURE 8. ENABLE AND DISABLE TIMING

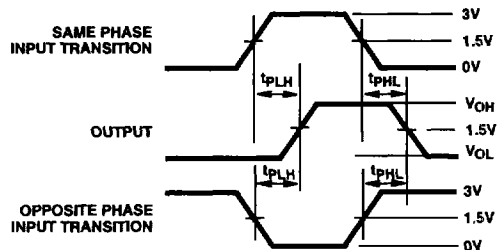


FIGURE 9. PROPAGATION DELAY