Freescale Semiconductor
Data Sheet: Technical Data

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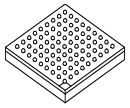
MCF5373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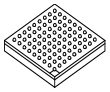
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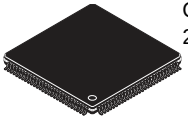

QFP–160
28mm x 28mm

MCF537*x* ColdFire® Microprocessor Data Sheet

Features

- Version 3 ColdFire variable-length RISC processor core
- System debug support
- JTAG support for system level board testing
- On-chip memories
  - 16-Kbyte unified write-back cache
  - 32-Kbyte dual-ported SRAM on CPU internal bus, accessible by core and non-core bus masters (e.g., DMA, FEC, and USB host and OTG)
- Power management
- Embedded Voice-over-IP (VoIP) system solution
- SDR/DDR SDRAM Controller
- Universal Serial Bus (USB) Host Controller
- Universal Serial Bus (USB) On-the-Go (OTG) controller
- Synchronous Serial Interface (SSI)
- Fast Ethernet Controller (FEC)
- Cryptography Hardware Accelerators
- FlexCAN Module
- Three Universal Asynchronous Receiver Transmitters (UARTs)
- I^2C Module
- Queued Serial Peripheral Interface (QSPI)
- Pulse Width Modulation (PWM) module
- Real Time Clock
- Four 32-bit DMA Timers
- Software Watchdog Timer
- Four Periodic Interrupt Timers (PITs)
- Phase Locked Loop (PLL)
- Interrupt Controllers (x2)
- DMA Controller
- FlexBus (External Interface)
- Chip Configuration Module (CCM)
- Reset Controller
- General Purpose I/O interface

Table of Contents

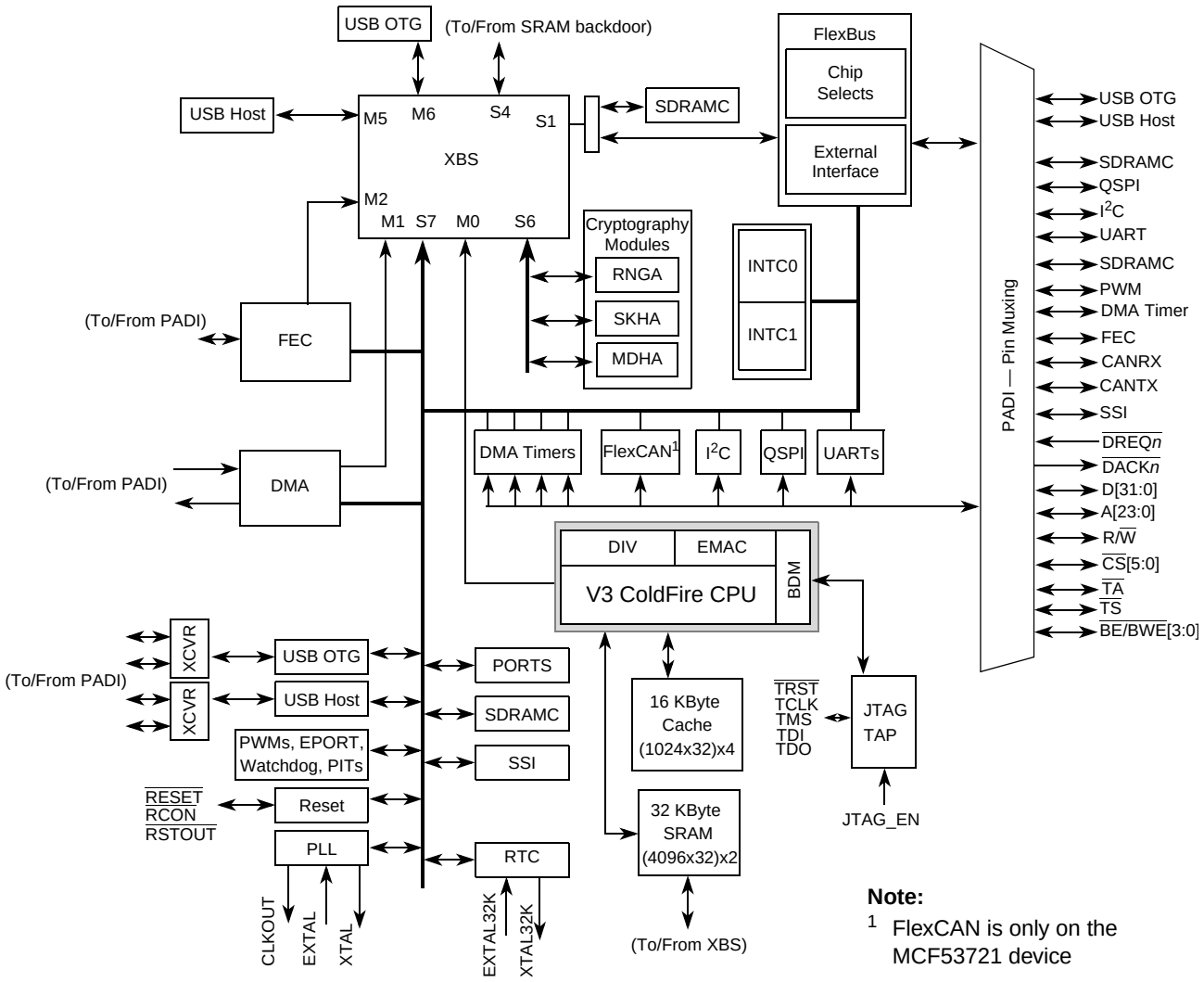


Figure 1. MCF5373 Block Diagram

1 MCF537*x* Family Comparison

The following table compares the various device derivatives available within the MCF537*x* family.

Table 1. MCF537*x* Family Configurations

Module	MCF5372	MCF5372L	MCF53721	MCF5373	MCF5373L
ColdFire Version 3 Core with EMAC (Enhanced Multiply-Accumulate Unit)	•	•	•	•	•
Core (System) Clock	up to 180 MHz	up to 240 MHz		up to 180 MHz	up to 240 MHz
Peripheral and External Bus Clock (Core clock ÷ 3)	up to 60 MHz	up to 80 MHz		up to 60 MHz	up to 80 MHz
Performance (Dhrystone/2.1 MIPS)	up to 158	up to 211		up to 158	up to 211
Instruction/Data Cache	16 Kbytes				

Table 1. MCF537*x* Family Configurations (continued)

Module	MCF5372	MCF5372L	MCF53721	MCF5373	MCF5373L
Static RAM (SRAM)	32 Kbytes				
SDR/DDR SDRAM Controller	•	•	•	•	•
USB 2.0 Host	—	•	•	—	•
USB 2.0 On-the-Go	—	•	•	—	•
Synchronous Serial Interface (SSI)	•	•	•	•	•
Fast Ethernet Controller (FEC)	•	•	•	•	•
Cryptography Hardware Accelerators	—	—	—	•	•
Embedded Voice-over-IP System Solution	—	—	•	—	—
FlexCAN 2.0B communication module	—	—	•	—	—
UARTs	3	3	3	3	3
I^2C	•	•	•	•	•
QSPI	•	•	•	•	•
PWM Module	—	•	•	—	•
Real Time Clock	•	•	•	•	•
32-bit DMA Timers	4	4	4	4	4
Watchdog Timer (WDT)	•	•	•	•	•
Periodic Interrupt Timers (PIT)	4	4	4	4	4
Edge Port Module (EPORT)	•	•	•	•	•
Interrupt Controllers (INTC)	2	2	2	2	2
16-channel Direct Memory Access (DMA)	•	•	•	•	•
FlexBus External Interface	•	•	•	•	•
General Purpose I/O (GPIO)	up to 46	up to 62	up to 62	up to 46	up to 62
JTAG - IEEE® 1149.1 Test Access Port	•	•	•	•	•
Package	160 QFP	196 MAPBGA	196 MAPBGA	160 QFP	196 MAPBGA

2 Ordering Information

Table 2. Orderable Part Numbers

Freescale Part Number	Description	Package	Speed	Temperature
MCF5372CAB180	MCF5372 RISC Microprocessor	160 QFP	180 MHz	–40° to +85° C
MCF5372LCVM240	MCF5372 RISC Microprocessor	196 MAPBGA	240 MHz	–40° to +85° C
MCF53721CVM240	MCF53721 RISC Microprocessor	196 MAPBGA	240 MHz	–40° to +85° C
MCF5373CAB180	MCF5373 RISC Microprocessor	160 QFP	180 MHz	–40° to +85° C
MCF5373LCVM240	MCF5373 RISC Microprocessor	196 MAPBGA	240 MHz	–40° to +85° C

3 Hardware Design Considerations

3.1 PLL Power Filtering

To further enhance noise isolation, an external filter is strongly recommended for PLL analog V_{DD} pins. The filter shown in Figure 2 should be connected between the board V_{DD} and the $PLLV_{DD}$ pins. The resistor and capacitors should be placed as close to the dedicated $PLLV_{DD}$ pin as possible.

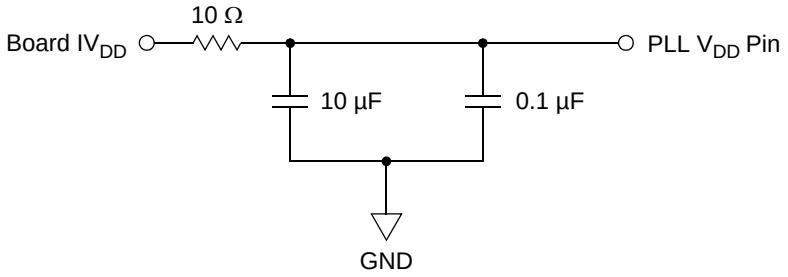


Figure 2. System PLL V_{DD} Power Filter

3.2 USB Power Filtering

To minimize noise, external filters are required for each of the USB power pins. The filter shown in Figure 3 should be connected between the board EV_{DD} or IV_{DD} and each of the $USBV_{DD}$ pins. The resistor and capacitors should be placed as close to the dedicated $USBV_{DD}$ pin as possible.

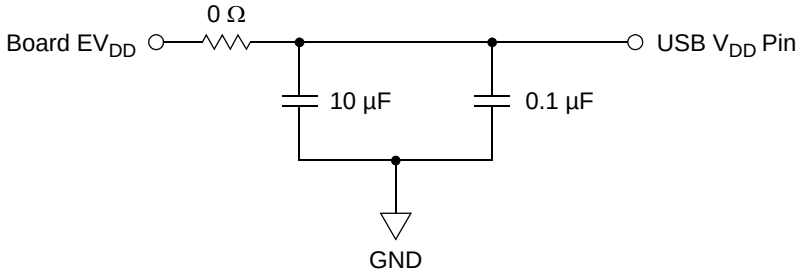


Figure 3. USB V_{DD} Power Filter

NOTE

In addition to the above filter circuitry, a 0.01 F capacitor is also recommended in parallel with those shown.

3.3 Supply Voltage Sequencing and Separation Cautions

The relationship between SDV_{DD} and EV_{DD} is non-critical during power-up and power-down sequences. SDV_{DD} (2.5V or 3.3V) and EV_{DD} are specified relative to IV_{DD}.

3.3.1 Power Up Sequence

If EV_{DD}/SDV_{DD} are powered up with IV_{DD} at 0 V, the sense circuits in the I/O pads cause all pad output drivers connected to the EV_{DD}/SDV_{DD} to be in a high impedance state. There is no limit on how long after EV_{DD}/SDV_{DD} powers up before IV_{DD} must powered up. IV_{DD} should not lead the EV_{DD}, SDV_{DD}, or $PLLV_{DD}$ by more than 0.4 V during power ramp-up or there is

high current in the internal ESD protection diodes. The rise times on the power supplies should be slower than 500 us to avoid turning on the internal ESD protection clamp diodes.

3.3.2 Power Down Sequence

If IV_{DD}/$PLLV_{DD}$ are powered down first, sense circuits in the I/O pads cause all output drivers to be in a high impedance state. There is no limit on how long after IV_{DD} and $PLLV_{DD}$ power down before EV_{DD} or SDV_{DD} must power down. IV_{DD} should not lag EV_{DD}, SDV_{DD}, or $PLLV_{DD}$ going low by more than 0.4 V during power down or there is undesired high current in the ESD protection diodes. There are no requirements for the fall times of the power supplies.

The recommended power down sequence is as follows:

1. Drop IV_{DD}/$PLLV_{DD}$ to 0 V.
2. Drop EV_{DD}/SDV_{DD} supplies.

4 Pin Assignments and Reset States

4.1 Signal Multiplexing

The following table lists all the MCF537*x* pins grouped by function. The Dir column is the direction for the primary function of the pin only. Refer to Section 7, "Package Information," for package diagrams. For a more detailed discussion of the MCF537*x* signals, consult the *MCF5373 Reference Manual* (MCF5373RM).

NOTE

In this table and throughout this document, a single signal within a group is designated without square brackets (i.e., A23), while designations for multiple signals within a group use brackets (i.e., A[23:21]) and is meant to include all signals within the two bracketed numbers when these numbers are separated by a colon.

NOTE

The primary functionality of a pin is not necessarily its default functionality. Pins that are muxed with GPIO default to their GPIO functionality.

Table 3. MCF5372/3 Signal Information and Muxing

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	Voltage Domain	MCF5372 MCF5373 160 QFP	MCF5372L MCF53721 MCF5373L 196 MAPBGA
Reset							
$\overline{\text{RESET}}$[2]	—	—	—	I	EVDD	95	K13
$\overline{\text{RSTOUT}}$	—	—	—	O	EVDD	86	L12
Clock							
EXTAL	—	—	—	I	EVDD	91	L14
XTAL[2]	—	—	—	O	EVDD	93	K14
EXTAL32K	—	—	—	I	EVDD	—	P13
XTAL32K	—	—	—	O	EVDD	—	N13
FB_CLK	—	—	—	O	SDVDD	40	N1

Table 3. MCF5372/3 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	Voltage Domain	MCF5372 MCF5373 160 QFP	MCF5372L MCF53721 MCF5373L 196 MAPBGA
Mode Selection							
$\overline{\text{RCON}}$[2]	—	—	—	I	EVDD	72	P8
DRAMSEL	—	—	—	I	EVDD	92	J11
FlexBus							
A[23:22]	—	$\overline{\text{FB\_CS}}$[5:4]	—	O	SDVDD	134, 133	A9, B9
A[21:16]	—	—	—	O	SDVDD	132–127	C9, D9, A10, B10, C10, D10
A[15:14]	—	SD_BA[1:0][3]	—	O	SDVDD	126, 123	A11, B11
A[13:11]	—	SD_A[13:11][3]	—	O	SDVDD	120–118	C11, A12, B12
A10	—	—	—	O	SDVDD	11 7	A13
A[9:0]	—	SD_A[9:0][3]	—	O	SDVDD	116–107	A14, B14, B13, C12, D11, C14, C13, D14–D12
D[31:16]	—	SD_D[31:16][4]	—	I/O	SDVDD	27–34, 46–53	J2, J1, K4–K1, L4, L3, N2, P1, P2, N3, L5, P3, N4, P4
D[15:1]	—	FB_D[31:17][4]	—	I/O	SDVDD	16–23, 57–63	F2, F1, G4–G1, H4, H3, L6, M6, N6, P6, L7, M7, N7
D0[2]	—	FB_D[16][4]	—	I/O	SDVDD	64	P7
$\overline{\text{BE/BWE}}$[3:0]	PBE[3:0]	$\overline{\text{SD\_DQM}}$[3:0][3]	—	O	SDVDD	26, 54, 24, 56	J3, M5, H2, P5
$\overline{\text{OE}}$	PBUSCTL3	—	—	O	SDVDD	66	M8
$\overline{\text{TA}}$[2]	PBUSCTL2	—	—	I	SDVDD	106	E14
R/$\overline{\text{W}}$	PBUSCTL1	—	—	O	SDVDD	65	L8
$\overline{\text{TS}}$	PBUSCTL0	$\overline{\text{DACK0}}$	—	O	SDVDD	12	E2
Chip Selects							
$\overline{\text{FB\_CS}}$[5:4]	PCS[5:4]	—	—	O	SDVDD	—	D8, C8
$\overline{\text{FB\_CS}}$[3:2]	PCS[3:2]	—	—	O	SDVDD	—	B8, A8
$\overline{\text{FB\_CS1}}$	PCS1	—	—	O	SDVDD	135	D7
$\overline{\text{FB\_CS0}}$	—	—	—	O	SDVDD	136	C7
SDRAM Controller							
SD_A10	—	—	—	O	SDVDD	43	M2
SD_CKE	—	—	—	O	SDVDD	14	F4

Table 3. MCF5372/3 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	Voltage Domain	MCF5372 MCF5373 160 QFP	MCF5372L MCF53721 MCF5373L 196 MAPBGA
SD_CLK	—	—	—	O	SDVDD	37	L1
$\overline{\text{SD\_CLK}}$	—	—	—	O	SDVDD	38	M1
$\overline{\text{SD\_CS0}}$	—	—	—	O	SDVDD	15	F3
SD_DQS3	—	—	—	O	SDVDD	25	H1
SD_DQS2	—	—	—	O	SDVDD	55	N5
$\overline{\text{SD\_SCAS}}$	—	—	—	O	SDVDD	44	M3
$\overline{\text{SD\_SRAS}}$	—	—	—	O	SDVDD	45	M4
SD_SDR_DQS	—	—	—	O	SDVDD	35	L2
$\overline{\text{SD\_WE}}$	—	—	—	O	SDVDD	13	E1
External Interrupts Port[5]							
$\overline{\text{IRQ7}}$[2]	PIRQ7[2]	—	—	I	EVDD	102	F13
$\overline{\text{IRQ6}}$[2]	PIRQ6[2]	USBHOST_ VBUS_EN	—	I	EVDD	—	F12
$\overline{\text{IRQ5}}$[2]	PIRQ5[2]	USBHOST_ VBUS_OC	—	I	EVDD	—	F11
$\overline{\text{IRQ4}}$[2]	PIRQ4[2]	SSI_MCLK	—	I	EVDD	101	G14
$\overline{\text{IRQ3}}$[2]	PIRQ3[2]	—	—	I	EVDD	—	G13
$\overline{\text{IRQ2}}$[2]	PIRQ2[2]	USB_CLKIN	—	I	EVDD	—	G12
$\overline{\text{IRQ1}}$[2]	PIRQ1[2]	$\overline{\text{DREQ1}}$[2]	SSI_CLKIN	I	EVDD	100	G11
FEC							
FEC_MDC	PFECI2C3	I2C_SCL[2]	—	O	EVDD	4	B1
FEC_MDIO	PFECI2C2	I2C_SDA[2]	—	I/O	EVDD	3	A1
FEC_COL	PFECH7	—	—	I	EVDD	144	B6
FEC_CRS	PFECH6	—	—	I	EVDD	145	A6
FEC_RXCLK	PFECH5	—	—	I	EVDD	146	A5
FEC_RXDV	PFECH4	—	—	I	EVDD	147	B5
FEC_RXD[3:0]	PFECH[3:0]	—	—	I	EVDD	148–151	C5, D5, A4, B4
FEC_RXER	PFECL7	—	—	I	EVDD	152	C4
FEC_TXCLK	PFECL6	—	—	I	EVDD	153	A3
FEC_TXEN	PFECL5	—	—	O	EVDD	154	B3
FEC_TXER	PFECL4	—	—	O	EVDD	155	A2
FEC_TXD[3:0]	PFECL[3:0]	—	—	O	EVDD	157, 158, 1, 2	D4, C3, B2, C2

Table 3. MCF5372/3 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	Voltage Domain	MCF5372 MCF5373 160 QFP	MCF5372L MCF53721 MCF5373L 196 MAPBGA
USB Host & USB On-the-Go							
USBOTG_M	—	—	—	I/O	USB VDD	—	H14
USBOTG_P	—	—	—	I/O	USB VDD	—	H13
USBHOST_M	—	—	—	I/O	USB VDD	—	J13
USBHOST_P	—	—	—	I/O	USB VDD	—	J12
FlexCAN (MCF53721 only)							
CANRX and CANTX do not have dedicated bond pads. Please refer to the following pins for muxing: I2C_SDA for CANRX and I2C_SCL for CANTX.							
PWM							
PWM7	PPWM7	—	—	I/O	EVDD	—	E13
PWM5	PPWM5	—	—	I/O	EVDD	—	E12
PWM3	PPWM3	DT3OUT	DT3IN	I/O	EVDD	—	E11
PWM1	PPWM1	DT2OUT	DT2IN	I/O	EVDD	—	F14
SSI							
The SSI signals do not have dedicated bond pads. Please refer to the following pins for muxing: $\overline{\text{IRQ4}}$ for SSI_MCLK, $\overline{\text{IRQ1}}$ for SSI_CLKIN, $\overline{\text{U1CTS}}$ for SSI_BCLK, $\overline{\text{U1RTS}}$ for SSI_FS, U1RXD for SSI_RXD, and U1TXD for SSI_TXD							
I²C							
I2C_SCL[2]	PFECI2C1	CANTX[6]	U2TXD	I/O	EVDD	—	E3
I2C_SDA[2]	PFECI2C0	CANRX[6]	U2RXD	I/O	EVDD	—	E4
DMA							
$\overline{\text{DACK}}$[1:0] and $\overline{\text{DREQ}}$[1:0] do not have dedicated bond pads. Please refer to the following pins for muxing: $\overline{\text{TS}}$ for $\overline{\text{DACK0}}$, DT0IN for $\overline{\text{DREQ0}}$, DT1IN for $\overline{\text{DACK1}}$, and $\overline{\text{IRQ1}}$ for $\overline{\text{DREQ1}}$.							
QSPI							
QSPI_CS2	PQSPI5	$\overline{\text{U2RTS}}$	—	O	EVDD	78	N12
QSPI_CS1	PQSPI4	PWM7	USBOTG_PU_EN	O	EVDD	—	M12
QSPI_CS0	PQSPI3	PWM5	—	O	EVDD	—	M11
QSPI_CLK	PQSPI2	I2C_SCL[2]	—	O	EVDD	77	P12
QSPI_DIN	PQSPI1	$\overline{\text{U2CTS}}$	—	I	EVDD	75	P11
QSPI_DOUT	PQSPI0	I2C_SDA[2]	—	O	EVDD	76	N11

Table 3. MCF5372/3 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	Voltage Domain	MCF5372 MCF5373 160 QFP	MCF5372L MCF53721 MCF5373L 196 MAPBGA
UARTs							
$\overline{\text{U1CTS}}$	PUARTL7	SSI_BCLK	—	I	EVDD	143	C6
$\overline{\text{U1RTS}}$	PUARTL6	SSI_FS	—	O	EVDD	142	D6
U1TXD	PUARTL5	SSI_TXD[2]	—	O	EVDD	141	A7
U1RXD	PUARTL4	SSI_RXD[2]	—	I	EVDD	140	B7
$\overline{\text{U0CTS}}$	PUARTL3	—	—	I	EVDD	85	M14
$\overline{\text{U0RTS}}$	PUARTL2	—	—	O	EVDD	84	M13
U0TXD	PUARTL1	—	—	O	EVDD	83	N14
U0RXD	PUARTL0	—	—	I	EVDD	80	P14
Note: The UART2 signals are multiplexed on the QSPI, DMA Timers, and I2C pins.							
DMA Timers							
DT3IN	PTIMER3	DT3OUT	U2RXD	I	EVDD	8	D1
DT2IN	PTIMER2	DT2OUT	U2TXD	I	EVDD	7	C1
DT1IN	PTIMER1	DT1OUT	$\overline{\text{DACK1}}$	I	EVDD	6	D2
DT0IN	PTIMER0	DT0OUT	$\overline{\text{DREQ0}}$[2]	I	EVDD	5	D3
BDM/JTAG[7]							
JTAG_EN[8]	—	—	—	I	EVDD	96	G10
DSCLK	—	$\overline{\text{TRST}}$[2]	—	I	EVDD	88	K11
PSTCLK	—	TCLK[2]	—	O	EVDD	70	N8
$\overline{\text{BKPT}}$	—	TMS[2]	—	I	EVDD	87	L13
DSI	—	TDI[2]	—	I	EVDD	90	K12
DSO	—	TDO	—	O	EVDD	74	L11
DDATA[3:0]	—	—	—	O	EVDD	—	L9, M9, N9, P9
PST[3:0]	—	—	—	O	EVDD	—	L10, M10, N10, P10
ALLPST	—	—	—	O	EVDD	73	—

Table 3. MCF5372/3 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	Voltage Domain	MCF5372 MCF5373 160 QFP	MCF5372L MCF53721 MCF5373L 196 MAPBGA
Test							
TEST[8]	—	—	—	I	EVDD	124	E10
Power Supplies							
EVDD	—	—	—	—	—	9, 69, 71, 81, 94, 103, 139, 160	E6, E7, F5–F7, G5, H10, J8, K8–K9
IVDD	—	—	—	—	—	36, 79, 97, 125, 156	E5, J9, K5, K10
PLL_VDD	—	—	—	—	—	99	J10
SD_VDD	—	—	—	—	—	11, 39, 41, 67, 105, 121, 137	E8–E9, F8–F10, J4–J7, H5, K6, K7
USB_VDD	—	—	—	—	—	—	H12
VSS	—	—	—	—	—	10, 42, 68, 82, 89, 104, 122, 138, 159	G6–G9, H6–H9
PLL_VSS	—	—	—	—	—	98	H11
USB_VSS	—	—	—	—	—	—	J14

1 Refers to pin's primary function.

2 Pull-up enabled internally on this signal for this mode.

3 The SDRAM functions of these signals are not programmable by the user. They are dynamically switched by the processor when accessing SDRAM memory space and are included here for completeness.

4 Primary functionality selected by asserting the DRAMSEL signal (SDR mode). Alternate functionality selected by negating the DRAMSEL signal (DDR mode). The GPIO module is not responsible for assigning these pins.

5 GPIO functionality is determined by the edge port module. The GPIO module is only responsible for assigning the alternate functions.

6 MCF53721 only.

7 If JTAG_EN is asserted, these pins default to Alternate 1 (JTAG) functionality. The GPIO module is not responsible for assigning these pins.

8 Pull-down enabled internally on this signal for this mode.

NOTE

4.2 Pinout—196 MAPBGA

The pinout for the MCF5373LCVM240, MCF5372LCVM240, and MCF53721CVM240 packages are shown below.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	FEC_ MDIO	FEC_ TXER	FEC_ TXCLK	FEC_ RXD1	FEC_ RXCLK	FEC_ CRS	U1TXD	FB_CS2	A23	A19	A15	A12	A10	A9	A
B	FEC_ MDC	FEC_ TXD1	FEC_ TXEN	FEC_ RXD0	FEC_ RXDV	FEC_ COL	U1RXD	FB_CS3	A22/	A18	A14	A11	A7	A8	B
C	DT2IN	FEC_ TXD0	FEC_ TXD2	FEC_ RXER	FEC_ RXD3	U1CTS	FB_CS0	FB_CS4	A21	A17	A13	A6	A3	A4	C
D	DT3IN	DT1IN	DT0IN	FEC_ TXD3	FEC_ RXD2	U1RTS	FB_CS1	FB_CS5	A20	A16	A5	A0	A1	A2	D
E	SD_WE	TS	I2C_SCL	I2C_SDA	IVDD	EVDD	EVDD	SD_VDD	SD_VDD	TEST	PWM3	PWM5	PWM7	TA	E
F	D14	D15	SD_CS0	SD_CKE	EVDD	EVDD	EVDD	SD_VDD	SD_VDD	SD_VDD	IRQ5	IRQ6	IRQ7	PWM1	F
G	D10	D11	D12	D13	EVDD	VSS	VSS	VSS	VSS	JTAG_ EN	IRQ1	IRQ2	IRQ3	IRQ4	G
H	SD_ DQS3	BE/ BWE1	D8	D9	SD_VDD	VSS	VSS	VSS	VSS	EVDD	PLL_ VSS	USBOTG _VDD	USB OTG_P	USB OTG_M	H
J	D30	D31	BE/ BWE3	SD_VDD	SD_VDD	SD_VDD	SD_VDD	EVDD	IVDD	PLL_ VDD	DRAM SEL	USB HOST_P	USB HOST_M	USBHOST _VSS	J
K	D26	D27	D28	D29	IVDD	SD_VDD	SD_VDD	EVDD	EVDD	IVDD	TRST/ DSCLK	TDI/DSI	RESET	XTAL	K
L	SD_CLK	SD_DR_ DQS	D24	D25	D19	D7	D3	R/W	DDATA3	PST3	TDO/ DSO	RSTOUT	TMS/ BKPT	EXTAL	L
M	SD_CLK	SD_A10	SD_CAS	SD_RAS	BE/ BWE2	D6	D2	OE	DDATA2	PST2	QSPI_ CS0	QSPI_ CS1	U0RTS	U0CTS	M
N	FB_CLK	D23	D20	D17	SD_ DQS2	D5	D1	TCLK/ PSTCLK	DDATA1	PST1	QSPI_ DOUT	QSPI_ CS2	XTAL 32K	U0TXD	N
P	D22	D21	D18	D16	BE/ BWE0	D4	D0	RCON	DDATA0	PST0	QSPI_ DIN	QSPI_ CLK	EXTAL 32K	U0RXD	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Figure 4. MCF5373LCVM240, MCF5372LCVM240, and MCF53721CVM240 Pinout Top View (196 MAPBGA)

4.3 Pinout—160 QFP

The pinout for the MCF5372CAB180 and MCF5373CAB180 packages is shown below.

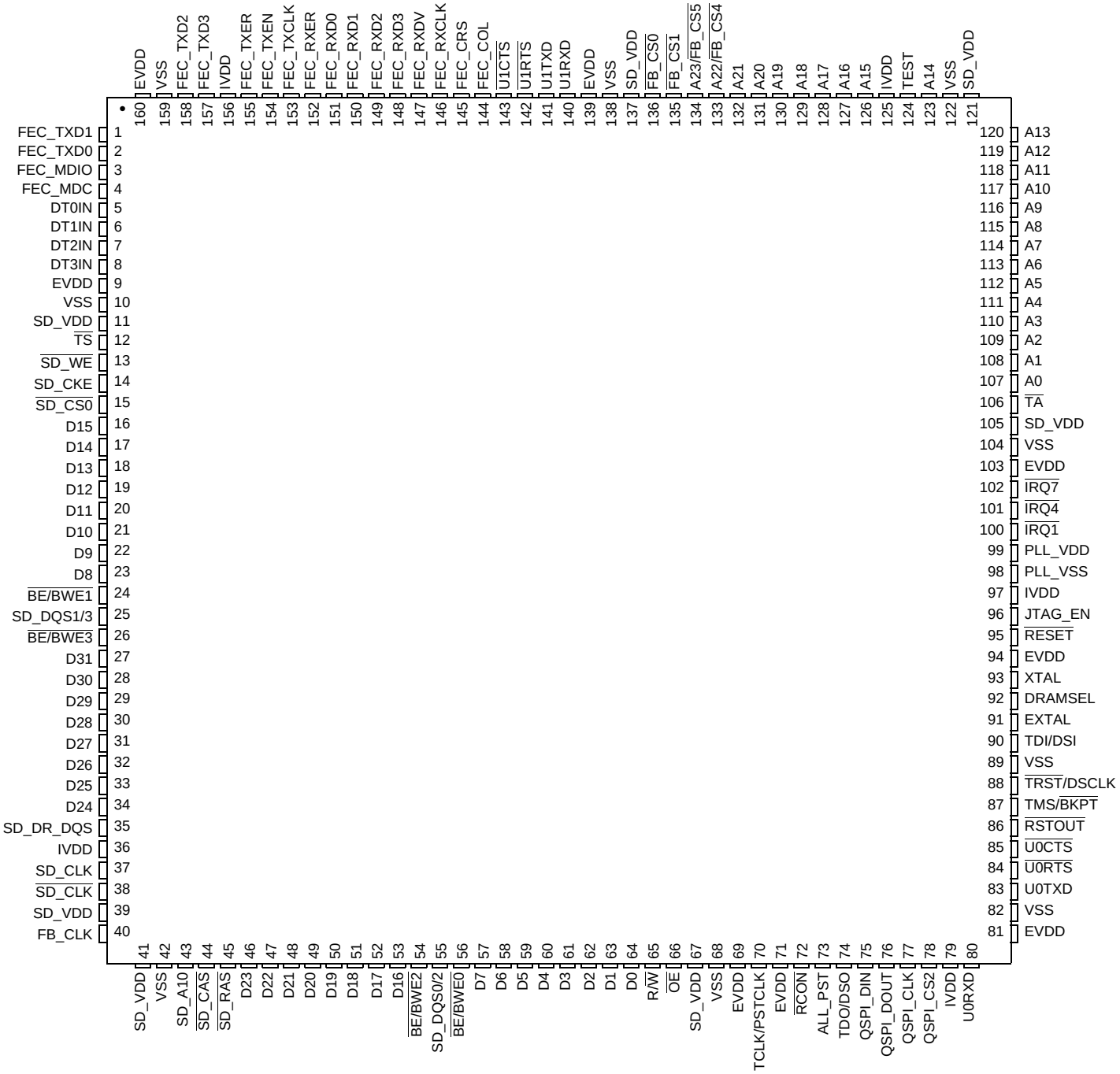


Figure 5. MCF5372CAB180 and MCF5373CAB180 Pinout Top View (160 QFP)

5 Electrical Characteristics

This document contains electrical specification tables and reference timing diagrams for the MCF5373 microcontroller unit. This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications of MCF5373.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. However, for production silicon, these specifications will be met. Finalized specifications will be published after complete characterization and device qualifications have been completed.

NOTE

The parameters specified in this MCU document supersede any values found in the module specifications.

5.1 Maximum Ratings

Table 4. Absolute Maximum Ratings[1, 2]

Rating	Symbol	Value	Unit
Core Supply Voltage	IV_{DD}	– 0.5 to +2.0	V
CMOS Pad Supply Voltage	EV_{DD}	– 0.3 to +4.0	V
DDR/Memory Pad Supply Voltage	SDV_{DD}	– 0.3 to +4.0	V
PLL Supply Voltage	$PLLV_{DD}$	– 0.3 to +2.0	V
Digital Input Voltage [3]	V_{IN}	– 0.3 to +3.6	V
Instantaneous Maximum Current Single pin limit (applies to all pins) [3, 4, 5]	I_D	25	mA
Operating Temperature Range (Packaged)	T_A (T_L - T_H)	– 40 to +85	°C
Storage Temperature Range	T_{stg}	– 55 to +150	°C

1 Functional operating conditions are given in Section 5.4, “DC Electrical Specifications.” Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Continued operation at these levels may affect device reliability or cause permanent damage to the device.

2 This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (V_{SS} or EV_{DD}).

3 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, and then use the larger of the two values.

4 All functional non-supply pins are internally clamped to V_{SS} and EV_{DD}.

5 Power supply must maintain regulation within operating EV_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > EV_{DD}$) is greater than I_{DD}, the injection current may flow out of EV_{DD} and could result in external power supply going out of regulation. Ensure external EV_{DD} load shunts current greater than maximum injection current. This is the greatest risk when the MCU is not consuming power (ex; no clock). Power supply must maintain regulation within operating EV_{DD} range during instantaneous and operating maximum current conditions.

5.2 Thermal Characteristics

Table 5. Thermal Characteristics

Characteristic		Symbol	256MBGA	196MBGA	160QFP	Unit
Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JMA}	37[1,2]	42[1,2]	49[1,2]	°C/W
Junction to ambient (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	34[1,2]	38[1,2]	44[1,2]	°C/W
Junction to board		θ_{JB}	27[3]	32[3]	40[3]	°C/W
Junction to case		θ_{JC}	16[4]	19[4]	39[4]	°C/W
Junction to top of package		Ψ_{jt}	4[1,5]	5[1,5]	12[1,5]	°C/W
Maximum operating junction temperature		T_j	105	105	105	°C

1. θ_{JMA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of θ_{JmA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.
2. Per JEDEC JESD51-6 with the board horizontal.
3. Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
5. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JMA}) \quad \textit{Eqn. 1}$$

Where:

T_A = Ambient Temperature, °C
Q_{JMA} = Package Thermal Resistance, Junction-to-Ambient, °C/W
P_D = P_{INT} + $P_{I/O}$
P_{INT} = I_{DD} × IV_{DD}, Watts – Chip Internal Power
$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be ignored. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = \frac{K}{(T_J + 273°C)} \quad \textit{Eqn. 2}$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A \times 273°C) + Q_{JMA} \times P_D^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

5.3 ESD Protection

Table 6. ESD Protection Characteristics[1, 2]

Characteristics	Symbol	Value	Units
ESD Target for Human Body Model	HBM	2000	V

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing is performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

5.4 DC Electrical Specifications

Table 7. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Unit
Core Supply Voltage	IV_{DD}	1.4	1.6	V
PLL Supply Voltage	$PLLV_{DD}$	1.4	1.6	V
CMOS Pad Supply Voltage	EV_{DD}	3.0	3.6	V
SDRAM and FlexBus Supply Voltage Mobile DDR/Bus Pad Supply Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V)	SDV_{DD}	 1.70 2.25 3.0	 1.95 2.75 3.6	V
USB Supply Voltage	$USBV_{DD}$	3.0	3.6	V
CMOS Input High Voltage	EV_{IH}	2	EV_{DD} + 0.3	V
CMOS Input Low Voltage	EV_{IL}	V_{SS} – 0.3	0.8	V
CMOS Output High Voltage I_{OH} = –5.0 mA	EV_{OH}	EV_{DD} _ 0.4	—	V
CMOS Output Low Voltage I_{OL} = 5.0 mA	EV_{OL}	—	0.4	V
SDRAM and FlexBus Input High Voltage Mobile DDR/Bus Input High Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V)	SDV_{IH}	 1.35 1.7 2	 SDV_{DD} + 0.3 SDV_{DD} + 0.3 SDV_{DD} + 0.3	V
SDRAM and FlexBus Input Low Voltage Mobile DDR/Bus Input High Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V)	SDV_{IL}	 V_{SS} – 0.3 V_{SS} – 0.3 V_{SS} – 0.3	 0.45 0.8 0.8	V
SDRAM and FlexBus Output High Voltage Mobile DDR/Bus Input High Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V) I_{OH} = –5.0 mA for all modes	SDV_{OH}	 SDV_{DD} – 0.35 2.1 2.4	 — — —	V

Table 7. DC Electrical Specifications (continued)

Characteristic	Symbol	Min	Max	Unit
SDRAM and FlexBus Output Low Voltage Mobile DDR/Bus Input High Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V) I_{OL} = 5.0 mA for all modes	SDV_{OL}	 — — —	 0.3 0.3 0.5	V
Input Leakage Current V_{in} = V_{DD} or V_{SS}, Input-only pins	I_{in}	–1.0	1.0	µA
Weak Internal Pull-Up Device Current, tested at V_{IL} Max.[1]	I_{APU}	–10	–130	µA
Input Capacitance [2] All input-only pins All input/output (three-state) pins	C_{in}	 — —	 7 7	pF

1 Refer to the signals section for pins having weak internal pull-up devices.
2 This parameter is characterized before qualification rather than 100% tested.

5.5 Oscillator and PLL Electrical Characteristics

Table 8. PLL Electrical Characteristics

Num	Characteristic	Symbol	Min. Value	Max. Value	Unit
1	PLL Reference Frequency Range Crystal reference External reference	 $f_{ref\_crystal}$ f_{ref_ext}	 12 12	 25[1] 40[1]	 MHz MHz
2	Core frequency CLKOUT Frequency[2]	f_{sys} $f_{sys/3}$	488 x 10^{-6} 163 x 10^{-6}	240 80	MHz MHz
3	Crystal Start-up Time[3, 4]	t_{cst}	—	10	ms
4	EXTAL Input High Voltage Crystal Mode[5] All other modes (External, Limp)	 V_{IHEXT} V_{IHEXT}	 V_{XTAL} + 0.4 E_{VDD}/2 + 0.4	 — —	 V V
5	EXTAL Input Low Voltage Crystal Mode[5] All other modes (External, Limp)	 V_{ILEXT} V_{ILEXT}	 — —	 V_{XTAL} – 0.4 E_{VDD}/2 – 0.4	 V V
7	PLL Lock Time [3, 6]	t_{lpll}	—	50000	CLKIN
8	Duty Cycle of reference [3]	t_{dc}	40	60	%
9	XTAL Current	I_{XTAL}	1	3	mA
10	Total on-chip stray capacitance on XTAL	C_{S_XTAL}		1.5	pF
11	Total on-chip stray capacitance on EXTAL	C_{S_EXTAL}		1.5	pF
12	Crystal capacitive load	C_L		See crystal spec	
13	Discrete load capacitance for XTAL	C_{L_XTAL}		2*C_L – C_{S_XTAL} – C_{PCB_XTAL}[7]	pF

Table 8. PLL Electrical Characteristics (continued)

Num	Characteristic	Symbol	Min. Value	Max. Value	Unit
14	Discrete load capacitance for EXTAL	C_{L_EXTAL}		$2*C_L - C_{S\_EXTAL} - C_{PCB\_EXTAL}$ [7]	pF
17	CLKOUT Period Jitter, [3, 4, 7, 8, 9] Measured at f_{SYS} Max Peak-to-peak Jitter (Clock edge to clock edge) Long Term Jitter	C_{jitter}	 — —	 10 TBD	 % $f_{sys/3}$ % $f_{sys/3}$
18	Frequency Modulation Range Limit [3, 10, 11] (f_{sys}Max must not be exceeded)	C_{mod}	0.8	2.2	%$f_{sys/3}$
19	VCO Frequency. $f_{vco} = (f_{ref} * PFD)/4$	f_{vco}	350	540	MHz

1 The maximum allowable input clock frequency when booting with the PLL enabled is 24MHz. For higher input clock frequencies the processor must boot in LIMP mode to avoid violating the maximum allowable CPU frequency.

2 All internal registers retain data at 0 Hz.

3 This parameter is guaranteed by characterization before qualification rather than 100% tested.

4 Proper PC board layout procedures must be followed to achieve specifications.

5 This parameter is guaranteed by design rather than 100% tested.

6 This specification is the PLL lock time only and does not include oscillator start-up time.

7 C_{PCB_EXTAL} and C_{PCB_XTAL} are the measured PCB stray capacitances on EXTAL and XTAL, respectively.

8 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{sys}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via PLL V_{DD}, EV_{DD}, and V_{SS} and variation in crystal oscillator frequency increase the Cjitter percentage for a given interval.

9 Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of Cjitter+Cmod.

10 Modulation percentage applies over an interval of 10 μs, or equivalently the modulation rate is 100 KHz.

11 Modulation range determined by hardware design.

5.6 External Interface Timing Characteristics

Table 9 lists processor bus input timings.

NOTE

All processor bus timings are synchronous; that is, input setup/hold and output delay with respect to the rising edge of a reference clock. The reference clock is the FB_CLK output.

All other timing relationships can be derived from these values. Timings listed in Table 9 are shown in Figure 7 and Figure 8.

* The timings are also valid for inputs sampled on the negative clock edge.

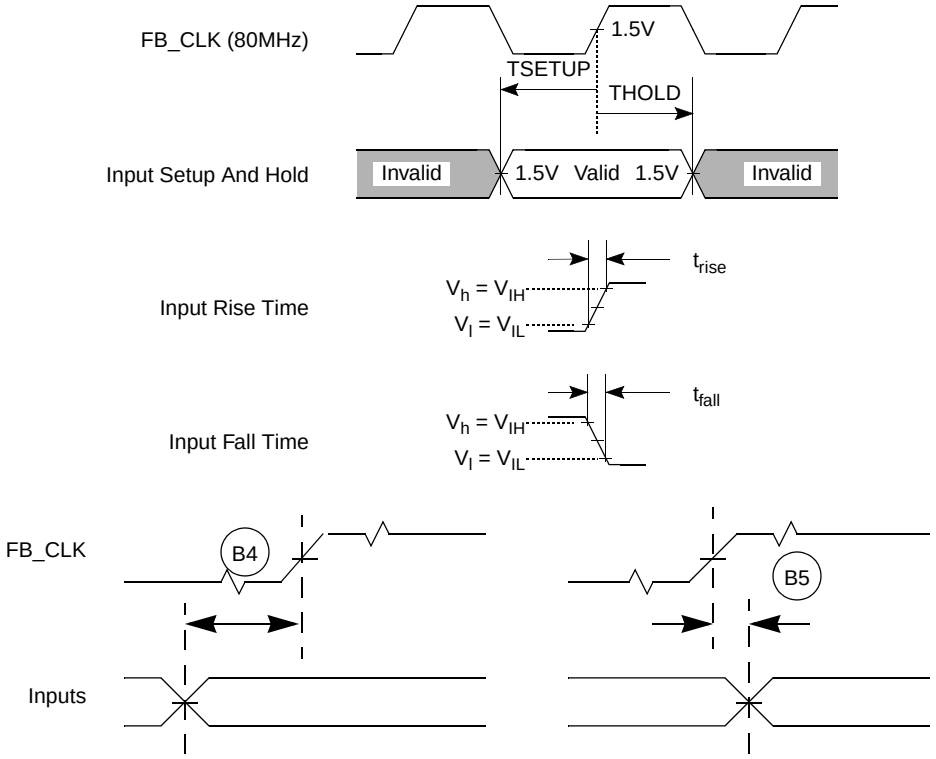


Figure 6. General Input Timing Requirements

5.6.1 FlexBus

A multi-function external bus interface called FlexBus is provided with basic functionality to interface to slave-only devices up to a maximum bus frequency of 80MHz. It can be directly connected to asynchronous or synchronous devices such as external boot ROMs, flash memories, gate-array logic, or other simple target (slave) devices with little or no additional circuitry. For asynchronous devices a simple chip-select based interface can be used. The FlexBus interface has six general purpose chip-selects ($\overline{FB\_CS}$[5:0]) which can be configured to be distributed between the FlexBus or SDRAM memory interfaces. Chip-select, $\overline{FB\_CS0}$ can be dedicated to boot ROM access and can be programmed to be byte (8 bits), word (16 bits), or longword (32 bits) wide. Control signal timing is compatible with common ROM/flash memories.

5.6.1.1 FlexBus AC Timing Characteristics

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the system clock.

Table 9. FlexBus AC Timing Specifications

Num	Characteristic	Symbol	Min	Max	Unit
—	Frequency of Operation	$f_{sys/3}$	—	80	Mhz
FB1	Clock Period (FB_CLK)	t_{FBCK} (t_{cyc})	12.5	—	ns
FB2	Address, Data, and Control Output Valid (A[23:0], D[31:0], $\overline{FB\_CS}$[5:0], R/$\overline{W}$, $\overline{TS}$, $\overline{BE/BWE}$[3:0] and $\overline{OE}$)[1]	$t_{FBCHDCV}$	—	7.0	ns
FB3	Address, Data, and Control Output Hold (A[23:0], D[31:0], $\overline{FB\_CS}$[5:0], R/$\overline{W}$, $\overline{TS}$, $\overline{BE/BWE}$[3:0], and $\overline{OE}$)[1, 2]	$t_{FBCHDCI}$	1	—	ns

Table 9. FlexBus AC Timing Specifications (continued)

Num	Characteristic	Symbol	Min	Max	Unit
FB4	Data Input Setup	t_{DVFBCH}	3.5	—	ns
FB5	Data Input Hold	t_{DIFBCH}	0	—	ns
FB6	Transfer Acknowledge ($\overline{TA}$) Input Setup	t_{CVFBCH}	4	—	ns
FB7	Transfer Acknowledge ($\overline{TA}$) Input Hold	t_{CIFBCH}	0	—	ns

1 Timing for chip selects only applies to the $\overline{FB\_CS}$[5:0] signals. Please see Section 5.7.2, "DDR SDRAM AC Timing Characteristics" for SD_CS[3:0] timing.

2 The FlexBus supports programming an extension of the address hold. Please consult the *Reference Manual* for more information.

NOTE

The processor drives the data lines during the first clock cycle of the transfer with the full 32-bit address. This may be ignored by standard connected devices using non-multiplexed address and data buses. However, some applications may find this feature beneficial.

The address and data busses are muxed between the FlexBus and SDRAM controller. At the end of the read and write bus cycles the address signals are indeterminate.

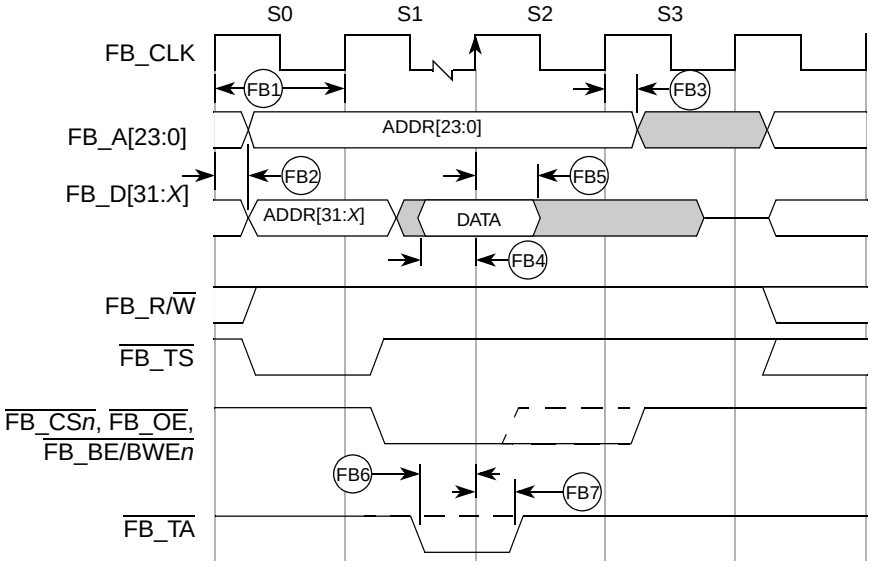


Figure 7. FlexBus Read Timing

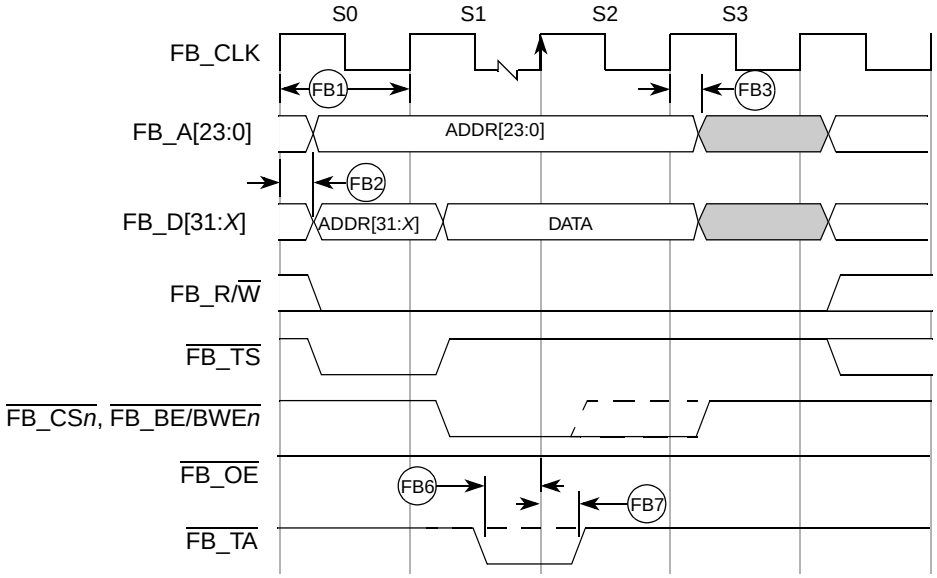


Figure 8. FlexBus Write Timing

5.7 SDRAM Bus

The SDRAM controller supports accesses to main SDRAM memory from any internal master. It supports standard SDRAM or double data rate (DDR) SDRAM, but it does not support both at the same time.

5.7.1 SDR SDRAM AC Timing Characteristics

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the memory bus clock, when operating in SDR mode on write cycles and relative to SD_DQS on read cycles. The device's SDRAM controller is a DDR controller that has an SDR mode. Because it is designed to support DDR, a DQS pulse must remain supplied to the device for each data beat of an SDR read. The processor accomplishes this by asserting a signal named SD_SDR_DQS during read cycles. Care must be taken during board design to adhere to the following guidelines and specs with regard to the SD_SDR_DQS signal and its usage.

Table 10. SDR Timing Specifications

Symbol	Characteristic	Symbol	Min	Max	Unit
•	Frequency of Operation[1]	•	60	80	MHz
SD1	Clock Period[2]	t_{SDCK}	12.5	16.67	ns
SD3	Pulse Width High[3]	t_{SDCKH}	0.45	0.55	SD_CLK
SD4	Pulse Width Low[4]	t_{SDCKH}	0.45	0.55	SD_CLK
SD5	Address, SD_CKE, $\overline{\text{SD\_CAS}}$, $\overline{\text{SD\_RAS}}$, $\overline{\text{SD\_WE}}$, SD_BA, SD_CS[1:0] - Output Valid	$t_{SDCHACV}$	—	0.5 × SD_CLK + 1.0	ns
SD6	Address, SD_CKE, $\overline{\text{SD\_CAS}}$, $\overline{\text{SD\_RAS}}$, $\overline{\text{SD\_WE}}$, SD_BA, SD_CS[1:0] - Output Hold	$t_{SDCHACI}$	2.0	—	ns
SD7	SD_SDR_DQS Output Valid[5]	t_{DQSOV}	—	Self timed	ns
SD8	SD_DQS[3:0] input setup relative to SD_CLK[6]	$t_{DQVSDCH}$	0.25 × SD_CLK	0.40 × SD_CLK	ns

Table 10. SDR Timing Specifications (continued)

Symbol	Characteristic	Symbol	Min	Max	Unit
SD9	SD_DQS[3:2] input hold relative to SD_CLK[7]	$t_{DQISDCH}$	Does not apply. 0.5×SD_CLK fixed width.		
SD10	Data (D[31:0]) Input Setup relative to SD_CLK (reference only)[8]	t_{DVSDCH}	0.25 × SD_CLK	—	ns
SD11	Data Input Hold relative to SD_CLK (reference only)	t_{DISDCH}	1.0	—	ns
SD12	Data (D[31:0]) and Data Mask(SD_DQM[3:0]) Output Valid	$t_{SDCHDMV}$	—	0.75 × SD_CLK + 0.5	ns
SD13	Data (D[31:0]) and Data Mask (SD_DQM[3:0]) Output Hold	$t_{SDCHDMI}$	1.5	—	ns

1 The FlexBus and SDRAM clock operates at the same frequency of the internal bus clock. See the PLL chapter of the *MCF5373 Reference Manual* for more information on setting the SDRAM clock rate.

2 SD_CLK is one SDRAM clock in (ns).

3 Pulse width high plus pulse width low cannot exceed min and max clock period.

4 Pulse width high plus pulse width low cannot exceed min and max clock period.

5 SD_DQS is designed to pulse 0.25 clock before the rising edge of the memory clock. This is a guideline only. Subtle variation from this guideline is expected. SD_DQS only pulses during a read cycle and one pulse occurs for each data beat.

6 SDR_DQS is designed to pulse 0.25 clock before the rising edge of the memory clock. This spec is a guideline only. Subtle variation from this guideline is expected. SDR_DQS only pulses during a read cycle and one pulse occurs for each data beat.

7 The SDR_DQS pulse is designed to be 0.5 clock in width. The timing of the rising edge is most important. The falling edge does not affect the memory controller.

8 Because a read cycle in SDR mode uses the DQS circuit within the device, it is most critical that the data valid window be centered 1/4 clk after the rising edge of DQS. Ensuring that this happens results in successful SDR reads. The input setup spec is provided as guidance.

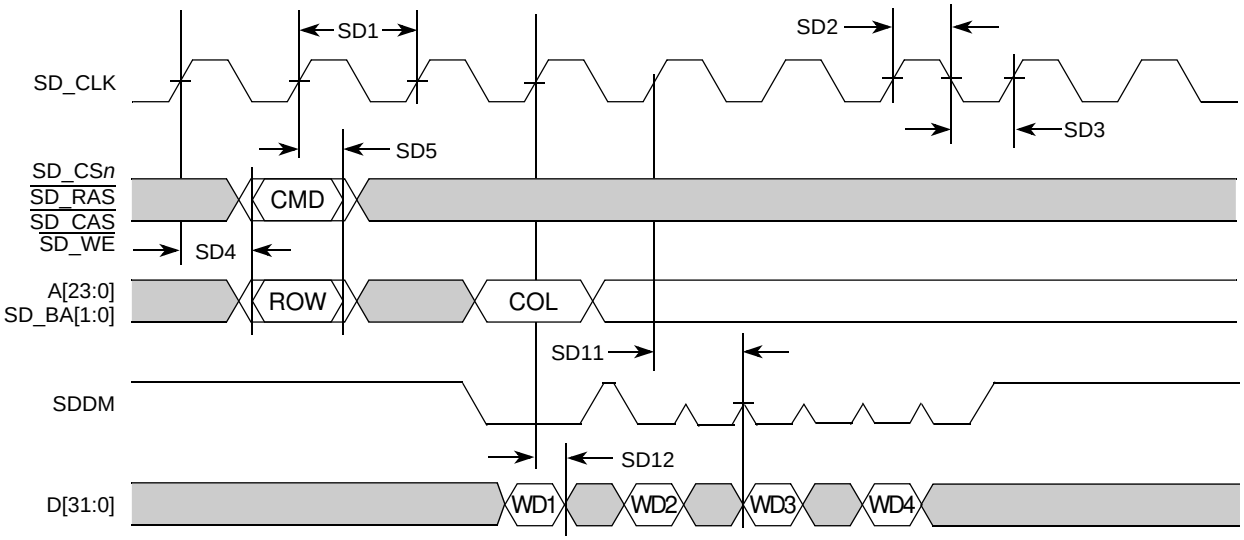


Figure 9. SDR Write Timing

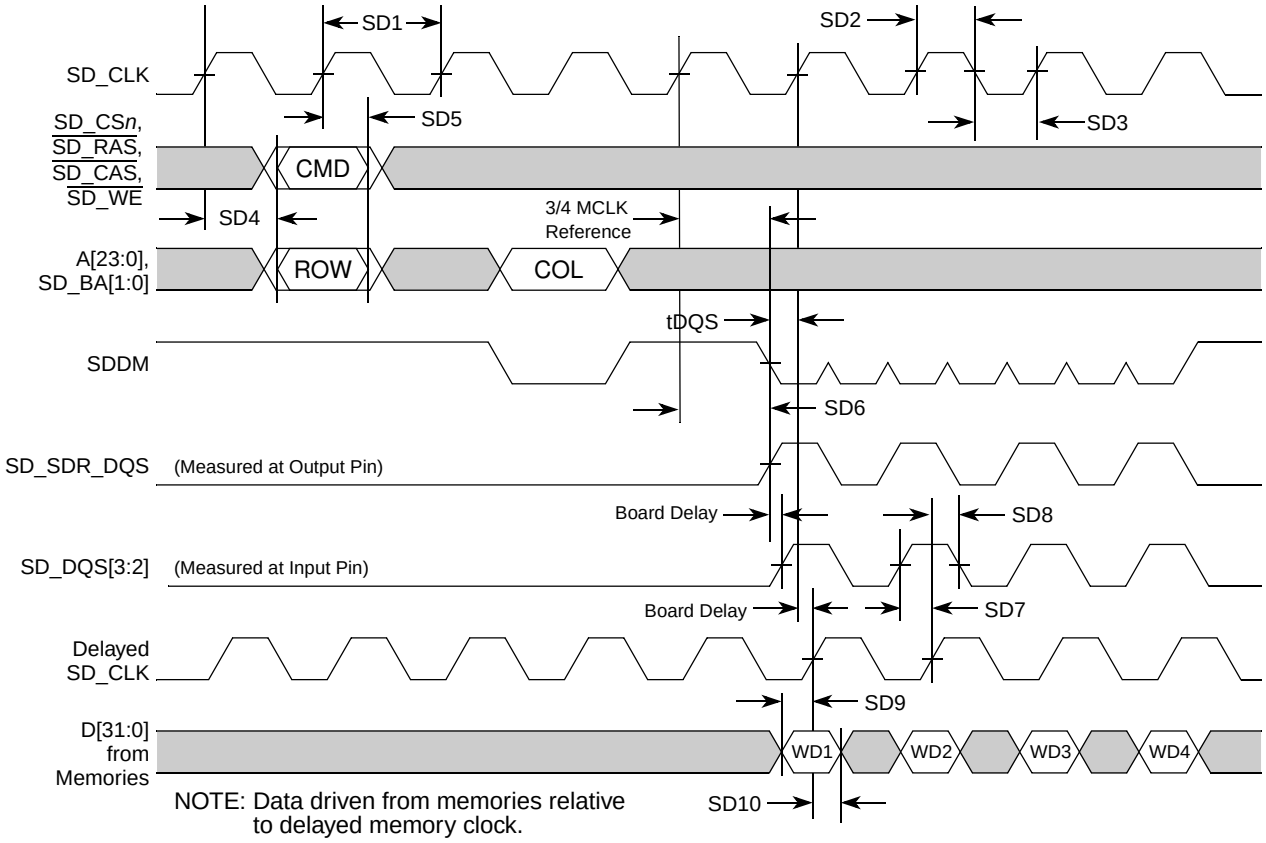


Figure 10. SDR Read Timing

5.7.2 DDR SDRAM AC Timing Characteristics

When using the SDRAM controller in DDR mode, the following timing numbers must be followed to properly latch or drive data onto the memory bus. All timing numbers are relative to the four DQS byte lanes.

Table 11. DDR Timing Specifications

Num	Characteristic	Symbol	Min	Max	Unit
•	Frequency of Operation	t_{DDCK}	60	80	Mhz
DD1	Clock Period[1]	t_{DDSK}	12.5	16.67	ns
DD2	Pulse Width High[2]	t_{DDCKH}	0.45	0.55	SD_CLK
DD3	Pulse Width Low[3]	t_{DDCKL}	0.45	0.55	SD_CLK
DD4	Address, SD_CKE, $\overline{\text{SD\_CAS}}$, $\overline{\text{SD\_RAS}}$, $\overline{\text{SD\_WE}}$, $\overline{\text{SD\_CS}}$[1:0] - Output Valid[3]	$t_{SDCHACV}$	—	0.5 × SD_CLK + 1.0	ns
DD5	Address, SD_CKE, $\overline{\text{SD\_CAS}}$, $\overline{\text{SD\_RAS}}$, $\overline{\text{SD\_WE}}$, $\overline{\text{SD\_CS}}$[1:0] - Output Hold	$t_{SDCHACI}$	2.0	—	ns
DD6	Write Command to first DQS Latching Transition	t_{CMDVDQ}	—	1.25	SD_CLK
DD7	Data and Data Mask Output Setup (DQ-->DQS) Relative to DQS (DDR Write Mode)[4, 5]	t_{DQDMV}	1.5	—	ns

Table 11. DDR Timing Specifications (continued)

Num	Characteristic	Symbol	Min	Max	Unit
DD8	Data and Data Mask Output Hold (DQS-->DQ) Relative to DQS (DDR Write Mode)[6]	t_{DQDMI}	1.0	—	ns
DD9	Input Data Skew Relative to DQS (Input Setup)[7]	t_{DVDQ}	—	1	ns
DD10	Input Data Hold Relative to DQS[8]	t_{DIDQ}	0.25 × SD_CLK + 0.5ns	—	ns
DD11	DQS falling edge from SDCLK rising (output hold time)	$t_{DQLSDCH}$	0.5	—	ns
DD12	DQS input read preamble width	t_{DQRPRE}	0.9	1.1	SD_CLK
DD13	DQS input read postamble width	t_{DQRPST}	0.4	0.6	SD_CLK
DD14	DQS output write preamble width	t_{DQWPRE}	0.25		SD_CLK
DD15	DQS output write postamble width	t_{DQWPST}	0.4	0.6	SD_CLK

1 SD_CLK is one SDRAM clock in (ns).

2 Pulse width high plus pulse width low cannot exceed min and max clock period.

3 Command output valid should be 1/2 the memory bus clock (SD_CLK) plus some minor adjustments for process, temperature, and voltage variations.

4 This specification relates to the required input setup time of today's DDR memories. The processor's output setup should be larger than the input setup of the DDR memories. If it is not larger, the input setup on the memory is in violation. MEM_DATA[31:24] is relative to MEM_DQS[3], MEM_DATA[23:16] is relative to MEM_DQS[2], MEM_DATA[15:8] is relative to MEM_DQS[1], and MEM_[7:0] is relative MEM_DQS[0].

5 The first data beat is valid before the first rising edge of DQS and after the DQS write preamble. The remaining data beats are valid for each subsequent DQS edge.

6 This specification relates to the required hold time of today's DDR memories. MEM_DATA[31:24] is relative to MEM_DQS[3], MEM_DATA[23:16] is relative to MEM_DQS[2], MEM_DATA[15:8] is relative to MEM_DQS[1], and MEM_[7:0] is relative MEM_DQS[0].

7 Data input skew is derived from each DQS clock edge. It begins with a DQS transition and ends when the last data line becomes valid. This input skew must include DDR memory output skew and system level board skew (due to routing or other factors).

8 Data input hold is derived from each DQS clock edge. It begins with a DQS transition and ends when the first data line becomes invalid.

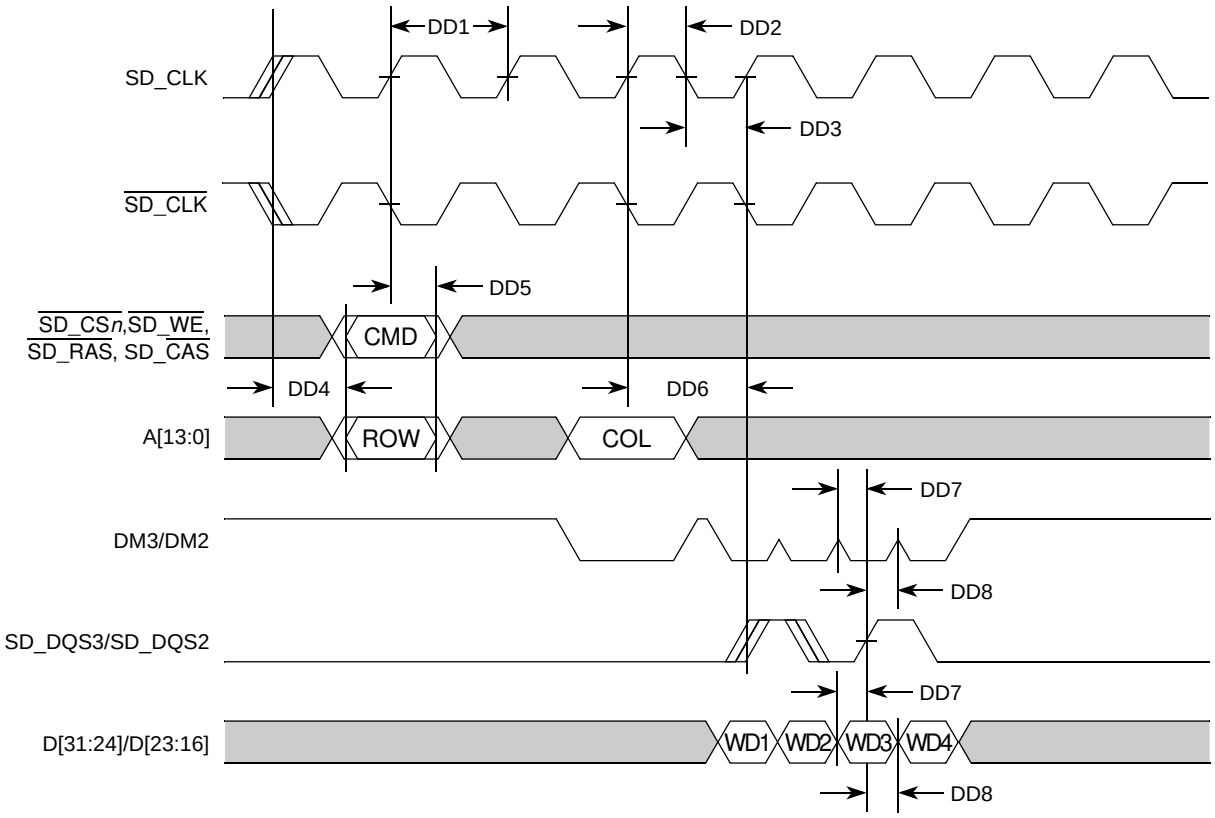


Figure 11. DDR Write Timing

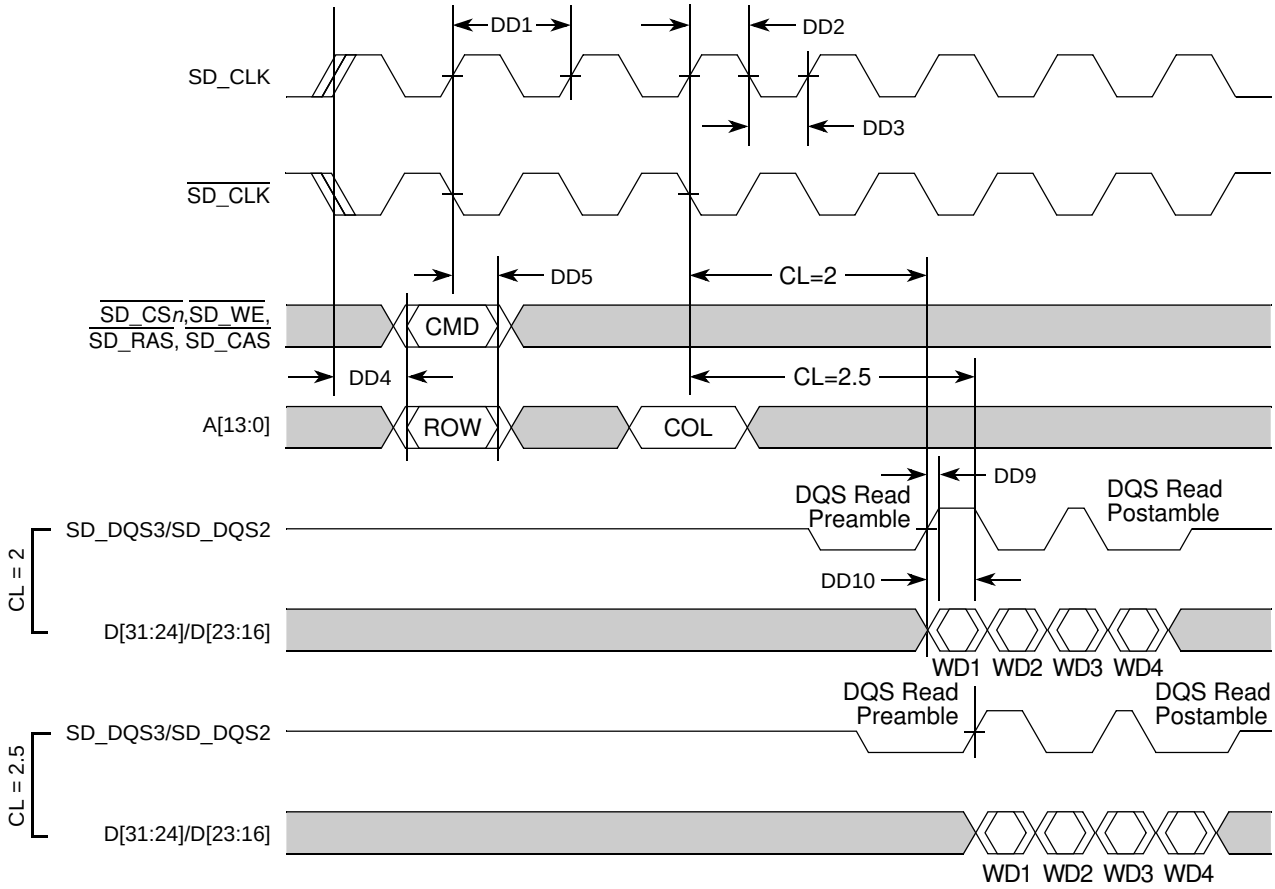


Figure 12. DDR Read Timing

5.8 General Purpose I/O Timing

Table 12. GPIO Timing[1]

Num	Characteristic	Symbol	Min	Max	Unit
G1	FB_CLK High to GPIO Output Valid	t_{CHPOV}	—	10	ns
G2	FB_CLK High to GPIO Output Invalid	t_{CHPOI}	1.5	—	ns
G3	GPIO Input Valid to FB_CLK High	t_{PVCH}	9	—	ns
G4	FB_CLK High to GPIO Input Invalid	t_{CHPI}	1.5	—	ns

1 GPIO pins include: $\overline{IRQn}$, PWM, UART, FlexCAN, and Timer pins.

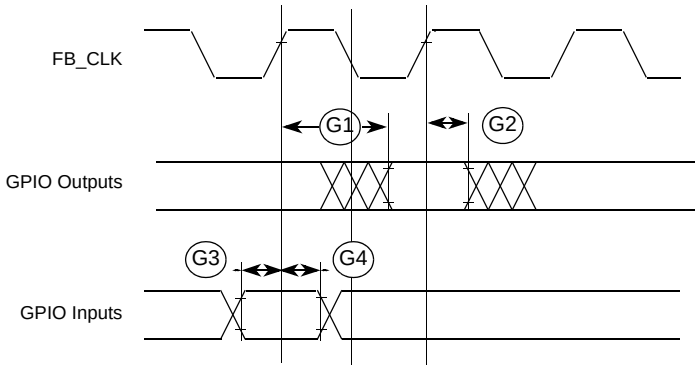


Figure 13. GPIO Timing

5.9 Reset and Configuration Override Timing

Table 13. Reset and Configuration Override Timing

Num	Characteristic	Symbol	Min	Max	Unit
R1	$\overline{\text{RESET}}$ Input valid to FB_CLK High	t_{RVCH}	9	—	ns
R2	FB_CLK High to $\overline{\text{RESET}}$ Input invalid	t_{CHRI}	1.5	—	ns
R3	$\overline{\text{RESET}}$ Input valid Time [1]	t_{RIVT}	5	—	t_{CYC}
R4	FB_CLK High to $\overline{\text{RSTOUT}}$ Valid	t_{CHROV}	—	10	ns
R5	$\overline{\text{RSTOUT}}$ valid to Config. Overrides valid	t_{ROVCV}	0	—	ns
R6	Configuration Override Setup Time to $\overline{\text{RSTOUT}}$ invalid	t_{COS}	20	—	t_{CYC}
R7	Configuration Override Hold Time after $\overline{\text{RSTOUT}}$ invalid	t_{COH}	0	—	ns
R8	$\overline{\text{RSTOUT}}$ invalid to Configuration Override High Impedance	t_{ROICZ}	—	1	t_{CYC}

[1] During low power STOP, the synchronizers for the $\overline{\text{RESET}}$ input are bypassed and $\overline{\text{RESET}}$ is asserted asynchronously to the system. Thus, $\overline{\text{RESET}}$ must be held a minimum of 100 ns.

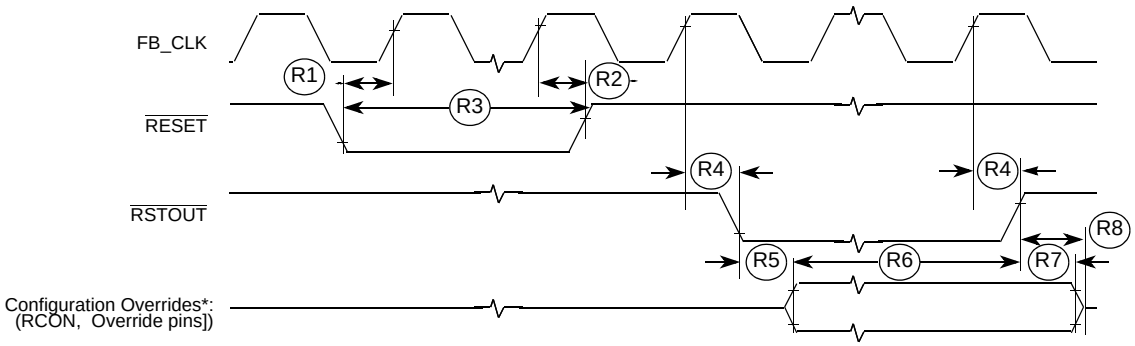


Figure 14. $\overline{\text{RESET}}$ and Configuration Override Timing

NOTE

Refer to the CCM chapter of the *MCF5373 Reference Manual* for more information.

5.10 USB On-The-Go

The MCF5373 device is compliant with industry standard USB 2.0 specification.

5.11 SSI Timing Specifications

This section provides the AC timings for the SSI in master (clocks driven) and slave modes (clocks input). All timings are given for non-inverted serial clock polarity (SSI_TCR[TSCKP] = 0, SSI_RCR[RSCKP] = 0) and a non-inverted frame sync (SSI_TCR[TFSI] = 0, SSI_RCR[RFSI] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (SSI_BCLK) and/or the frame sync (SSI_FS) shown in the figures below.

Table 14. SSI Timing – Master Modes[1]

Num	Description	Symbol	Min	Max	Units
S1	SSI_MCLK cycle time[2]	t_{MCLK}	$8 \times t_{SYS}$	—	ns
S2	SSI_MCLK pulse width high / low		45%	55%	t_{MCLK}
S3	SSI_BCLK cycle time[3]	t_{BCLK}	$8 \times t_{SYS}$	—	ns
S4	SSI_BCLK pulse width		45%	55%	t_{BCLK}
S5	SSI_BCLK to SSI_FS output valid		—	15	ns
S6	SSI_BCLK to SSI_FS output invalid		-2	—	ns
S7	SSI_BCLK to SSI_TXD valid		—	15	ns
S8	SSI_BCLK to SSI_TXD invalid / high impedence		-4	—	ns
S9	SSI_RXD / SSI_FS input setup before SSI_BCLK		15	—	ns
S10	SSI_RXD / SSI_FS input hold after SSI_BCLK		0	—	ns

1 All timings specified with a capactive load of 25pF.

2 SSI_MCLK can be generated from SSI_CLKIN or a divided version of the internal system clock (SYSCLK).

3 SSI_BCLK can be derived from SSI_CLKIN or a divided version of SYSCLK. If the SYSCLK is used, the minimum divider is 6. If the SSI_CLKIN input is used, the programmable dividers must be set to ensure that SSI_BCLK does not exceed 4 x f_{SYS}.

Table 15. SSI Timing – Slave Modes[1]

Num	Description	Symbol	Min	Max	Units
S11	SSI_BCLK cycle time	t_{BCLK}	$8 \times t_{SYS}$	—	ns
S12	SSI_BCLK pulse width high/low		45%	55%	t_{BCLK}
S13	SSI_FS input setup before SSI_BCLK		10	—	ns
S14	SSI_FS input hold after SSI_BCLK		3	—	ns
S15	SSI_BCLK to SSI_TXD/SSI_FS output valid		—	15	ns
S16	SSI_BCLK to SSI_TXD/SSI_FS output invalid/high impedence		-2	—	ns
S17	SSI_RXD setup before SSI_BCLK		10	—	ns
S18	SSI_RXD hold after SSI_BCLK		3	—	ns

1 All timings specified with a capactive load of 25pF.

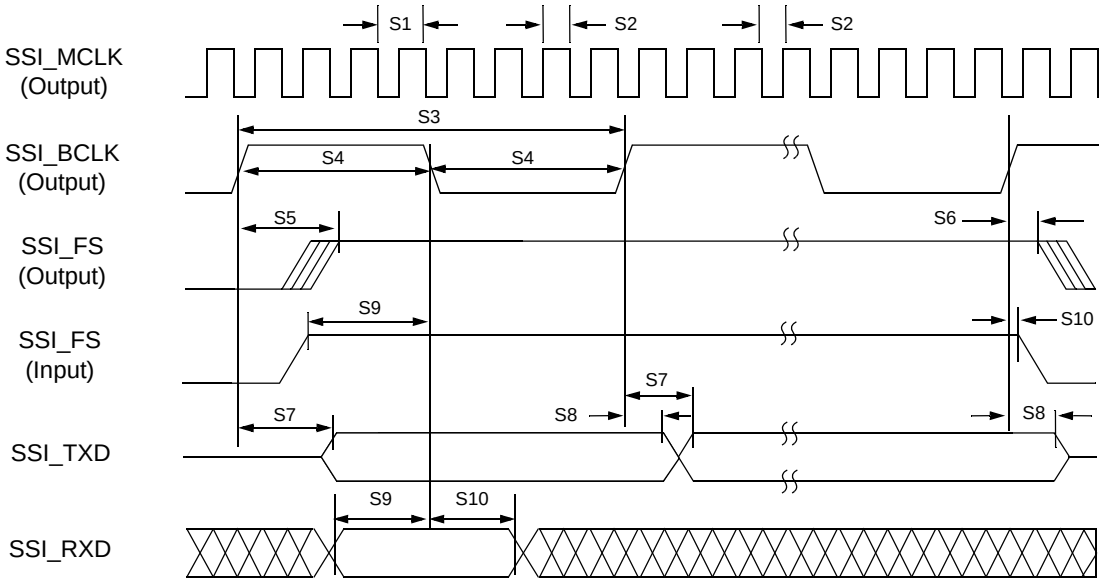


Figure 15. SSI Timing – Master Modes

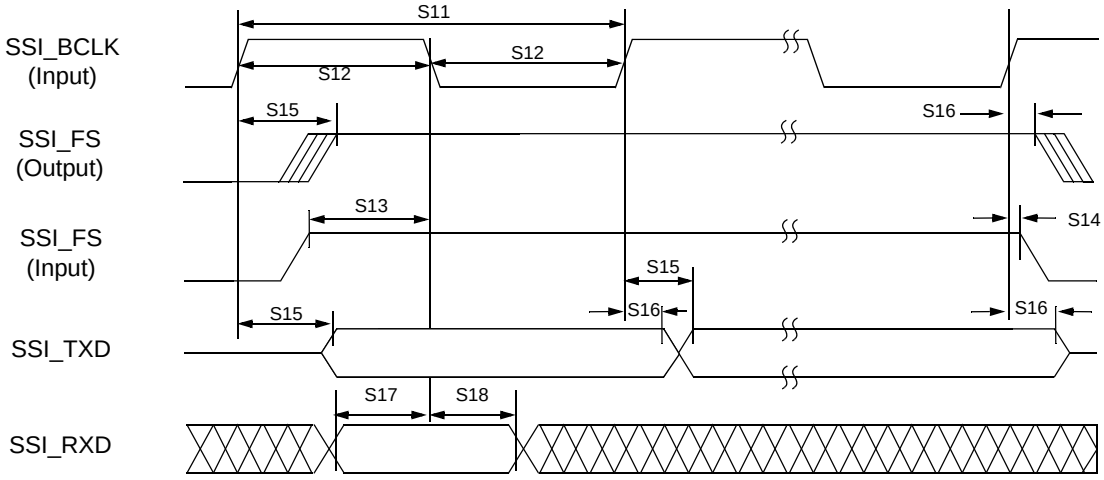


Figure 16. SSI Timing – Slave Modes

5.12 I²C Input/Output Timing Specifications

Table 16 lists specifications for the I²C input timing parameters shown in Figure 17.

Table 16. I²C Input Timing Specifications between SCL and SDA

Num	Characteristic	Min	Max	Units
I1	Start condition hold time	2	—	t_{cyc}
I2	Clock low period	8	—	t_{cyc}
I3	I2C_SCL/I2C_SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	1	ms
I4	Data hold time	0	—	ns

Table 16. I²C Input Timing Specifications between SCL and SDA (continued)

Num	Characteristic	Min	Max	Units
I5	I2C_SCL/I2C_SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	1	ms
I6	Clock high time	4	—	t_{cyc}
I7	Data setup time	0	—	ns
I8	Start condition setup time (for repeated start condition only)	2	—	t_{cyc}
I9	Stop condition setup time	2	—	t_{cyc}

Table 17 lists specifications for the I²C output timing parameters shown in Figure 17.

Table 17. I²C Output Timing Specifications between SCL and SDA

Num	Characteristic	Min	Max	Units
I1[1]	Start condition hold time	6	—	t_{cyc}
I2 [1]	Clock low period	10	—	t_{cyc}
I3 [2]	I2C_SCL/I2C_SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	—	µs
I4 [1]	Data hold time	7	—	t_{cyc}
I5 [3]	I2C_SCL/I2C_SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	3	ns
I6 [1]	Clock high time	10	—	t_{cyc}
I7 [1]	Data setup time	2	—	t_{cyc}
I8 [1]	Start condition setup time (for repeated start condition only)	20	—	t_{cyc}
I9 [1]	Stop condition setup time	10	—	t_{cyc}

1 Output numbers depend on the value programmed into the IFDR; an IFDR programmed with the maximum frequency (IFDR = 0x20) results in minimum output timings as shown in Table 17. The I²C interface is designed to scale the actual data transition time to move it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed into the IFDR; however, the numbers given in Table 17 are minimum values.

2 Because I2C_SCL and I2C_SDA are open-collector-type outputs, which the processor can only actively drive low, the time I2C_SCL or I2C_SDA take to reach a high level depends on external signal capacitance and pull-up resistor values.

3 Specified at a nominal 50-pF load.

Figure 17 shows timing for the values in Table 17 and Table 16.

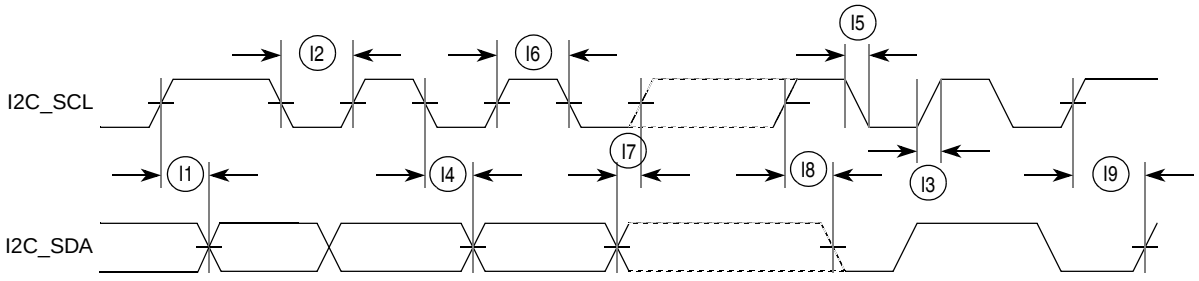


Figure 17. I²C Input/Output Timings

5.13 Fast Ethernet AC Timing Specifications

MII signals use TTL signal levels compatible with devices operating at 5.0 V or 3.3 V.

5.13.1 MII Receive Signal Timing

The receiver functions correctly up to a FEC_RXCLK maximum frequency of 25 MHz +1%. The processor clock frequency must exceed twice the FEC_RXCLK frequency.

Table 18 lists MII receive channel timings.

Table 18. MII Receive Signal Timing

Num	Characteristic	Min	Max	Unit
M1	FEC_RXD[3:0], FEC_RXDV, FEC_RXER to FEC_RXCLK setup	5	—	ns
M2	FEC_RXCLK to FEC_RXD[3:0], FEC_RXDV, FEC_RXER hold	5	—	ns
M3	FEC_RXCLK pulse width high	35%	65%	FEC_RXCLK period
M4	FEC_RXCLK pulse width low	35%	65%	FEC_RXCLK period

Figure 18 shows MII receive signal timings listed in Table 18.

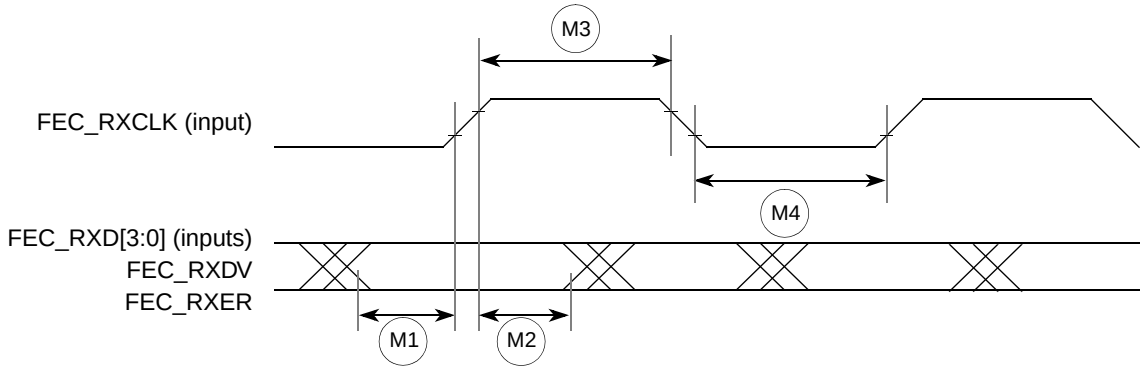


Figure 18. MII Receive Signal Timing Diagram

5.13.2 MII Transmit Signal Timing

Table 19 lists MII transmit channel timings.

The transmitter functions correctly up to a FEC_TXCLK maximum frequency of 25 MHz +1%. The processor clock frequency must exceed twice the FEC_TXCLK frequency.

Table 19. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
M5	FEC_TXCLK to FEC_TXD[3:0], FEC_TXEN, FEC_TXER invalid	5	—	ns
M6	FEC_TXCLK to FEC_TXD[3:0], FEC_TXEN, FEC_TXER valid	—	25	ns
M7	FEC_TXCLK pulse width high	35%	65%	FEC_TXCLK period
M8	FEC_TXCLK pulse width low	35%	65%	FEC_TXCLK period

Figure 19 shows MII transmit signal timings listed in Table 19.

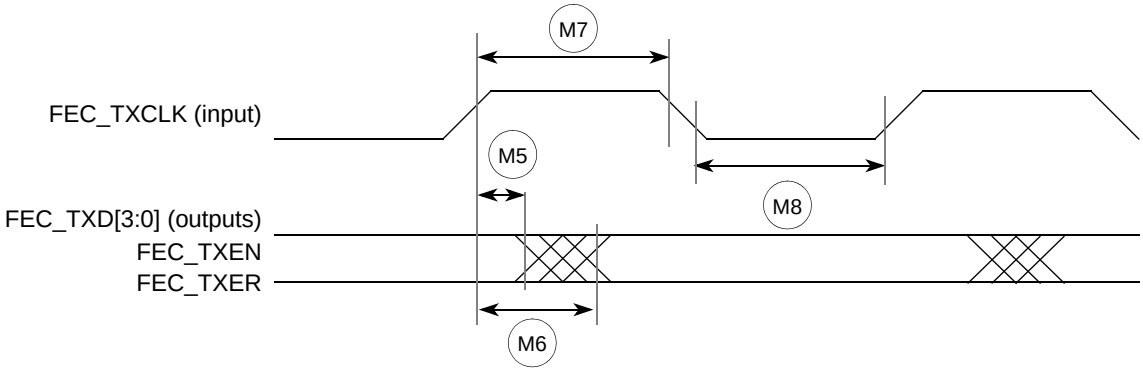


Figure 19. MII Transmit Signal Timing Diagram

5.13.3 MII Async Inputs Signal Timing

Table 20 lists MII asynchronous inputs signal timing.

Table 20. MII Async Inputs Signal Timing

Num	Characteristic	Min	Max	Unit
M9	FEC_CRS, FEC_COL minimum pulse width	1.5	—	FEC_TXCLK period

Figure 20. MII Async Inputs Timing Diagram

5.13.4 MII Serial Management Channel Timing

Table 21 lists MII serial management channel timings. The FEC functions correctly with a maximum MDC frequency of 2.5 MHz.

Table 21. MII Serial Management Channel Timing

Num	Characteristic	Min	Max	Unit
M10	FEC_MDC falling edge to FEC_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	FEC_MDC falling edge to FEC_MDIO output valid (max prop delay)	—	25	ns
M12	FEC_MDIO (input) to FEC_MDC rising edge setup	10	—	ns
M13	FEC_MDIO (input) to FEC_MDC rising edge hold	0	—	ns
M14	FEC_MDC pulse width high	40%	60%	FEC_MDC period
M15	FEC_MDC pulse width low	40%	60%	FEC_MDC period

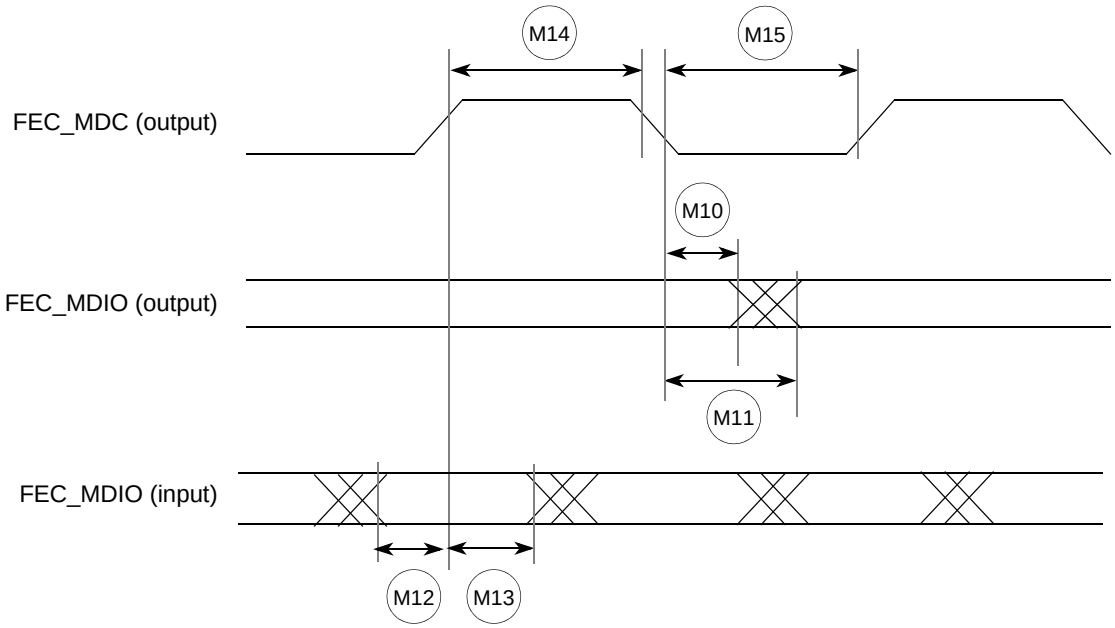


Figure 21. MII Serial Management Channel Timing Diagram

5.14 32-Bit Timer Module Timing Specifications

Table 22 lists timer module AC timings.

Table 22. Timer Module AC Timing Specifications

Name	Characteristic	Min	Max	Unit
T1	DT0IN / DT1IN / DT2IN / DT3IN cycle time	3	—	t_{CYC}
T2	DT0IN / DT1IN / DT2IN / DT3IN pulse width	1	—	t_{CYC}

5.15 QSPI Electrical Specifications

Table 23 lists QSPI timings.

Table 23. QSPI Modules AC Timing Specifications

Name	Characteristic	Min	Max	Unit
QS1	QSPI_CS[3:0] to QSPI_CLK	1	510	t_{CYC}
QS2	QSPI_CLK high to QSPI_DOUT valid.	—	10	ns
QS3	QSPI_CLK high to QSPI_DOUT invalid. (Output hold)	2	—	ns
QS4	QSPI_DIN to QSPI_CLK (Input setup)	9	—	ns
QS5	QSPI_DIN to QSPI_CLK (Input hold)	9	—	ns

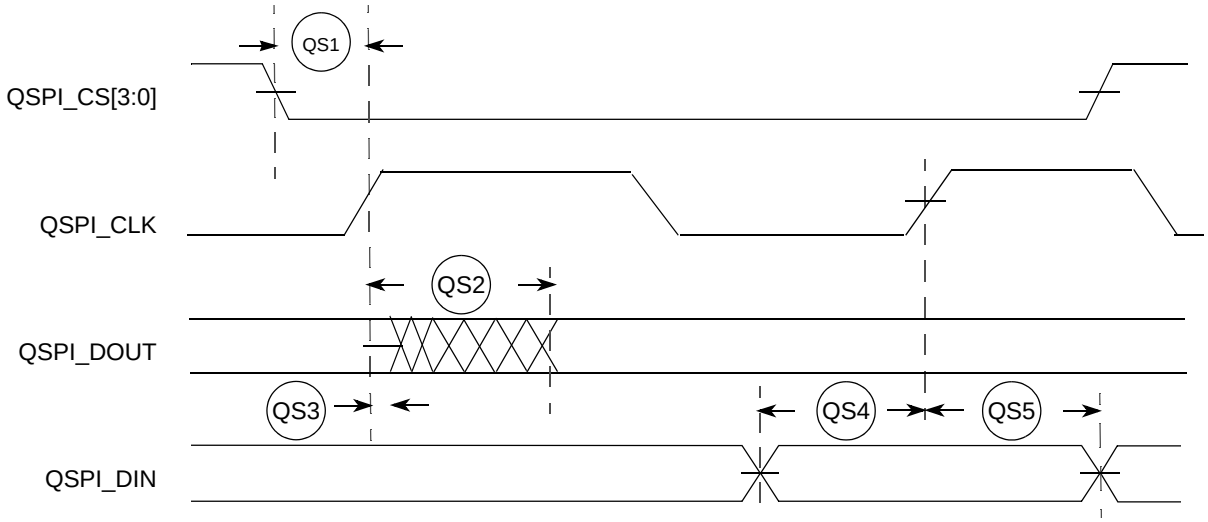


Figure 22. QSPI Timing

5.16 JTAG and Boundary Scan Timing

Table 24. JTAG and Boundary Scan Timing

Num	Characteristics[1]	Symbol	Min	Max	Unit
J1	TCLK Frequency of Operation	f_{JCYC}	DC	1/4	$f_{sys/3}$
J2	TCLK Cycle Period	t_{JCYC}	4	—	t_{CYC}
J3	TCLK Clock Pulse Width	t_{JCW}	26	—	ns
J4	TCLK Rise and Fall Times	t_{JCRF}	0	3	ns
J5	Boundary Scan Input Data Setup Time to TCLK Rise	t_{BSDST}	4	—	ns
J6	Boundary Scan Input Data Hold Time after TCLK Rise	t_{BSDHT}	26	—	ns
J7	TCLK Low to Boundary Scan Output Data Valid	t_{BSDV}	0	33	ns
J8	TCLK Low to Boundary Scan Output High Z	t_{BSDZ}	0	33	ns
J9	TMS, TDI Input Data Setup Time to TCLK Rise	t_{TAPBST}	4	—	ns
J10	TMS, TDI Input Data Hold Time after TCLK Rise	t_{TAPBHT}	10	—	ns
J11	TCLK Low to TDO Data Valid	t_{TDODV}	0	26	ns
J12	TCLK Low to TDO High Z	t_{TDODZ}	0	8	ns
J13	$\overline{\text{TRST}}$ Assert Time	t_{TRSTAT}	100	—	ns
J14	$\overline{\text{TRST}}$ Setup Time (Negation) to TCLK High	t_{TRSTST}	10	—	ns

1 JTAG_EN is expected to be a static signal. Hence, specific timing is not associated with it.

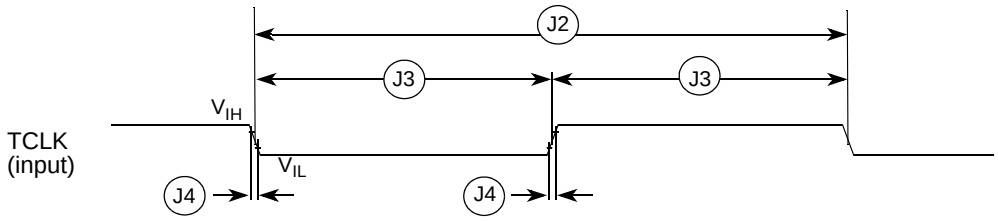


Figure 23. Test Clock Input Timing

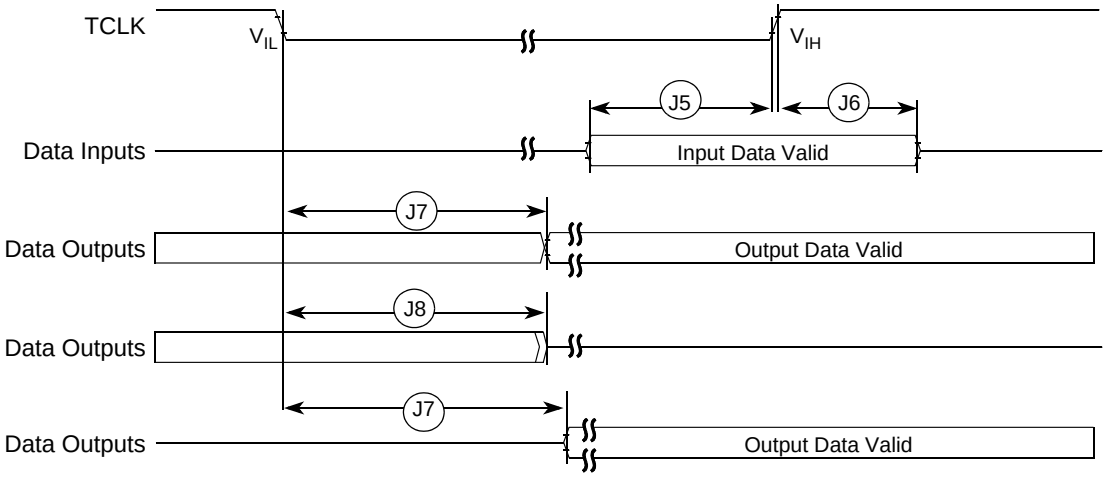


Figure 24. Boundary Scan (JTAG) Timing

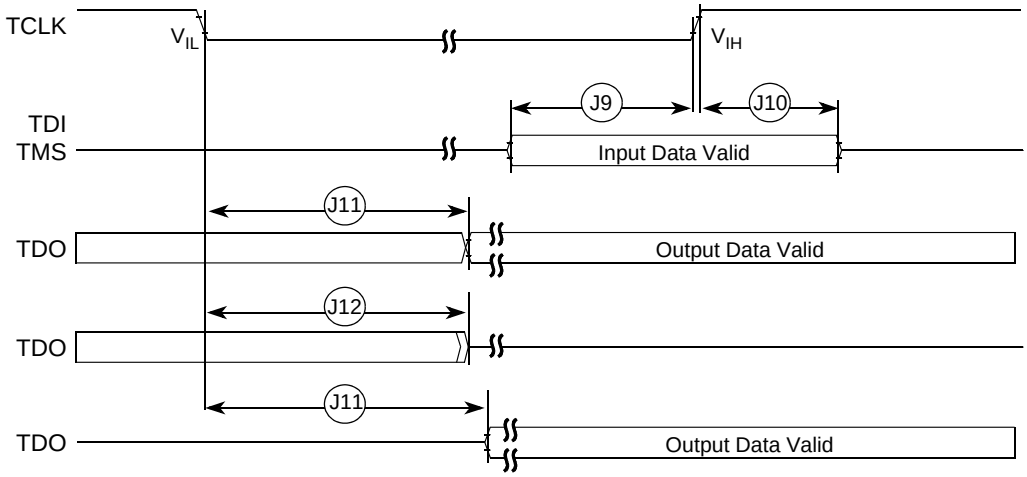


Figure 25. Test Access Port Timing

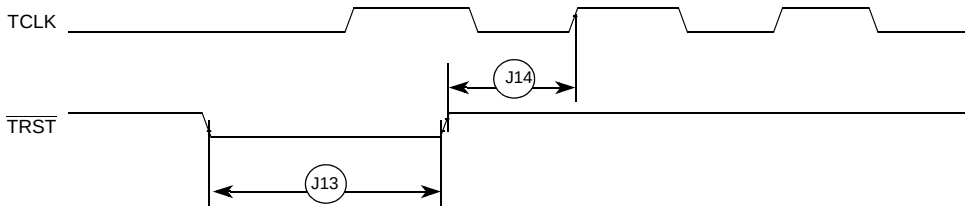


Figure 26. $\overline{\text{TRST}}$ Timing

5.17 Debug AC Timing Specifications

Table 25 lists specifications for the debug AC timing parameters shown in Figure 27.

Table 25. Debug AC Timing Specification

Num	Characteristic	Min	Max	Units
D0	PSTCLK cycle time	2	2	$t_{SYS} = 1/f_{SYS}$
D1	PSTCLK rising to PSTDDATA valid	—	3.0	ns
D2	PSTCLK rising to PSTDDATA invalid	1.5	—	ns
D3	DSI-to-DSCLK setup	1	—	PSTCLK
D4[1]	DSCLK-to-DSO hold	4	—	PSTCLK
D5	DSCLK cycle time	5	—	PSTCLK
D6	BKPT assertion time	1	—	PSTCLK

1 DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of PSTCLK.

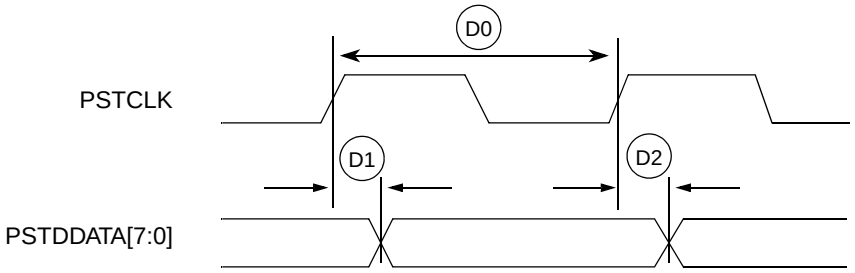


Figure 27. Real-Time Trace AC Timing

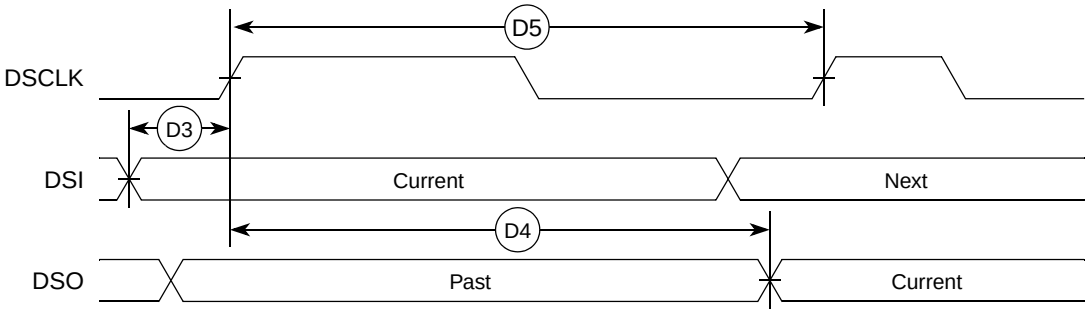


Figure 28. BDM Serial Port AC Timing

6 Current Consumption

All current consumption data is lab data measured on a single device using an evaluation board. Table 26 shows the typical power consumption in low-power modes. These current measurements are taken after executing a STOP instruction.

Table 26. Current Consumption in Low-Power Modes[1,2]

Mode	Voltage	58 MHz (Typ)[3]	64 MHz (Typ)[3]	72 MHz (Typ)[3]	80 MHz (Typ)[3]	80 MHz (Peak)[4]	Units
Stop Mode 3 (Stop 11)[5]	3.3 V	3.9	3.92	4.0	4.0	4.0	mA
	1.5 V	1.04	1.04	1.04	1.04	1.08	
Stop Mode 2 (Stop 10)[4]	3.3 V	4.69	4.72	4.8	4.8	4.8	
	1.5 V	2.69	2.69	2.70	2.70	2.75	
Stop Mode 1(Stop 01)[4]	3.3 V	4.72	4.73	4.81	4.81	4.81	
	1.5 V	15.28	16.44	17.85	19.91	20.42	
Stop Mode 0 (Stop 00)[4]	3.3 V	21.65	21.68	24.33	26.13	26.16	
	1.5 V	15.47	16.63	18.06	20.12	20.67	
Wait/Doze	3.3 V	22.49	22.52	25.21	27.03	39.8	
	1.5 V	26.79	28.85	30.81	34.47	97.4	
Run	3.3 V	33.61	33.61	42.3	50.5	62.6	
	1.5 V	56.3	60.7	65.4	73.4	132.3	

1 All values are measured with a 3.30V EV_{DD}, 3.30V SDV_{DD} and 1.5V IV_{DD} power supplies. Tests performed at room temperature with pins configured for high drive strength.

2 Refer to the Power Management chapter in the *MCF537x Reference Manual* for more information on low-power modes.

3 All peripheral clocks except UART0, FlexBus, INTC0, reset controller, PLL, and edge port off before entering low power mode. All code executed from flash.

4 All peripheral clocks on before entering low power mode. All code is executed from flash.

5 See the description of the low-power control register (LCPR) in the *MCF537x Reference Manual* for more information on stop modes 0–3.

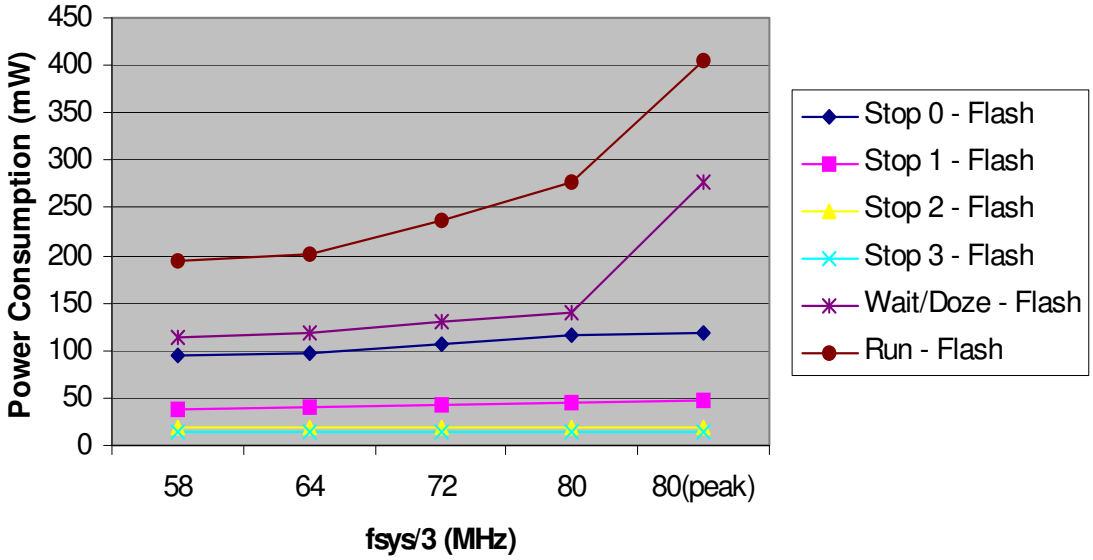


Figure 29. Current Consumption in Low-Power Modes

Table 27. Typical Active Current Consumption Specifications[1]

$f_{sys/3}$ Frequency	Voltage	Typical[2] Active (Flash)	Peak[3]	Unit
1.333 MHz	3.3V	7.73	7.74	mA
	1.5V	2.87	3.56	
2.666 MHz	3.3V	8.57	8.60	
	1.5V	4.37	5.52	
58 MHz	3.3V	40.10	49.3	
	1.5V	65.90	91.70	
64 MHz	3.3V	44.40	54.0	
	1.5V	69.50	97.0	
72 MHz	3.3V	53.6	63.7	
	1.5V	74.6	104.7	
80 MHz	3.3V	63.0	73.7	
	1.5V	79.6	112.9	

1 All values are measured with a 3.30 V EV_{DD}, 3.30 V SDV_{DD} and 1.5 V IV_{DD} power supplies. Tests performed at room temperature with pins configured for high drive strength.

2 CPU polling a status register. All peripheral clocks except UART0, FlexBus, INTC0, reset controller, PLL, and edge port disabled.

3 Peak current measured while running a while(1) loop with all modules active.

Figure 30 shows the estimated maximum power consumption.

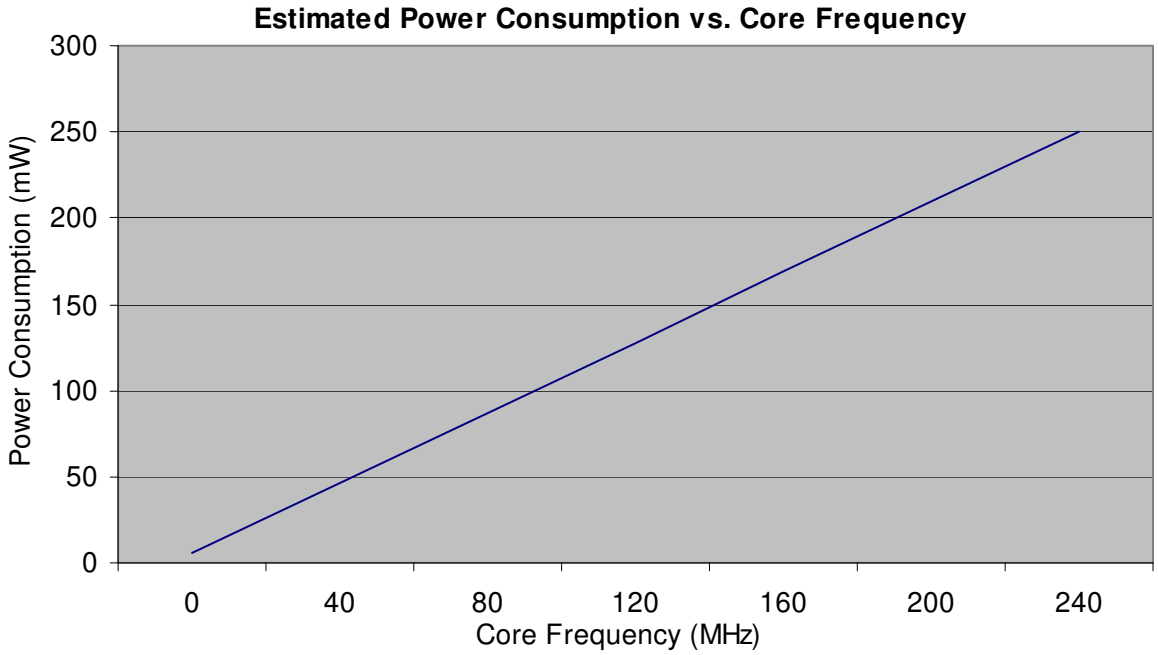


Figure 30. Estimated Maximum Power Consumption

7 Package Information

This section contains drawings showing the pinout and the packaging and mechanical characteristics of the MCF537*x* devices.

NOTE

The mechanical drawings are the latest revisions at the time of publication of this document. The most up-to-date mechanical drawings can be found at the product summary page located at http://www.freescale.com/coldfire.

7.1 Package Dimensions—196 MAPBGA

Figure 31 shows the MCF5373LCVM240, MCF5372LCVM240, and MCF53721CVM240 package dimensions.

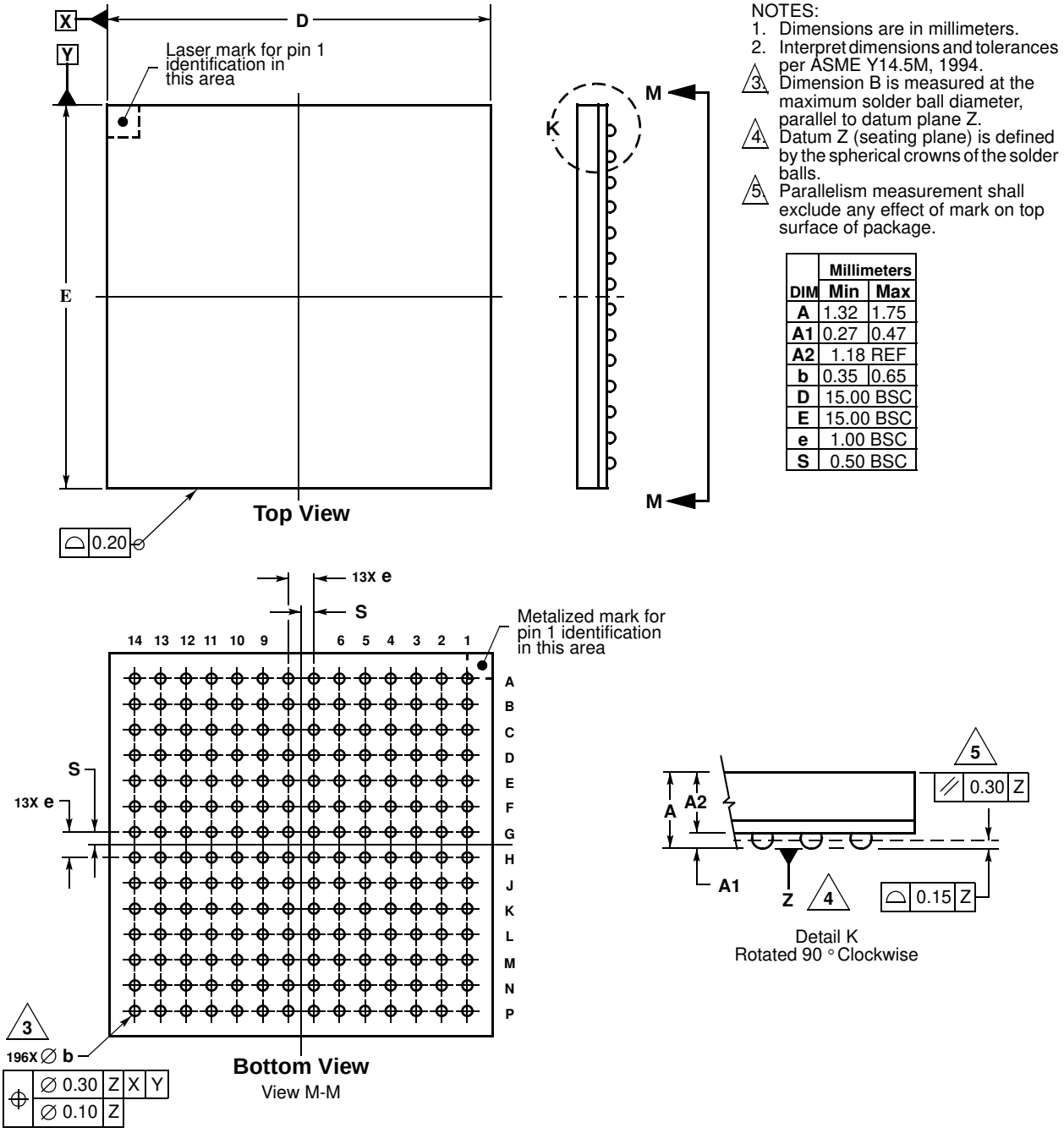


Figure 31. 196 MAPBGA Package Dimensions (Case No. 1128A-01)

7.2 Package Dimensions—160 QFP

Figure 32 and Figure 33 show the MCF5372CAB180 and MCF5373CAB180 package dimensions.

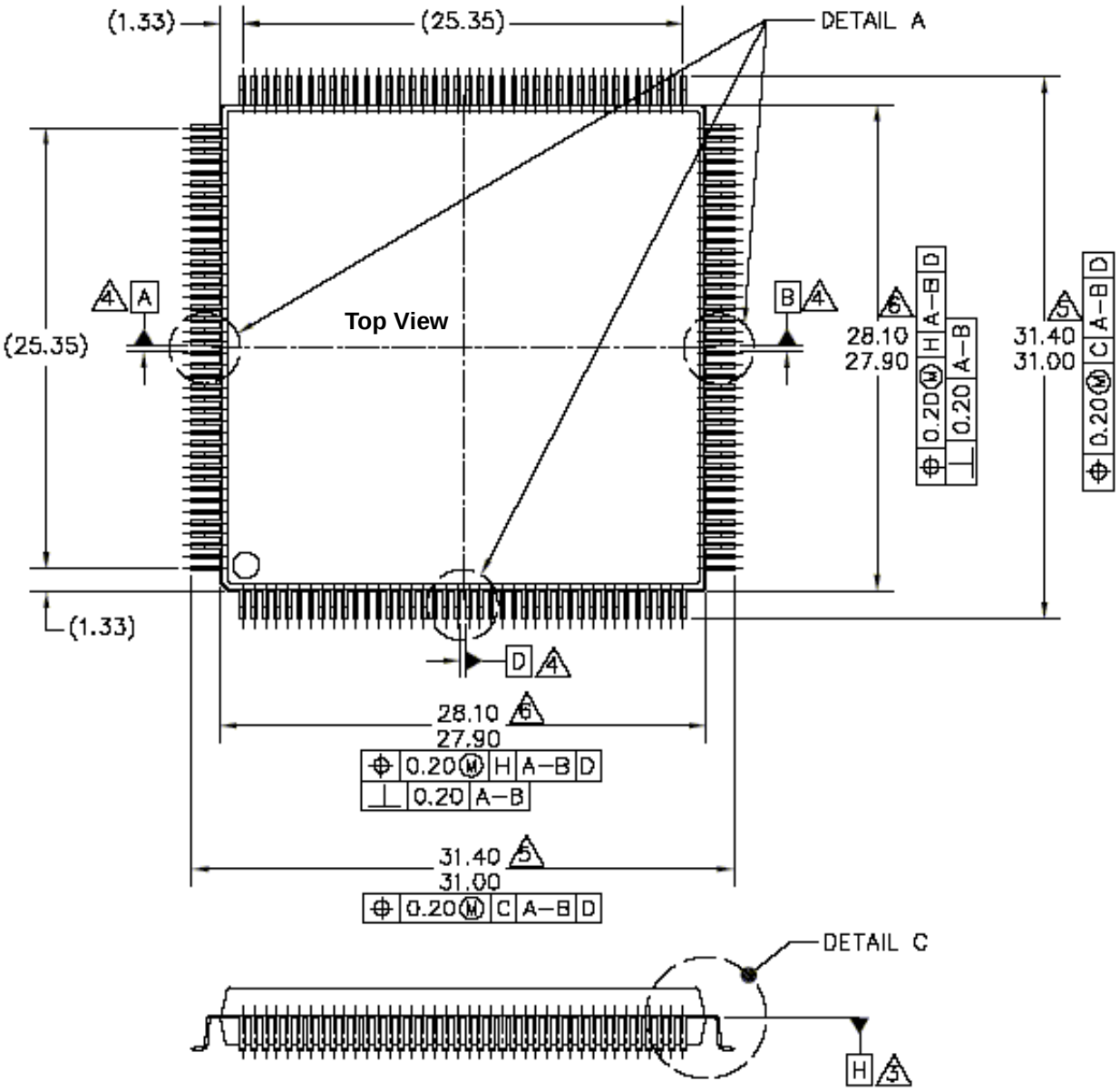
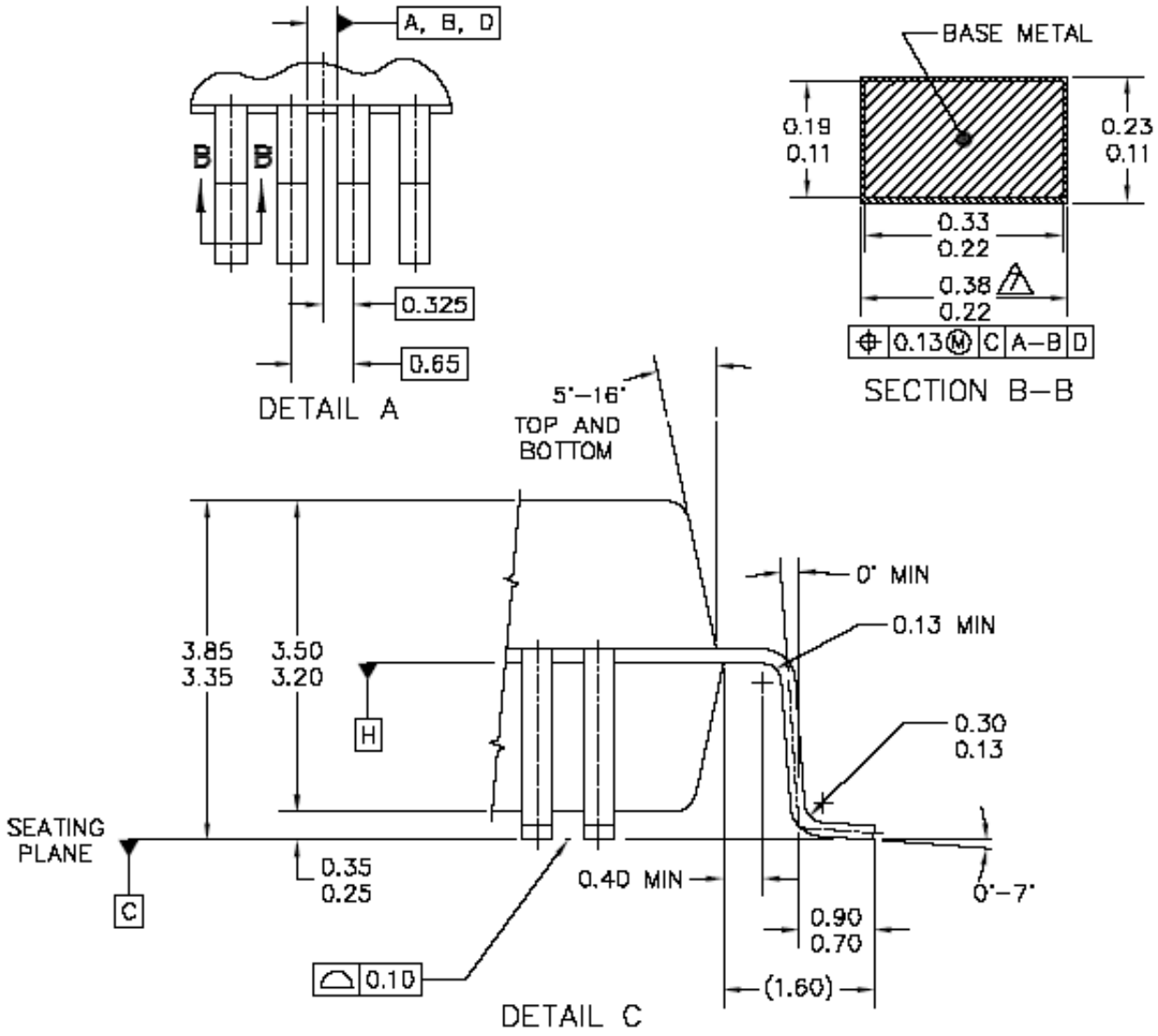


Figure 32. 160QFP Package Dimensions (Sheet 1 of 2)



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS TO BE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
7. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

Figure 33. 160QFP Package Dimensions (Sheet 2 of 2)

8 Revision History

Table 28. MCF5373DS Document Revision History

Rev. No.	Substantive Changes	Date of Release
0	• Initial release	11/2005
0.1	• Swapped pin locations PLL_VSS (J11->H11) and DRAMSEL (H11->J11) in Table 1. Figure 4 is correct.	12/2005
0.2	• Added not to Section 7, “Package Information.” • Added “top view” and “bottom view” where appropriate in mechanical drawings and pinout figures. • Figure 6: Corrected “FB_CLK (75MHz)” label to “FB_CLK (80MHz)”	3/2006
0.3	• Changed 160QFP pinouts in Figure 5 and Table 2: Removed IRQ3 pin, shifted pins 89–99 up one pin to 90–100. Pin 89 is now VSS. • Table 2: Rearranged GPIO signal names for FEC pins. • Removed ULPI specifications as the device does not support ULPI.	4/2006
1	• Updated thermal characteristic values in Table 7. • Updated DC electricals values in Table 7. • Updated Section 3.3, “Supply Voltage Sequencing and Separation Cautions” and subsections. • Updated and added Oscillator/PLL characteristics in Table 8. • Table 9: Swapped min/max for FB1; Removed FB8 & FB9. • Updated SDRAM write timing diagram, Figure 9. • Table 11: Added values for frequency of operation and DD1. • Replaced figure & table Section 5.11, “SSI Timing Specifications,” with slave & master mode versions. • Removed second sentence from Section 5.13.2, “MII Transmit Signal Timing,” regarding no minimum frequency requirement for TXCLK. • Removed third and fourth paragraphs from Section 5.13.2, “MII Transmit Signal Timing,” as this feature is not supported on this device. • Updated figure & table Section 5.17, “Debug AC Timing Specifications.” • Renamed & moved previous version’s Section 5.5 “Power Consumption” to Section 6, “Current Consumption.” Added additional real-world data to this section as well.	7/2007
2	• Added MCF53721 device information throughout: features list, family configuration table, ordering information table, signals description table, and relevant package diagram titles • Remove Footnote 1 from Table 11. • Changed document type from Advance Information to Technical Data.	8/2007

Table 28. MCF5373DS Document Revision History (continued)

Rev. No.	Substantive Changes	Date of Release
3	• Removed cryptography from Table 1 for the MCF53721 device. • Corrected D0 spec in Table 25 from 1.5 x t_{sys} to 2 x t_{sys} for min and max balues. • Updated FlexBus read and write timing diagrams in Figure 7 and Figure 8. • Corrected package information in Table 2 for MCF5373LCVM240 device from “256 MAPBGA” to “196 MAPBGA”. • Removed footnote 2 from the IRQ[7:1] alternate functions USBHOST VBUS_EN, USBHOST VBUS_OC, SSI_MCLK, USB_CLKIN, and SSI_CLKIN signals in Table 6.	4/2008
4	Changed the following specs in Table 10 and Table 11: • Minimum frequency of operation from TBD to 60MHz • Maximum clock period from TBD to 16.67 ns Added FlexCAN for the MCF53721 device in features list, block diagram, Signal Information and Muxing table, and GPIO timing diagram	11/2008

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