S1C17M10 (rev1.1)

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16-bit Single Chip Microcontroller

- Smart card Interface (ISO7816-3) is embedded.
- 64KB Flash ROM: Read/program protection function, 4KB RAM
- Supports 1.8V to 5.5V wide range operating voltage.
- Equipped with an LCD driver capable of driving an 80 SEG × 16 COM / 88 SEG × 8 COM LCD panel.
- Supports various kinds of interfaces (UART, SPI, I^2C)

■ DESCRIPTIONS

The S1C17M10 is a 16-bit embedded Flash MCU that features low power consumption. It includes various serial interfaces and an LCD driver on the compact die, and is ideal for battery-driven electronic equipment such as smart card read type eTokens and remote control units with a high-definition LCD display.

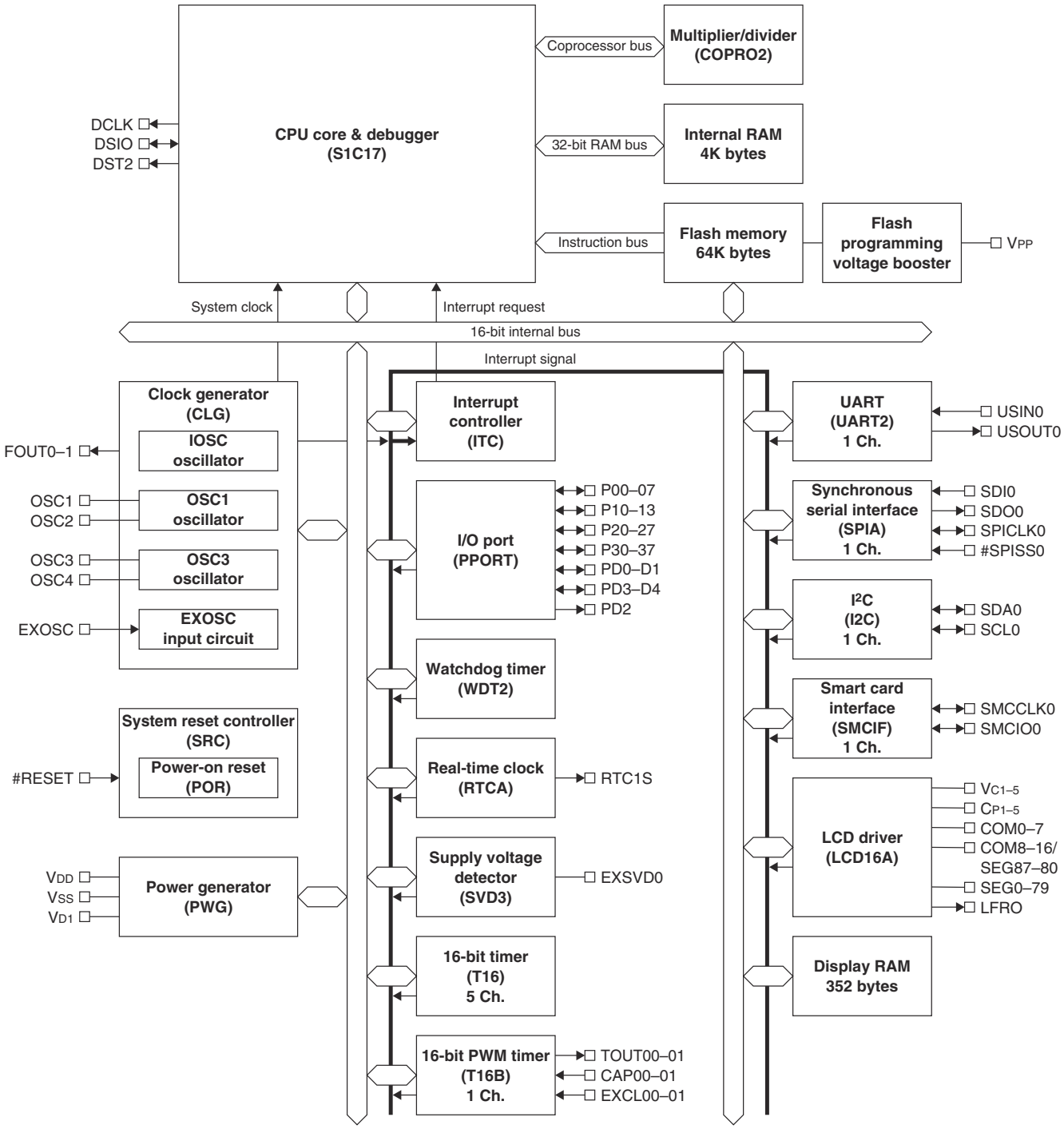
■ FEATURES

Model	S1C17M10
CPU	
CPU core	Seiko Epson original 16-bit RISC CPU core S1C17
Other	On-chip debugger
Embedded Flash memory	
Capacity	64K bytes (for both instructions and data)
Erase/program count	1,000 times (min.) * Programming by the debugging tool ICDmini
Other	Security function to protect from reading/programming by ICDmini
	On-board programming function using ICDmini
	Flash programming voltage can be generated internally.
Embedded RAM	
Capacity	4K bytes
Embedded display RAM	
Capacity	352 bytes
Clock generator (CLG)	
System clock source	4 sources (IOSC/OSC1/OSC3/EXOSC)
System clock frequency (operating frequency)	16.8 MHz (max.)
IOSC oscillator circuit (boot clock source)	700 kHz (typ.) embedded oscillator
	23 µs (max.) starting time (time from cancelation of SLEEP state to vector table read by the CPU)
OSC1 oscillator circuit	32.768 kHz (typ.) crystal oscillator
	32 kHz (typ.) embedded oscillator
	Oscillation stop detection circuit included
OSC3 oscillator circuit	16.8 MHz (max.) crystal/ceramic oscillator
	4, 8, 12, and 16 MHz-switchable embedded oscillator
	Auto-trimming function for the embedded oscillator
EXOSC clock input	16.8 MHz (max.) square or sine wave input
Other	Configurable system clock division ratio
	Configurable system clock used at wake up from SLEEP state
	Operating clock frequency for the CPU and all peripheral circuits is selectable.
I/O port (PPORT)	
Number of general-purpose I/O ports	Input/output port: 32 bits (max.)
	Output port: 1 bit (max.)
	Pins are shared with the peripheral I/O.
Number of input interrupt ports	28 bits (max.)
Number of ports that support universal port multiplexer (UPMUX)	28 bits
	A peripheral circuit I/O function selected via software can be assigned to each port.
Timers	
Watchdog timer (WDT2)	Generates NMI or watchdog timer reset.
	Programmable NMI/reset generation cycle
Real-time clock (RTCA)	128–1 Hz counter, second/minute/hour/day/day of the week/month/year counters
	Theoretical regulation function for 1-second correction
	Alarm and stopwatch functions
16-bit timer (T16)	5 channels
	Generates the SPIA master clock.

Model	S1C17M10
Timers	
16-bit PWM timer (T16B)	1 channel
	Event counter/capture function
	PWM waveform generation function
	Number of PWM output or capture input ports: 2 ports/channel
Supply voltage detector (SVD3)	
Detection voltage	V_{DD} or external voltage (one external voltage input port is provided and an external voltage level can be detected even if it exceeds V_{DD}.)
Detection level	V_{DD}: 28 levels (1.8 to 5.0 V)/external voltage: 32 levels (1.2 to 5.0 V)
Other	Intermittent operation mode
	Generates an interrupt or reset according to the detection level evaluation.
Serial interfaces	
UART (UART2)	1 channel
	Baud-rate generator included, IrDA1.0 supported
	Open drain output, signal polarity, and baud rate division ratio are configurable.
Synchronous serial interface (SPIA)	1 channel
	2 to 16-bit variable data length
	The 16-bit timer (T16) can be used for the baud-rate generator in master mode.
I^2C (I2C) *1	1 channel
	Baud-rate generator included
Smart card interface (SMCIF)	1 channel
	Baud-rate generator included
LCD driver (LCD16A)	
LCD output	88SEG × 1–8COM (max.), 80SEG × 9–16COM (max.)
LCD contrast	16 levels
Other	1/4 or 1/5 bias power supply included, external voltage can be applied.
Multiplier/divider (COPRO2)	
Arithmetic functions	16-bit × 16-bit multiplier
	16-bit × 16-bit + 32-bit multiply and accumulation unit
	32-bit ÷ 32-bit divider
Reset	
#RESET pin	Reset when the reset pin is set to low.
Power-on reset	Reset at power on.
Key entry reset	Reset when the P00 to P01/P02/P03 keys are pressed simultaneously (can be enabled/disabled using a register).
Watchdog timer reset	Reset when the watchdog timer overflows (can be enabled/disabled using a register).
Supply voltage detector reset	Reset when the supply voltage detector detects the set voltage level (can be enabled/disabled using a register).
Interrupt	
Non-maskable interrupt	4 systems (Reset, address misaligned interrupt, debug, NMI)
Programmable interrupt	External interrupt: 1 system (8 levels)
	Internal interrupt: 14 systems (8 levels)
Power supply voltage	
V_{DD} operating voltage	1.8 to 5.5 V
V_{DD} operating voltage for Flash programming	2.4 to 5.5 V (V_{PP} = 7.5 V external power supply is required.) 2.4 to 5.5 V (When V_{PP} is generated internally)
Operating temperature	
Operating temperature range	-40 to 85 °C
Current consumption (Typ. value)	
SLEEP mode *2	0.16 µA IOSC = OFF, OSC1 = OFF, OSC3 = OFF
HALT mode	0.6 µA OSC1 = 32 kHz (crystal oscillator), RTC = ON
RUN mode	4 µA OSC1 = 32 kHz (crystal oscillator), RTC = ON, CPU = OSC1
	145 µA OSC1 = 32 kHz (crystal oscillator), RTC = ON, OSC3 = 1 MHz (ceramic oscillator), CPU = OSC3
Shipping form	
1 *3	TQFP15-128PIN (P-TQFP128-1414-0.40, 14 × 14 mm, t = 1.2 mm, 0.4 mm pitch)
2	Die form (Pad pitch: 80 µm (min.))

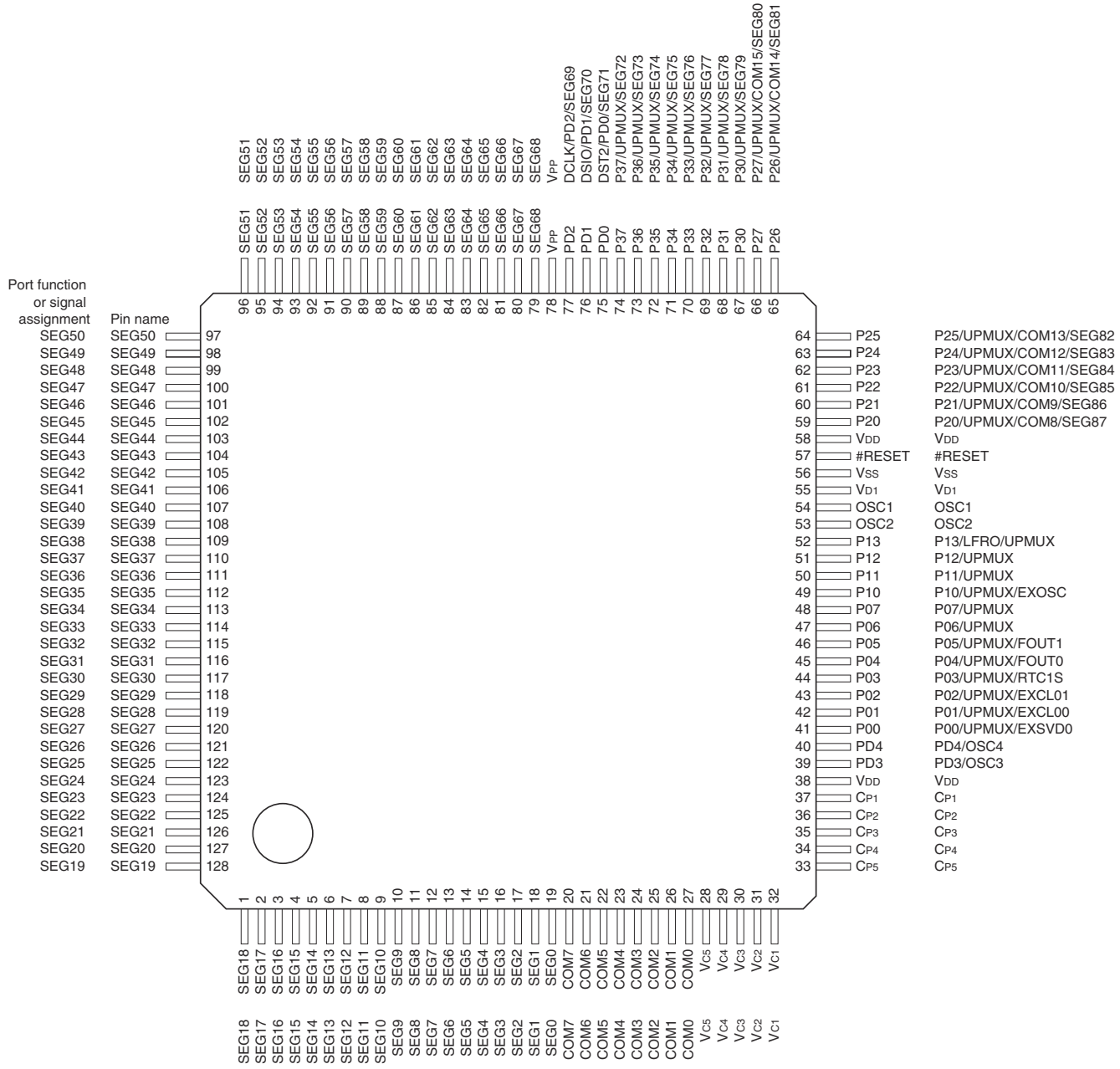
*1 The input filter in I2C (SDA and SCL inputs) does not comply with the standard for removing noise spikes less than 50 ns.
*2 The RAM retains data even in SLEEP mode.
*3 Shown in parentheses is a JEITA package name.

■ BLOCK DIAGRAM

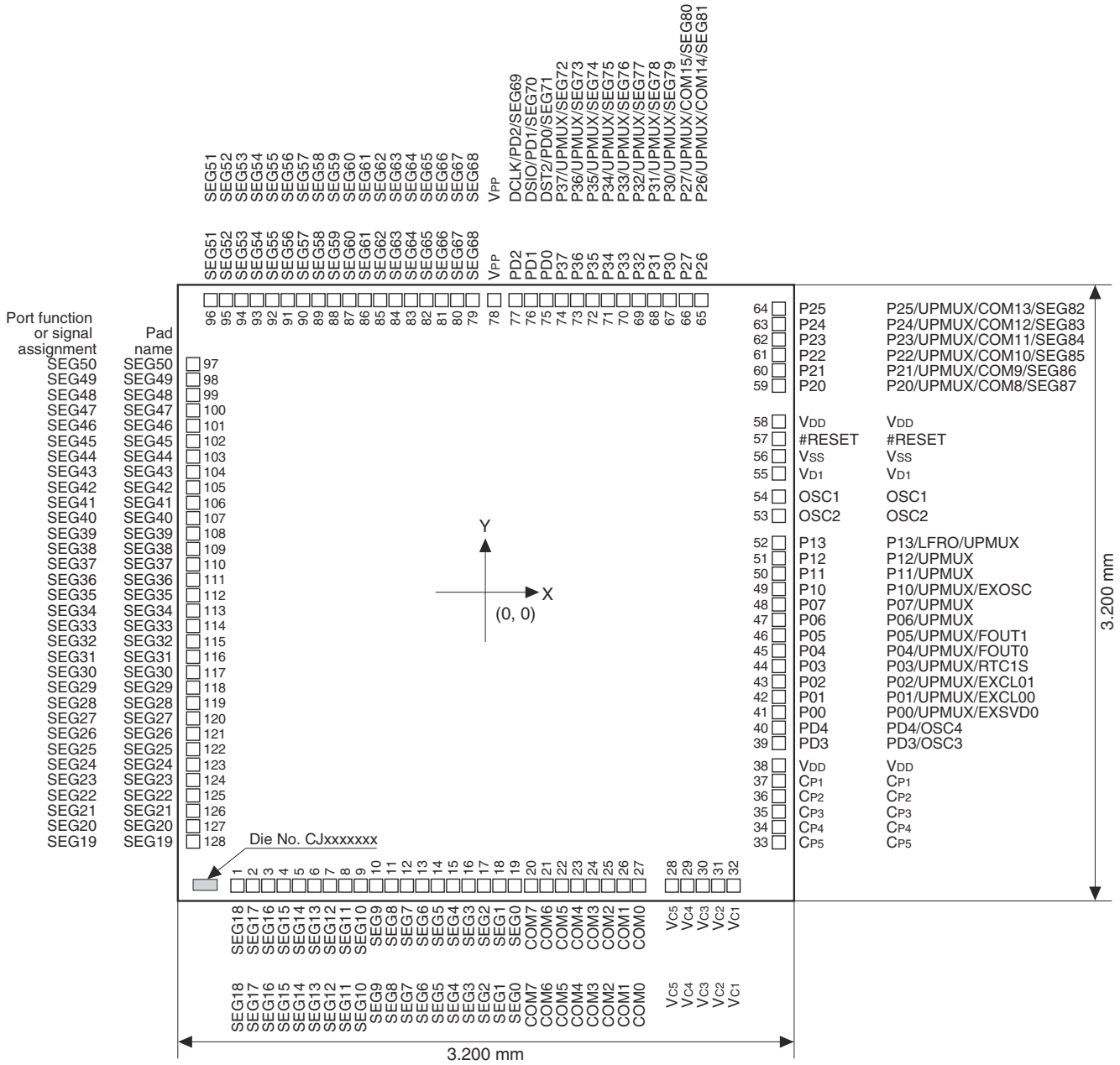


■ PIN CONFIGURATION DIAGRAMS

TQFP15-128PIN



Chip


Port function or signal assignment
Pad name
SEG50 SEG50 97
SEG49 SEG49 98
SEG48 SEG48 99
SEG47 SEG47 100
SEG46 SEG46 101
SEG45 SEG45 102
SEG44 SEG44 103
SEG43 SEG43 104
SEG42 SEG42 105
SEG41 SEG41 106
SEG40 SEG40 107
SEG39 SEG39 108
SEG38 SEG38 109
SEG37 SEG37 110
SEG36 SEG36 111
SEG35 SEG35 112
SEG34 SEG34 113
SEG33 SEG33 114
SEG32 SEG32 115
SEG31 SEG31 116
SEG30 SEG30 117
SEG29 SEG29 118
SEG28 SEG28 119
SEG27 SEG27 120
SEG26 SEG26 121
SEG25 SEG25 122
SEG24 SEG24 123
SEG23 SEG23 124
SEG22 SEG22 125
SEG21 SEG21 126
SEG20 SEG20 127
SEG19 SEG19 128
Die No. CJxxxxxxx
64 P25 P25/UPMUX/COM13/SEG82
63 P24 P24/UPMUX/COM12/SEG83
62 P23 P23/UPMUX/COM11/SEG84
61 P22 P22/UPMUX/COM10/SEG85
60 P21 P21/UPMUX/COM9/SEG86
59 P20 P20/UPMUX/COM8/SEG87
58 VDD VDD
57 #RESET #RESET
56 VSS VSS
55 VD1 VD1
54 OSC1 OSC1
53 OSC2 OSC2
52 P13 P13/LFRO/UPMUX
51 P12 P12/UPMUX
50 P11 P11/UPMUX
49 P10 P10/UPMUX/EXOSC
48 P07 P07/UPMUX
47 P06 P06/UPMUX
46 P05 P05/UPMUX/FOUT1
45 P04 P04/UPMUX/FOUT0
44 P03 P03/UPMUX/RTC1S
43 P02 P02/UPMUX/EXCL01
42 P01 P01/UPMUX/EXCL00
41 P00 P00/UPMUX/EXSVD0
40 PD4 PD4/OSC4
39 PD3 PD3/OSC3
38 VDD VDD
37 CP1 CP1
36 CP2 CP2
35 CP3 CP3
34 CP4 CP4
33 CP5 CP5
Y
X
(0, 0)
3.200 mm
3.200 mm

■ PIN DESCRIPTIONS

Symbol meanings

Assigned signal: The signal listed at the top of each pin is assigned in the initial state. The pin function must be switched via software to assign another signal (see the "I/O Ports" chapter).

I/O:
- I = Input
- O = Output
- I/O = Input/output
- P = Power supply
- A = Analog signal
- Hi-Z = High impedance state

Initial state:
- I (Pull-up) = Input with pulled up
- I (Pull-down) = Input with pulled down
- Hi-Z = High impedance state
- O (H) = High level output
- O (L) = Low level output

Tolerant fail-safe structure:
- ✓ = Over voltage tolerant fail-safe type I/O cell included (see the "I/O Ports" chapter)
  The over voltage tolerant fail-safe type I/O cell allows interfacing without passing unnecessary current even if a voltage exceeding V_{DD} is applied to the port. Also unnecessary current is not consumed when the port is externally biased without supplying V_{DD}.

Pin/pad name	Assigned signal	I/O	Initial state	Tolerant fail-safe structure	Function
V_{DD}	V_{DD}	P	–	–	Power supply (+)
V_{SS}	V_{SS}	P	–	–	GND
V_{PP}	V_{PP}	P	–	–	Power supply for Flash programming
V_{D1}	V_{D1}	A	–	–	V_{D1} regulator output
V_{C1-5}	V_{C1-5}	P	–	–	LCD panel driver power supply
C_{P1-5}	C_{P1-5}	A	–	–	LCD power supply booster capacitor connect pins
OSC1	OSC1	A	–	–	OSC1 oscillator circuit input
OSC2	OSC2	A	–	–	OSC1 oscillator circuit output
#RESET	#RESET	I	I (Pull-up)	–	Reset input
P00	P00	I/O	Hi-Z	✓	I/O port
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	EXSVD0	A			External power supply voltage detection input
P01	P01	I/O	Hi-Z	✓	I/O port
	EXCL00	I			16-bit PWM timer Ch.0 event counter input 0
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P02	P02	I/O	Hi-Z	✓	I/O port
	EXCL01	I			16-bit PWM timer Ch.0 event counter input 1
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P03	P03	I/O	Hi-Z	✓	I/O port
	RTC1S	O			Real-time clock 1-second cycle pulse output
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P04	P04	I/O	Hi-Z	✓	I/O port
	FOUT0	O			Clock external output
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P05	P05	I/O	Hi-Z	✓	I/O port
	FOUT1	O			Clock external output
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P06	P06	I/O	Hi-Z	✓	I/O port
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P07	P07	I/O	Hi-Z	✓	I/O port
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P10	P10	I/O	Hi-Z	✓	I/O port
	EXOSC	I			Clock generator external clock input
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P11	P11	I/O	Hi-Z	✓	I/O port
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P12	P12	I/O	Hi-Z	✓	I/O port
	UPMUX	I/O			User-selected I/O (universal port multiplexer)

Pin/pad name	Assigned signal	I/O	Initial state	Tolerant fail-safe structure	Function
P13	P13	I/O	Hi-Z	✓	I/O port
	LFRO	O			LCD frame signal monitor output
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P20	P20	I/O	Hi-Z	✓	I/O port
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	COM8	A			LCD common output
	SEG87	A			LCD segment output
P21	P21	I/O	Hi-Z	✓	I/O port
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	COM9	A			LCD common output
	SEG86	A			LCD segment output
P22	P22	I/O	Hi-Z	✓	I/O port
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	COM10	A			LCD common output
	SEG85	A			LCD segment output
P23	P23	I/O	Hi-Z	✓	I/O port
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	COM11	A			LCD common output
	SEG84	A			LCD segment output
P24	P24	I/O	Hi-Z	✓	I/O port
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	COM12	A			LCD common output
	SEG83	A			LCD segment output
P25	P25	I/O	Hi-Z	✓	I/O port
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	COM13	A			LCD common output
	SEG82	A			LCD segment output
P26	P26	I/O	Hi-Z	✓	I/O port
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	COM14	A			LCD common output
	SEG81	A			LCD segment output
P27	P27	I/O	Hi-Z	✓	I/O port
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	COM15	A			LCD common output
	SEG80	A			LCD segment output
P30	P30	I/O	Hi-Z	✓	I/O port
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	SEG79	A			LCD segment output
P31	P31	I/O	Hi-Z	✓	I/O port
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	SEG78	A			LCD segment output
P32	P32	I/O	Hi-Z	✓	I/O port
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	SEG77	A			LCD segment output
P33	P33	I/O	Hi-Z	✓	I/O port
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	SEG76	A			LCD segment output
P34	P34	I/O	Hi-Z	✓	I/O port
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	SEG75	A			LCD segment output
P35	P35	I/O	Hi-Z	✓	I/O port
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	SEG74	A			LCD segment output
P36	P36	I/O	Hi-Z	✓	I/O port
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	SEG73	A			LCD segment output
P37	P37	I/O	Hi-Z	✓	I/O port
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	SEG72	A			LCD segment output
PD0	DST2	O	O (L)	✓	On-chip debugger status output
	PD0	I/O			I/O port
	SEG71	A			LCD segment output

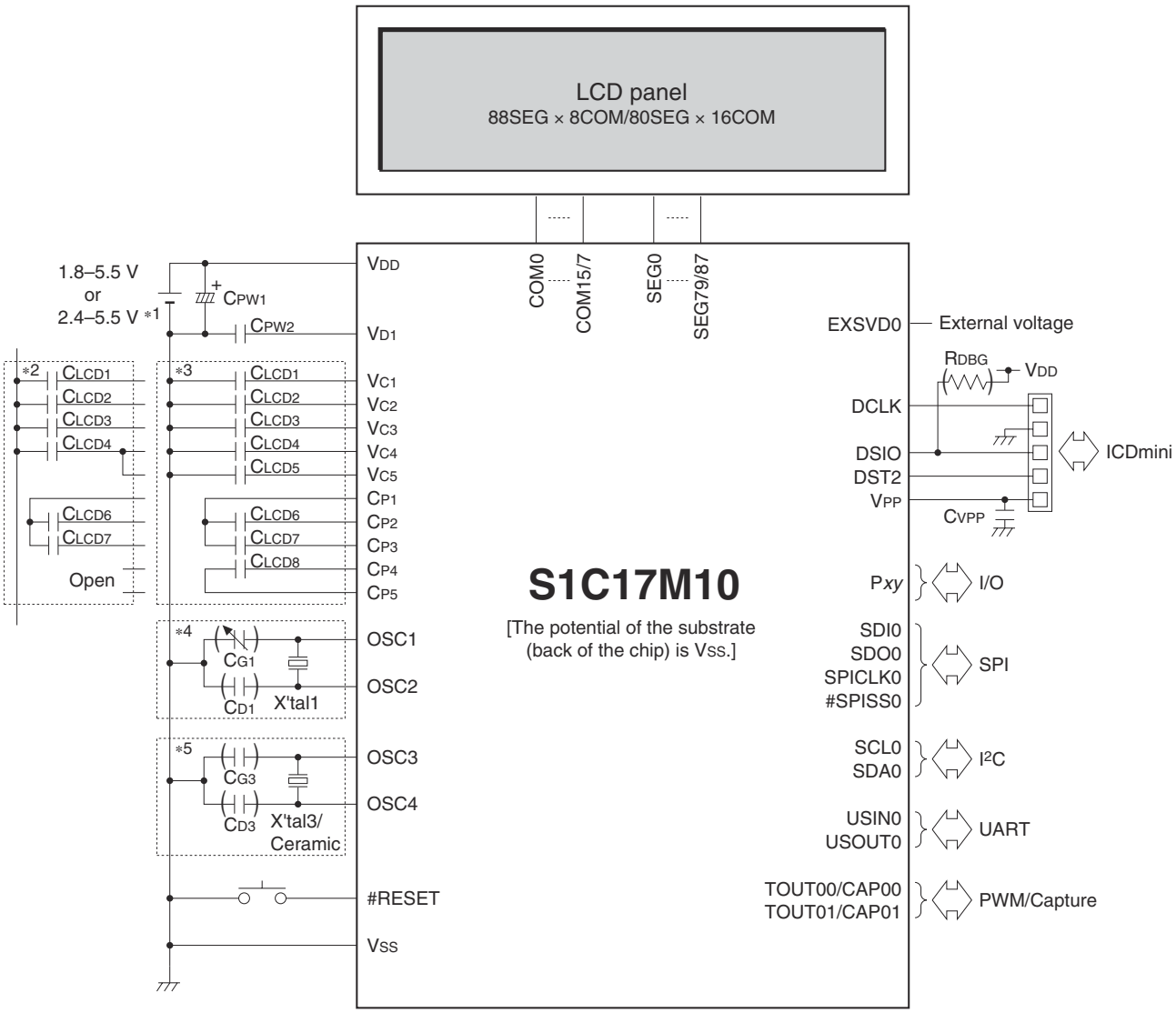
Pin/pad name	Assigned signal	I/O	Initial state	Tolerant fail-safe structure	Function
PD1	DSIO	I/O	I (Pull-up)	✓	On-chip debugger data input/output
	PD1	I/O			I/O port
	SEG70	A			LCD segment output
PD2	DCLK	O	O (H)	–	On-chip debugger clock output
	PD2	O			Output port
	SEG69	A			LCD segment output
PD3	PD3	I/O	Hi-Z	✓	I/O port
	OSC3	A			OSC3 oscillator circuit input
PD4	PD4	I/O	Hi-Z	✓	I/O port
	OSC4	A			OSC3 oscillator circuit output
COM0–8	COM0–8	A	Hi-Z	–	LCD common output
SEG0–68	SEG0–68	A	Hi-Z	–	LCD segment output

Universal port multiplexer (UPMUX)

The universal port multiplexer (UPMUX) allows software to select the peripheral circuit input/output function to be assigned to each pin from those listed below. Note, however, that a function cannot be assigned to two or more pins simultaneously.

Peripheral circuit	Signal to be assigned	I/O	Channel number *n*	Function
Synchronous serial interface (SPIA)	SDI*n*	I	*n* = 0	SPIA Ch.*n* data input
	SDO*n*	O		SPIA Ch.*n* data output
	SPICLK*n*	I/O		SPIA Ch.*n* clock input/output
	#SPISS*n*	I		SPIA Ch.*n* slave-select input
I^2C (I2C)	SCL*n*	I/O	*n* = 0	I2C Ch.*n* clock input/output
	SDA*n*	I/O		I2C Ch.*n* data input/output
UART (UART2)	USIN*n*	I	*n* = 0	UART2 Ch.*n* data input
	USOUT*n*	O		UART2 Ch.*n* data output
16-bit PWM timer (T16B)	TOUT*n*0/CAP*n*0	I/O	*n* = 0	T16B Ch.*n* PWM output/capture input 0
	TOUT*n*1/CAP*n*1	I/O		T16B Ch.*n* PWM output/capture input 1
Smart card interface (SMCIF)	SMCCLK*n*	I/O	*n* = 0	SMCIF Ch.*n* clock input/output
	SMCIO*n*	I/O		SMCIF Ch.*n* data input/output

■ BASIC EXTERNAL CONNECTION DIAGRAM



∗1: For Flash programming
∗2: When 1/4 bias is selected
∗3: When 1/5 bias is selected
∗4: When OSC1 crystal oscillator is selected
∗5: When OSC3 crystal/ceramic oscillator is selected
( ): Do not mount components if unnecessary.

S1C17M10

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