TPS62152-Q1 Automotive Wide Input, Fixed 3-V Output Voltage, 1-A Step-Down Converter in 3 × 3-mm QFN Package

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C4B
- DCS-Control Topology
- Input Voltage Range: 4 V to 17 V
- Up to 1-A Output Current
- Fixed Output Voltage: 3.3 V
- Programmable Soft Start and Tracking
- Seamless Power-Save Mode Transition
- Quiescent Current of 17 µA (Typ.)
- Selectable Operating Frequency
- Power-Good Output
- 100% Duty-Cycle Mode
- Short-Circuit Protection
- Overtemperature Protection
- Available in a 3-mm × 3-mm, VQFN-16 Package

2 Applications

- Automotive Infotainment and Cluster
  - Instrument Cluster
  - Center Stack
  - Head Unit
  - Rear-Seat Entertainment
- Advanced Driver-Assistance System (ADAS)
  - Surround View
  - Rear-View Camera
  - Front Camera

3 Description

The TPS62152-Q1 device is an easy-to-use synchronous step-down dc-dc converter optimized for applications with high power density and features a fixed 3.3-V output with a current capability of up to 1 A. A high switching frequency of 2.5 MHz (typical) allows the use of small inductors and provides fast transient response as well as high output-voltage accuracy by use of the DCS-Control topology.

With a wide operating input voltage range of 4 V to 17 V, the device is ideally suited for systems powered from either a Li-Ion or other batteries as well as from 12-V intermediate power rails.

The soft-start pin controls the output voltage start-up ramp, which allows operation either as a standalone power supply or in tracking configurations. Power sequencing is also possible by configuring the enable and open-drain power-good pins.

In power-save mode, the device draws quiescent current of about 17 µA from VIN. Power-save mode, entered automatically and seamlessly if the load is small, maintains high efficiency over the entire load range. Entering shutdown mode turns the device off, and shutdown current consumption is less than 2 µA.

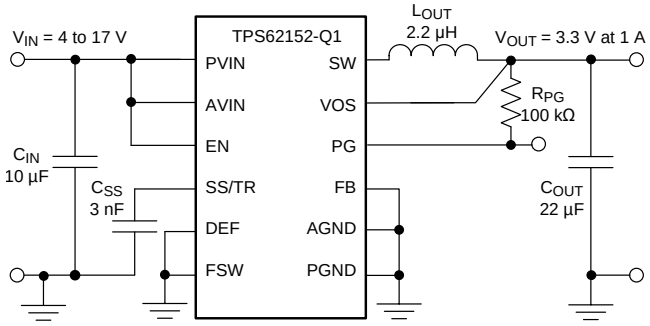
The device package is a 16-pin VQFN measuring 3-mm × 3-mm (RGT) and has an exposed thermal pad for better thermal performance.

Device Information(1)

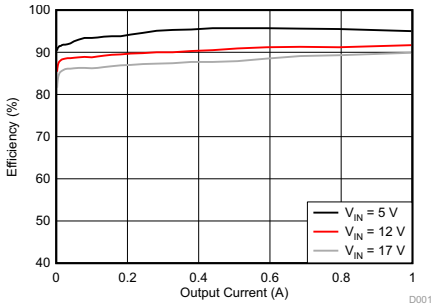
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS62152-Q1	VQFN (16)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application



Efficiency Vs Output Current



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (July 2013) to Revision B — **Page**

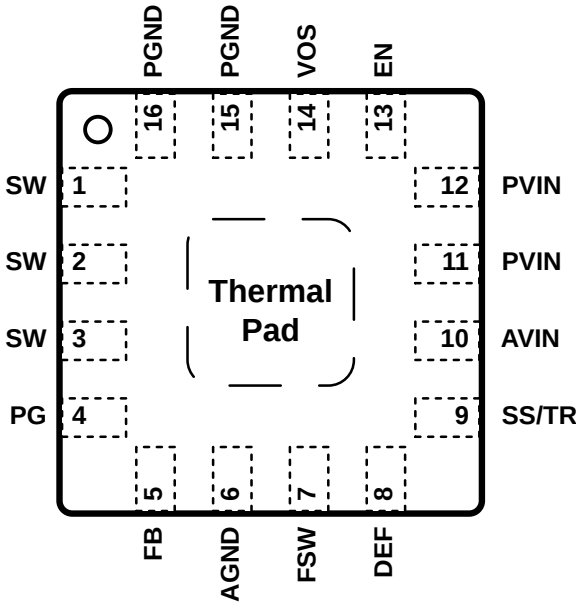
- Changed output voltage in the *Features* section ... 1
- Changed output voltage in second paragraph of the *Description* section ... 1
- Added the *ESD Ratings* table, *Feature Description* section, *Programming* section, *Application and Implementation* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed the minimum supply voltage value from 3 to 4 in the *Recommended Operating Conditions* table ... 4
- Added the capacitor and inductor parameters to the *Recommended Operating Conditions* table ... 4
- Changed the minimum input voltage value from 3 to 4 in the *Electrical Characteristics* table ... 5
- Deleted all references to the TPS62150-Q1 device and adjustable output versions ... 5
- Changed the values of the output voltage range parameter in the *Electrical Characteristics* from 0.9 (min) and 6 (max) to 3.3 (typ) ... 5
- Added inductor and capacitor values to some of the graphs in the *Typical Characteristics* section ... 6
- Deleted empty rows 0.47 µH and 4.7 µH and columns for 4.7 µF and 400 µF from the *L-C Output Filter Combinations* table ... 18

Changes from Original (July 2013) to Revision A — **Page**

- Device going from Product Preview to Production Data. ... 1
- Deleted T_J from Recommended Operating Conditions table. ... 4

5 Pin Configuration and Functions

RGT Package
16-Pin VQFN With Exposed Thermal Pad
Top View



Pin Functions

PIN[1]		TYPE[2]	DESCRIPTION
NAME	NO.		
AGND	6	G	Analog ground. Connected AGND directly to the exposed thermal pad and common ground plane.
AVIN	10	S	Supply voltage for control circuitry. Connect to the same source as PVIN.
DEF	8	I	Output voltage scaling (Low = nominal, High = nominal + 5%)[3]
EN	13	I	Enable input (High = enabled, Low = disabled)[3]
FB	5	I	TI recommends connecting FB to AGND for improved thermal performance.
FSW	7	I	Switching frequency select (Low ≈ 2.5 MHz, High ≈ 1.25 MHz[4] for typical operation)[3]
PG	4	O	Output power good (High = VOUT ready, Low = VOUT below nominal regulation); open drain (requires pullup resistor; goes high-impedance when device is switched off)
PGND	15	G	Power ground. Must be connected directly to the exposed thermal pad and common ground plane.
	16		
PVIN	11	S	Supply voltage for power stage. Connect to same source as AVIN.
	12		
SS/TR	9	I	Soft-start or tracking pin. An external capacitor connected to this pin sets the internal voltage-reference rise time. The pin can be used for tracking and sequencing.
SW	1	O	Switch node, which is connected to the internal MOSFET switches. Connect inductor between SW and output capacitor.
	2		
	3		
VOS	14	I	Output-voltage sense pin and connection for the control-loop circuitry.
Exposed thermal pad		—	Connect to AGND (pin 6), PGND (pins 15,16) and common ground plane[5]. Solder to PCB to achieve appropriate power dissipation and mechanical reliability.

(1) For more information about connecting pins, see *Detailed Description* and *Application Information* sections.
(2) G = ground, S = supply, I = input, O = output
(3) An internal pulldown resistor keeps the logic level low, if the pin is floating.
(4) Connect FSW to VOUT or PG in this case.
(5) See Figure 37.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Pin voltage range(2)	AVIN, PVIN	–0.3	20	V
	EN, SS/TR	–0.3	V_{IN} + 0.3	
	SW	–0.3	V_{IN} + 0.3	
	DEF, FSW, FB, PG, VOS	–0.3	7	
Power-good sink current	PG		10	mA
Operating junction temperature, T_J		–40	125	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network ground terminal.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins (1, 4, 5, 8, 9, 12, 13, 16)	±750	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Supply voltage at AVIN and PVIN(1)	4	17	V
C_{IN}	Input filter capacitor	10		µF
C_{OUT}	Output buffer capacitor	10		µF
L_{OUT}	Output inductor	1	3.3	µH
T_A	Operating free air temperature	–40	125	°C

(1) The device is still functional down to the undervoltage lockout (see the V_{UVLO} parameter in the *Electrical Characteristics* table).

6.4 Thermal Information

THERMAL METRIC(1)		TPS62152-Q1 RGT (VQFN) 16 Pins	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	45	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	17.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over free-air temperature range (T_A= –40°C to 125°C), typical values at VIN = AVIN = PVIN = 12 V and T_A = 25°C (unless otherwise noted)

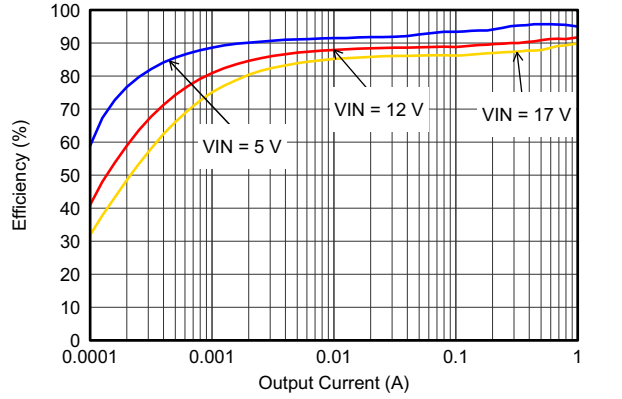
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN}	Input voltage range(1)		4		17	V
I_Q	Operating quiescent current	EN = High, I_{OUT} = 0 mA, device not switching		17	25	µA
I_{SD}	Shutdown current(2)	EN = Low		1.5	4	µA
V_{UVLO}	Undervoltage lockout threshold	Falling input voltage	2.6	2.7	2.8	V
		Hysteresis		200		mV
T_{SD}	Thermal shutdown temperature			160		°C
	Thermal shutdown hysteresis			20		°C
CONTROL (EN, DEF, FSW, SS/TR, PG)						
V_H	High-level input threshold voltage (EN, DEF, FSW)		0.9			V
V_L	Low-level input threshold voltage (EN, DEF, FSW)				0.3	V
I_{LKG}	Input leakage current (EN, DEF, FSW)	EN = V_{IN} or GND; DEF, FSW = V_{OUT} or GND		0.01	1	µA
V_{TH_PG}	Power-good threshold voltage	Rising (%V_{OUT})	92%	95%	98%	
		Falling (%V_{OUT})	87%	90%	94%	
V_{OL_PG}	Power-good output low	I_{PG} = –2 mA		0.07	0.3	V
I_{LKG_PG}	Input leakage current (PG)	V_{PG} = 1.8 V		1	400	nA
$I_{SS/TR}$	SS/TR pin source current		2.3	2.5	2.7	µA
POWER SWITCH						
$R_{DS(ON)}$	High-side MOSFET on-resistance	V_{IN} ≥ 6 V		90	170	mΩ
		V_{IN} = 3 V		120		
	Low-side MOSFET on-resistance	V_{IN} ≥ 6 V		40	70	
		V_{IN} = 3 V		50		
I_{LIMF}	High-side MOSFET forward current limit(3)	V_{IN} = 12 V, T_A= 25°C	1.4	1.7	2.2	A
OUTPUT						
VREF	Internal reference voltage(4)			0.8		V
I_{LKG_FB}	Input leakage current (FB)	V_{FB} = 0.8 V		1	100	nA
V_{OUT}	Output voltage range	V_{IN} ≥ V_{OUT}		3.3		V
	DEF (Output voltage programming)	DEF = 0 (GND)		V_{OUT}		V
		DEF = 1 (V_{OUT})		V_{OUT} + 5%		
	Initial output voltage accuracy(5)	PWM mode operation, V_{IN} ≥ V_{OUT} + 1 V	–1.8%		1.8%	
		Power-save mode operation, C_{OUT} = 22 µF	–2.3%		2.8%	
	Load regulation(6)	V_{IN} = 12 V, V_{OUT} = 3.3 V, PWM mode operation		0.05		%/A
	Line regulation(6)	3 V ≤ V_{IN} ≤ 17 V, V_{OUT} = 3.3 V, I_{OUT} = 1 A, PWM mode operation		0.02		%/V

(1) The device is still functional down to undervoltage lockout (see parameter V_{UVLO}).
(2) Current into AVIN + PVIN pin
(3) This is the static current limit. It can be temporarily higher in applications because of internal propagation delay (see *Current-Limit and Short-Circuit Protection* section).
(4) This is the voltage regulated at the FB pin.
(5) This is the accuracy provided by the device itself (line and load regulation effects are not included). The (internal) resistive divider is included.
(6) Line and load regulation depend on external component selection and layout (see Figure 5 and Figure 6).

6.6 Typical Characteristics

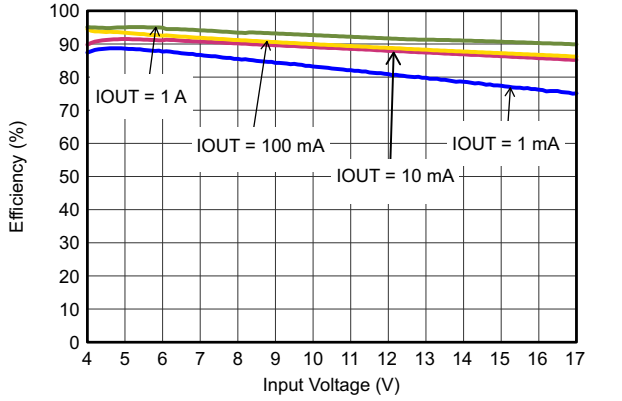
Table 1. Table of Graphs

DESCRIPTION		FIGURE
Efficiency	vs Output Current	Figure 1, Figure 3
	vs Input Voltage	Figure 2, Figure 4
Output Voltage Accuracy	Load Regulation	Figure 5
	Line Regulation	Figure 6
Switching Frequency	vs Input Voltage	Figure 7
	vs Output Current	Figure 8
Input Quiescent Current	vs Input voltage	Figure 9
Input Shutdown Current	vs Input voltage	Figure 10
High-Side Static Drain-Source-Resistance (R_{DSon})	vs Input voltage	Figure 11
Low-Side Static Drain-Source-Resistance (R_{DSon})	vs Input voltage	Figure 12
Output Voltage Ripple	vs Output Current	Figure 13
Output Current	vs Input Voltage	Figure 14
Power-Supply Rejection Ratio	vs Frequency	Figure 15, Figure 16
PWM-PSM-Transition		Figure 17
Load Transient Response		Figure 18
Load Transient Response	Rising Edge	Figure 19
	Falling Edge	Figure 20
Startup	Into 100 mA	Figure 21
	Into 1 A	Figure 22
Typical Operation in PWM Mode		Figure 23
Typical Operation in Power Save Mode		Figure 24



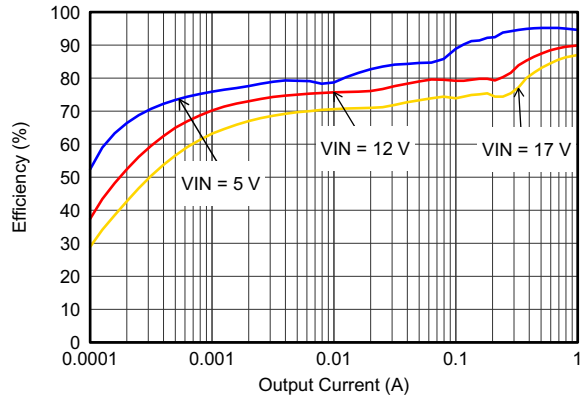
FSW = 1.25 MHz L = 2.2 µH (XFL4020) C_{OUT} = 22 µF
C_{IN} = 10 µF

Figure 1. Efficiency vs Output Current for Different Input Voltages



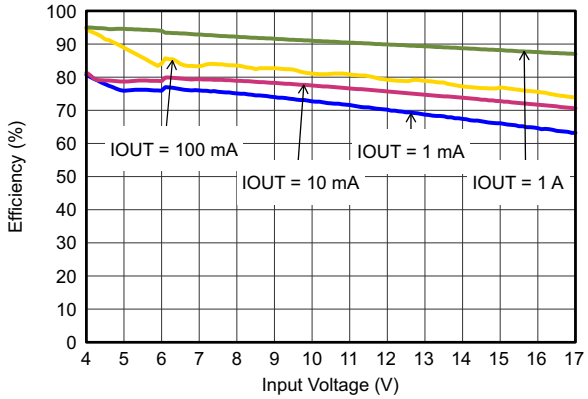
FSW = 1.25 MHz L = 2.2 µH (XFL4020) C_{OUT} = 22 µF
C_{IN} = 10 µF

Figure 2. Efficiency vs Input Voltage for Different Output Currents



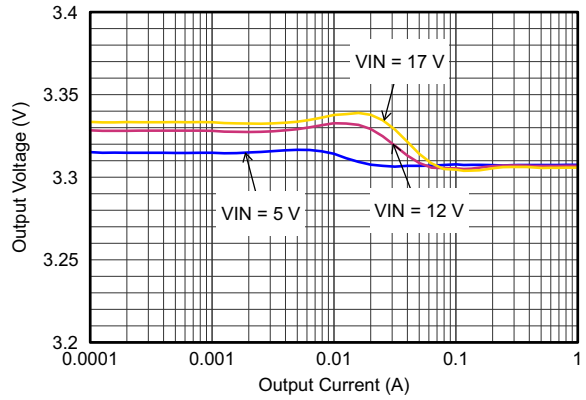
FSW = 2.5 MHz L = 2.2 µH (XFL4020) C_{OUT} = 22 µF
C_{IN} = 10 µF

Figure 3. Efficiency vs Output Current for Different Input Voltages



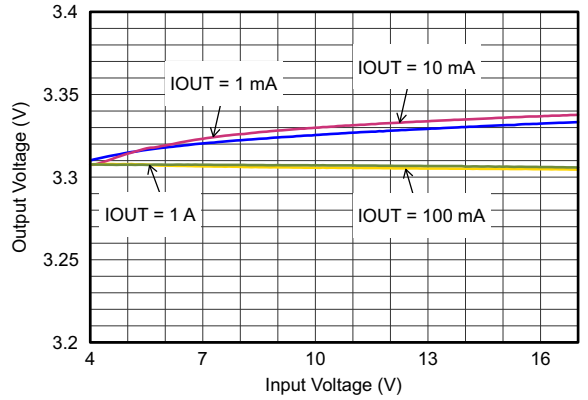
FSW = 2.5 MHz L = 2.2 µH (XFL4020) C_{OUT} = 22 µF
C_{IN} = 10 µF

Figure 4. Efficiency vs Input Voltage for Different Output Currents



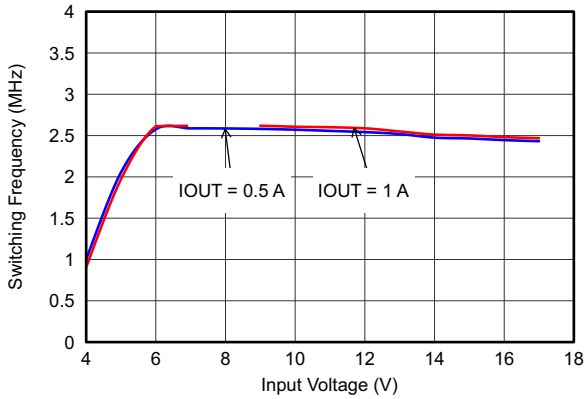
L = 2.2 µH (XFL4020) C_{OUT} = 22 µF C_{IN} = 10 µF

Figure 5. Output Voltage Accuracy (Load Regulation)



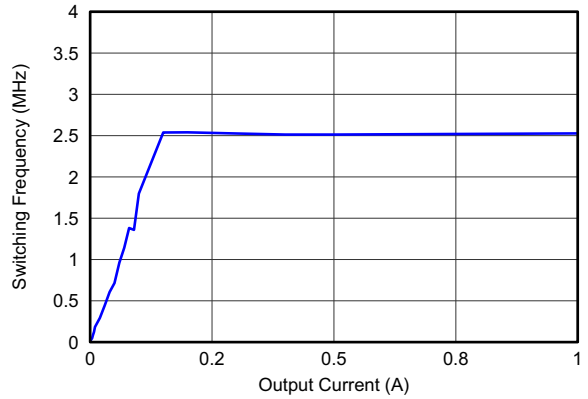
L = 2.2 µH (XFL4020) C_{OUT} = 22 µF C_{IN} = 10 µF

Figure 6. Output Voltage Accuracy (Line Regulation)



L = 2.2 µH (XFL4020) C_{OUT} = 22 µF C_{IN} = 10 µF

Figure 7. Switching Frequency vs Input Voltage



FSW = Low L = 2.2 µH (XFL4020) C_{OUT} = 22 µF
C_{IN} = 10 µF

Figure 8. Switching Frequency vs Output Current

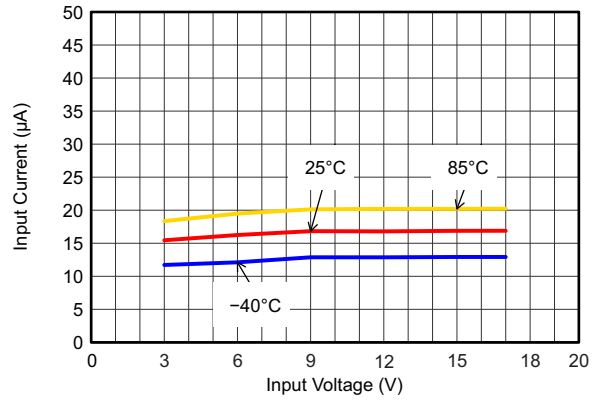


Figure 9. Input Quiescent Current vs Input Voltage

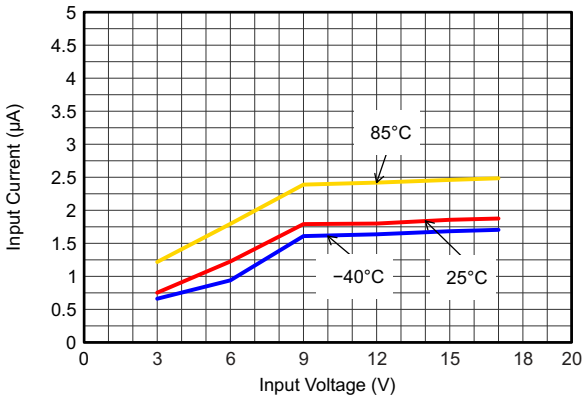


Figure 10. Input Shutdown Current vs Input Voltage

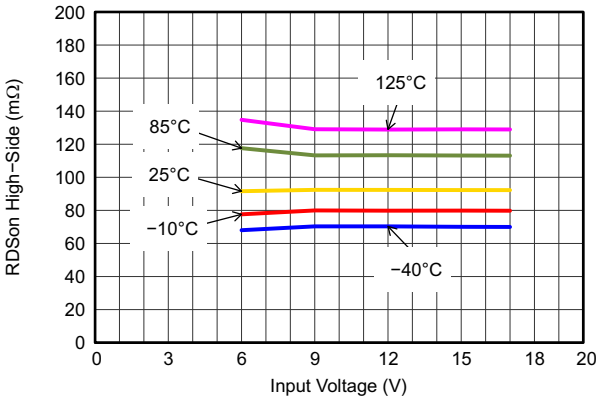


Figure 11. High-Side Static Drain-Source-Resistance (R_{DSon}) vs Input Voltage

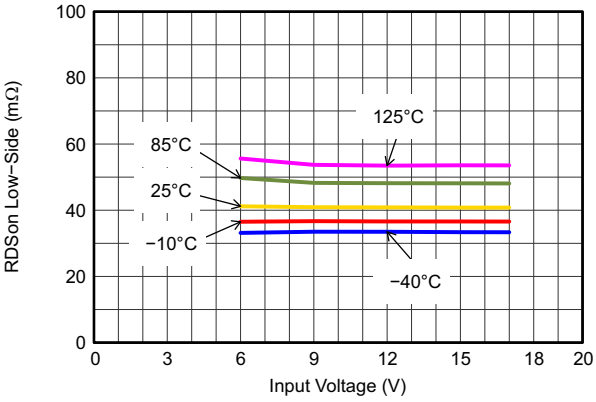


Figure 12. Low-Side Static Drain-Source-Resistance (R_{DSon}) vs Input Voltage

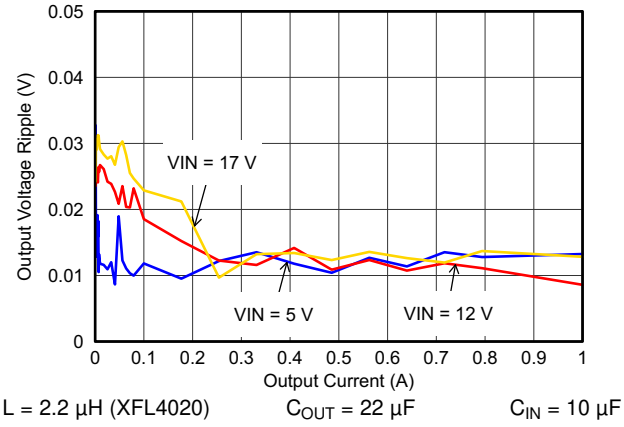


Figure 13. Output Voltage Ripple vs Output Current

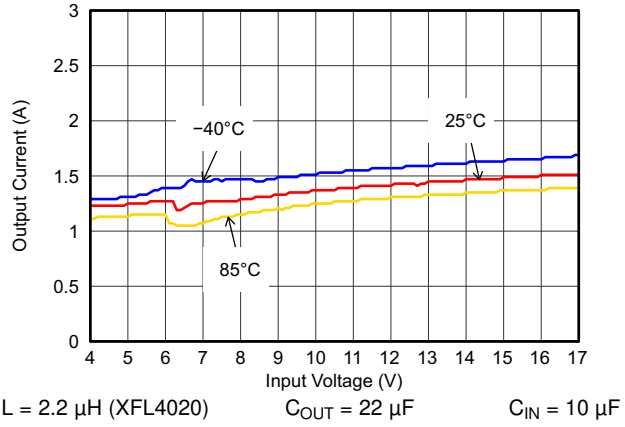
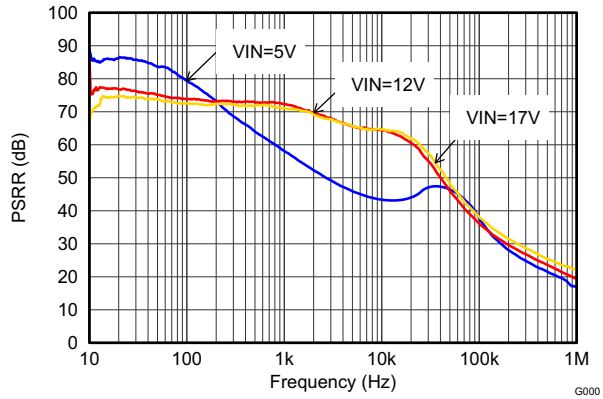
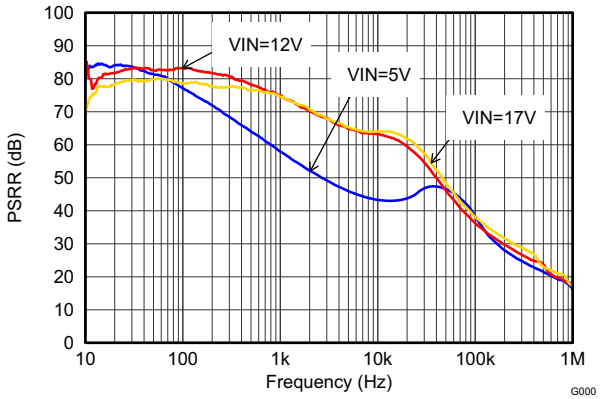


Figure 14. Output Current vs Input Voltage



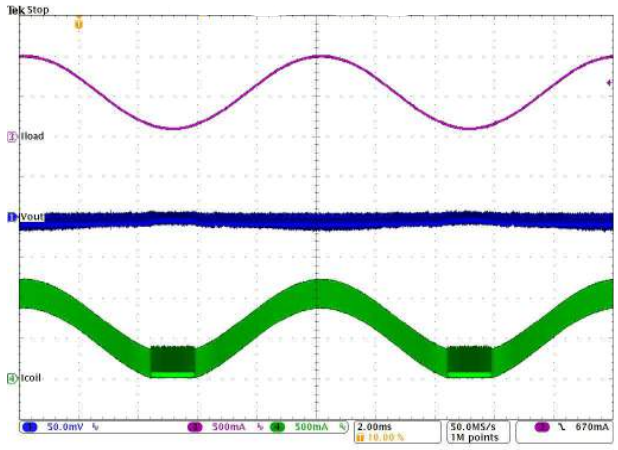
FSW = 2.5 MHz L = 2.2 µH (XFL4020) C_{OUT} = 22 µF
C_{IN} = 10 µF

Figure 15. Power-Supply Rejection Ratio vs Frequency



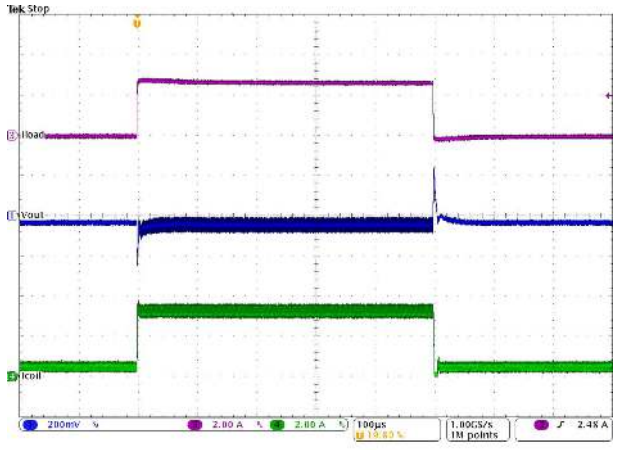
FSW = 2.5 MHz L = 2.2 µH (XFL4020) C_{OUT} = 22 µF
C_{IN} = 10 µF

Figure 16. Power-Supply Rejection Ratio vs Frequency



V_{IN} = 12 V With 50 mV/div

Figure 17. PWM-PSM-Transition



V_{IN} = 12 V I_{OUT} = 0 to 5 A and back to 0 A

Figure 18. Load Transient Response

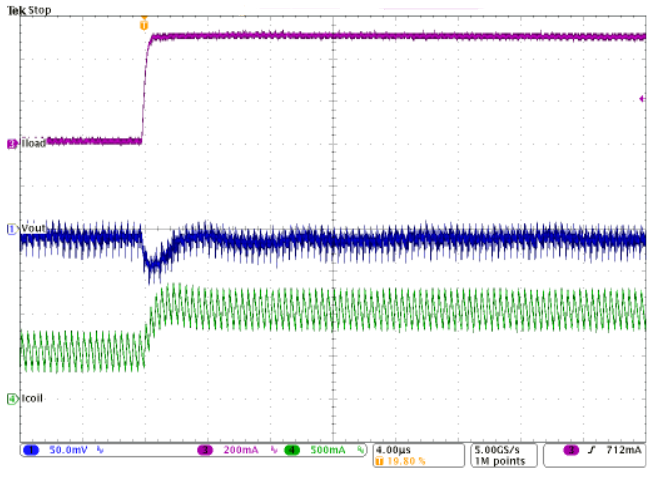


Figure 19. Load Transient Response of Figure 18, Rising Edge

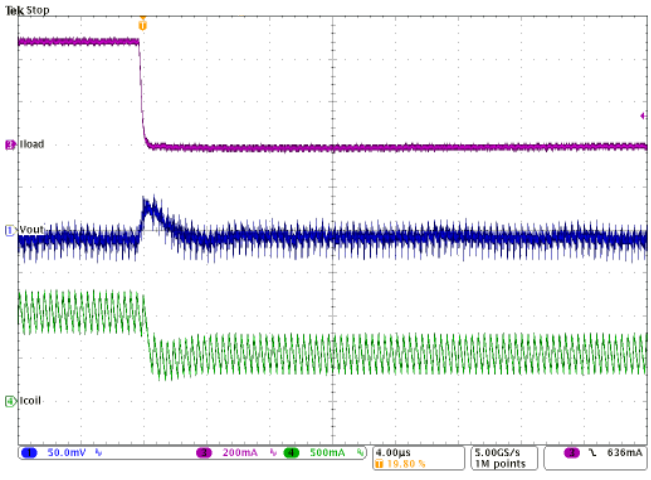
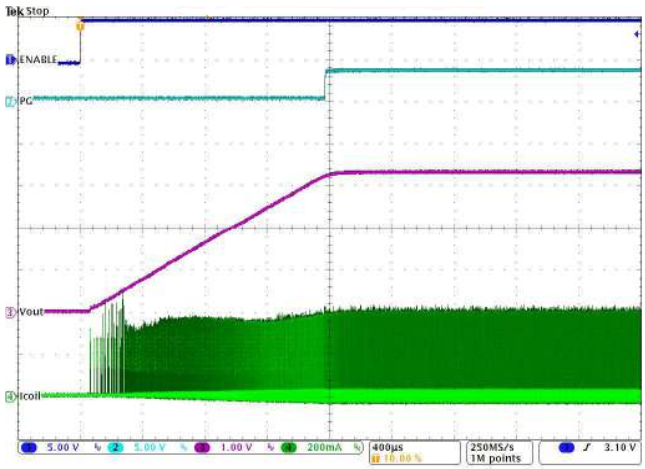
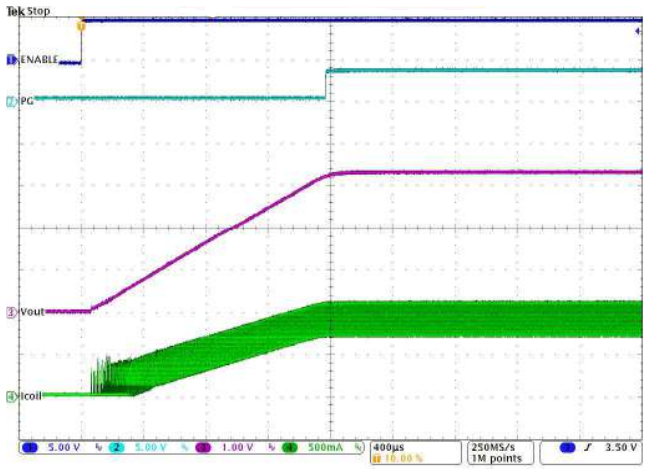


Figure 20. Load Transient Response of Figure 18, Falling Edge



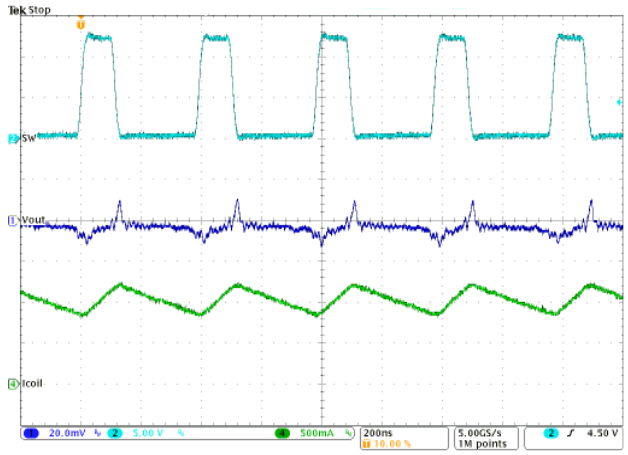
V_{IN} = 12 V

Figure 21. Startup into 100 mA



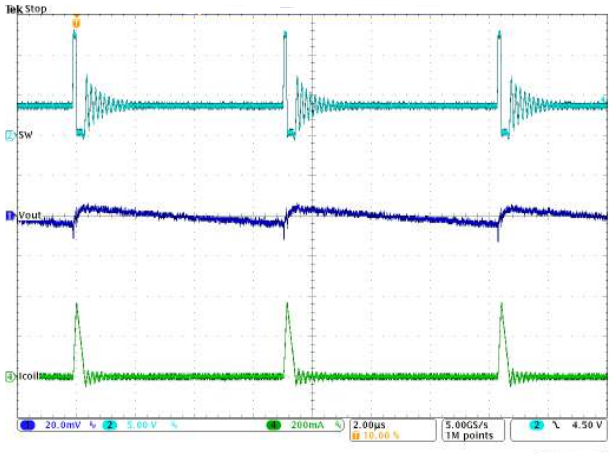
V_{IN} = 12 V

Figure 22. Startup into 1 A



I_{OUT} = 1 A

Figure 23. Typical Operation in PWM Mode



I_{OUT} = 10 mA

Figure 24. Typical Operation in Power Save Mode

7 Detailed Description

7.1 Overview

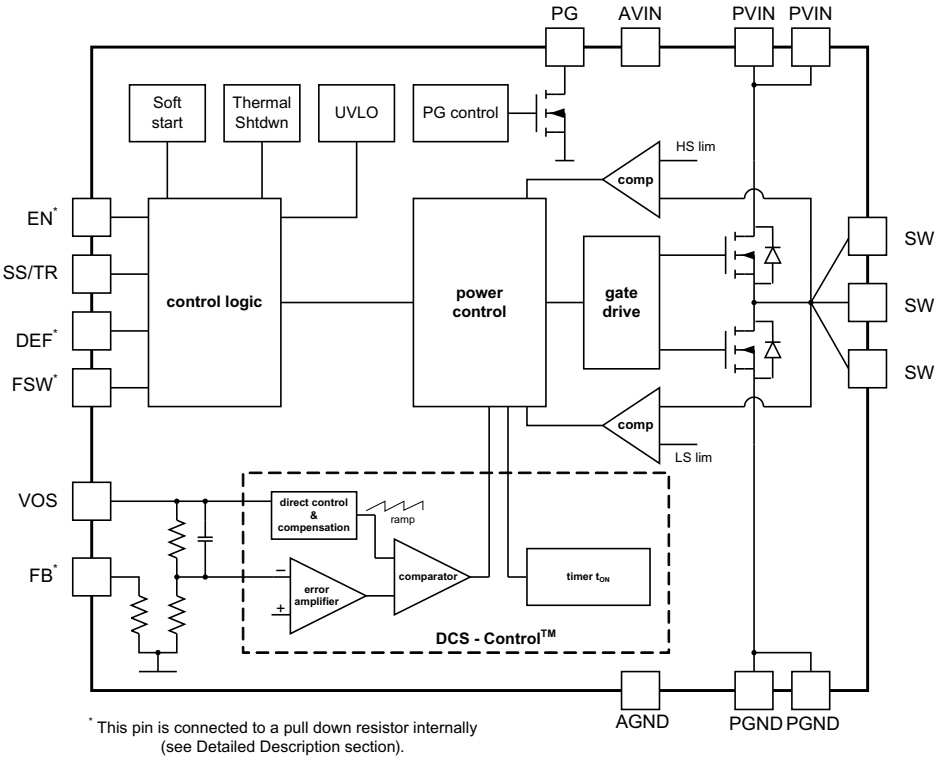
The base for the TPS62152-Q1 synchronous switched-mode power converters is the DCS-Control™ topology (direct control with seamless transition into power-save mode), an advanced regulation topology that combines the advantages of hysteretic, voltage-mode and current mode control including an ac loop directly associated to the output voltage. This control loop takes information about output voltage changes and feeds it directly to a fast comparator stage. The control loop sets the switching frequency, which is constant for steady-state operating conditions, and provides immediate response to dynamic load changes. A voltage feedback loop obtains accurate dc load regulation. The internally compensated regulation network achieves fast and stable operation with small external components and low-ESR capacitors.

The DCS-Control topology supports pulse-width modulation (PWM) mode for medium and heavy load conditions and a power save-mode at light loads. During PWM, the device operates at the nominal switching frequency in continuous-conduction mode. This frequency is typically about 2.5 MHz, with a controlled frequency variation depending on the input voltage. If the load current decreases, the converter enters power-save mode to sustain high efficiency down to very light loads. In power-save mode, the switching frequency decreases linearly with the load current. Because DCS-Control topology supports both operation modes within one single building block, the transition from PWM to power-save mode is seamless, without effects on the output voltage.

Because the TPS62152-Q1 device has a fixed output voltage of 3.3 V, the device provide smallest solution size and lowest current consumption, requiring only three external components. An internal current limit supports nominal output currents of up to 1 A.

The TPS62152-Q1 device offers both excellent dc voltage and superior load-transient regulation, combined with very low output-voltage ripple, minimizing interference with RF circuits.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Pulse-Width Modulation (PWM) Operation

The TPS62152-Q1 device operates with pulse-width modulation in continuous conduction mode (CCM) with a nominal switching frequency of 2.5 MHz or 1.25 MHz, selectable with the FSW pin. The frequency variation in PWM is controlled and depends on V_{IN}, V_{OUT} and the inductance. The device operates in PWM mode as long the output current is higher than half the inductor ripple current. To maintain high efficiency at light loads, the device enters power-save mode at the boundary to discontinuous-conduction mode (DCM). This happens if the output current becomes smaller than half the inductor ripple current.

7.3.2 100% Duty-Cycle Operation

D = VOUT / VIN gives the duty cycle of the buck converter, which increases as the input voltage comes close to the output voltage. In this case, the device starts 100% duty-cycle operation, turning on the high-side switch 100% of the time. The high-side switch stays turned on as long as the output voltage is below the internal set point. This allows the conversion of small input-to-output voltage differences, for example, for longest operation time of battery-powered applications. In 100% duty-cycle mode, the low-side FET switches off.

The calculation for minimum input voltage to maintain output voltage regulation, depending on the load current and the output voltage level, is:

$$V_{IN(min)} = V_{OUT(min)} + I_{OUT}\left(R_{DS(on)} + R_L\right) \quad (1)$$

where

- I_{OUT} is the output current
- $R_{DS(on)}$ is the on resistance of the high-side FET
- R_L is the DC resistance of the inductor used

7.3.3 Enable / Shutdown (EN)

Setting enable (EN) High starts operation of the device.

Pulling EN Low forces shutdown, with a shutdown current of typically 1.5 µA. The shutdown state turns off the internal power MOSFETs as well as the entire control circuitry. The internal resistive divider pulls down the output voltage smoothly. An internal pulldown resistor of about 400 kΩ is connected and keeps EN logic low, if the pin is floating. Driving the pin High disconnects the pulldown.

Connecting the EN pin to an appropriate output signal of another power rail provides sequencing of multiple power rails.

7.3.4 Soft Start or Tracking (SS/TR)

The internal soft-start circuitry controls the output voltage slope during start-up. This control avoids excessive inrush current, ensures a controlled output-voltage rise time, and prevents unwanted voltage drops from high-impedance power sources or batteries. On setting EN to start device operation, the device begins switching after a delay of about 50 µs and VOUT rises with a slope controlled by an external capacitor connected to the SS/TR pin. See Figure 21 and Figure 22 for typical start-up operation.

Connecting SS/TR directly to AVIN provides fastest start-up behavior. The TPS62152-Q1 device can start into a pre-biased output. During monotonic pre-biased start-up, neither power MOSFET turns on until the internal ramp of the device sets an output voltage above the pre-bias voltage. If EN = GND, setting the device to shutdown, or the device is in undervoltage lockout or thermal shutdown, an internal resistor pulls the SS/TR pin down to ensure a proper low level. Returning from those shutdown states causes a new start-up sequence as set by the SS/TR connection.

The device can track a master voltage supplied to SS/TR. The output voltage follows this voltage in both directions, up and down (see the *Application Information* section).

Feature Description (continued)

7.3.5 Current-Limit and Short-Circuit Protection

The TPS62152-Q1 device has protection against heavy loads and short-circuit events. At heavy loads, the current limit determines the maximum output current. On reaching the current limit, the high-side FET turns off. To avoid shoot-through current, the low-side FET switches on to sink the inductor current. The high-side FET turns on again only if the current in the low-side FET has decreased below the low-side current-limit threshold.

The current limit (see the *Electrical Characteristics* table) restricts the output current of the device. Because of internal propagation delay, the actual current can exceed the static current limit during this propagation delay time. The calculation for the dynamic current limit is as follows:

$$I_{peak(typ)} = I_{LIMF} + \frac{V_L}{L} \times t_{PD}$$

where

- I_{LIMF} is the static current limit, specified in the *Electrical Characteristics* table
- V_L is the voltage across the inductor ($V_{IN} - V_{OUT}$)
- L is the inductor value
- t_{PD} is the internal propagation delay (2)

The current limit can exceed static values, especially if the input voltage is high and the circuit uses very small inductances. The calculation for the peak current in the dynamic high-side switch is as follows:

$$I_{peak(typ)} = I_{LIMF} + \frac{\left(V_{IN} - V_{OUT}\right)}{L} \times 30\ ns \quad (3)$$

7.3.6 Power Good (PG)

The TPS62152-Q1 device has a built-in power-good (PG) function to indicate whether the output voltage has reached its appropriate level or not. One use of the PG signal is for start-up sequencing of multiple rails. The PG pin is an open-drain output that requires a pullup resistor to any voltage below 7 V. The pin can sink 2 mA of current and maintain its specified logic-low level. The pin is high-impedance when EN, UVLO, or thermal shutdown turns the device off. The TPS62152-Q1 device features PG = Low in this case and can be used to actively discharge VOUT. The V_{IN} voltage must remain present for the PG pin to stay Low.

7.3.7 Pin-Selectable Output Voltage (DEF)

Setting the DEF pin to High can increase the output voltage of the TPS62152-Q1 device by 5% above the nominal voltage (the maximum allowed voltage is 7 V; therefore, TI recommends connecting the DEF pin to VOUT or PG, not VIN). When DEF is Low, the device regulates to the nominal output voltage. Increasing the nominal voltage allows adapting the power supply voltage to the variations of the application hardware. See *Voltage Margining Using the TPS62130*, SLVA489, for detailed information on voltage margining using the TPS62152-Q1 device. A pulldown resistor of about 400 kΩ internally connects to the pin, to ensure a proper logic level if the pin is high-impedance or floating after initially set to Low. Setting the pin to High disconnects the resistor.

7.3.8 Frequency Selection (FSW)

To get high power density with a very small solution size, a high switching frequency allows the use of small external components for the output filter. However, switching losses increase with the switching frequency. If efficiency is the key parameter, more than solution size, set the switching frequency to half (1.25 MHz typical) by pulling FSW to High. It is mandatory to start with FSW = Low to limit inrush current. Connecting the pin to VOUT or PG is one way to ensure FSW = Low at start-up. Running with lower frequency achieves higher efficiency, but also creates higher output-voltage ripple. Pull FSW to Low for high frequency operation (2.5 MHz typical). To get low ripple and full output current at the lower switching frequency, TI recommends using an inductor of at least 2.2 µH. The device accommodates a change of switching frequency during operation, if needed. A pulldown resistor of about 400 kΩ internally connects to the pin, acting the same way as at the DEF pin (see *Pin-Selectable Output Voltage (DEF)*).

Feature Description (continued)

7.3.9 Undervoltage Lockout (UVLO)

If the input voltage drops, the undervoltage lockout prevents improper operation of the device by switching off both the power FETs. The typical setting of the undervoltage lockout threshold is 2.7 V. The device is fully operational for voltages above the UVLO threshold and turns off if the input voltage trips the threshold. The converter starts operation again once the input voltage exceeds the threshold by a hysteresis of typically 200 mV.

7.3.10 Thermal Shutdown

An internal temperature sensor monitors the junction temperature (T_J) of the device. If T_J exceeds 160°C (typ), the device goes into thermal shutdown. Both the high-side and low-side power FETs turn off, and PG goes into the high-impedance state. When T_J decreases below the hysteresis amount, the converter resumes normal operation, beginning with soft start. To avoid unstable conditions, the device implements a hysteresis of typically 20°C on the thermal shutdown temperature.

7.3.11 Tracking Function

For implementing a tracking function, use the SS/TR pin for this purpose by connecting it to an external tracking voltage. The output voltage tracks the external tracking voltage. If the tracking voltage is between 50 mV and 1.2 V, the FB pin tracks the SS/TR pin voltage as described in Equation 4 and shown in Figure 25.

$$V_{FB} \approx 0.64 \times V_{SS/TR} \quad (4)$$

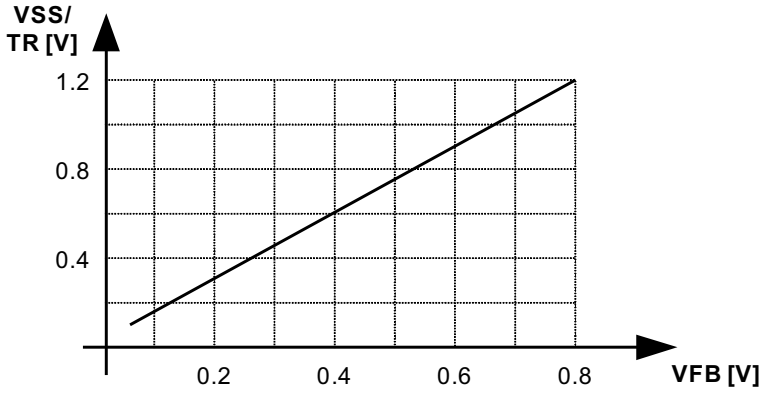


Figure 25. Voltage Tracking Relationship

When the SS/TR pin voltage reaches about 1.2 V, a clamp locks the internal voltage to the internal feedback voltage, and the device goes to normal regulation. This process works for rising and falling tracking voltages with the same behavior, as long as the input voltage is within the recommended operating conditions. For decreasing SS/TR pin voltage, the device does not sink current from the output. So, the resulting decrease of the output voltage may be slower than the SS/TR pin voltage if the load is light. When driving the SS/TR pin with an external voltage, do not exceed the voltage rating of the SS/TR pin, which is V_{IN} + 0.3 V.

If the input voltage drops into undervoltage lockout or even down to zero, the output voltage goes to zero, independent of the tracking voltage. Figure 26 shows how to connect devices to get ratiometric and simultaneous sequencing by using the tracking function.

Feature Description (continued)

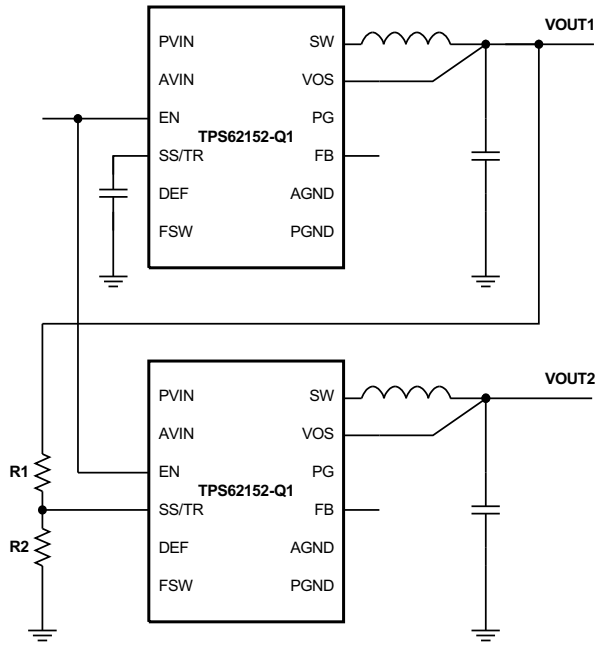


Figure 26. Sequence for Ratiometric and Simultaneous Start-Up

The resistive divider of R1 and R2 can be used to change the ramp rate of VOUT2 faster, slower, or the same as VOUT1.

To achieve a sequential start-up, connect the PG pin of VOUT1 to the EN pin of VOUT2. A ratiometric start-up sequence happens if both supplies share the same soft-start capacitor. Equation 10 calculates the soft-start time, though this circuit arrangement requires doubling the SS/TR current. See *TPS62130/40/50 Sequencing and Tracking*, SLVA470, for details about these and other tracking and sequencing circuits.

NOTE

If the voltage at the FB pin is below its typical value of 0.8 V, the output voltage accuracy may have a wider tolerance than specified.

7.3.12 Feedback Pin (FB)

The FB pin is pulled down internally and may be left floating. Connecting to AGND to improve thermal resistance is recommended.

7.4 Device Functional Modes

7.4.1 Power-Save Mode Operation

If the load current decreases, the TPS62152-Q1 device enters the built-in power-save mode seamlessly. This transition secures a high efficiency in light load operation. The device remains in power-save mode as long as the inductor current is discontinuous.

In power-save mode, the switching frequency decreases linearly with the load current, maintaining high efficiency. The transition into and out of power-save mode happens within the entire regulation scheme and is seamless in both directions.

The TPS62152-Q1 device includes a fixed on-time circuitry. The calculation for estimated on-time, in steady-state operation, is:

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times 400\ ns \tag{5}$$

For very small output voltages, the device keeps an absolute minimum on-time of about 80 ns to limit switching losses, thereby reducing the operating frequency from its nominal value, which keeps efficiency high. Use t_{ON} in Equation 6 to approximate the typical peak inductor current in power-save mode.

$$I_{LPSM(peak)} = \frac{(V_{IN} - V_{OUT})}{L} \times t_{ON} \tag{6}$$

When V_{IN} decreases to typically 15% above V_{OUT}, the TPS62152-Q1 device does not enter power-save mode, regardless of the load current. The device maintains output regulation in PWM mode.

7.4.2 Active Output Discharge

The TPS62152A-Q1 pulls the PG pin Low, when the device is shut down by EN, UVLO, or thermal shutdown. Connecting PG to VOUT through a resistor can be used to discharge VOUT in those cases (see Figure 27). The discharge rate can be adjusted by R_{PG}, which is also used to pull up the PG pin in normal operation. For reliability, keep the maximum current into the PG pin less than 10 mA.

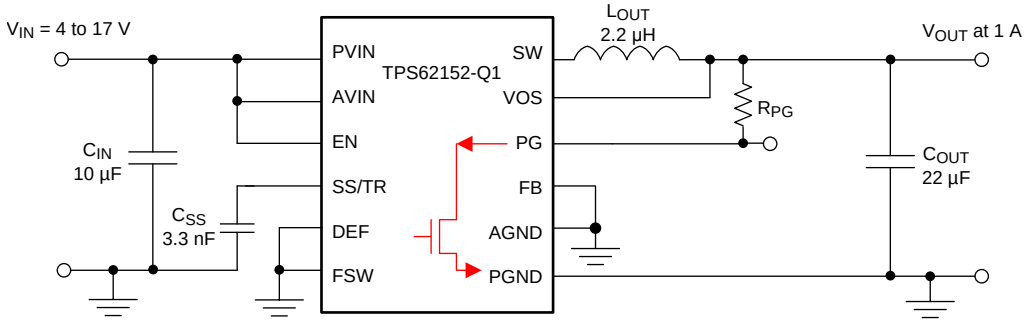


Figure 27. Active Output Discharge Through PG Pin

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS62152-Q1 device is an automotive wide-input, synchronous step-down, DC-DC converter with a 3.3-V fixed output voltage and an output current of up to 1 A. The device can be used in buck-converter applications with an input range from 4 V to 17 V. The TPS62152-Q1 device is optimized for space constrained applications and consumes 17-µA (typical) current in power-save mode. Selectable switching frequency (1.25 MHz or 2.25 MHz) allows regulator design to be optimized for efficiency or solution size.

8.2 Typical Application

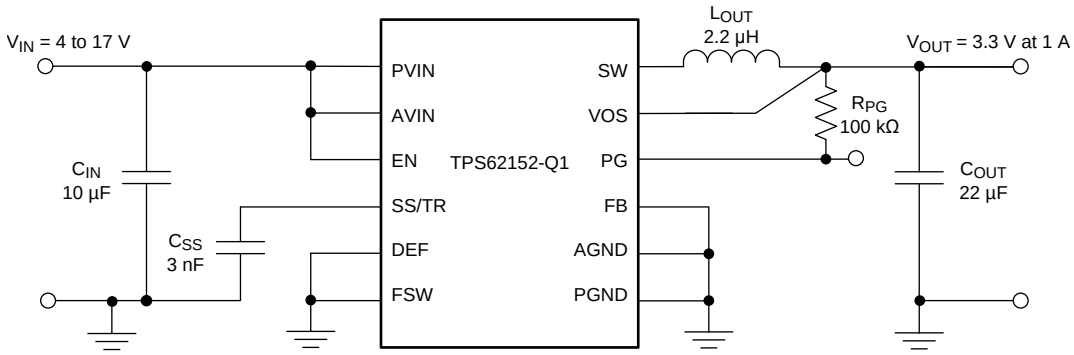


Figure 28. 3.3-V, 1-A Power Supply

8.2.1 Design Requirements

The device is optimized for a certain range of output inductor and output capacitor values. See the *Detailed Design Procedure* section for details. The *Recommended Operating Conditions* table lists the allowed ranges for the input voltage, input buffer capacitor, output inductor, and output buffer capacitor. The values listed in this table must be followed when designing the regulator. Low-ESR ceramic capacitors should be used at the input and output for better filtering and ripple performance. The *Detailed Design Procedure* section provides the necessary equations and guidelines for selecting external components for this regulator.

8.2.2 Detailed Design Procedure

8.2.2.1 External Component Selection

The external components must fulfill the needs of the application, but also the stability criteria of the device control loop. Table 2 lists recommended components based on the schematic in Figure 28.

Table 2. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
IC	17-V, 1-A step-down converter, VQFN	TPS62152-Q1 RGT, Texas Instruments
L_{OUT}	Inductor, 2.2-µH, 3.1-A, 0.165 in × 0.165 in (4,24 cm × 4,24 cm)	XFL4020-222MEB, Coilcraft
C_{IN}	Capacitor, 10-µF, 25-V, ceramic	Standard
C_{OUT}	Capacitor, 22-µF, 6.3-V, ceramic	Standard
C_{SS}	Capacitor, 3300-pF, 25-V, ceramic	
R_{PG}	Resistor, 100 kΩ, chip, 0603, 1/16 W, 1%	Standard

The TPS62152-Q1 works optimally within a range of external components. Consider the inductance and capacitance if the LC output filter in conjunction so as to create a double pole, responsible for the corner frequency of the converter (see the *Output Filter and Loop Stability* section). Use Table 3 to simplify the output-filter component selection.

Table 3. L-C Output Filter Combinations(1)

	10 µF	22 µF	47 µF	100 µF	200 µF
1 µH		√	√	√	√
2.2 µH	√	√(2)	√	√	√
3.3 µH	√	√	√	√	

(1) The values in the table are nominal values.
(2) This LC combination is the standard value and recommended for most applications.

The TPS62152-Q1 device can run with an inductor as low as 1 µH or 2.2 µH for the high-frequency setting (FSW = Low). However, for applications running with the low-frequency setting (FSW = High) or with low input voltages, 3.3 µH is a better recommendation. See *Optimizing the TPS62130/40/50/60/70 Output Filter*, SLVA463, for detailed information on further LC combinations.

8.2.2.1.1 Inductor Selection

Several effects like inductor ripple current, output ripple voltage, PWM-to-PSM transition point and efficiency affect the inductor selection. In addition, the inductor selected require rating for appropriate saturation current and dc resistance (DCR). Equation 7 and Equation 8 calculate the maximum inductor current under static load conditions.

$$I_{L(max)} = I_{OUT(max)} + \frac{\Delta I_{L(max)}}{2} \quad (7)$$

where

- I_L(max) is the maximum inductor current.

ΔI_L is the peak-to-peak inductor ripple current.

- (7)

$$\Delta I_{L(max)} = V_{OUT} \times \left(\frac{1 - \frac{V_{OUT}}{V_{IN(max)}}}{L_{(min)} \times f_{SW}} \right) \quad (8)$$

where

- $L_{(min)}$ is the minimum effective inductor value.
- f_{SW} is the actual PWM switching frequency.

Calculating the maximum inductor current using the actual operating conditions gives the minimum required saturation current of the inductor. TI recommends adding a margin of about 20%. A larger inductor value is also useful to achieve lower ripple current, but increases the transient response time and may require a larger package. TI recommends the inductors listed in Table 4, which have worked successfully with the TPS62152-Q1.

Table 4. List of Inductors

TYPE	INDUCTANCE [µH]	SATURATION CURRENT [A](1)	DIMENSIONS [L × W × H, mm]	MANUFACTURER
XFL4020-222ME_	2.2 µH, ±20%	3.5	4 × 4 × 2.1	Coilcraft
XFL3012-222MEC	2.2 µH, ±20%	1.6	3 × 3 × 1.2	Coilcraft
XFL3012-332MEC	3.3 µH, ±20%	1.4	3 × 3 × 1.2	Coilcraft
VLS252012T-2R2M1R3	2.2 µH, ±20%	1.3	2.5 × 2 × 1.2	TDK
LPS3015-332	3.3 µH, ±20%	1.4	3 × 3 × 1.4	Coilcraft
744025003	3.3 µH, ±20%	1.5	2.8 × 2.8 × 2.8	Wuerth
PSI25201B-2R2MS	2.2 µH, ±20%	1.3	2 × 2.5 × 1.2	Cyntec
NR3015T-2R2M	2.2 µH, ±20%	1.5	3 × 3 × 1.5	Taiyo Yuden

(1) Lower of I_{RMS} at 40°C rise or I_{SAT} at 30% drop.

The inductor value also determines the load current at which the device enters power-save mode as shown in Equation 9.

$$I_{load(PSM)} = \frac{1}{2}\Delta I_L \quad (9)$$

The designer can use Equation 8 to calculate the inductor value for changing this current level.

8.2.2.1.2 Output Capacitor

The recommended value for the output capacitor is 22 µF. The architecture of the TPS62152-Q1 device allows the use of ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output-voltage ripple and are ideal. To keep low resistance up to high frequencies and to get narrow capacitance variation with temperature, TI recommends using X7R or X5R dielectric. Using a higher value can have some advantages, such as smaller voltage ripple and a tighter DC output accuracy in power-save mode (see SLVA463).

NOTE

In power-save mode, the output-voltage ripple depends on the output capacitance and the ESR and peak inductor current of the capacitor. Using ceramic capacitors provides low ESR and low ripple.

8.2.2.1.2.1 Input Capacitor

For most applications, 10 µF is sufficient and recommended, though a larger value reduces input current ripple further. The input capacitor buffers the input voltage for transient events and also decouples the converter from the supply. TI recommends low-ESR multilayer ceramic capacitor for best filtering. Place the capacitor between PVIN and PGND as close as possible to those pins. Even though the AVIN and PVIN supply must come from the same input source, it is a good idea to place a capacitance of 0.1 µF from AVIN to AGND, to avoid potential noise coupling. Use of an RC low-pass filter from PVIN to AVIN is allowable but not mandatory.

8.2.2.1.2.2 Soft-Start Capacitor

A capacitance connected between SS/TR pin and AGND allows a user-programmable start-up slope of the output voltage. A constant-current source provides 2.5 µA to charge the external capacitance. Use Equation 10 to calculate the capacitance required for a given soft-start ramp time for the output voltage.

$$C_{SS} = t_{SS} \times \frac{2.5\ \mu A}{1.25\ V} \quad [F] \quad (10)$$

where

- C_{SS} is the capacitance (F) required at the SS/TR pin
- t_{SS} is the desired soft-start ramp time (s).

NOTE

DC bias effect: High-capacitance ceramic capacitors have a DC bias effect, which has a strong influence on the final effective capacitance. Therefore, choose the right capacitor value carefully. Package size and voltage rating in combination with dielectric material are responsible for differences between the rated capacitor value and the effective capacitance.

8.2.2.2 Output Filter and Loop Stability

The TPS62152-Q1 device has internal compensation to be stable with L-C filter combinations corresponding to a corner frequency calculated with Equation 11.

$$f_{LC} = \frac{1}{2\pi\sqrt{L \times C}} \tag{11}$$

Table 3 gives proven and recommended nominal values for inductance and ceramic capacitance. Different values may work, but take care not to affect the loop stability. See *Optimizing the TPS62130/40/50/60/70 Output Filter*, SLVA463, for more information, including a detailed L-C stability matrix.

The TPS62152-Q1 device includes an internal 25-pF feedforward capacitor, connected between the VOS and FB pins. This capacitor impacts the frequency behavior and sets a pole and zero in the control loop with the resistors of the feedback divider, according to equations Equation 12 and Equation 13.

$$f_{zero} = \frac{1}{2\pi \times R_1 \times 25\ pF} \tag{12}$$

$$f_{pole} = \frac{1}{2\pi \times 25\ pF} \times \left(\frac{1}{R_1} + \frac{1}{R_2} \right) \tag{13}$$

Though the TPS62152-Q1 device is stable without the pole and zero being in a particular location, adjusting their location to the specific needs of the application can provide better performance in power-save mode and/or improved transient response. An external feedforward capacitor can also be added. The application reports *Optimizing Transient Response of Internally Compensated dc-dc Converters With Feedforward Capacitor*, SLVA289, and *Using a Feedforward Capacitor to Improve Stability and Bandwidth of TPS62130/40/50/60/70*, SLVA466, provide a more-detailed discussion on the optimization for stability vs transient response.

8.2.3 Application Curves

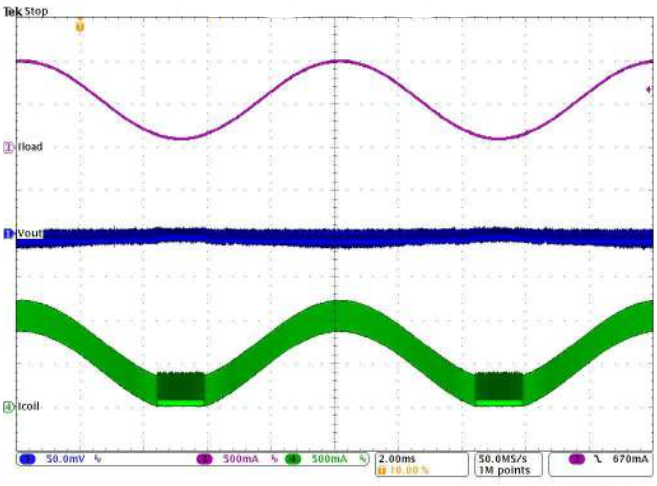


Figure 29. PWM-PSM-Transition for V_{IN} = 12 V With 50 mV/div

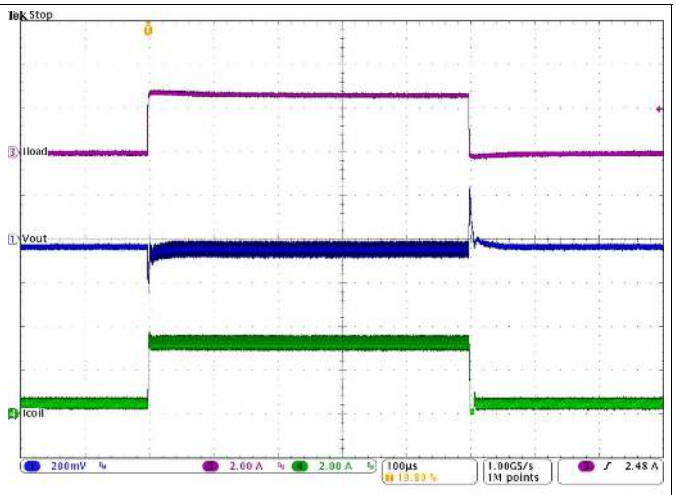


Figure 30. Load Transient Response for V_{IN} = 12 V and I_{OUT}= 0 A to 2.5 A and back to 0 A

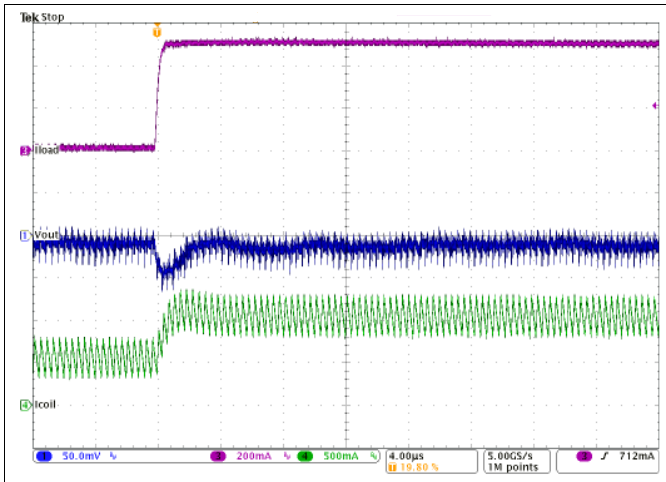


Figure 31. Load Transient Response of Figure 30, Rising Edge

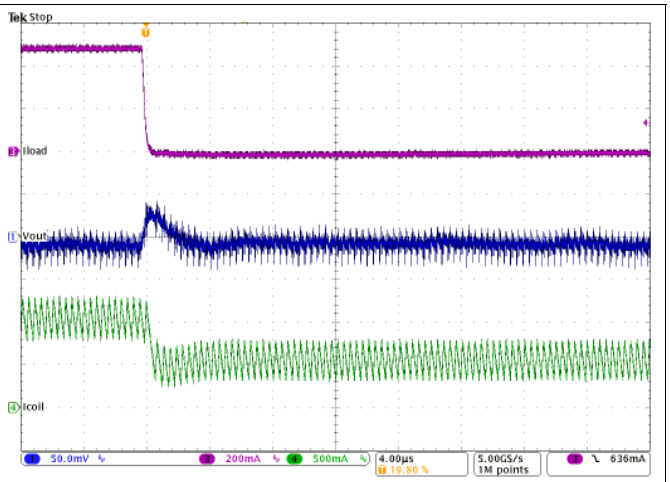


Figure 32. Load Transient Response of Figure 30, Falling Edge

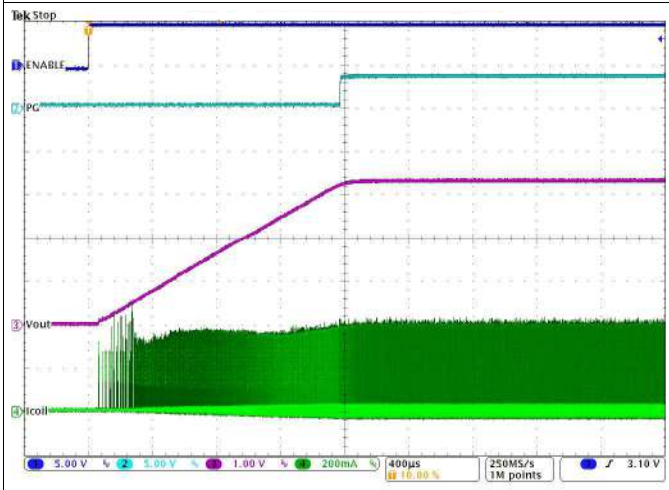


Figure 33. Startup into 100 mA for V_{IN} = 12 V

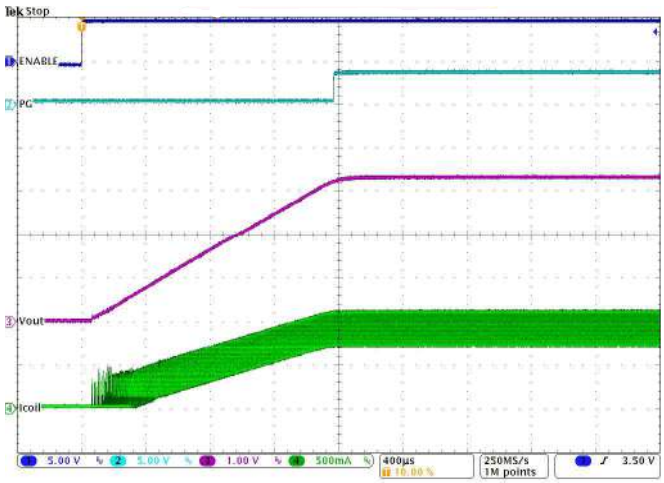


Figure 34. Startup into 1 A for V_{IN} = 12 V

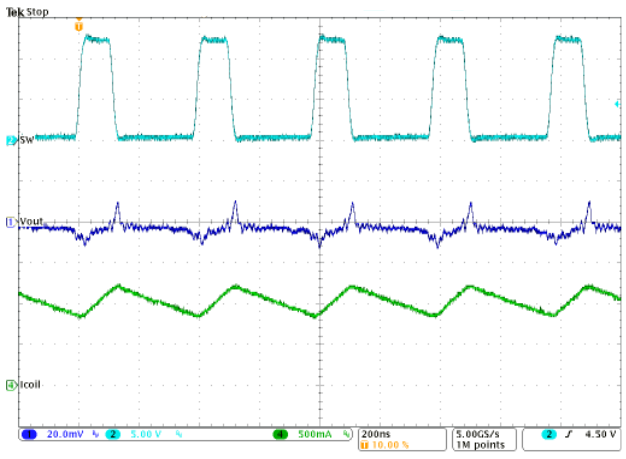


Figure 35. Typical Operation in PWM Mode With I_{OUT} = 1 A

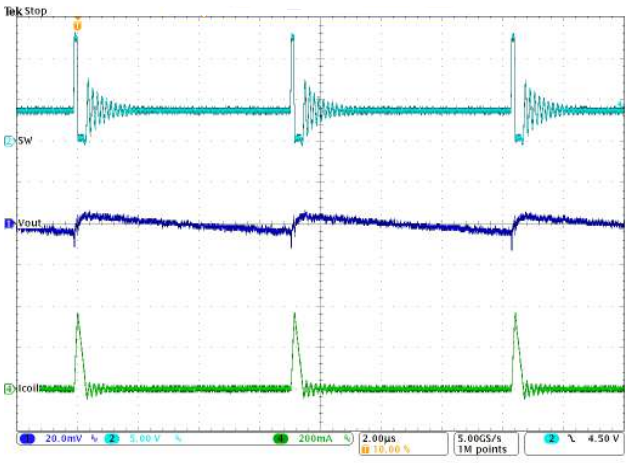


Figure 36. Typical Operation in Power Save Mode With I_{OUT} = 10 mA

9 Power Supply Recommendations

The TPS62590-Q1 device is designed to operate with a wide range of input voltages ranging from 4 V to 17 V. For most applications, a 10-µF capacitor is sufficient and recommended at the PVIN pin. Connect a capacitor with a larger value to further reduce input current ripple. The input capacitor buffers the input voltage for transient events and also decouples the converter from the supply. TI recommends using a low-ESR multilayer ceramic capacitor for the best filtering. Place the capacitor between the PVIN and PGND pins, as close as possible to these pins. Although the AVIN and PVIN supply must come from the same input source, placing a capacitor with a value of 0.1 µF from the AVIN pin to the AGND pin is recommended to avoid potential noise coupling. Use of an RC low-pass filter from the PVIN to AVIN pin is allowed but not required.

Capacitance derating for aging, temperature, and DC bias must be taken into consideration while determining the capacitor value.

10 Layout

10.1 Layout Guidelines

- A proper layout is critical for the operation of a switched-mode power supply, even more at high switching frequencies. Therefore, the PCB layout of the TPS62152-Q1 device demands careful attention to ensure operation and to get the performance specified. A poor layout can lead to issues like poor regulation (both line and load), stability and accuracy weaknesses, increased EMI radiation, and noise sensitivity.
- See Figure 37 for the recommended layout of the TPS62152-Q1 device, which is designed for common external ground connections. Therefore, both AGND and PGND pins connect directly to the exposed thermal pad. On the PCB, the direct common ground connection of AGND and PGND to the exposed thermal pad and the system ground (ground plane) is mandatory.
- Provide low-inductive, low-resistive paths for loops with high di/dt. Paths conducting the switched load current should be as short and wide as possible.
- Provide low-capacitive paths (with respect to all other nodes) for wires with high dv/dt.
- Place the input and output capacitance as close as possible to the IC pins and provide short connections between C_{IN} to GND and C_{OUT} to GND.
- Avoid parallel wiring over long distances as well as narrow traces.
- Use loops that conduct an alternating current to outline an area as small as possible because the energy radiated is proportional to this area.
- VOS must be connected with a short trace and must be adequate distance from high dv/dt signals (for example, SW). Because this node caries information about the output voltage, it should have connections as close as possible to the actual output voltage (at the output capacitor).
- Because this device has fixed output voltage, TI recommends connecting the FB pin to GND with a short trace.
- Keep the capacitor on the SS/TR pin and on AVIN close to the device. Connect these pins directly to the system ground plane.
- Solder the exposed thermal pad to the circuit board for mechanical reliability and to achieve appropriate power dissipation.
- The recommended layout is implemented on the EVM and shown in *TPS62130EVM-505, TPS62140EVM-505, and TPS62150EVM-505 Evaluation Modules*, SLVU437. Additionally, the EVM Gerber data is available for download in the zipped file: SLVC394 from the device product folder, www.ti.com/product/TPS62152-Q1.

10.2 Layout Example

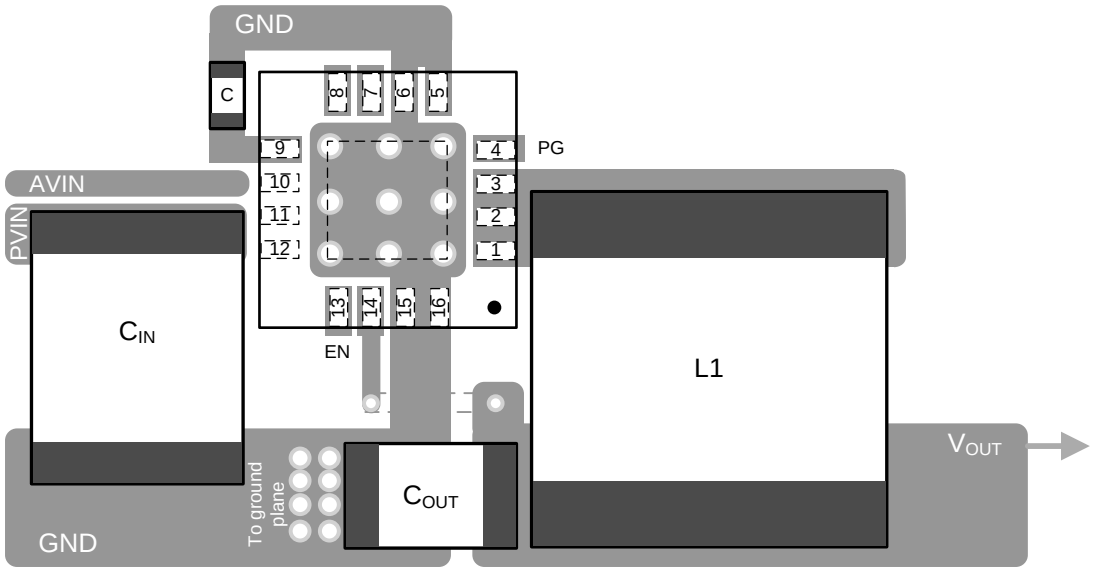


Figure 37. Layout Example

10.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB by soldering the exposed thermal pad
- Introducing airflow in the system

For more details on how to use the thermal parameters, see *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs*, SZZA017, and *Semiconductor and IC Package Thermal Metrics*, SPRA953.

The design of the TPS62152-Q1 device is for a maximum operating junction temperature (T_J) of 125°C. Therefore, the power losses that can be dissipated over the actual thermal resistance impose a limit on the maximum output power, given the package and the surrounding PCB structures. If the thermal resistance of the package is given, the increasing the size of the surrounding copper area and making a proper thermal connection of the IC can reduce the thermal resistance. A recommendation for getting improved thermal behavior is to use top layer metal to connect the device with wide and thick metal lines. Internal ground layers can connect to vias directly under the IC for improved thermal performance.

If short circuit or overload conditions are present, the device is protected by limiting internal power dissipation.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.1.2 Development Support

For the EVM Gerber data, see SLVC394.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *Optimizing the TPS62130/40/50/60/70 Output Filter*, SLVA463
- *Optimizing Transient Response of Internally Compensated dc-dc Converters With Feedforward Capacitor*, SLVA289
- *Semiconductor and IC Package Thermal Metrics*, SPRA953
- *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs*, SZZA017
- *TPS62130/40/50 Sequencing and Tracking*, SLVA470
- *TPS62130EVM-505, TPS62140EVM-505, and TPS62150EVM-505 Evaluation Modules*, SLVU437
- *Using a Feedforward Capacitor to Improve Stability and Bandwidth of TPS62130/40/50/60/70*, SLVA466
- *Voltage Margining Using the TPS62130*, SLVA489

11.3 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

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11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

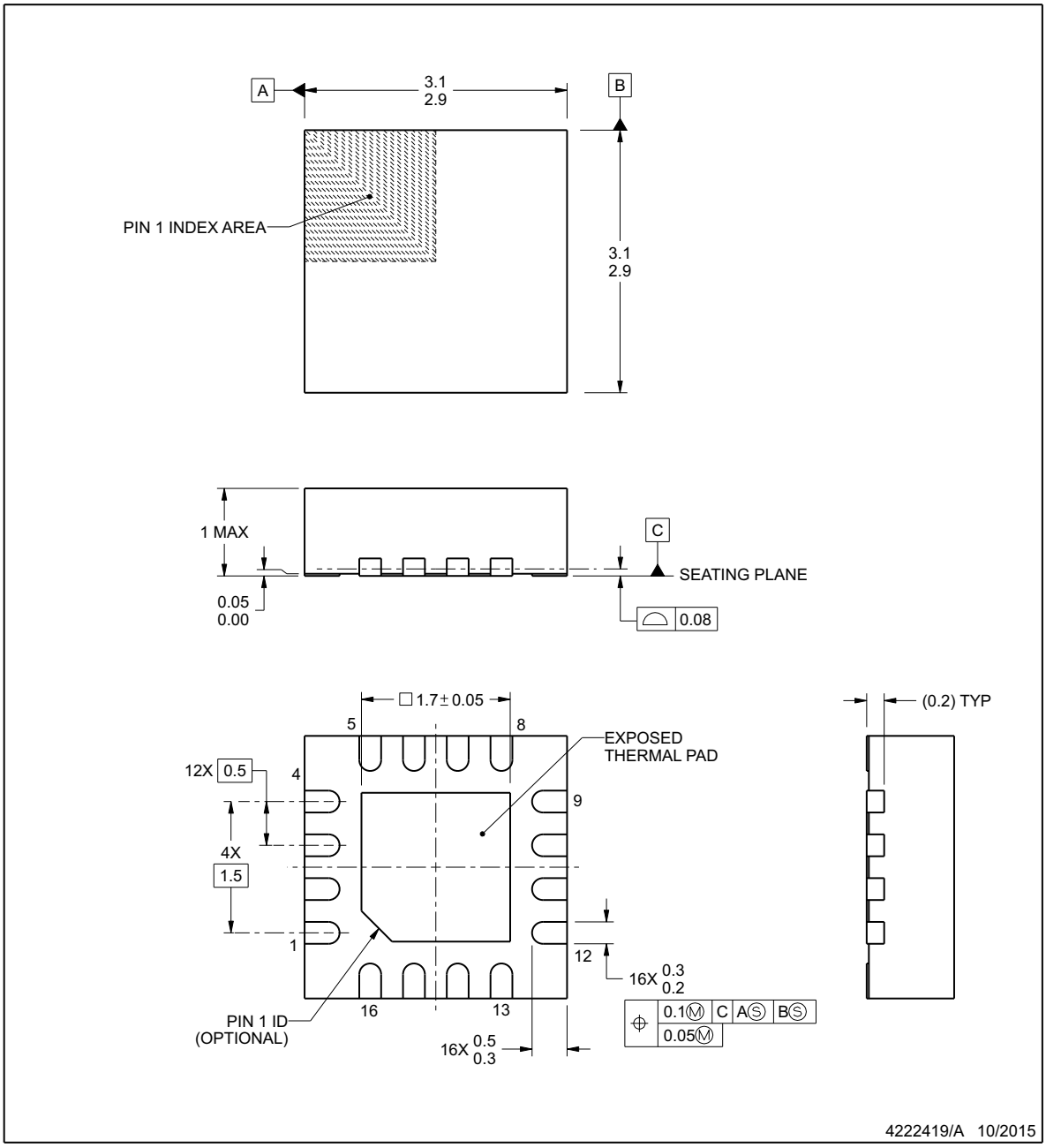
The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

RGT0016C

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

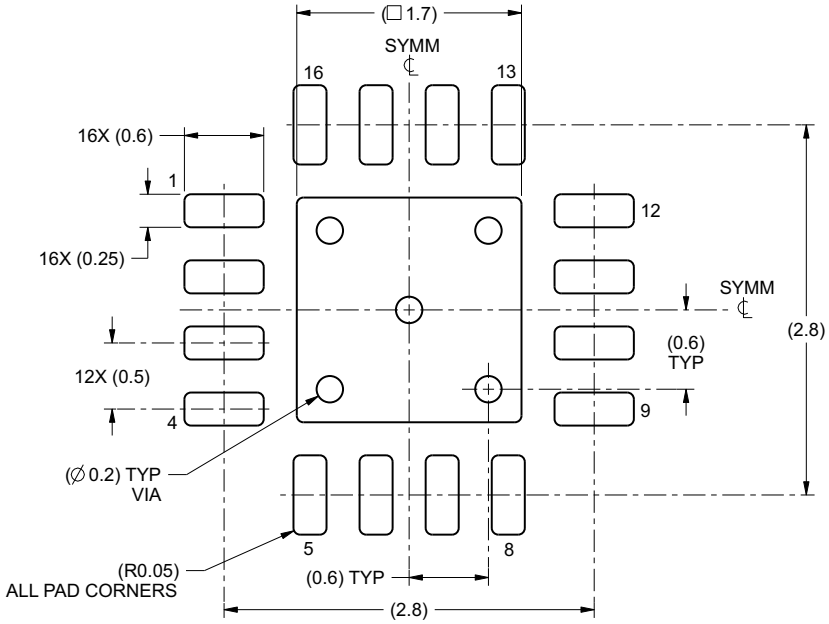
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

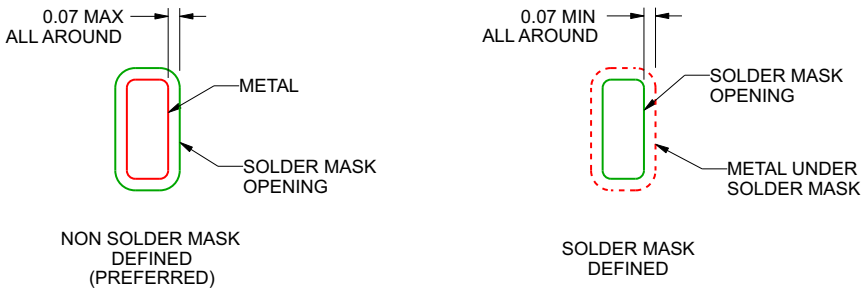
RGT0016C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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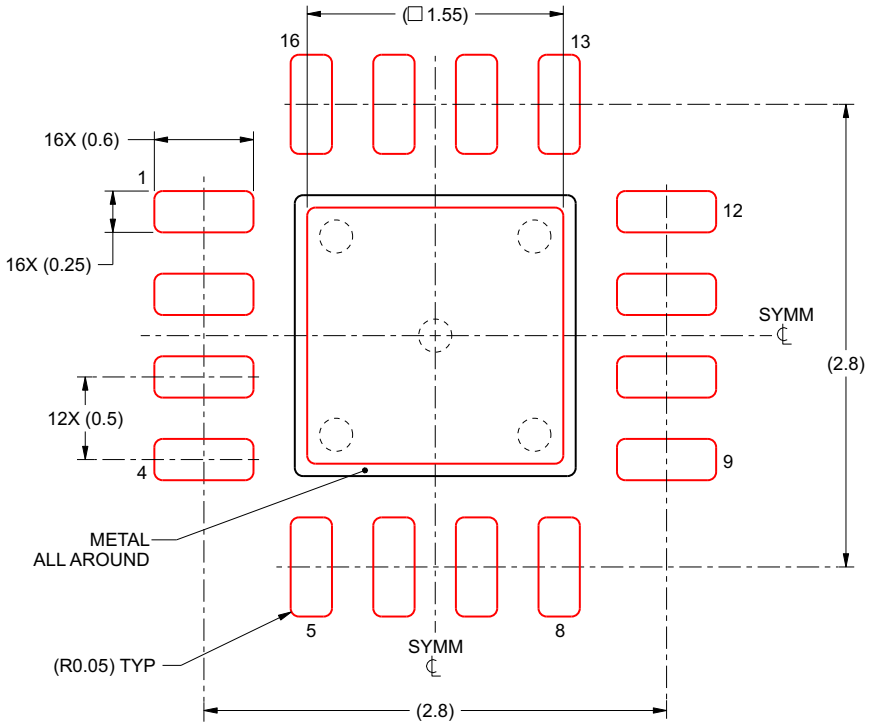
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

RGT0016C — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
83% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4222419/A 10/2015

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62152QRGTRQ1	NRND	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SJJ	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS62152-Q1 :

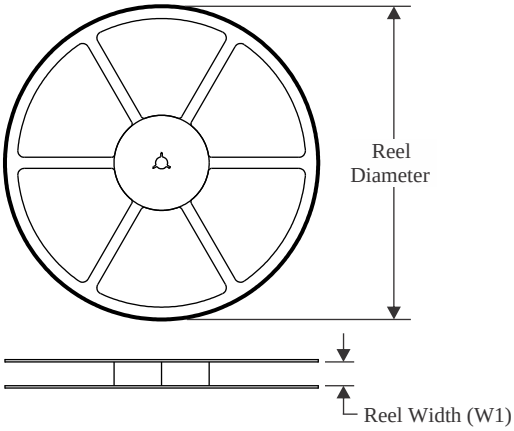
- Catalog: TPS62152

NOTE: Qualified Version Definitions:

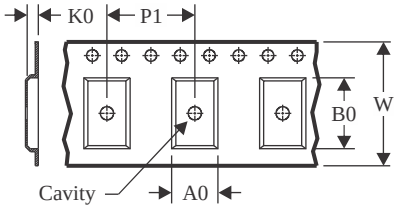
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

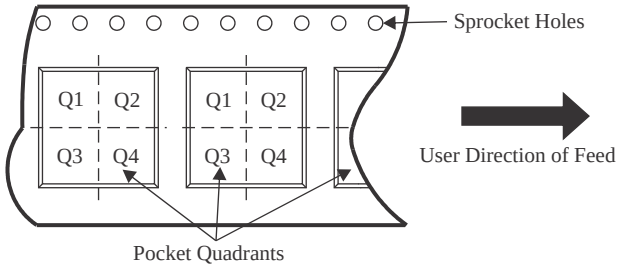


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

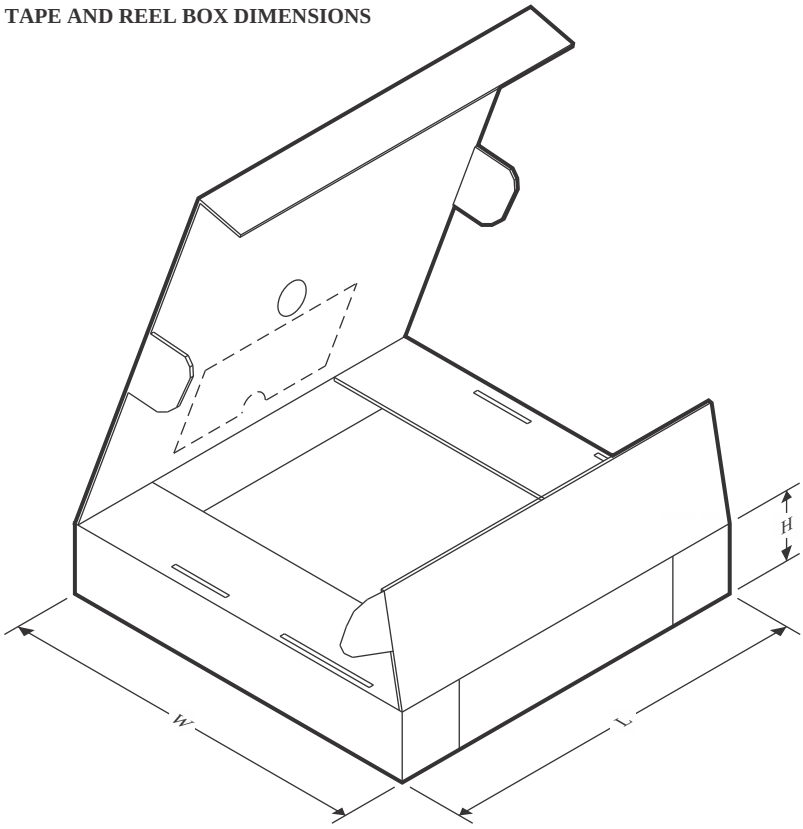
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62152QRGTRQ1	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62152QRGTRQ1	VQFN	RGT	16	3000	346.0	346.0	33.0

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