SmartJitter™ PWM Flyback Controller

General Description

The RT7736 series is a high performance enhanced PWM flyback controller with proprietary SmartJitter™ technology. The innovative SmartJitter™ technology not only reduces EMI emissions of SMPS when the system enters burst switching green mode, but also eliminates output jittering ripple.

The RT7736 is a current mode PWM controller including built-in slope compensation, internal Leading Edge Blanking (LEB) and cycle-by-cycle current limit. It provides excellent green power performance, especially under light load and no load conditions. It allows for simpler design and reduces external component count.

This controller integrates comprehensive safety protection functions for robust designs including input Under-Voltage Lockout (UVLO), Over-Voltage Protection (OVP), Over-Load Protection (OLP), Secondary Rectifier Short Protection (SRSP), CS pin open protection and cycle-by-cycle current limit.

The RT7736 is a cost-effective and compact solution for NB adaptor applications. It is available in the SOT-23-6 package.

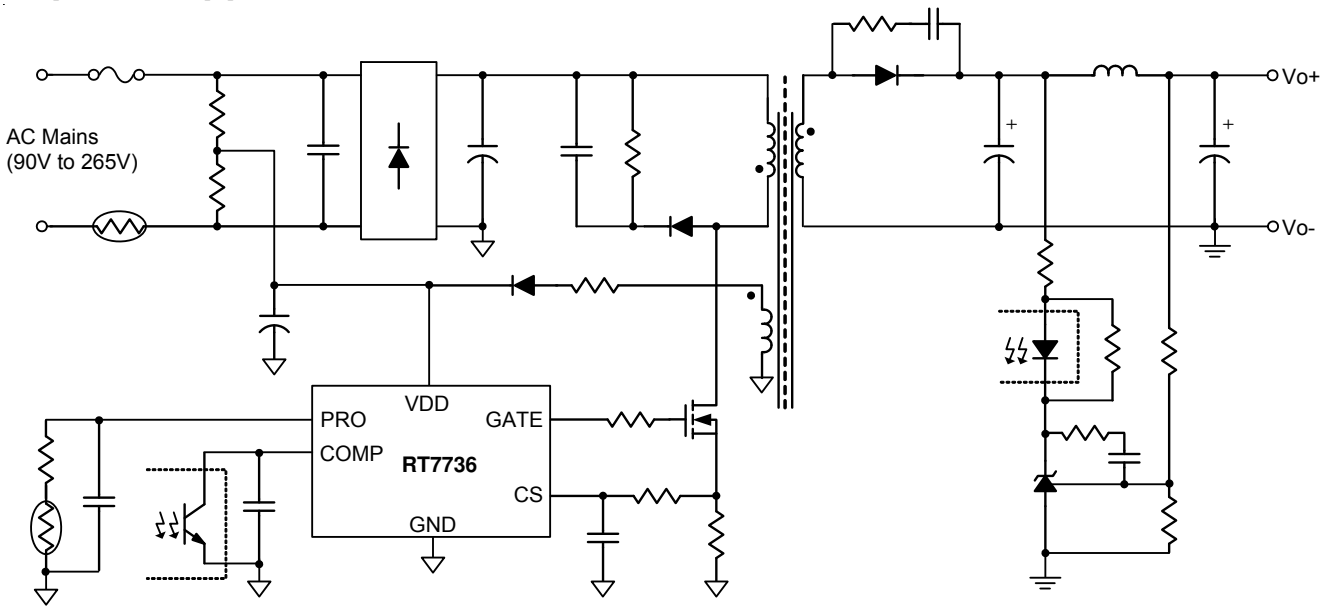
Features

- **Proprietary SmartJitter™ Technology**
  - **Reducing EMI Emissions of SMPS**
  - **Output Jittering Ripple Elimination**
- **No Load Input Power Under 100mW (RT7736G/R/L/E)**
- **Accurate Over Load Protection**
- **UVLO 9V/14.5V**
- **PRO Pin for External Arbitrary OVP/OTP**
- **IC ON/OFF Control (RT7736G/R/L)**
- **BNO Pin for Brown-In/Out (RT7736B/D/F)**
- **Soft Driving for EMI Noise Reduction**
- **Driver Capability : 300mA/–300mA**
- **High Noise Immunity**
- **RoHS Compliant and Halogen Free**

Applications

- Switching AC/DC Adaptor
- DVD Open Frame Power Supply
- Set-Top Box (STB)
- ATX Standby Power
- TV/Monitor Standby Power
- PC Peripherals
- NB Adaptor

Simplified Application Circuit



Ordering Information

RT7736□□□

- Package Type: E : SOT-23-6
- Lead Plating System: G : Green (Halogen Free and Pb Free)
- RT7736 Version (Refer to Version Table)

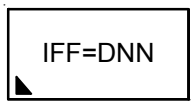
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

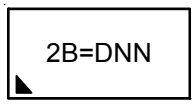
Marking Information

RT7736GGE



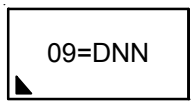
IFF= : Product Code
DNN : Date Code

RT7736RGE



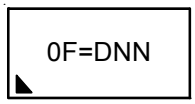
2B= : Product Code
DNN : Date Code

RT7736LGE



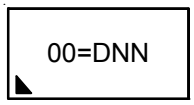
09= : Product Code
DNN : Date Code

RT7736EGE



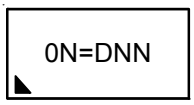
0F= : Product Code
DNN : Date Code

RT7736BGE



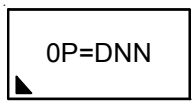
00= : Product Code
DNN : Date Code

RT7736DGE



0N= : Product Code
DNN : Date Code

RT7736FGE



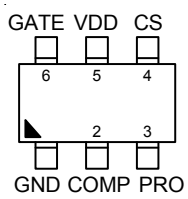
0P= : Product Code
DNN : Date Code

RT7736 Version Table

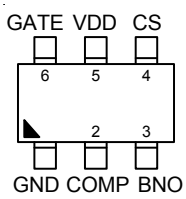
Version	RT7736G	RT7736R	RT7736L	RT7736E	RT7736B	RT7736D	RT7736F
Frequency	65kHz	65kHz	65kHz	65kHz	65kHz	65kHz	65kHz
OLP Delay Time	56ms	56ms	56ms	56ms	56ms	88ms	64ms
Internal OVP	Auto Recovery	Auto Recovery	Latch	Latch	Auto Recovery	Auto Recovery	Auto Recovery
OLP & SRSP	Auto Recovery	Auto Recovery	Auto Recovery	Auto Recovery	Auto Recovery	Auto Recovery	Auto Recovery
PRO Pin High	Latch	Auto Recovery	Latch	Latch	X	X	X
PRO Pin Low	Auto Recovery	Auto Recovery	Auto Recovery	Latch	X	X	X
External OTP by PRO	Auto Recovery	Auto Recovery	Latch	Latch	X	X	X
External Brown-In/Out	X	X	X	X	○	○	○

Pin Configurations

(TOP VIEW)



RT7736G/R/L/E
SOT-23-6



RT7736B/D/F
SOT-23-6

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	GND	Ground of the Controller.
2	COMP	Feedback Voltage Input. Connect an opto-coupler to close the control loop and achieve output voltage regulation.
3	PRO	Protection Input for OVP, OTP or ON/OFF Control. (RT7736G/R/L/E)
	BNO	Brown-In/Out Detection Input for RT7736B/D/F Only.
4	CS	Current Sense Input. The current sense resistor between this pin and GND is used for current limit setting.
5	VDD	Supply Voltage Input. The controller will be enabled when VDD exceeds V_{TH_ON} (14.5V typ.) and disabled when VDD decreases lower than V_{TH_OFF} (9V typ.)
6	GATE	Gate Driver Output for External Power MOSFET.

Function Block Diagram

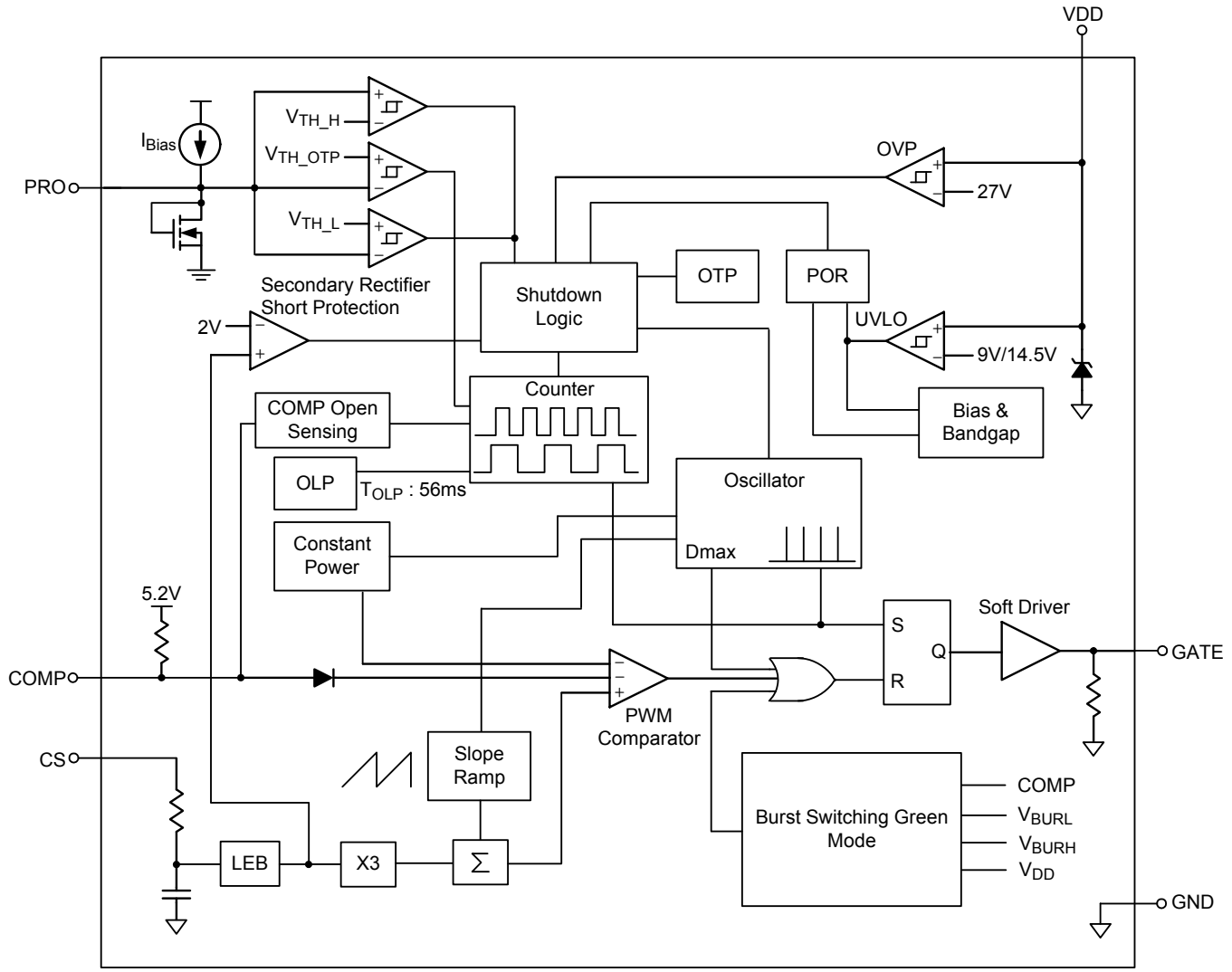


Figure 1. Block Diagram for RT7736G, RT7736R, RT7736L and RT7736E

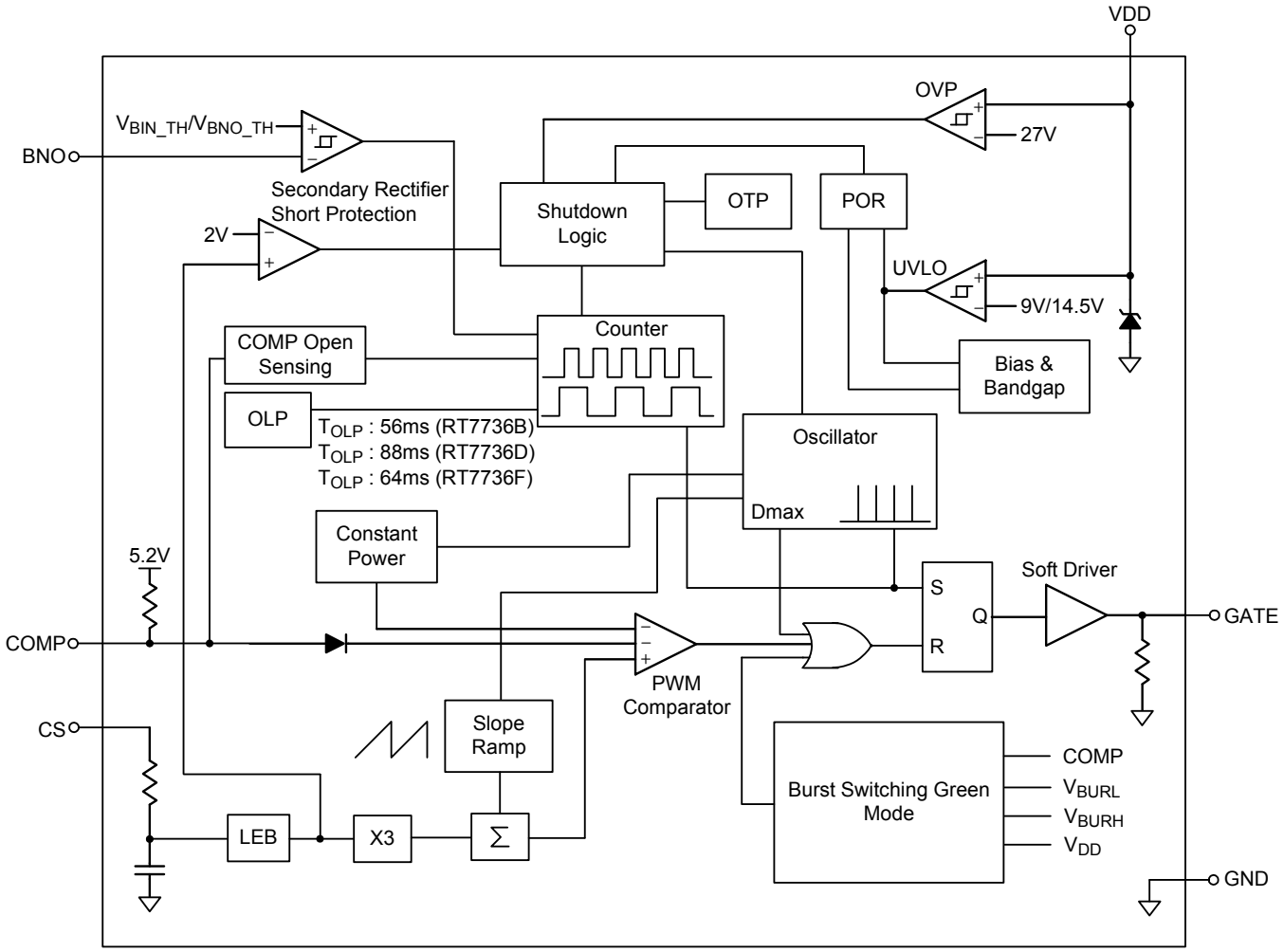


Figure 2. Block Diagram for RT7736B, RT7736D and RT7736F

Operation

Burst Switching Green Mode

The burst mode is designed to reduce switching loss. When the output load reduces, and the V_{COMP} drops and reaches V_{BURL}, the controller will cease switching. After output voltage decreases and the V_{COMP} goes up to V_{BURH}, the switching will be resumed.

VDD Holdup Mode

Under very light load conditions, the V_{DD} may drop down to turn-off threshold voltage. To avoid this situation when V_{DD} drops to a set threshold, V_{DD_ET}, the hysteresis comparator will bypass PWM and burst mode loop, and then force switching at a very low level to supply energy to VDD pin. VDD holdup mode is also improved to hold up V_{DD} by less switching cycles. This mode is very useful for reducing start-up resistor loss and keeping start-up time within specification. This function makes bias winding design and transient design easier.

Oscillator

The oscillator runs at 65kHz and features frequency jittering function. Its jittering depth is Δf with about T_{JIT} envelope frequency at f_{OSC}. It also generates slope compensation saw-tooth, maximum duty cycle pulse and overload protection slope.

Leading Edge Blanking (LEB)

To prevent unexpectedly gate switching interruption from the initial spike on CS pin, the LEB delay is designed to block this spike at the beginning of gate switching.

Gate Driver

A totem pole gate driver is designed to meet both EMI and efficiency requirements in low power applications. An internal pull-low circuit is activated after pretty low V_{DD} to prevent external MOSFET from accidentally turning on during UVLO.

PRO Pin (RT7736G/R/L/E)

The RT7736G/R/L/E features a PRO pin, and it can be applied for external arbitrary OVP or OTP applications (RT7736G/R/L/E), and also can be applied for IC ON/OFF control (RT7736G/R/L).

BNO Pin (RT7736B/D/F)

The RT7736B/D/F features a BNO pin, and it can be applied for external arbitrary brown-in/out. The BNO pin is connected to the AC line input or bulk capacitor with a resistive divider to achieve brown-in/out protection.

Cycle-by-Cycle Current Limit

This is a basic but very useful function and it can be implemented easily in current mode controller.

Over-Load Protection

In over load conditions, long time current limit will lead to system thermal stress problem. To further protect the system, the RT7736 is designed with a proprietary prolonged turn-off period during hiccup. The power loss and temperature during OLP will be averaged to an acceptable level over the ON/OFF cycle.

CS Pin Open Protection

When the CS pin is opened, the controller will shut down after a few cycles.

Over-Voltage Protection

Output voltage can be roughly sensed by the VDD pin. If the sensed voltage reaches V_{OVP} threshold, the controller will shut down after deglitch delay. The controller will resume once the fault is removed.

Feedback Open and Opto-Coupler Short

If the output voltage feedback loop is open or the opto-coupler is shorted, the OVP/OLP function will be triggered depending on which one occurs first.

Secondary Rectifier Short Protection

The current spike during secondary rectifier short test is extremely high because of the saturated main transformer. Meanwhile, the transformer acts like a leakage inductance. During high line, the current in power MOSFET is sometimes too high for OLP delay time. To offer better and easier protection design, the RT7736 will shut down after a few of cycles before fuse is impacted.

Output Short Protection

The RT7736 implements output short protection by detecting GATE width with delay time. It could minimize the power loss and temperature during output short, especially at high line input voltage.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VDD to GND ---------- –0.3V to 30V
- GATE to GND ---------- –0.3V to 16.5V
- PRO, BNO, COMP, CS to GND ---------- –0.3V to 6.5V
- Power Dissipation, P_D @ T_A = 25°C
  SOT-23-6 ---------- 0.38W
- Package Thermal Resistance (Note 2)
  SOT-23-6, θ_{JA} ---------- 260.7°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 3kV
  MM (Machine Model) ---------- 250V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VDD ---------- 12V to 25V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{DD} = 15V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDD Section						
V_{DD} Over-Voltage Protection Level	V_{OVP}		26	27	28	V
V_{DD} Zener Clamp	V_Z		29	--	--	V
On Threshold Voltage	V_{TH_ON}		13.5	14.5	15.5	V
Off Threshold Voltage	V_{TH_OFF}		8.5	9	9.5	V
Disable Brown-in Detection to Avoid Start-up Failed	V_{DD_BNI}		11	12	13	V
VDD Holdup Mode Entry Point	V_{DD_ET}	V_{COMP} < 1.3V	9.5	10	10.5	V
VDD Holdup Mode Ending Point	V_{DD_ED}	V_{COMP} < 1.3V	10	10.5	11	V
Latch-off Clamping Voltage	V_{DD_LH}		--	5.5	--	V
Threshold Voltage for Latch-off Release	V_{LH_OFF}		--	5	--	V
Start-up Current	I_{DD_ST}	V_{DD} < V_{TH_ON} – 0.1V, T_A = –40°C to 80°C	--	5	10	μA
Latch-off Operating Current	I_{DD_LH}	T_A = –40°C to 80°C	2	--	10	μA
Operating Supply Current	I_{DD_OP1}	V_{DD} = 15V, GATE pin open, V_{COMP} = 2.5V	--	1	--	mA
Operating Supply Current	I_{DD_OP2}	V_{DD} = 15V, GATE pin open, V_{COMP} = 1.7V	--	0.9	--	mA
I_{DD} Sinking Current of Waiting Brown-in After Start-up	I_{DD_BNI}	For RT7736B/D/F ; V_{DD} = 15V, GATE and COMP pin open	100	150	200	μA

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
I_{DD} Sinking Current	I_{DD_ARP}	During entering auto recovery protection		300	400	500	μA
Oscillator Section							
Normal PWM Frequency	f_{OSC}	V_{COMP} > V_{BS_ET}		60	65	70	kHz
Maximum Duty Cycle	DCY_{MAX}			70	75	80	%
Minimum Burst Switching Green Mode Frequency	f_{BS_MIN}			18.5	22	25.5	kHz
PWM Frequency Jittering Range	Δf			--	±6	--	%
PWM Frequency Jittering Period	T_{JIT}			--	16	--	ms
Frequency Variation Versus VDD Deviation	f_{DV}	V_{DD} = 9V to 23V		--	--	2	%
Frequency Variation Versus Temperature Deviation	f_{DT}	T_A = −30°C to105°C		--	--	5	%
COMP Input Section							
Open Loop Voltage	V_{COMP_OP}	COMP pin open		5	5.2	5.4	V
Short Circuit Current of COMP	I_{ZERO}	V_{COMP} = 0V		0.24	0.29	0.34	mA
Delay Time of COMP Open-loop Protection	T_{OLP}	f_{OSC} = 65kHz	RT7736G/R/L/E/B	--	56	--	ms
			RT7736D	--	88	--	
			RT7736F	--	64	--	
Burst Switching Green Mode Entry Voltage	V_{BS_ET}			2.3	2.35	2.4	V
Burst Switching Green Mode Ending Voltage	V_{BS_ED}			2.1	2.15	2.2	V
Delay Time of Output Short Protection	T_{D_OSP}	f_{OSC} = 65kHz, RT7736G/R/L/E/B		--	8	--	ms
Current Sense Section							
Maximum Current Limit	V_{CS_MAX}	(Note 5)		1.05	1.1	1.15	V
Leading Edge Blanking Time	T_{LEB}	(Note 5)		150	250	350	ns
Internal Propagation Delay Time	T_{PD}	(Note 5)		--	100	--	ns
Minimum On-Time	T_{ON_MIN}			250	350	450	ns
Detection On-Time of Output Short Protection	T_{ON_OSP}	f_{OSC} = 65kHz, RT7736G/R/L/E/B (Note 6)		0.7	1.1	1.5	μs
GATE Section							
Rising Time	T_R	V_{DD} = 15V, C_L = 1nF		--	60	--	ns
Falling Time	T_F	V_{DD} = 15V, C_L = 1nF		--	40	--	ns
Gate Output Clamping Voltage	V_{CLAMP}	V_{DD} = 23V		--	13.5	--	V
PRO Interface Section (RT7736G/R/L/E)							
Pull High Threshold	V_{TH_H}			1.75	1.8	1.85	V
Pull Low OTP Threshold	V_{TH_OTP}			0.47	0.5	0.53	V
Pull Low Threshold	V_{TH_L}			0.25	0.3	0.35	V

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Open Loop Voltage	V_{PRO_OP}	PRO pin open		--	1.3	--	V
Internal Bias Current	I_{BIAS}			90	100	110	μA
Pull High Sinking Current	I_{SIN}			--	--	500	μA
Delay Time of OTP by PRO	T_{D_OTP}	f_{OSC} = 65kHz		--	56	--	ms
BNO Interface Section (RT7736B/D/F)							
Brown-In Threshold	V_{BNI_TH}			0.96	1	1.04	V
Brown-Out Threshold	V_{BNO_TH}			0.81	0.85	0.89	V
De-bounce Time of V_{BNO_TH}	T_{D_BNO}	f_{OSC} = 65kHz	RT7736B	--	56	--	ms
			RT7736D	--	88	--	
			RT7736F	--	24	--	
Over-Temperature Protection (OTP) Section							
Over-Temperature Protection	T_{OTP}	On Chip OTP (Note 6)		--	140	--	°C

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured in natural convection (still air) at T_A = 25°C with the component mounted on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Leading edge blanking time and internal propagation delay time are guaranteed by design.

Note 6. Guaranteed by design.

Typical Application Circuit

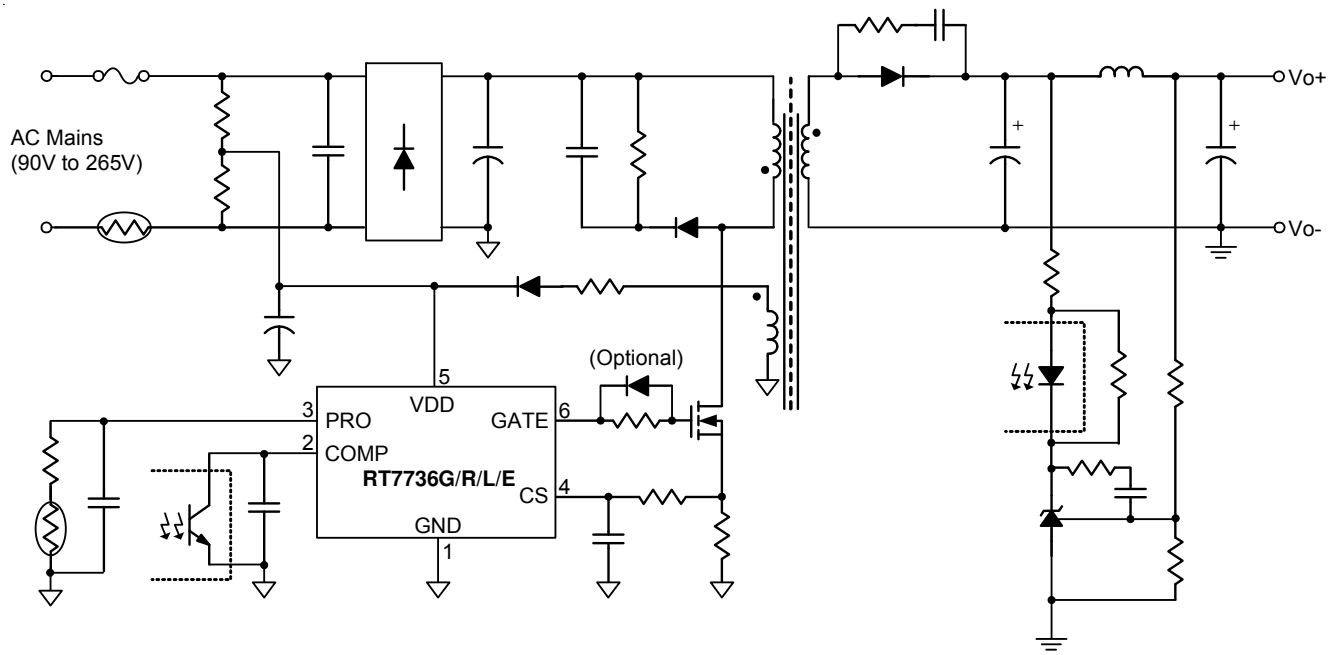


Figure 3. Application Circuit For RT7736G, RT7736R, RT7736L and RT7736E

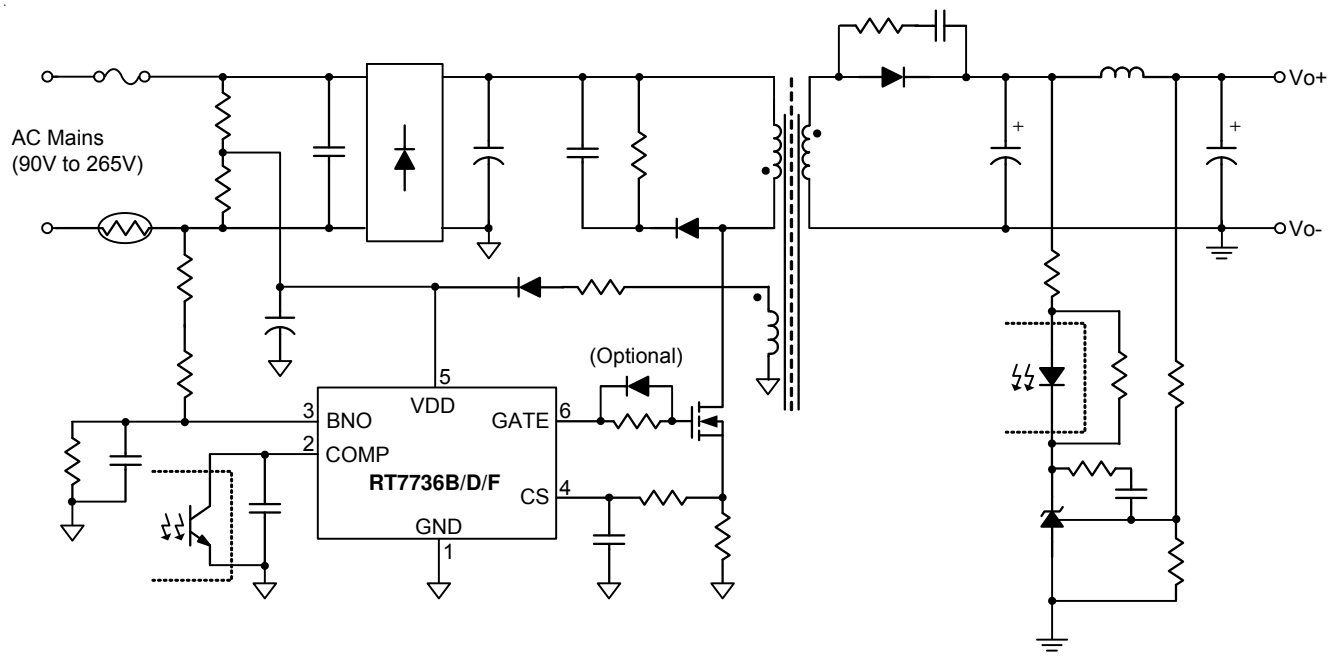
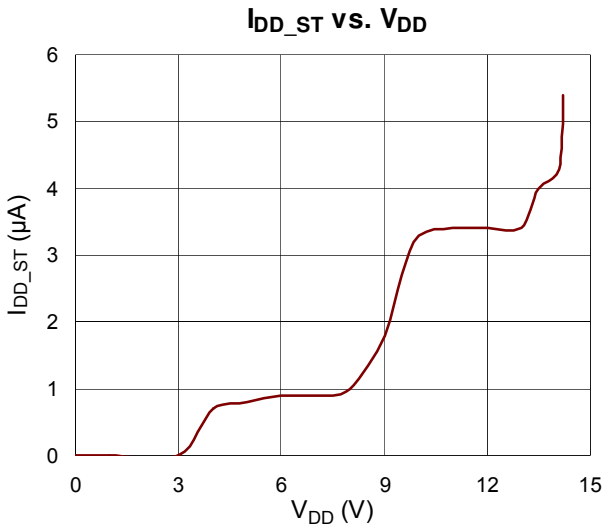
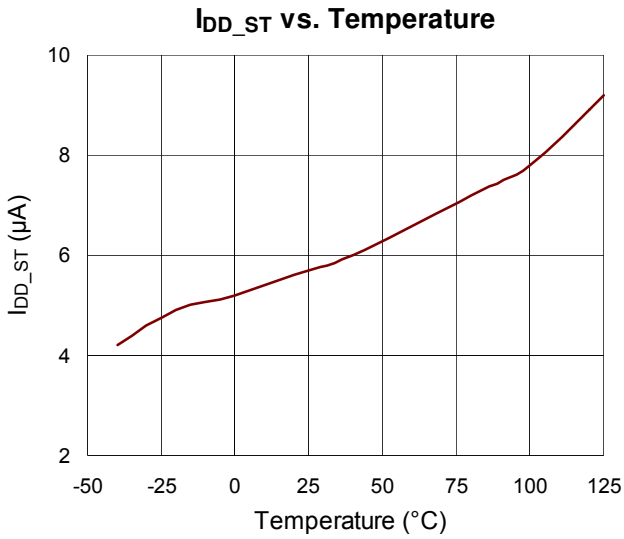
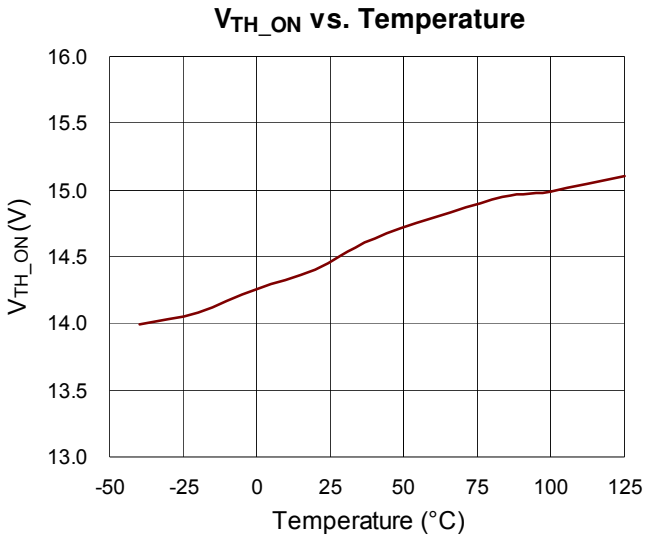


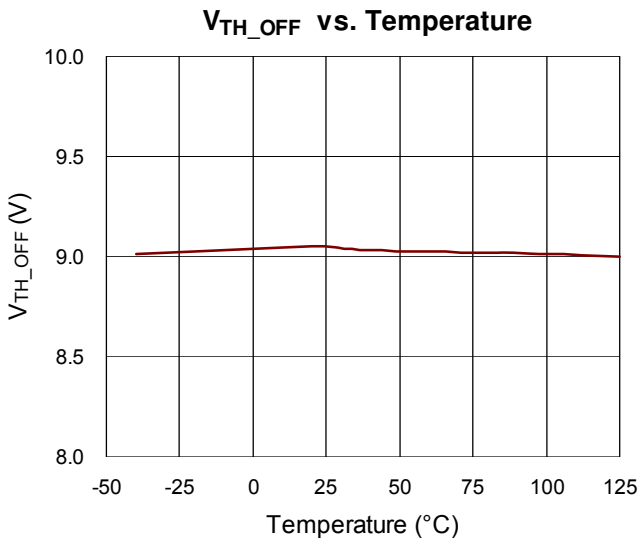
Figure 4. Application Circuit for RT7736B, RT7736D and RT7736F

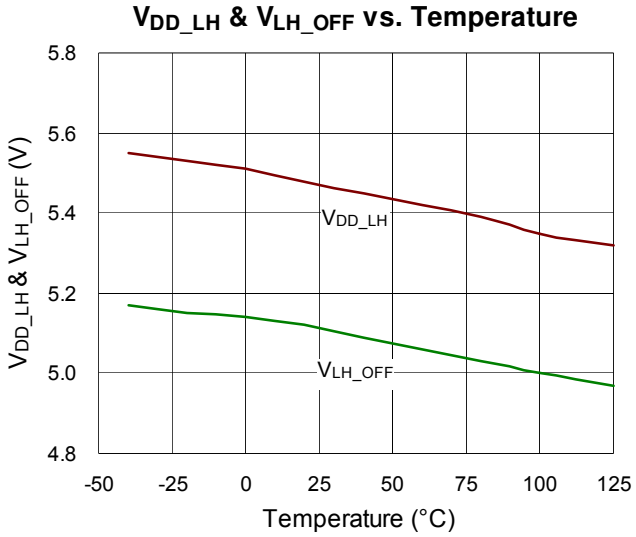
Typical Operating Characteristics

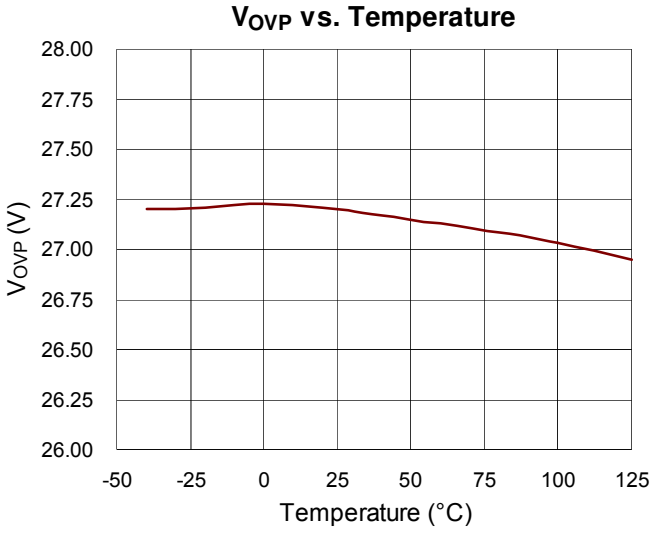


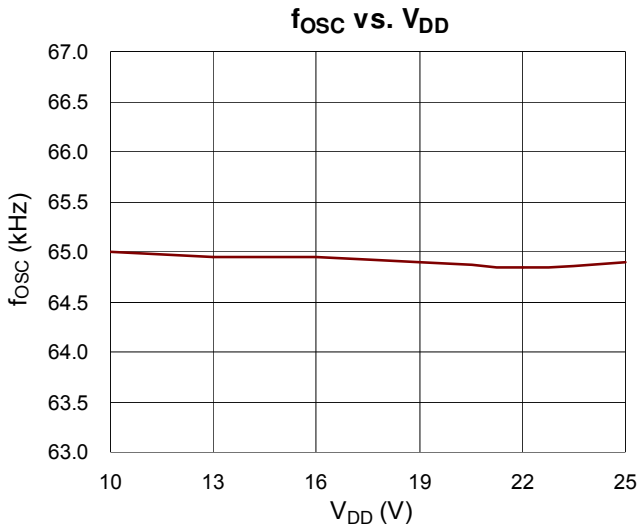


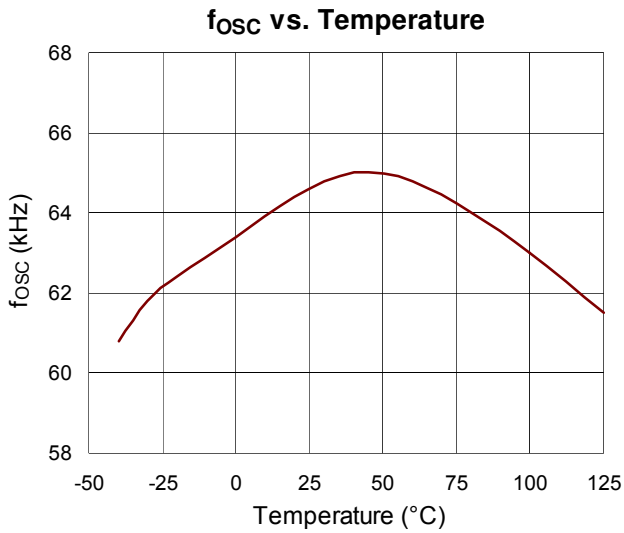


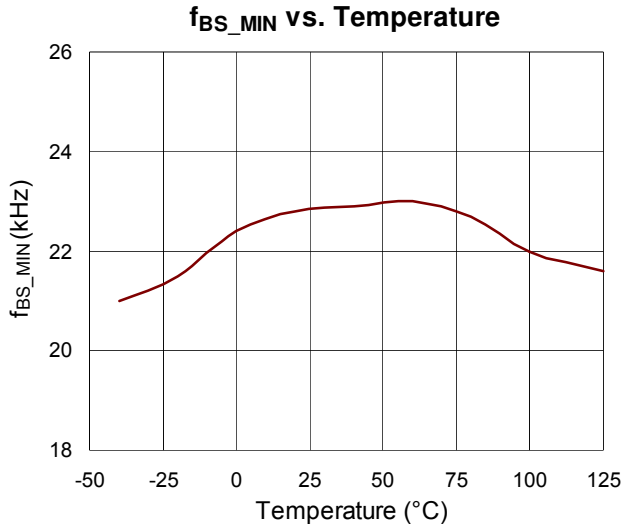


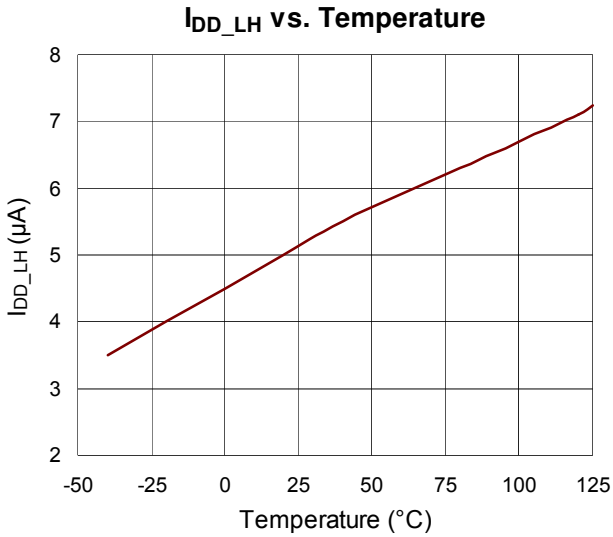


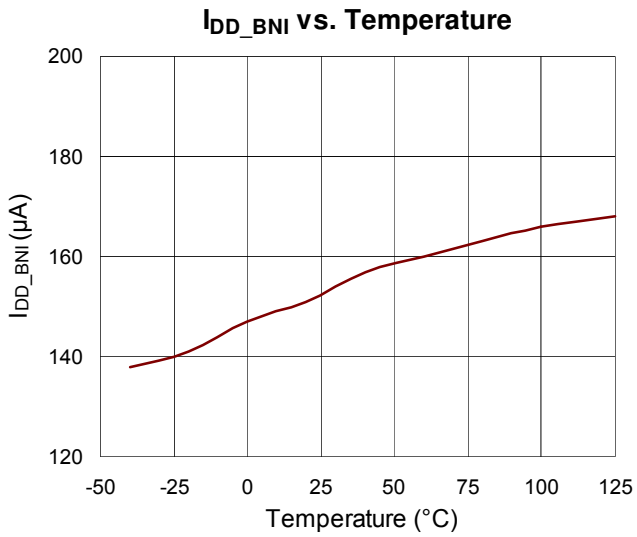


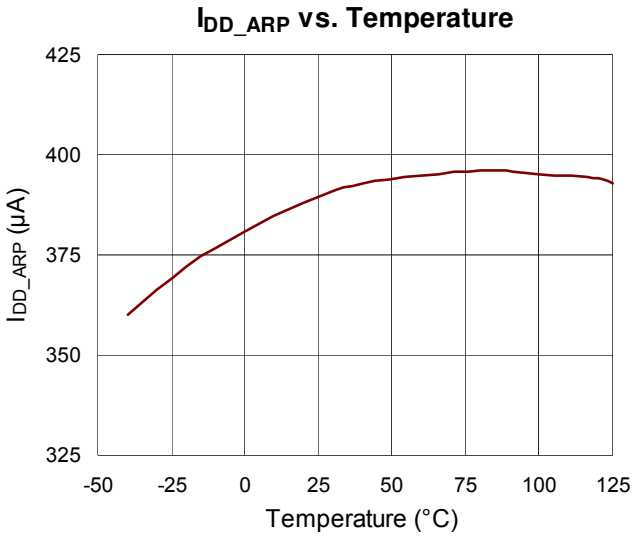




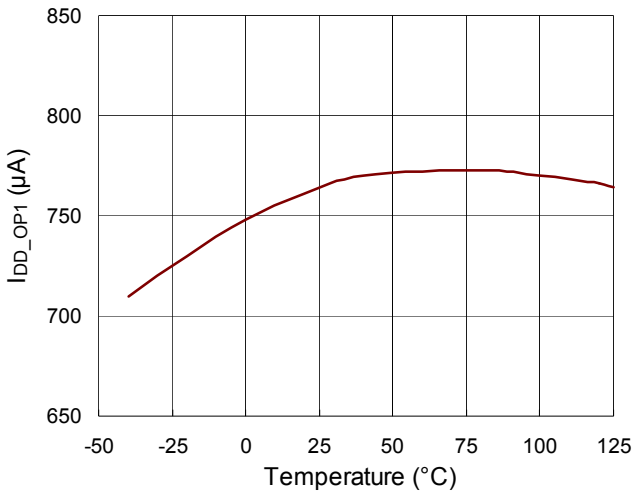




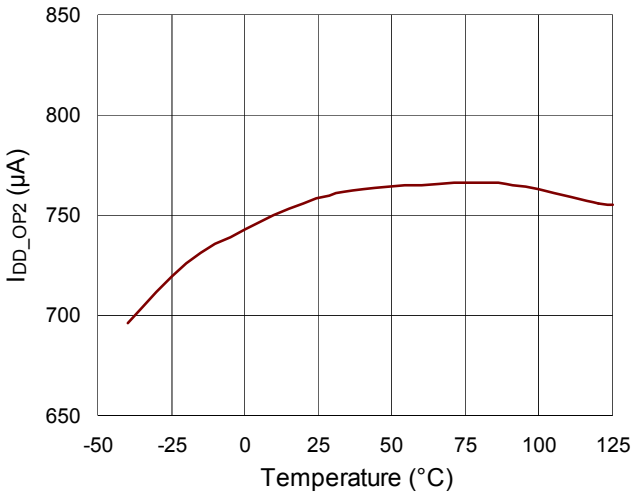




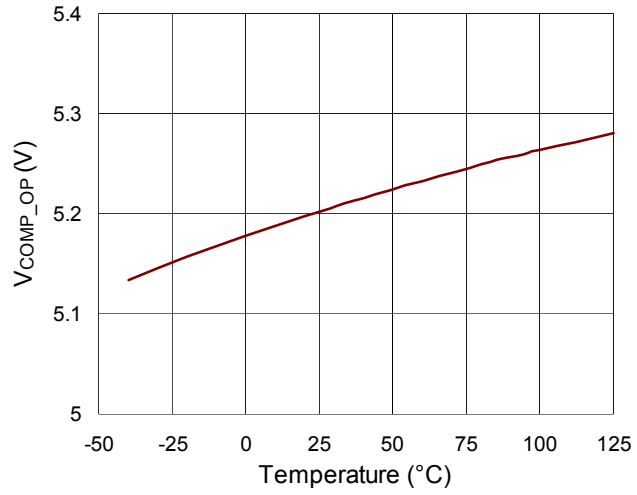
I_{DD_OP1} vs. Temperature



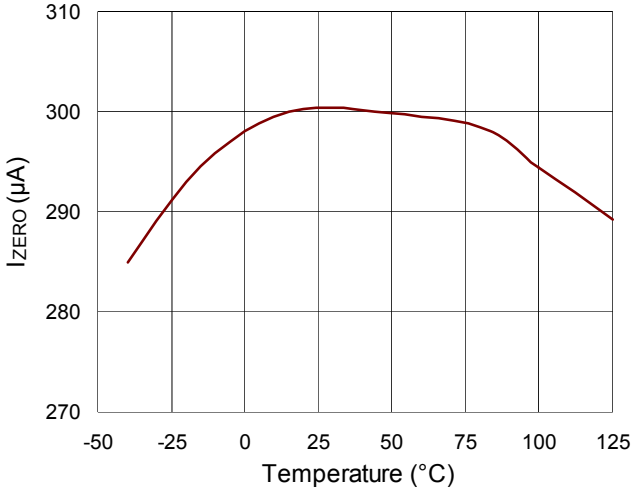
I_{DD_OP2} vs. Temperature



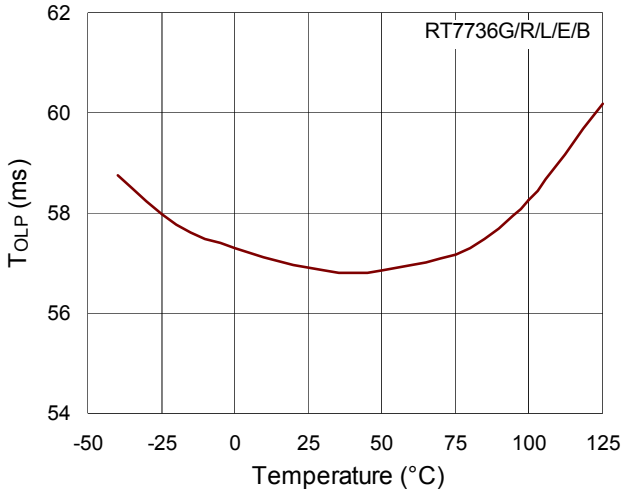
V_{COMP_OP} vs. Temperature



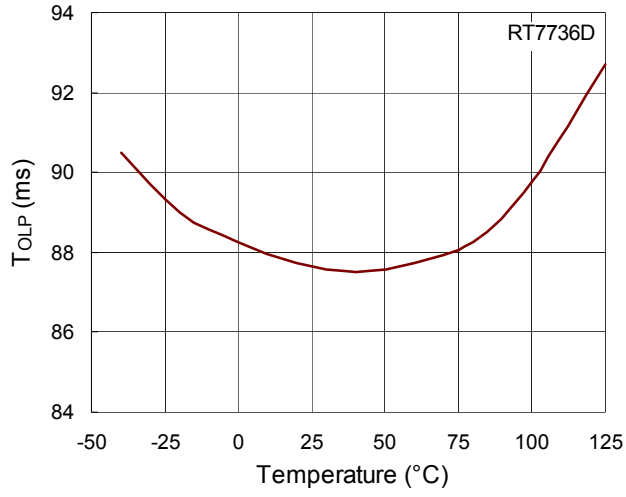
I_{ZERO} vs. Temperature



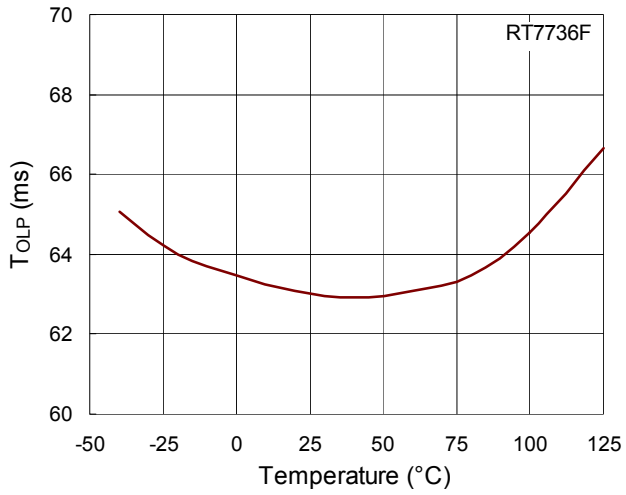
T_{OLP} vs. Temperature



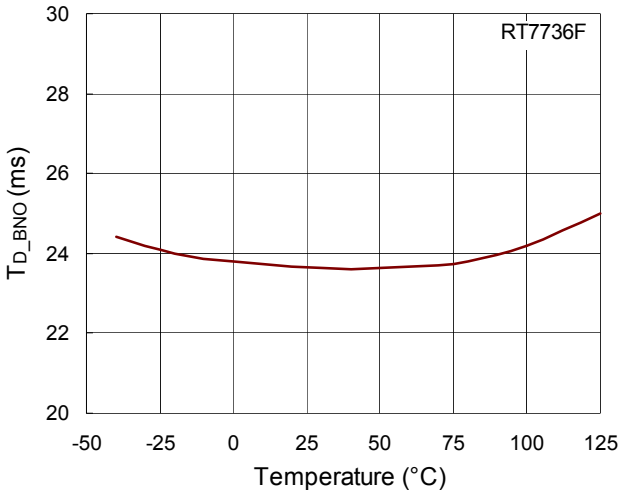
T_{OLP} vs. Temperature



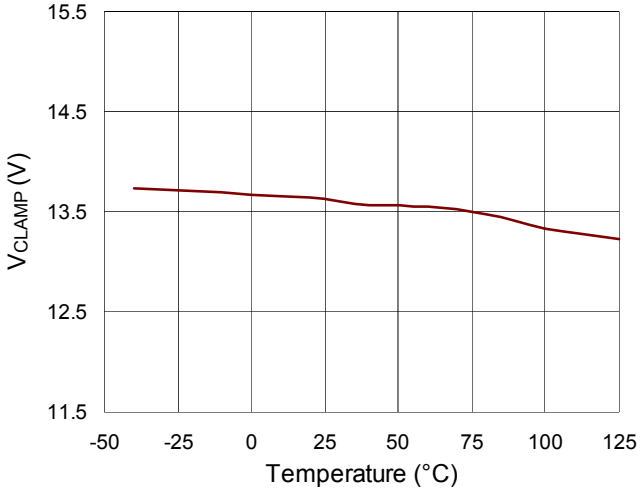
T_{OLP} vs. Temperature



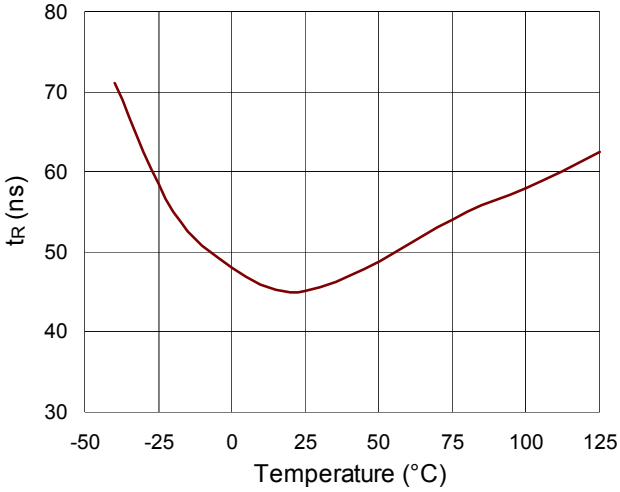
T_{D_BNO} vs. Temperature



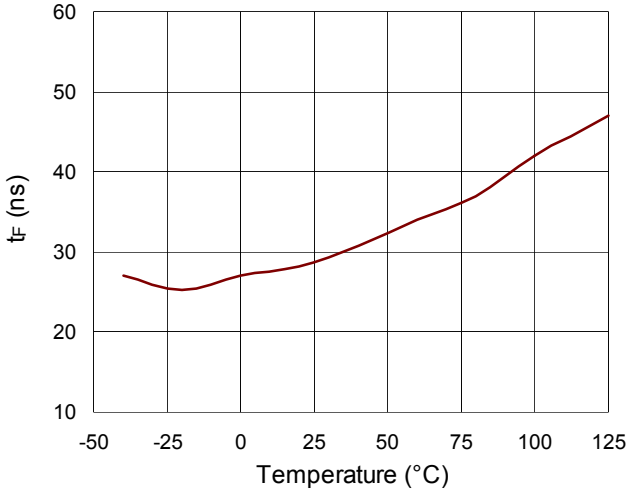
V_{CLAMP} vs. Temperature



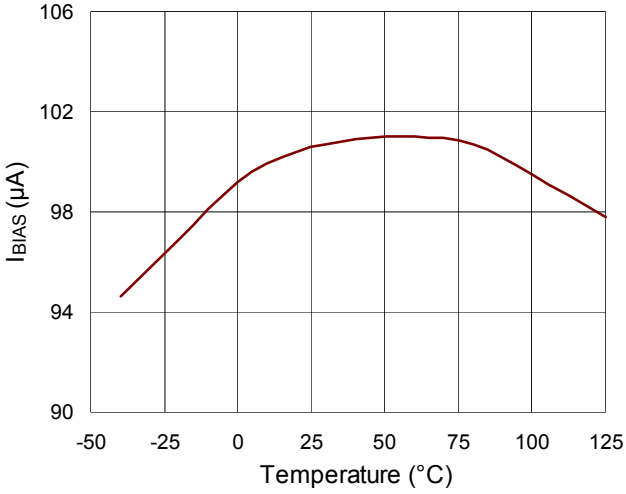
t_R vs. Temperature



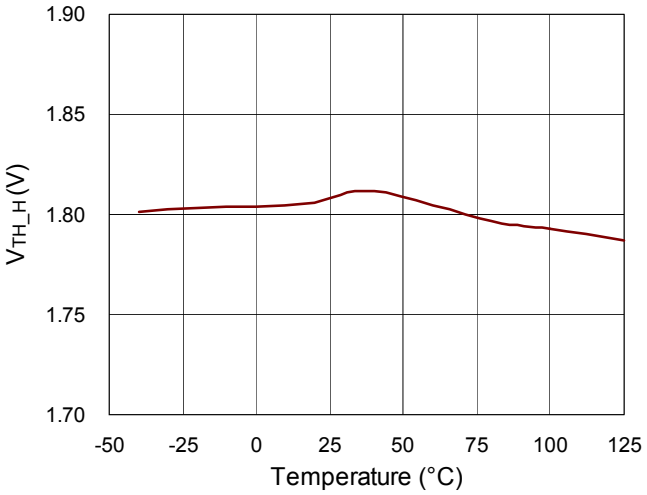
t_F vs. Temperature



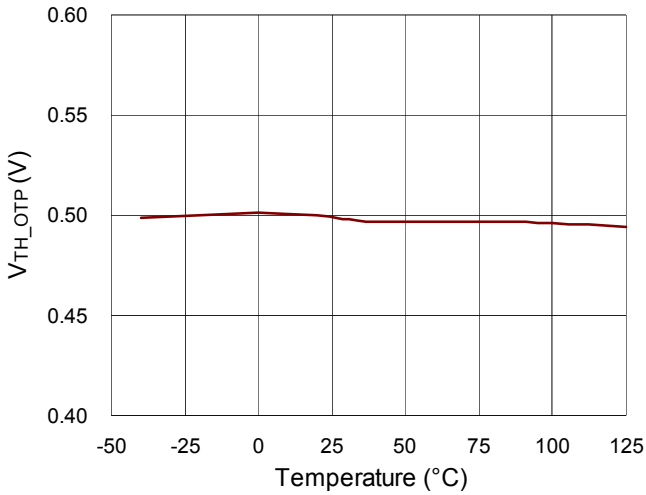
I_{BIAS} vs. Temperature



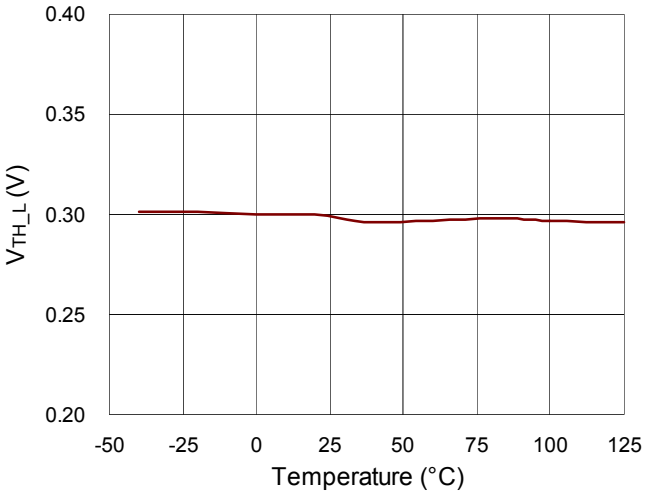
V_{TH_H} vs. Temperature



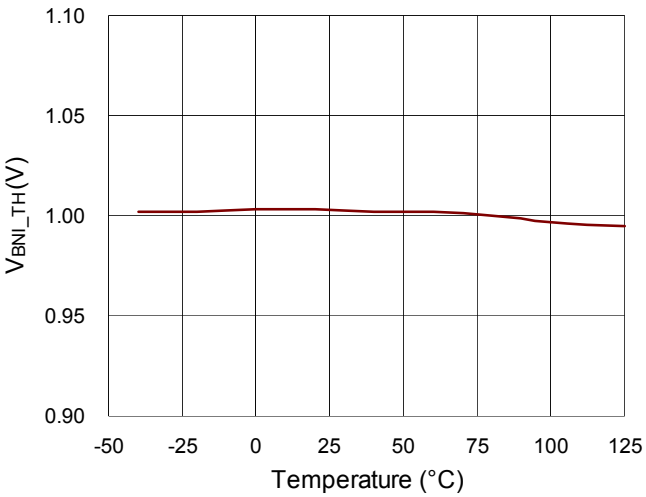
V_{TH_OTP} vs. Temperature



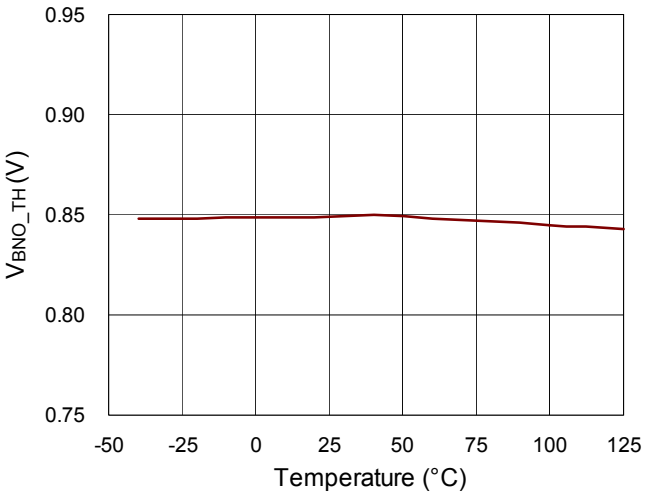
V_{TH_L} vs. Temperature



V_{BNI_TH} vs. Temperature



V_{BNO_TH} vs. Temperature



Application Information

SmartJitter™ Technology

The RT7736 series applies RICHTEK proprietary SmartJitter™ technology.

In order to reduce switching loss for lower power consumption during light load or no load, general PWM controllers have green mode function according to the feedback voltage V_{COMP}.

The output power equation is :

$$P_{o\_DCM}(V_{COMP}) = \frac{1}{2} \times L_p \times \left(\frac{x_1 \times V_{COMP}}{R_{CS}} \right)^2 \times f_s(V_{COMP}) \times \eta$$

Where L_P is the magnetizing inductance of the transformer, R_{CS} is the current sense resistor, V_{COMP} is the feedback voltage of the COMP pin. f_S is the switching frequency of the power switch, η is the conversion efficiency, and x_1 is a constant coefficient.

Output power is a function of feedback voltage V_{COMP}. Frequency jittering technique is typically used to improve EMI problems in general PWM controllers, and the frequency jittering period is based on PWM switching frequency.

When the system enters green mode, a output power relationship is formed between the feedback voltage V_{COMP} and the PWM switching frequency, and a new stable equilibrium point is eventually reached after back-and-forth adjustments. It limits the frequency jittering range is limited and the improving EMI function is poor, as shown in Figure 5.

The innovative SmartJitter™ technology not only helps reduce EMI emissions of SMPS when the system entering green mode, but also eliminates output jittering ripple.

Accurate Over-Load Protection and Tight Current Limit Tolerance

Generally, the saw current limit is applied to low cost flyback controllers because of simple design. The RT7736 series applies with RICHTEK proprietary technology through well foundry control, design and test/trim mode in final test. Therefore, the current limit tolerance is tight enough to make design and mass production easier, and it provides accurate over-load protection.

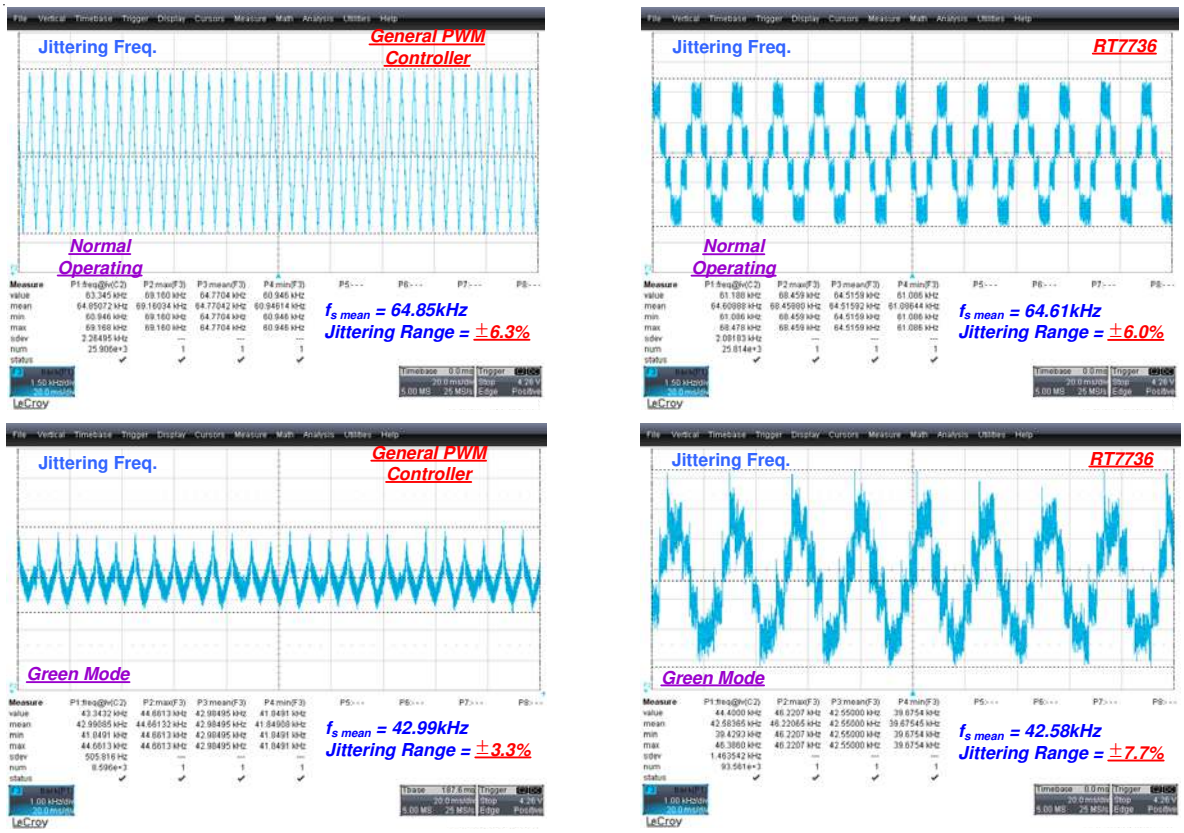


Figure 5. Frequency Jittering Range During Green Mode : General PWM Controller vs. RT7736

Start-Up Circuit

To minimize power loss, it's recommended to connect the start-up circuit to the bleeding resistors. It's power saving and also could reset latch mode protection quickly. Figure 6 shows I_{DD_Avg} vs. $R_{Bleeding}$ curve. Users can apply this curve to design the adequate bleeding resistors.

In order to prolong turn-off period and minimize the power loss and thermal rising during hiccup, the controller is designed to have smaller sinking current during entering auto-recovery protection, I_{DD_ARP}. Therefore, the start-up current at maximum AC line input voltage must be smaller than I_{DD_ARP} ($I_{DD\_ARP(min)}$ = 300μA). Otherwise, when the controller enters auto-recovery protection, the VDD capacitor won't be dropped down to V_{TH_OFF} by IC's sinking current and then restart. The controller behaves like latch protection or triggers the SCR of VDD.

The RT7736 implemented brown-in detected function (RT7736B/D/F) as described in "BNO Pin Application" section. In order to avoid start-up failure, the controller is designed to have smaller sinking current after start-up and then wait for brown-in, I_{DD_BNI}. Therefore, the start-up current at brown-in voltage of AC line input must be smaller than I_{DD_BNI} ($I_{DD\_BN\ (min)}$ = 100μA). Otherwise, the VDD voltage will rise up continuously and then trigger the SCR of VDD.

VDD Discharge Time in Auto Recovery Mode

Figure 7 shows the V_{DD} and V_{GATE} waveforms during an auto recovery protection (e.g., OLP). In this mode, the start-up resistors, VDD sinking current and VDD decoupling capacitor will affect the restart time. The discharge time $t_{D\_Discharge}$ of VDD voltage can be calculated by using the following equation :

$$t_{D\_Discharge} = \frac{C_{VDD} \times (V_{DD\_DIS} - V_{TH\_OFF})}{I_{DD\_ARP} - I_{ST}}$$

Where the C_{VDD} is the VDD decoupling capacitor, the V_{DD_DIS} is the initial VDD voltage after entering the auto recovery mode, the V_{TH_OFF} (9V typ.) is the falling UVLO voltage threshold of the controller, the I_{DD_ARP} (300μA typ.) is the sinking current of the VDD pin in the auto recovery mode, and I_{ST} is the start-up current of the power system.

Please note that the start-up current at high input voltage must be smaller than the I_{DD_ARP}. Otherwise, the VDD voltage can't reach the V_{TH_OFF} to activate the next start-up process after an auto recovery protection. Therefore, the system behavior resembles the behavior of latch mode.

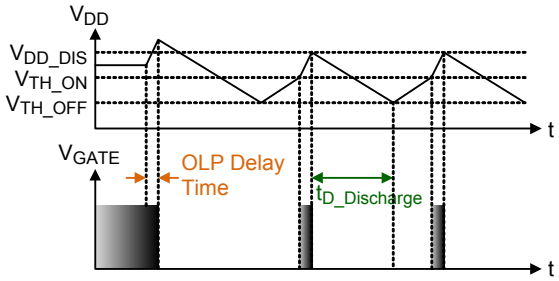


Figure 7. Auto Recovery Mode (e.g., OLP)

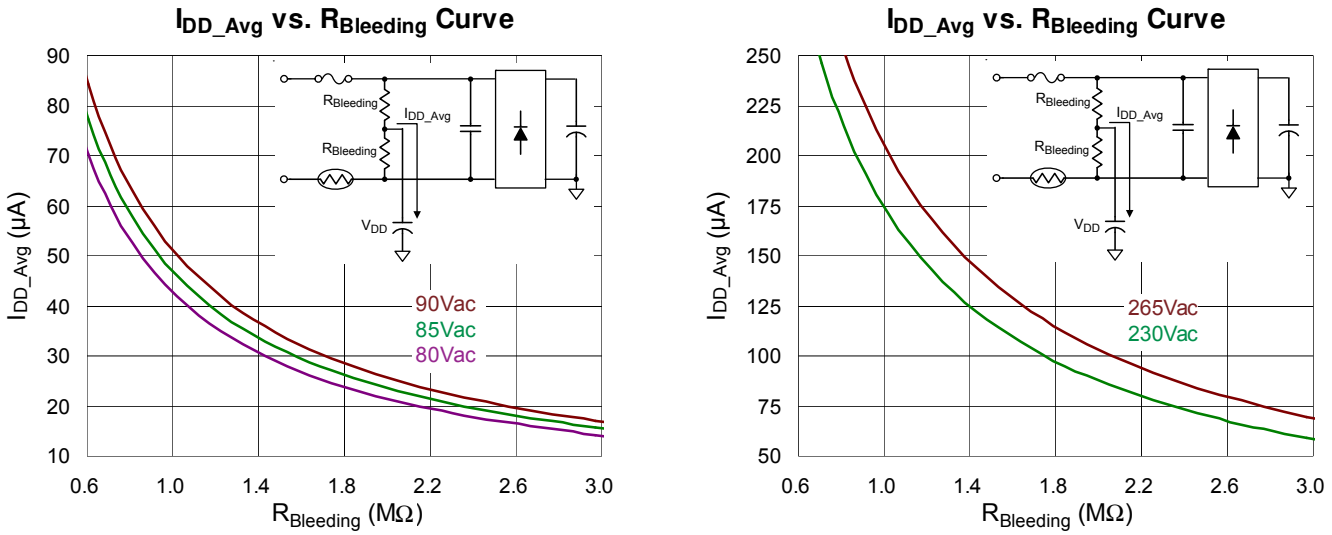


Figure 6. I_{DD_Avg} vs. $R_{Bleeding}$ Curve

VDD Holdup Mode

The VDD holdup mode is only designed to prevent VDD from decreasing to the turn-off threshold voltage under light load or load transient. Relative to burst mode, the VDD holdup mode brings higher switching. Hence, it is highly recommended that the system should avoid operating at this mode during light load or no load conditions, normally.

BNO Pin Application (RT7736B/D/F)

The RT7736 features a BNO pin (RT7736B/D/F), and it can be applied for external arbitrary brown-in/out. The BNO pin is connected to the AC line input or bulk capacitor by resistive divider to achieve brown-in/out function. Comparing the BNO pin connected to the AC line input with bulk capacitor, the advantage of the BNO pin connected to the AC line input is having brown-in/out function regardless of output loads.

Figure 8 shows the application circuit of the BNO pin connected to AC line input with resistive divider. The resistive divider (R_A and R_B) can be calculated by the following equations :

$$V_{Brown\text{-}in\_AC\_rms} \times \sqrt{2} \cong V_{BNI\_TH} \times \left(1 + \frac{R_A}{R_B}\right)$$

$$V_{Brown\text{-}out\_AC\_rms} \times \sqrt{2} \cong V_{BNO\_TH} \times \left(1 + \frac{R_A}{R_B}\right)$$

The sum of resistor values (R_A and R_B) should be smaller than 1.5MΩ because parasitic capacitors of bridge of diode may make hysteresis of brown-in/out function invalid.

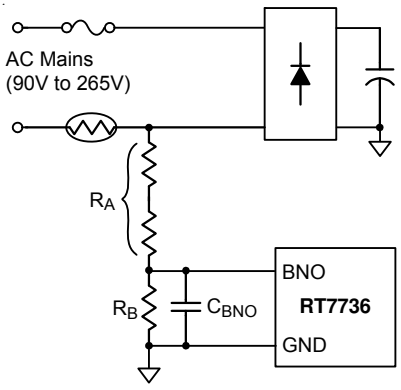


Figure 8. Brown-in/out Detected from AC Line Input

The Brown-in/out detected from bulk capacitor is shown in Figure 9, and the resistive divider (R_C and R_D) can be calculated by the following equations :

$$V_{Bulk\_Brown\text{-}in} \cong V_{BNI\_TH} \times \left(1 + \frac{R_C}{R_D}\right)$$

$$V_{Bulk\_Brown\text{-}out} \cong V_{BNO\_TH} \times \left(1 + \frac{R_C}{R_D}\right)$$

The BNO pin application from bulk capacitor can use higher resistance on the divider for power saving, but this method can't have brown-in/out function at light load because bulk capacitor still has energy stored when AC line input is turned off. The recommended bypass capacitor C_{BNO} is smaller than 1nF.

To avoid start-up failure, the RT7736 implements brown-in detected function, as shown in Figure 10. When V_{DD} is greater than V_{TH_ON}, the controller starts to operate and waits for brown-in signal. If brown-in signal is not enabled before V_{DD} falls below V_{DD_BNI}, the controller will be shut down and then re-start. If the brown-in signal V_{BNO} is higher than V_{BNI_TH}, the controller will be enabled.

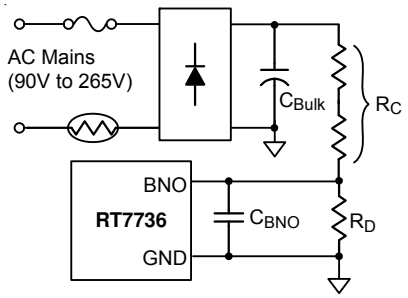


Figure 9. Brown-in/out Detected from Bulk Capacitor

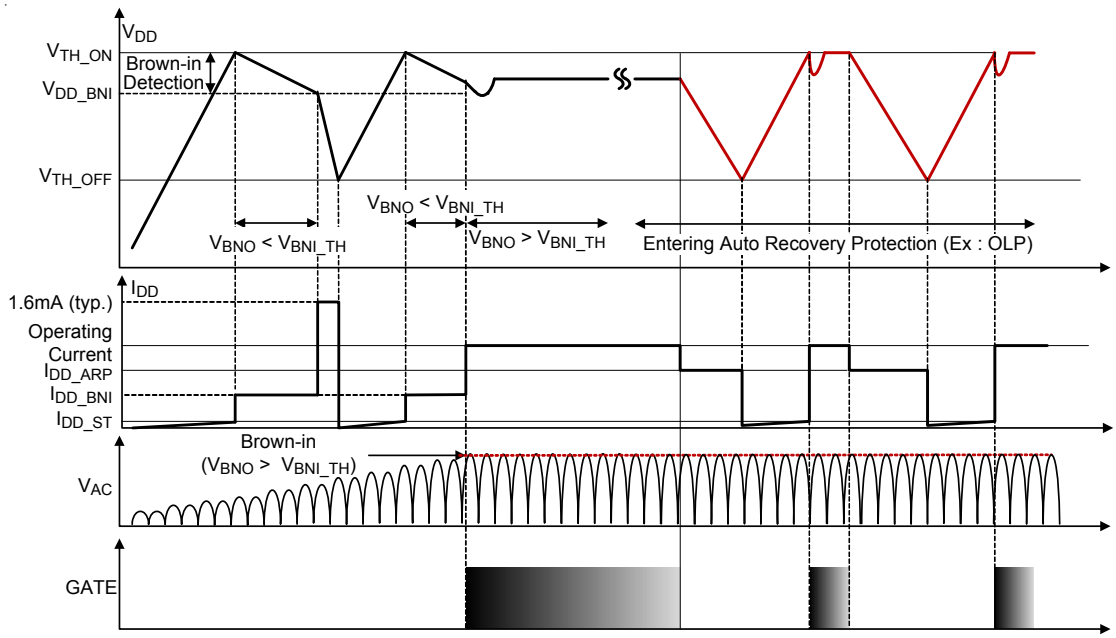


Figure 10. RT7736 Brown-in Detected Function

PRO Pin Application (RT7736G/R/L/E)

The RT7736 provides a PRO pin for external arbitrary OVP/ OTP or IC ON/OFF applications as shown in Figure 12 to Figure 15.

In Figure 11, when the voltage of the PRO pin is between V_{TH_OTP} and V_{TH_H}, the controller is enabled for normal operation. If the voltage of the PRO pin is lower than V_{TH_OTP} and higher than V_{TH_L} after delay time T_{D_OTP}, the controller will be shut down and cease switching. If the voltage of the PRO pin is higher than V_{TH_H} or lower than V_{TH_L}, the controller will be shut down and cease switching after deglitch delay.

When the voltage of the PRO pin is pulled above V_{TH_H}, the supply current of the PRO pin must be higher than 500μA and be limited below 5mA. When IC enters latch mode, V_{DD} will be clamped at latched voltage V_{DD_LH}, and it will be released until V_{DD} falls to latched reset voltage V_{LH_OFF}.

When the PRO pin is open, it is set at 1.3V internally. Leave the PRO pin open if it is not used. If designer needs to apply a bypass capacitor on the PRO pin, the capacitance should be less than 1nF. The internal bias current of the PRO pin is 100μA (typ.).

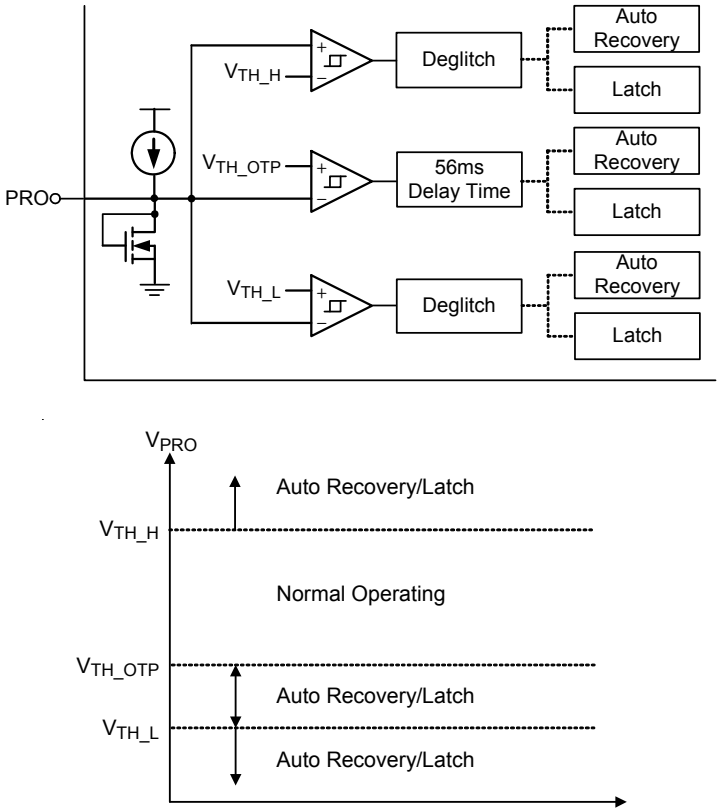


Figure 11. PRO Pin Diagram

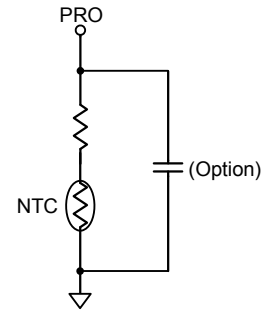


Figure 12. External OTP

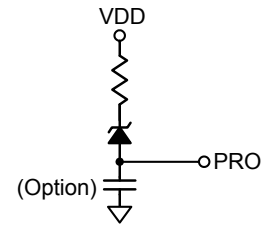


Figure 13. OVP for VDD

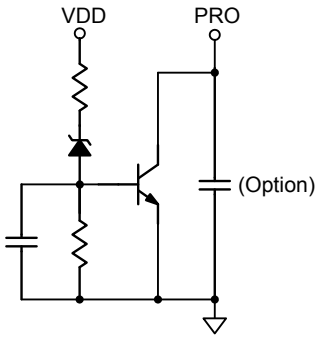


Figure 14. OVP for VDD

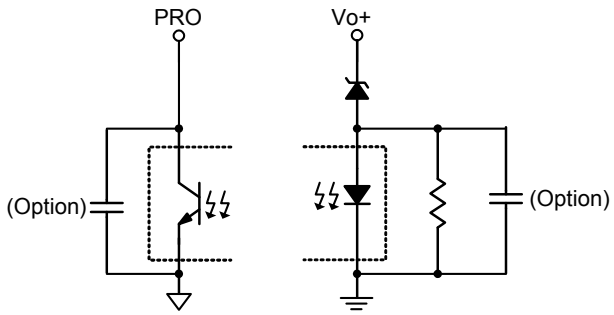


Figure 15. OVP for Output Voltage

Output Short Protection (RT7736G/R/L/E/B)

The RT7736 implements output short protection (RT7736G/R/L/E/B) by detecting GATE width with delay time T_{D_OSP}. It can minimize the power loss during output short, especially at high line input voltage.

Because it is hard to distinguish the difference between output short and big capacitance load, circuit design must be careful to make sure GATE width is larger than T_{ON_OSP} (t_{ON} > $t_{ON\_OSP(MAX)}$) after delay time T_{D_OSP} during start-up.

Resistors on GATE Pin

In Figure 16, R_G is applied to alleviate ringing spike of gate drive loop in typical application circuits. The value of R_G must be considered carefully with respect to EMI and efficiency for the system.

The built-in internal discharge resistor R_{ID} in parallel with GATE pin prevents the MOSFET from any uncertain conditions. If the connection between the GATE pin and the Gate of the MOSFET is disconnected, the MOSFET will be false triggered by the residual energy through the Gate-to-Drain parasitic capacitor C_{GD} of the MOSFET and the system will be damaged. Therefore, it's highly recommended to add an external discharge-resistor R_{ED} connected between the Gate of MOSFET and GND terminals. The energy through the C_{GD} is discharged by the external discharge-resistor to avoid MOSFET false triggering.

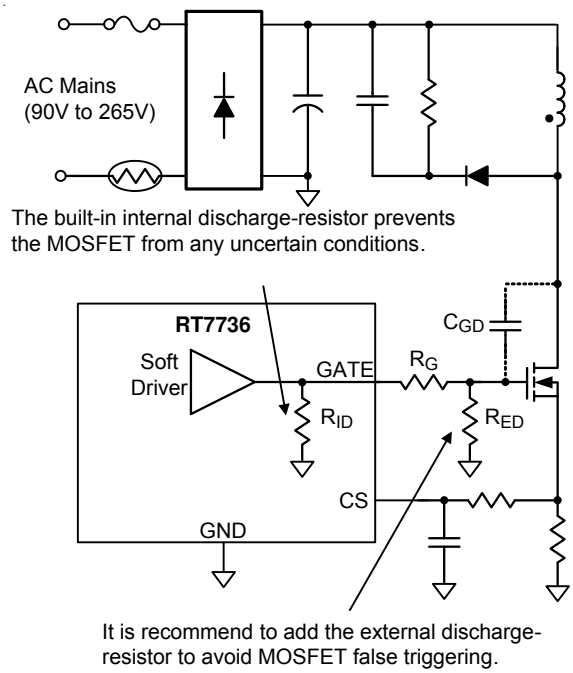


Figure 16. Resistors on Gate Pin

Feedback Resistor

In order to enhance light load efficiency, the loss of the feedback resistor in parallel with photo-coupler is reduced, as shown in Figure 17. Due to small feedback resistor current, shunt regulator selection (e.g. TL-431) and minimum regulation current design must be considered carefully to make sure it's able to regulate under low cathode current.

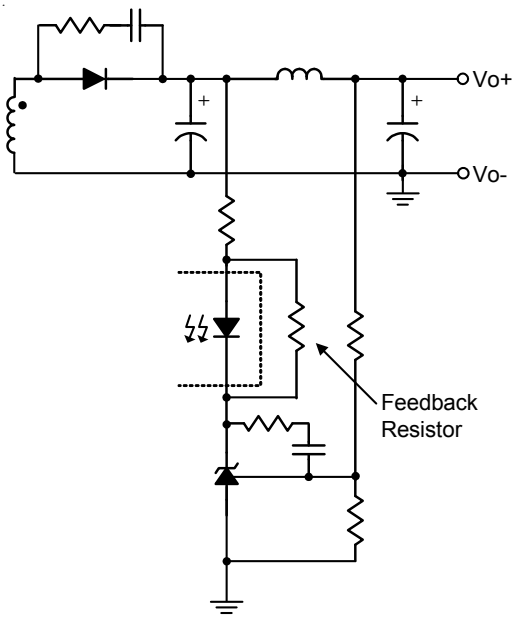


Figure 17. Feedback Resistor

Negative Voltage Spike on Each Pin

Negative voltage (< –0.3V) to the controller pins will cause substrate injection and lead to controller damage or circuit false triggering. For example, the negative spike voltage at the CS pin may come from improper PCB layout or inductive current sense resistor. Therefore, it is highly recommended to add an R-C filter to avoid the CS pin damage, as shown in Figure 18. Proper PCB layout and component selection should be considered during circuit design.

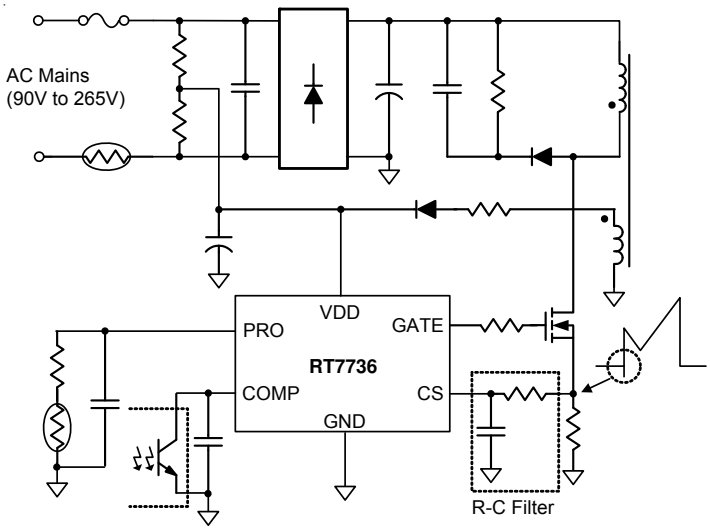


Figure 18. R-C Filter on CS Pin

Over-Temperature Protection (OTP)

The RT7736 provides an internal OTP function to protect the controller itself from suffering thermal stress and permanent damage. It's not suggested to use the function as precise control of over temperature. Once the junction temperature is higher than the OTP threshold, the controller will shut down until the temperature cools down. Meanwhile, if V_{DD} reaches turn-off threshold voltage V_{TH_OFF}, the controller will hiccup till the over-temperature condition is removed.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For

SOT-23-6 package, the thermal resistance, θ_{JA}, is 260.7°C/W on a standard JEDEC 51-3 single-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (260.7°C/W) = 0.38W for SOT-23-6 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 19 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

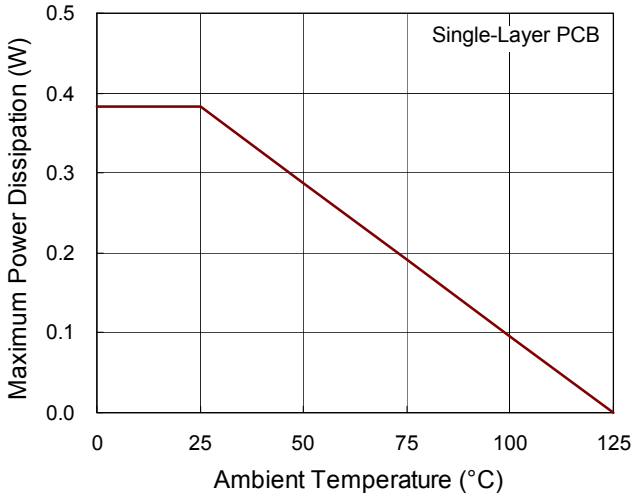


Figure 19. Derating Curve of Maximum Power Dissipation

Layout Consideration

A proper PCB layout can abate unknown noise interference and EMI issue in the switching power supply. Please refer to the guidelines when you want to design PCB layout for switching power supply :

- The current path (1) through bulk capacitor, transformer, MOSFET, R_{CS} returns to bulk capacitor is a high frequency current loop. It must be as short as possible to decrease noise coupling and keep away from other low voltage traces, such as IC control circuit paths, especially.
- The path (2) of the RCD snubber circuit is also a high switching loop. Keep it as small as possible.
- Separate the ground traces of bulk capacitor(a), MOSFET(b), auxiliary winding(c) and IC control circuit(d) for reducing noise, output ripple and EMI issue. Connect these ground traces together at bulk capacitor ground (a). The areas of these ground traces should be large enough.
- Place the bypass capacitor as close to the controller as possible.
- In order to reduce reflected trace inductance and EMI, minimize the area of the loop connecting the secondary winding, output diode and output filter capacitor. In additional, apply sufficient copper area at the anode and cathode terminal of the diode for heatsinking.

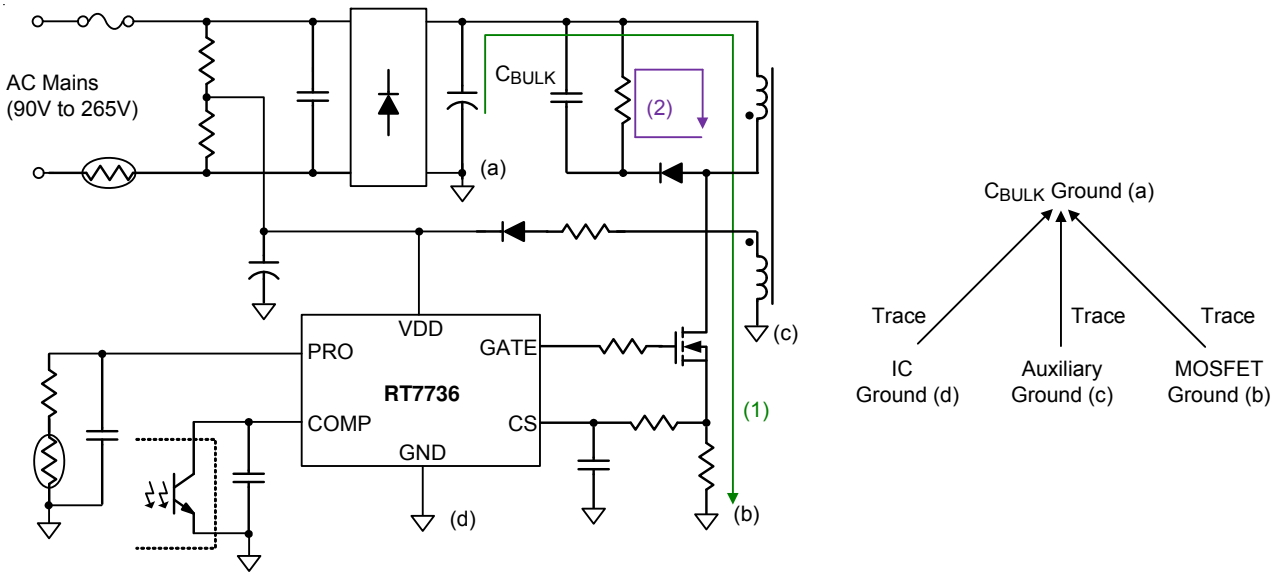
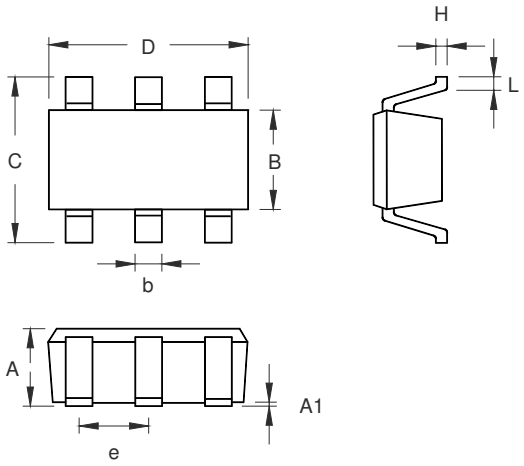


Figure 20. PCB Layout Guide

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.889	1.295	0.031	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.250	0.560	0.010	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

SOT-23-6 Surface Mount Package

Richtek Technology Corporation

14F, No. 8, Tai Yuen 1st Street, Chupei City

Hsinchu, Taiwan, R.O.C.

Tel: (8863)5526789