



PCM1716

SoundPLUS™ 24-Bit, 96kHz Sampling CMOS Delta-Sigma Stereo Audio DIGITAL-TO-ANALOG CONVERTER

FEATURES

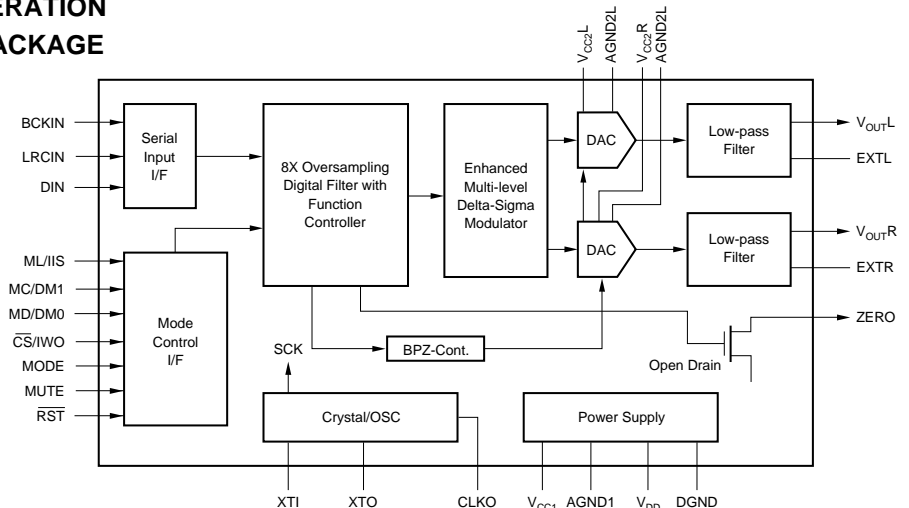
- ENHANCED MULTI-LEVEL DELTA-SIGMA DAC
- SAMPLING FREQUENCY (f_s): 16kHz - 96kHz
- INPUT AUDIO DATA WORD: 16-, 20-, 24-Bit
- HIGH PERFORMANCE: THD+N: -96dB
Dynamic Range: 106dB
SNR: 106dB
Analog Output Range: $0.62 \times V_{CC}$ (Vp-p)
- 8x OVERSAMPLING DIGITAL FILTER: Stop Band Attenuation: -82dB
Passband Ripple: ± 0.002 dB
Slow Roll Off
- MULTI FUNCTIONS: Digital De-emphasis
L/R Independent Digital Attenuation
Soft Mute
Zero Detect Mute
Zero Flag
Chip Select
Reversible Output Phase
- +5V SINGLE SUPPLY OPERATION
- SMALL 28-LEAD SSOP PACKAGE

DESCRIPTION

The PCM1716 is designed for Mid to High grade Digital Audio applications which achieve 96kHz sampling rates with 24-bit audio data. PCM1716 uses a newly developed, enhanced multi-level delta-sigma modulator architecture that improves audio dynamic performance and reduces jitter sensitivity in actual applications.

The internal digital filter operates at 8x over sampling at a 96kHz sampling rate, with two kinds of roll-off performances that can be selected: sharp roll-off, or slow roll-off, as required for specific applications.

PCM1716 is suitable for Mid to High grade audio applications such as CD, DVD-Audio, and Music Instruments, since the device has superior audio dynamic performance, 24-bit resolution and 96kHz sampling.



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Internet: <http://www.burr-brown.com/> • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

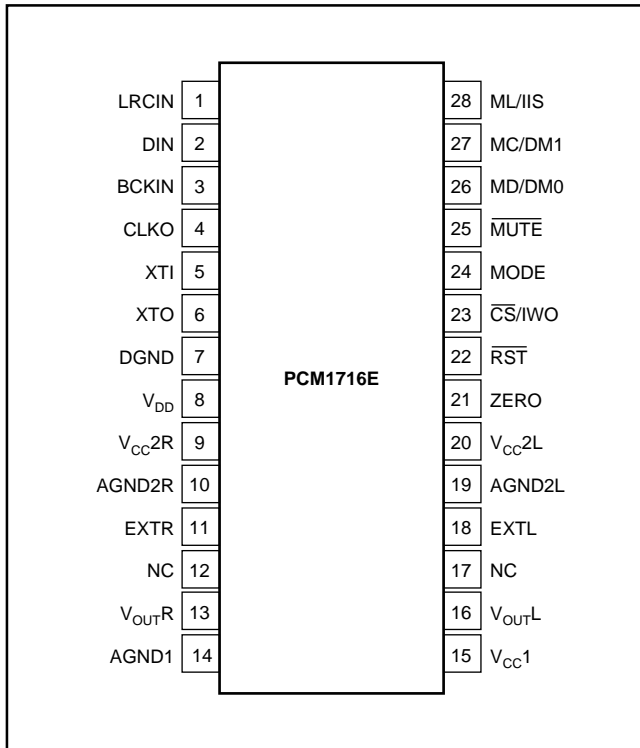
SPECIFICATIONS

All specifications at +25°C, +V_{CC} = +V_{DD} = +5V, f_S = 44.1kHz, and 24-bit input data, SYSCLK = 384f_S, unless otherwise noted.

| PARAMETER | CONDITIONS | PCM1716 | | | UNITS |
|---|--|---|--|---|--|
| | | MIN | TYP | MAX | |
| RESOLUTION | | | 24 | | Bits |
| DATA FORMAT Audio Data Interface Format Data Bit Length Audio Data Format Sampling Frequency (f _S) System Clock Frequency ⁽¹⁾ | | 16 | Standard/I ² S 16/20/24 Selectable MSB First, 2's Comp 256/384/512/768f _S | 96 | kHz |
| DIGITAL INPUT/OUTPUT LOGIC LEVEL Input Logic Level Output Logic Level (CLKO) | V _{IH} V _{IL} V _{OH} V _{OL} I _{OH} = 2mA I _{OL} = 4mA | 2.0 4.5 | | 0.8 0.5 | V V V V |
| CLKO PERFORMANCE⁽²⁾ Output Rise Time Output Fall Time Output Duty Cycle | 20 ~ 80% V _{DD} , 10pF 80 ~ 20% V _{DD} , 10pF 10pF Load | | 5.5 4 37 | | ns ns % |
| DYNAMIC PERFORMANCE⁽³⁾ (24-Bit Data) THD+N Dynamic Range Signal-to-Noise Ratio ⁽⁴⁾ Channel Separation | V _O = 0dB V _O = -60dB f _S = 44.1kHz f _S = 96kHz f _S = 44.1kHz f _S = 44.1kHz EIAJ A-weighted f _S = 96kHz A-weighted f _S = 44.1kHz EIAJ A-weighted f _S = 96kHz A-weighted f _S = 44.1kHz f _S = 96kHz | | -97 -94 -42 106 103 106 103 102 101 | -90 | dB dB dB dB dB dB dB dB dB |
| DYNAMIC PERFORMANCE⁽³⁾ (16-Bit Data) THD+N Dynamic Range | V _O = 0dB f _S = 44.1kHz f _S = 96kHz f _S = 44.1kHz EIAJ A-weighted f _S = 96kHz A-weighted | | -94 -92 98 97 | | dB dB dB dB |
| DC ACCURACY Gain Error Gain Mismatch: Channel-to-Channel Bipolar Zero Error | V _O = 0.5V _{CC} at Bipolar Zero | | ±1.0 ±1.0 ±30 | ±3.0 ±3.0 ±60 | % of FSR % of FSR mV |
| ANALOG OUTPUT Output Voltage Center Voltage Load Impedance | Full Scale (0dB) AC Load | | 0.62 V _{CC} 0.5 V _{CC} 5 | | V _{p-p} V kΩ |
| DIGITAL FILTER PERFORMANCE Filter Characteristics 1 (Sharp Roll-Off) Passband Stopband Passband Ripple Stopband Attenuation Filter Characteristics 2 (Slow Roll-Off) Passband Stopband Passband Ripple Stopband Attenuation Delay Time De-emphasis Error | ±0.002dB -3dB Stop Band = 0.546f _S Stop Band = 0.567f _S ±0.002dB -3dB Stopband = 0.732f _S | 0.546f _S -75 -82 0.732f _S -82 | | 0.454f _S 0.490f _S ±0.002 0.274f _S 0.454f _S ±0.002 30/f _S ±0.1 | dB dB dB dB dB dB sec dB |
| INTERNAL ANALOG FILTER -3dB Bandwidth Passband Response | f = 20kHz | | 100 -0.16 | | kHz dB |
| POWER SUPPLY REQUIREMENTS Voltage Range Supply Current: I _{CC} + I _{DD} Power Dissipation | V _{DD} , V _{CC} f _S = 44.1kHz f _S = 96kHz f _S = 44.1kHz f _S = 96kHz | 4.5 | 5 32 45 160 225 | 5.5 45 225 | VDC mA mA mW mW |
| TEMPERATURE RANGE Operation Storage | | -25 -55 | | +85 +100 | °C °C |

NOTES: (1) Refer section of system clock. (2) External buffer is recommended. (3) Dynamic performance specs are tested with 20kHz low pass filter and THD+N specs are tested with 30kHz LPF, 400Hz HPF, Average Mode. (4) SNR is tested at internally infinity zero detection off.

PIN CONFIGURATION



PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER ⁽¹⁾ |
|----------|-------------|---------------------------------------|
| PCM1716E | 28-Pin SSOP | 324 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

| | |
|---|-----------------------------------|
| Power Supply Voltage | +6.5V |
| +V _{CC} to +V _{DD} Difference | ±0.1V |
| Input Logic Voltage | -0.3V to (V _{DD} + 0.3V) |
| Input Current (except power supply) | ±10mA |
| Power Dissipation | 400mW |
| Operating Temperature Range | -25°C to +85°C |
| Storage Temperature | -55°C to +125°C |
| Lead Temperature (soldering, 5s) | +260°C |

PIN ASSIGNMENTS

| PIN | NAME | I/O | DESCRIPTION |
|-----|---------------------|-----|---|
| 1 | LRCIN | IN | Left and Right Clock Input. This clock is equal to the sampling rate - f_s . ⁽¹⁾ |
| 2 | DIN | IN | Serial Audio Data Input ⁽¹⁾ |
| 3 | BCKIN | IN | Bit Clock Input for Serial Audio Data. ⁽¹⁾ |
| 4 | CLKO | OUT | Buffered Output of Oscillator. Equivalent to System Clock. |
| 5 | XTI | IN | Oscillator Input (External Clock Input) |
| 6 | XTO | OUT | Oscillator Output |
| 7 | DGND | — | Digital Ground |
| 8 | V _{DD} | — | Digital Power +5V |
| 9 | V _{CC2R} | — | Analog Power +5V |
| 10 | AGND2R | — | Analog Ground |
| 11 | EXTR | OUT | Rch, Common Pin of Analog Output Amp |
| 12 | NC | — | No Connection |
| 13 | V _{OUTR} | OUT | Rch, Analog Voltage Output of Audio Signal |
| 14 | AGND1 | — | Analog Ground |
| 15 | V _{CC1} | — | Analog Power +5V |
| 16 | V _{OUTL} | OUT | Lch, Analog Voltage Output of Audio Signal |
| 17 | NC | — | No Connection |
| 18 | EXTL | OUT | Lch, Common Pin of Analog Output Amp |
| 19 | AGND2L | — | Analog Ground |
| 20 | V _{CC2L} | — | Analog Power +5V |
| 21 | ZERO | OUT | Zero Data Flag |
| 22 | RST | IN | Reset. When this pin is low, the DF and modulators are held in reset. ⁽²⁾ |
| 23 | CS/IWO | IN | Chip Select/Input Format Selection. When this pin is low, the Mode Control is effective. ⁽³⁾ |
| 24 | MODE | IN | Mode Control Select. (H: Software, L: Hardware) ⁽²⁾ |
| 25 | MUTE | IN | Mute Control |
| 26 | MD/DM0 | IN | Mode Control, DATA/De-emphasis Selection 1 ⁽²⁾ |
| 27 | MC/DM1 | IN | Mode Control, BCK/De-emphasis Selection 2 ⁽²⁾ |
| 28 | ML/I ² S | IN | Mode Control, WDCK/Input Format Selection ⁽²⁾ |

NOTES: (1) Pins 1, 2, 3; Schmitt Trigger input. (2) Pins 22, 24, 25, 26, 27, 28; Schmitt Trigger input with pull-up resistor. (3) Pin 23; Schmitt Trigger input with pull-down resistor.



ELECTROSTATIC DISCHARGE SENSITIVITY

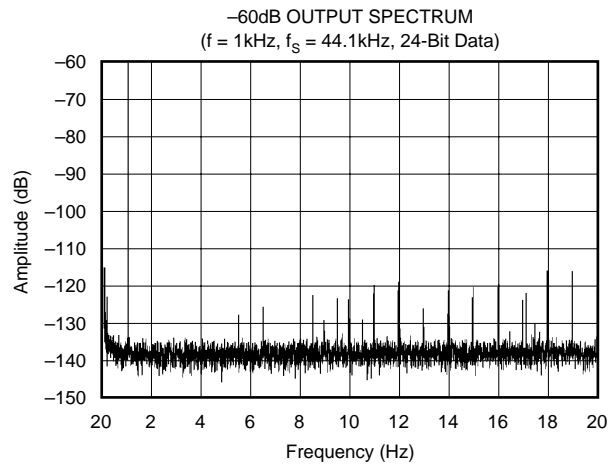
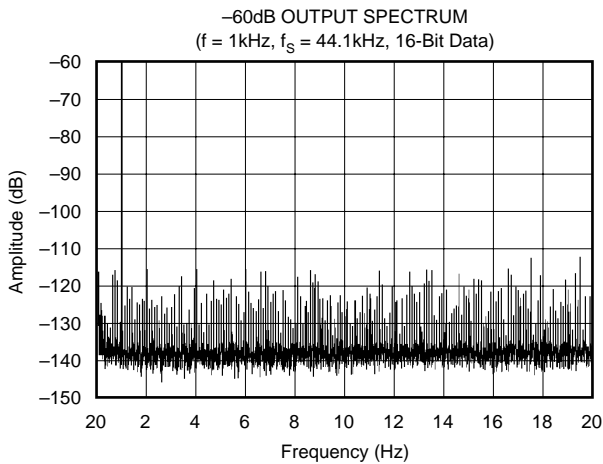
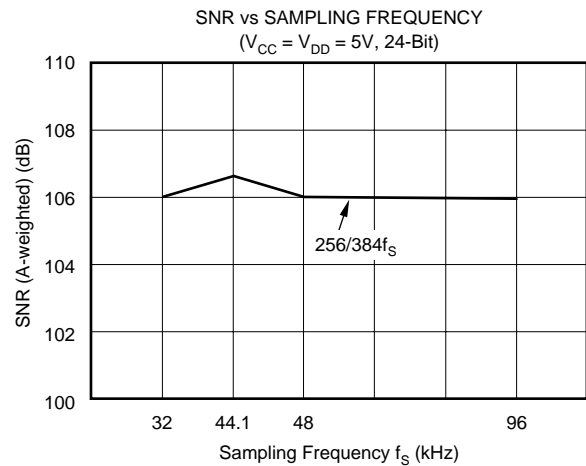
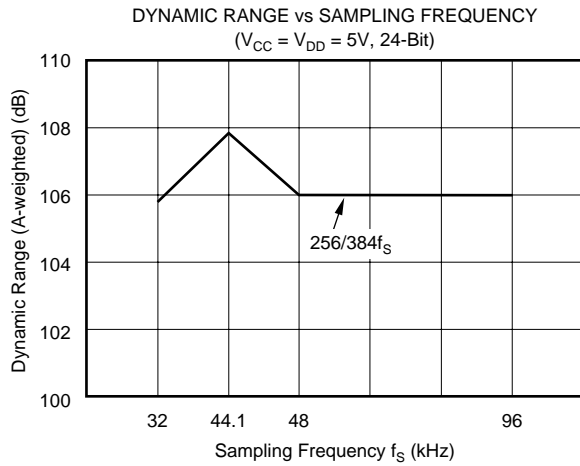
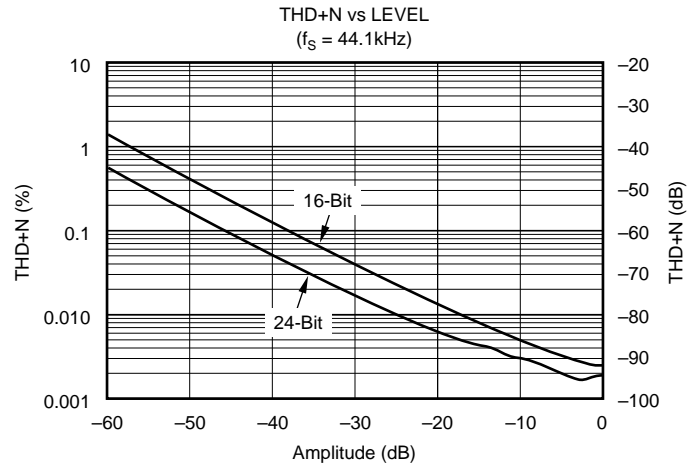
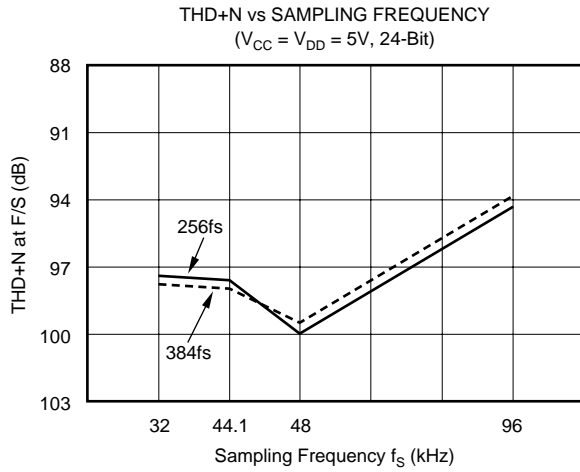
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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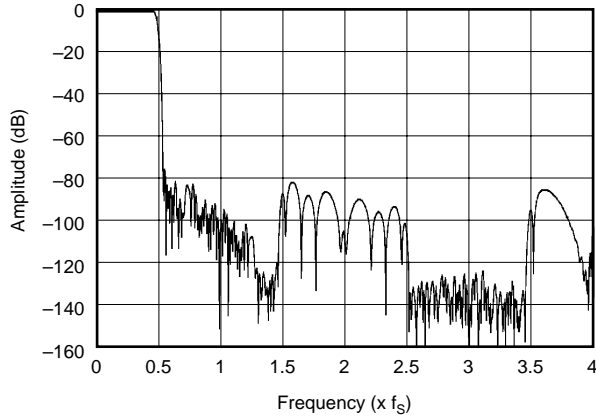
TYPICAL PERFORMANCE CURVES

All specifications at +25°C, +V_{CC} = +V_{DD} = +5V, f_S = 44.1kHz, and 24-bit input data, SYSCLK = 384f_S, unless otherwise noted.

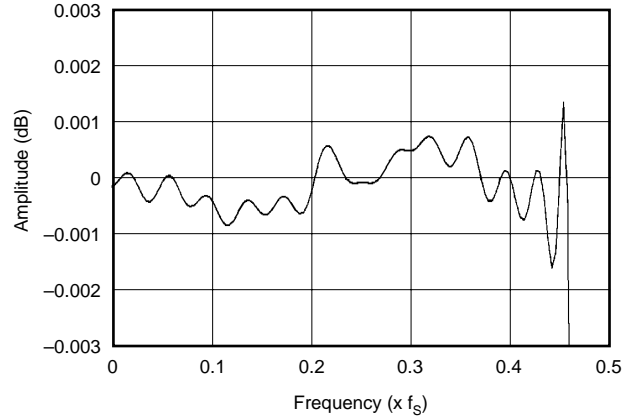


TYPICAL PERFORMANCE CURVES (CONT)

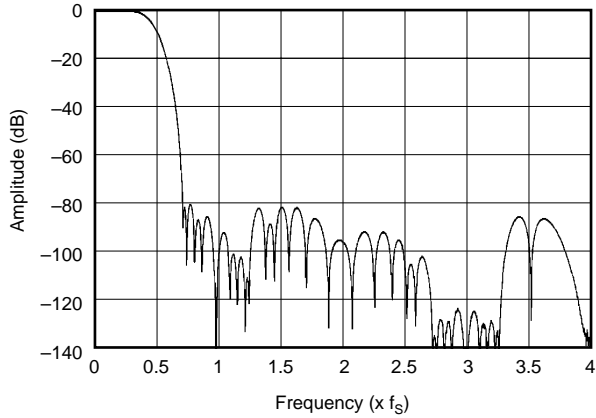
OVERALL FREQUENCY CHARACTERISTIC
(Sharp Roll-Off)



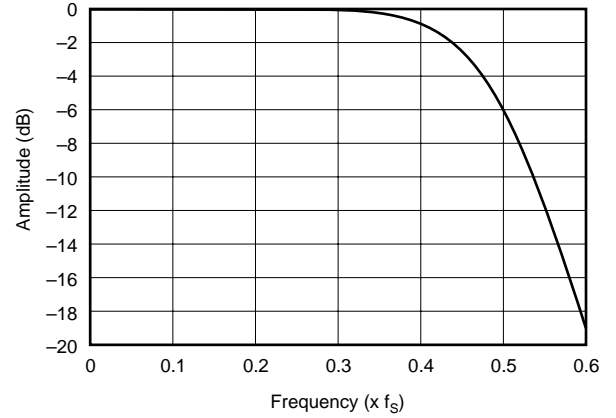
PASSBAND RIPPLE CHARACTERISTIC
(Sharp Roll-Off)



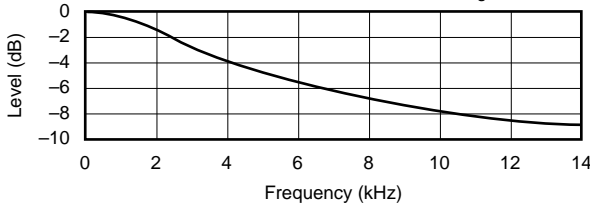
OVERALL FREQUENCY CHARACTERISTIC
(Slow Roll-Off)



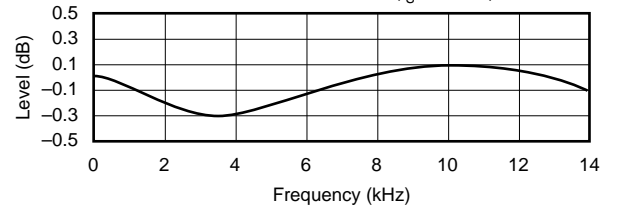
FREQUENCY CHARACTERISTIC
(Slow Roll-Off)



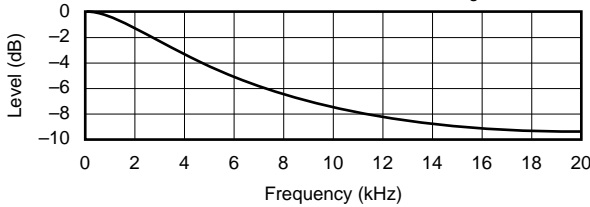
DE-EMPHASIS FREQUENCY RESPONSE ($f_s = 32\text{kHz}$)



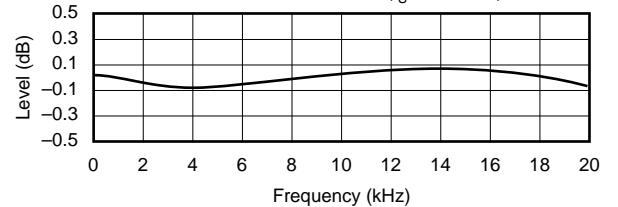
DE-EMPHASIS ERROR ($f_s = 32\text{kHz}$)



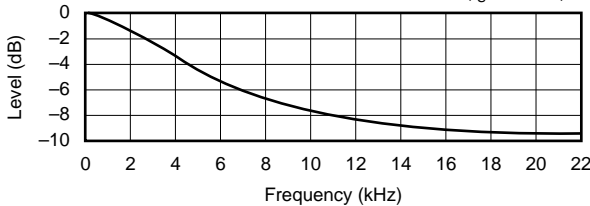
DE-EMPHASIS FREQUENCY RESPONSE ($f_s = 44.1\text{kHz}$)



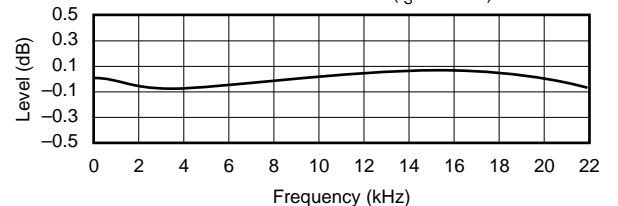
DE-EMPHASIS ERROR ($f_s = 44.1\text{kHz}$)



DE-EMPHASIS FREQUENCY RESPONSE ($f_s = 48\text{kHz}$)



DE-EMPHASIS ERROR ($f_s = 48\text{kHz}$)



SYSTEM CLOCK

The system clock for PCM1716 must be either $256f_s$, $384f_s$, $512f_s$ or $768f_s$, where f_s is the audio sampling frequency (typically 32kHz, 44.1kHz, 48kHz, or 96kHz). But $768f_s$ at 96kHz is not accepted.

The system clock can be either a crystal oscillator placed between XTI (pin 5) and XTO (pin 6), or an external clock input to XTI. If an external system clock is used, XTO is open (floating). Figure 1 illustrates the typical system clock connections.

PCM1716 has a system clock detection circuit which automatically senses if the system clock is operating at $256f_s \sim 768f_s$. The system clock should be synchronized with LRCIN (pin 1) clock. LRCIN (left-right clock) operates at the sampling frequency f_s . In the event these clocks are not synchronized, PCM1716 can compensate for the phase difference internally. If the phase difference between left-right and system clocks is greater than 6-bit clocks (BCKIN), the synchronization is performed internally. While the synchronization is processing, the analog output is forced to a DC level at bipolar zero. The synchronization typically occurs in less than 1 cycle of LRCIN.

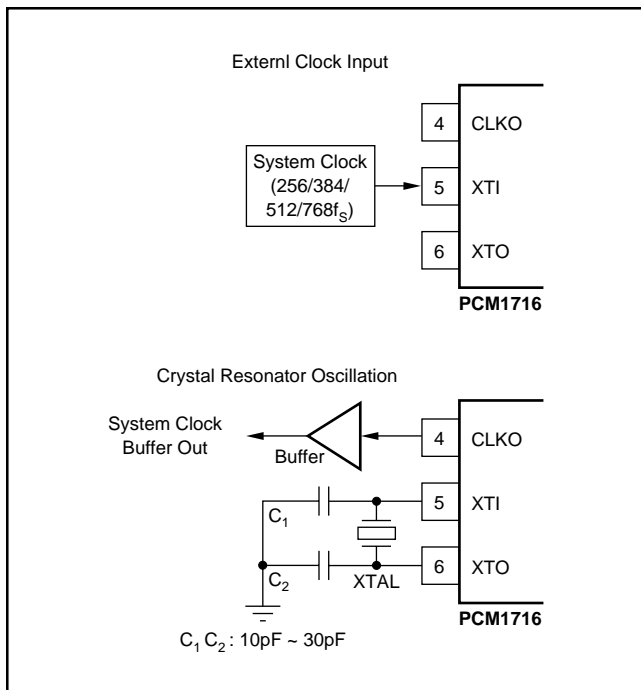


FIGURE 1. System Clock Connection.

Typical input system clock frequencies to the PCM1716 are shown in Table I, also, external input clock timing requirements are shown in Figure 2.

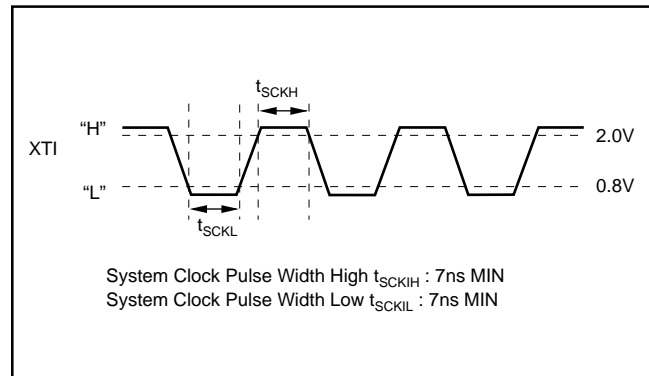


FIGURE 2. XTI Clock Timing.

DATA INTERFACE FORMATS

Digital audio data is interfaced to PCM1716 on pins 1, 2, and 3, LRCIN (left-right clock), DIN (data input) and BCKIN (bit clock). PCM1716 can accept both standard, I²S, and left justified data formats.

Figure 3 illustrates acceptable input data formats. Figure 4 shows required timing specification for digital audio data.

Reset

PCM1716 has both internal power-on reset circuit and the \overline{RST} pin (pin 22) which accepts an external forced reset by $\overline{RST} = \text{LOW}$. For internal power on reset, initialize (reset) is done automatically at power on $V_{DD} > 2.2\text{V}$ (typ). During internal reset = LOW, the output of the DAC is invalid and the analog outputs are forced to $V_{CC}/2$. Figure 5 illustrates the timing of the internal power on reset.

PCM1716 accepts an external forced reset when $\overline{RST} = \text{L}$. When $\overline{RST} = \text{L}$, the output of the DAC is invalid and the analog outputs are forced to $V_{CC}/2$ after internal initialization (1024 system clocks count after $\overline{RST} = \text{H}$.) Figure 6 illustrates the timing of the \overline{RST} pin.

Zero Out (pin 21)

If the input data is continuously zero for 65536 cycles of BCK, an internal FET is switched to "ON". The drain of the internal FET is the zero-pin, it will enable "wired-or" with external circuit. This zero detect function is available in both software mode and hardware mode.

| SAMPLING RATE FREQUENCY (f_s) - LRCIN | SYSTEM CLOCK FREQUENCY - MHz | | | |
|---|------------------------------|------------------------|------------------------|------------------------|
| | 256 f_s | 384 f_s | 512 f_s | 768 f_s |
| 32kHz | 8.1920 | 12.2880 | 16.3840 | 24.5760 |
| 44.1kHz | 11.2896 | 16.9340 | 22.5792 | 33.8688 ⁽¹⁾ |
| 48kHz | 12.2880 | 18.4320 | 24.5760 | 36.8640 ⁽¹⁾ |
| 96kHz | 24.5760 | 36.8640 ⁽¹⁾ | 49.1520 ⁽¹⁾ | — |

NOTE: (1) The Internal Crystal oscillator frequency cannot be larger than 24.576MHz.

TABLE I. Typical System Clock Frequency.

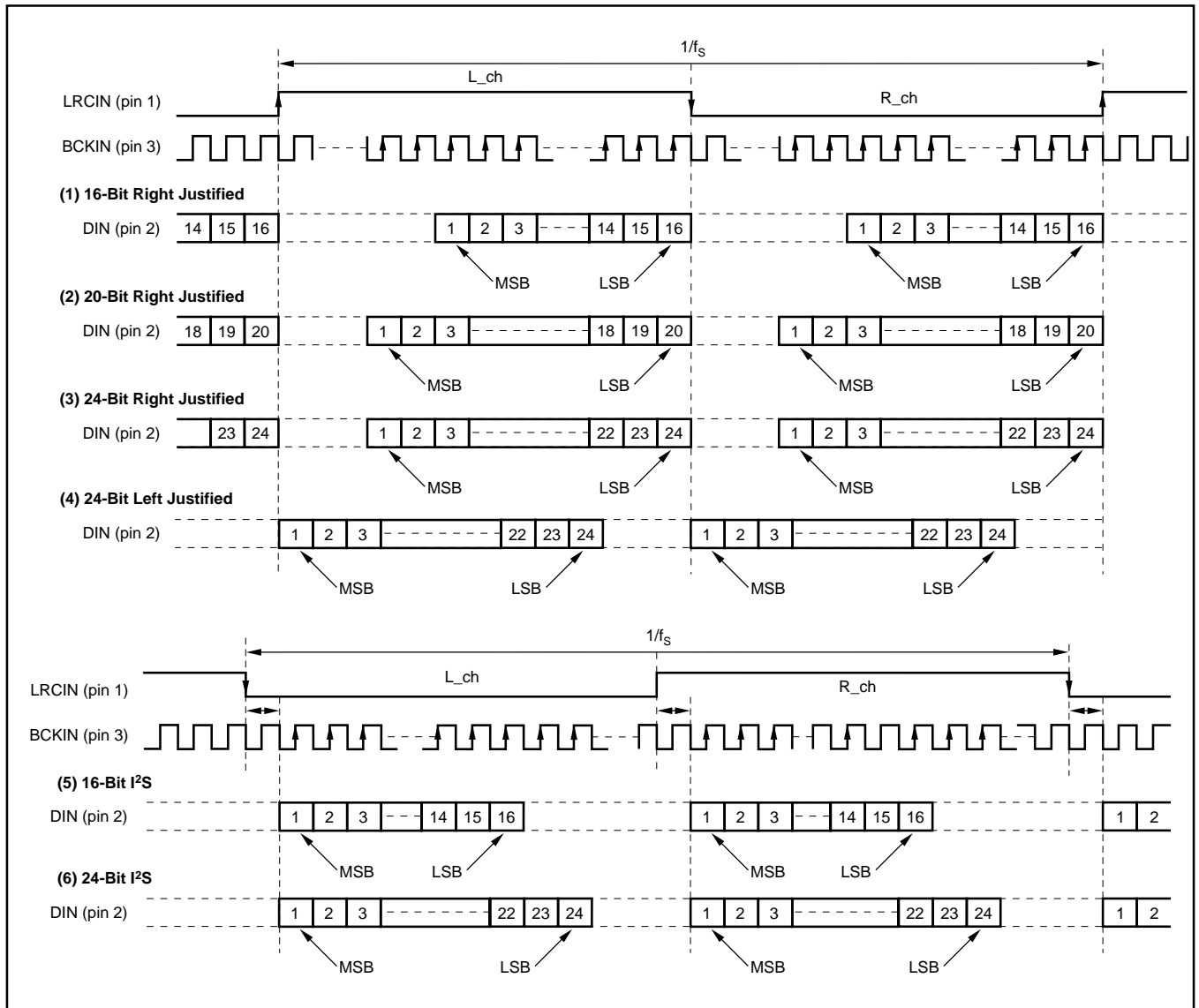


FIGURE 3. Audio Data Input Formats.

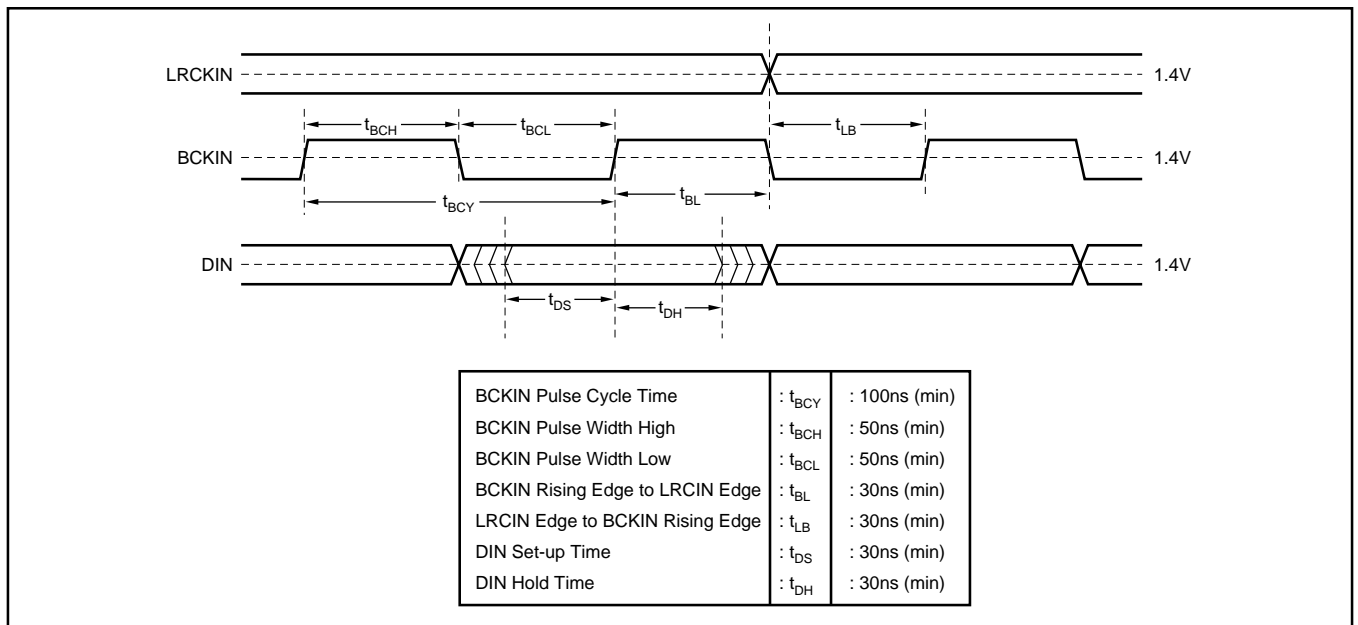


FIGURE 4. Audio Data Input Timing Specification.

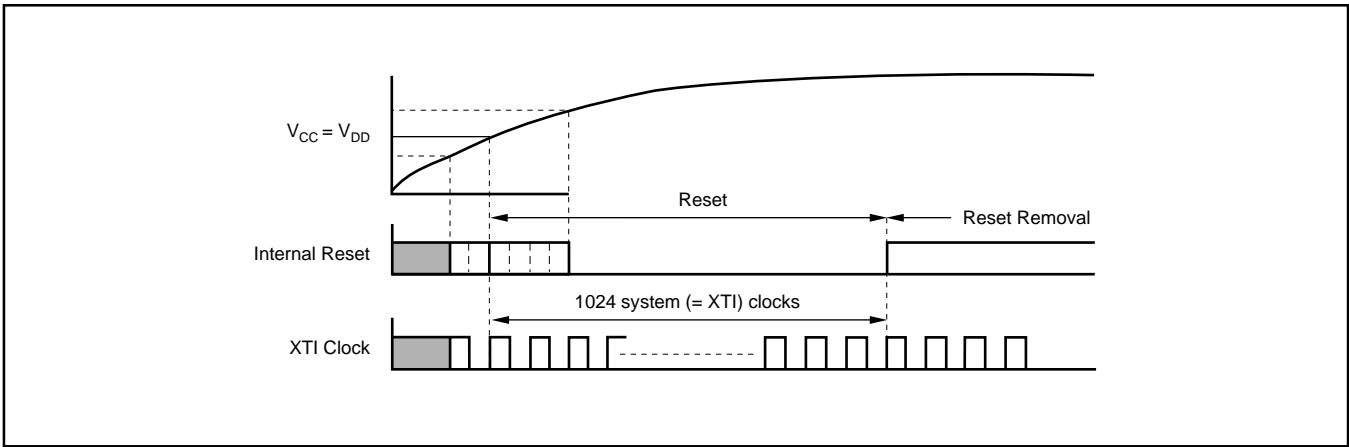


FIGURE 5. Internal Power-On Reset Timing.

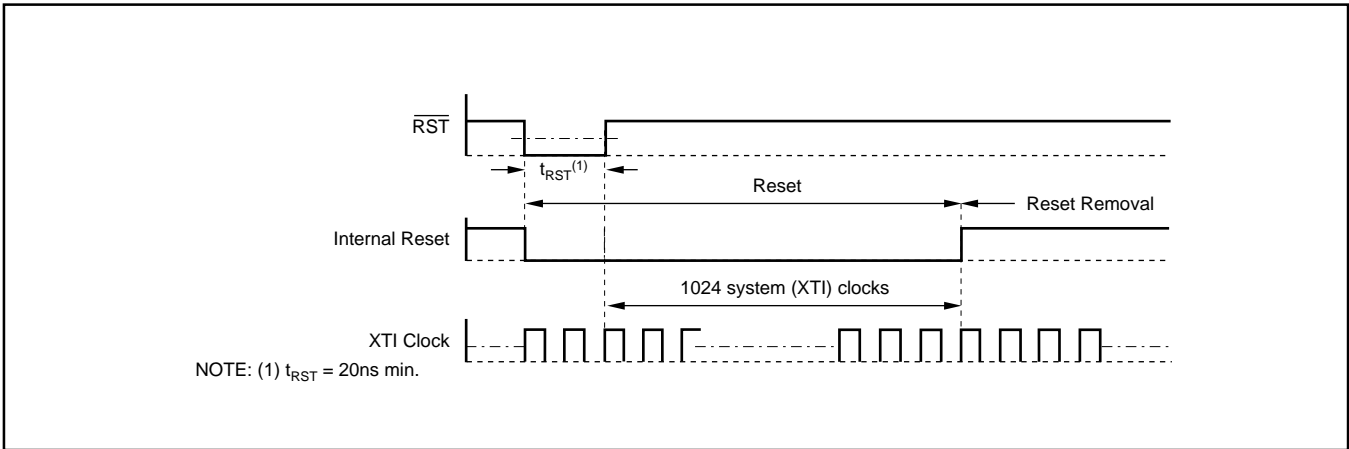


FIGURE 6. External Forced Reset Timing.

FUNCTIONAL DESCRIPTION

PCM1716 has several built-in functions including digital attenuation, digital de-emphasis, input data format selection, and others. These functions are software controlled. PCM1716 can be operated in two different modes, software mode or hardware mode. Software mode is a three-wire interface using pin 28 (ML), 27 (MC), and 26 (MD).

PCM1716 can also be operated in hardware mode, where static control signals are used on pin 28 (115), pin 27 (DM1), pin 26 (DM0) and pin 23 (IWO).

This basic operation mode as software or hardware can be selected by pin 24 (MODE) as shown in Table II.

| | |
|-------------------|---------------|
| MODE (pin 24) = H | Software Mode |
| MODE (pin 24) = L | Hardware Mode |

TABLE II. Mode Control.

Table III indicates which functions are selectable within the users chosen mode. All of the functions shown are selectable within the software mode, but only de-emphasis control, soft mute and input data format may be selected when using PCM1716 in the hardware mode.

| FUNCTION | SOFTWARE (Mode = H) | HARDWARE (Mode = L) |
|--------------------------------|---------------------|---------------------|
| Input Data Format Selection | O | O |
| Input Data Bit Selection | O | O |
| Input LRCIN Polarity Selection | O | X |
| De-emphasis Control | O | O |
| Mute | O | O |
| Attenuation | O | X |
| Infinity Zero Mute Control | O | X |
| DAC Operation Control | O | X |
| Slow Roll-Off Selection | O | X |
| Output Phase Selection | O | X |
| CLKO Output Selection | O | X |

NOTE: O = Selectable, X: Not Selectable.

TABLE III. Mode Control, Selectable Functions.

HARDWARE MODE (MODE = L)

In hardware mode, the following function can be selected.

De-emphasis control

De-emphasis control can be selected by DM1 (pin 27) and DM0 (pin 26)

| DM1 (Pin 27) | DM0 (Pin 26) | DE-EMPHASIS |
|--------------|--------------|-------------|
| L | L | OFF |
| L | H | 48kHz |
| H | L | 44.1kHz |
| H | H | 32kHz |

TABLE IV. De-emphasis Control.

Input Audio Data Format

Input data format can be selected by I²S (pin 28) and IWO (pin 23)

| I ² S (Pin 28) | IWO (Pin 23) | DATA FORMAT |
|---------------------------|--------------|---|
| L | L | 16-Bit Data Word, Normal, Right Justified |
| L | H | 20-Bit Data Word, Normal, Right Justified |
| H | L | 16-Bit Data Word, I ² S Format |
| H | H | 24-Bit Data Word, I ² S Format |

TABLE V. Data Format Control.

SOFT MUTE

Soft Mute function can be controlled by $\overline{\text{MUTE}}$ (pin 25)

| $\overline{\text{MUTE}}$ (Pin 25) | SOFT MUTE |
|-----------------------------------|-----------------------------|
| L | Mute ON |
| H | Mute OFF (Normal Operation) |

SOFTWARE MODE (MODE = H)

PCM1716's special functions at software mode is shown in Table VI. These functions are controlled using a ML, MC, MD serial control signal.

MAPPING OF PROGRAM REGISTERS

| | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|-------|-----|-----|-----|-----|-----|-----|----|-----|-----|-----|-----|-----|-----|-----|-----|------------------|
| MODE0 | res | res | res | res | res | A1 | A0 | LDL | AL7 | AL6 | AL5 | AL4 | AL3 | AL2 | AL1 | AL0 |
| MODE1 | res | res | res | res | res | A1 | A0 | LDR | AR7 | AR6 | AR5 | AR4 | AR3 | AR2 | AR1 | AR0 |
| MODE2 | res | res | res | res | res | A1 | A0 | res | res | res | res | IW1 | IW0 | OPE | DEM | MUT |
| MODE3 | res | res | res | res | res | A1 | A0 | IZD | SF1 | SF0 | CK0 | REV | SR0 | ATC | LRP | I ² S |

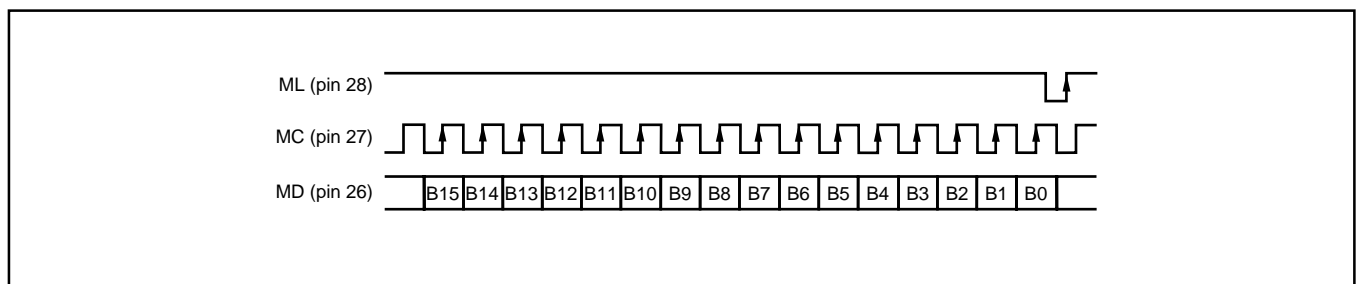


FIGURE 7. Three-Wire Serial Interface.

| FUNCTION | DEFAULT MODE |
|---|----------------------------------|
| Input Audio Data Format Selection Standard Format Left Justified I ² S Format | Standard Format |
| Input Audio Data Bit Selection 16-Bit 20-Bit 24-Bit | 16-Bit |
| Input LRCIN Polarity Selection Lch/Rch = High/Low Lch/Rch = Low/High | Lch/Rch = High/Low |
| De-emphasis Control | OFF |
| Soft Mute Control | OFF |
| Attenuation Control Lch, Rch Individually Lch, Rch Common | 0dB, Individual |
| Infinite Zero Mute Control | Not Operated |
| DAC Operation Control | Operated |
| Sampling Rate Selection for De-emphasis Standard Frequency 44.1kHz 48kHz 32kHz | 44.1kHz |
| Slow Roll-Off Selection | Not Selected (Sharp Roll-Off) |
| Output Phase Selection | Not Inverted |
| CLK0 Output Selection | Input Frequency |

TABLE VI. Selectable Functions and Default.

PROGRAM REGISTER BIT MAPPING

PCM1716's special functions are controlled using four program registers which are 16 bits long. These registers are all loaded using MD. After the 16 data bits are clocked in, ML is used to latch in the data to the appropriate register. Table VII shows the complete mapping of the four registers and Figure 7 illustrates the serial interface timing.

| REGISTER NAME | BIT NAME | DESCRIPTION |
|---------------|------------------|---|
| Register 0 | AL (7:0) | DAC Attenuation Data for Lch |
| | LDL | Attenuation Data Load Control for Lch |
| | A (1:0) res | Register Address Reserved, should be "L" |
| Register 1 | AR (7:0) | DAC Attenuation Data for Rch |
| | LDR | Attenuation Data Load Control for Rch |
| | A (1:0) res | Register Address Reserved, should be "L" |
| Register 2 | MUT | Left and Right DACs Soft Mute Control |
| | DEM | De-emphasis Control |
| | OPE | Left and Right DACs Operation Control |
| | IW (1:0) | Input Audio Data Bit and Format Select |
| | res | Reserved |
| | A (1:0) res | Register Address Reserved, should be "L" |
| Register 3 | I ² S | Audio Data Format Select |
| | LRP | Polarity of LRCIN Select |
| | ATC | Attenuator Control |
| | SRO | Slow Roll-Off Select |
| | REV | Output Phase Select |
| | CKO | CLKO Output Select |
| | SF (1:0) | Sampling Rate Select |
| | IZD | Internal Zero Detection Circuit Control |
| | A (1:0) | Register Address |
| | res | Reserved, should be "L" |

TABLE VII. Register Functions

REGISTER 0 (A1 = 0, A0 = 0)

| | | | | | | | | | | | | | | | |
|-----|-----|-----|-----|-----|-----|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| res | res | res | res | res | A1 | A0 | LDL | AL7 | AL6 | AL5 | AL4 | AL3 | AL2 | AL1 | AL0 |

Register 0 is used to control left channel attenuation. Bits 0 - 7 (AL0 - AL7) are used to determine the attenuation level. The level of attenuation is given by:

$$ATT = 0.5 \times (\text{data} - 255) \text{ (dB)}$$

$$FFh = -0\text{dB}$$

$$FEh = -0.5\text{dB}$$

$$\vdots$$

$$01h = -127.5\text{dB}$$

$$00h = -\infty (= \text{Mute})$$

ATTENUATION DATA LOAD CONTROL

Bit 8 (LDL) is used to control the loading of attenuation data in B0:B7. When LDL is set to 0, attenuation data will be loaded into AL0:AL7, but it will not affect the attenuation level until LDL is set to 1. LDR in Register 1 has the same function for right channel attenuation.

REGISTER 1 (A1 = 0, A0 = 1)

| | | | | | | | | | | | | | | | |
|-----|-----|-----|-----|-----|-----|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| res | res | res | res | res | A1 | A0 | LDR | AR7 | AR6 | AR5 | AR4 | AR3 | AR2 | AR1 | AR0 |

Register 1 is used to control right channel attenuation. As in Register 1, bits 0 - 7 (AR0 - AR7) control the level of attenuation.

REGISTER 2 (A1 = 1, A0 = 0)

| | | | | | | | | | | | | | | | |
|-----|-----|-----|-----|-----|-----|----|-----|-----|-----|-----|-----|-----|-----|-----|------|
| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| res | res | res | res | res | A1 | A0 | res | res | res | res | IW1 | IW0 | OPE | DEM | MUTE |

Register 2 is used to control soft mute, de-emphasis, operation enable, input resolution, and input audio data bit and format.

| MUT (B0) | |
|----------|---------------|
| MUT = L | Soft Mute OFF |
| MUT = H | Soft Mute ON |

| DEM (B1) | |
|----------|-----------------|
| DEM = L | De-emphasis OFF |
| DEM = H | De-emphasis ON |

| OPE (B2) | |
|----------|-------------------|
| OPE = L | Normal Operation |
| OPE = H | DAC Operation OFF |

when OPE (B2) is "HIGH", the output of the DAC will be forced to bipolar zero, irrespective of any input data.

IWO (B3), IW1 (B4) and I²S (B0) of Register 3

These registers, IWO, IW1, I²S determine the input data word and input data format as shown below.

| IW1 | IW0 | I ² S | Audio Interface |
|-----|-----|------------------|-----------------------------------|
| 0 | 0 | 0 | 16-Bit Standard (Right-Justified) |
| 0 | 1 | 0 | 20-Bit Standard (Right-Justified) |
| 1 | 0 | 0 | 24-Bit Standard (Right-Justified) |
| 1 | 1 | 0 | 24-Bit Left-Justified (MSB First) |
| 0 | 0 | 1 | 16-Bit I ² S |
| 0 | 1 | 1 | 24-Bit I ² S |
| 1 | 0 | 1 | Reserved |
| 1 | 1 | 1 | Reserved |

REGISTER 3 (A1 = 1, A0 = 1)

| | | | | | | | | | | | | | | | |
|-----|-----|-----|-----|-----|-----|----|-----|-----|-----|-----|-----|-----|-----|-----|------------------|
| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| res | res | res | res | res | A1 | A0 | IZD | SF1 | SF0 | CKO | REV | SRO | ATC | LRP | I ² S |

REGISTER 3 (A1 = 1, A0 = 1)

Register 3 is used to control input data format and polarity, attenuation channel control, system clock frequency, sampling frequency, infinite zero detection, output phase, CLKO output, and slow roll-off.

Bit 8 is used to control the infinite zero detection function (IZD).

When IZD is "LOW", the zero detect circuit is off. Under this condition, no automatic muting will occur if the input is continuously zero. When IZD is "HIGH", the zero detect feature is enabled. If the input data is continuously zero for 65, 536 cycles of BCKIN, the output will be immediately

forced to a bipolar zero state ($V_{CC}/2$). The zero detection feature is used to avoid noise which may occur when the input is DC. When the output is forced to bipolar zero, there may be an audible click. PCM1716 allows the zero detect feature to be disabled so the user can implement an external muting circuit.

| | |
|-----------------|----------------------|
| IZD (B8) | |
| B8 = L | Zero Detect Mute OFF |
| B8 = H | Zero Detect Mute ON |

Bits 6 (SF0) and 7 (SF1) are used to select the sampling frequency for De-emphasis.

| SF1 | SF0 | Sampling Rate |
|-----|-----|---------------|
| 0 | 0 | Reserved |
| 0 | 1 | 48kHz |
| 1 | 0 | 44.1kHz |
| 1 | 1 | 32kHz |

CKO (B5) is output frequency control at CLKO pin, can be selected as Buffer (1/1) or half rate of input frequency (1/2).

| | |
|---------|---|
| CKO = L | Buffer Out of XT _i Clock |
| CKO = H | Half (1/2) Frequency Out of XT _i Clock |

REF (B4) is output analog signal phase control.

| | |
|---------|-----------------|
| REV = L | Normal Output |
| REV = H | Inverted Output |

SRO (B3) is roll-off performance of digital filter selection.

| | |
|---------|----------------|
| SRO = L | Sharp Roll-Off |
| SRO = H | Slow Roll-Off |

ATC (B2) is used as an attenuation control. When bit 3 is set HIGH, the attenuation data on Register 0 is used for both channels, and the data in Register 1 is ignored. When bit 3 is LOW, each channel has separate attenuation data.

| | |
|---------|---------------------------|
| ATC = L | Ch Individual ATT Control |
| ATC = H | Common ATT Control |

Bits 0 (I²S) and 1 (LRP) are used to control the input data format. A “LOW” on bit 0 sets the format to (MSB-first, right-justified Japanese format) and a “HIGH” sets the format to I²S (Philips serial data protocol). Bit 1 (LRP) is used to select the polarity of LRCIN (sample rate clock). When bit 1 is “LOW”, left channel data is assumed when LRCIN is in a “HIGH” phase and right channel data is assumed when LRCIN is in a “LOW” phase. When bit 1 is “HIGH”, the polarity assumption is reversed.

| | | | |
|---------|---|---|---|
| LRP = L | <table border="1"><tr><td>L</td><td>R</td></tr></table> H/Lch | L | R |
| L | R | | |
| LRP = H | <table border="1"><tr><td>L</td><td>R</td></tr></table> L/Lch | L | R |
| L | R | | |

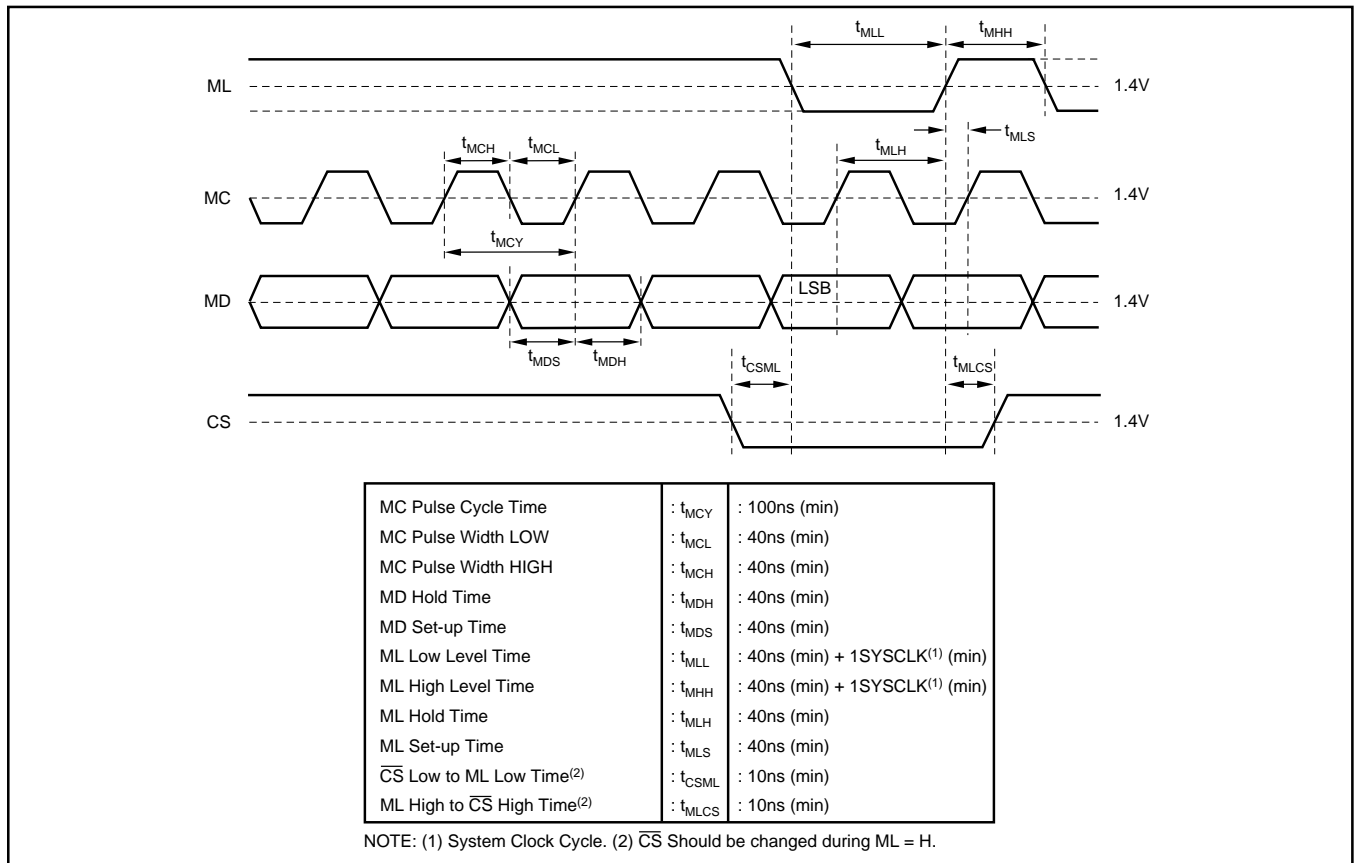


FIGURE 8. Program Register Input Timing.

THEORY OF OPERATION

The delta-sigma section of PCM1716 is based on a 8-level amplitude quantizer and a 4th-order noise shaper. This section converts the oversampled input data to 8-level delta-sigma format.

This newly developed, “Enhanced Multi-level Delta-Sigma” architecture achieves high-grade audio dynamic performance and sound quality.

A block diagram of the 8-level delta-sigma modulator is shown in Figure 9. This 8-level delta-sigma modulator has

the advantage of stability and clock jitter sensitivity over the typical one-bit (2 level) delta-sigma modulator.

The combined oversampling rate of the delta-sigma modulator and the internal 8-times interpolation filter is $64f_s$ for all system clock ratios ($256/384/512/768f_s$).

The theoretical quantization noise performance of the 8-level delta-sigma modulator is shown in Figure 10. This enhanced multi-level delta-sigma architecture also has advantages for input clock jitter sensitivity due to the multi-level quantizer, simulated jitter sensitivity is shown in Figure 11.

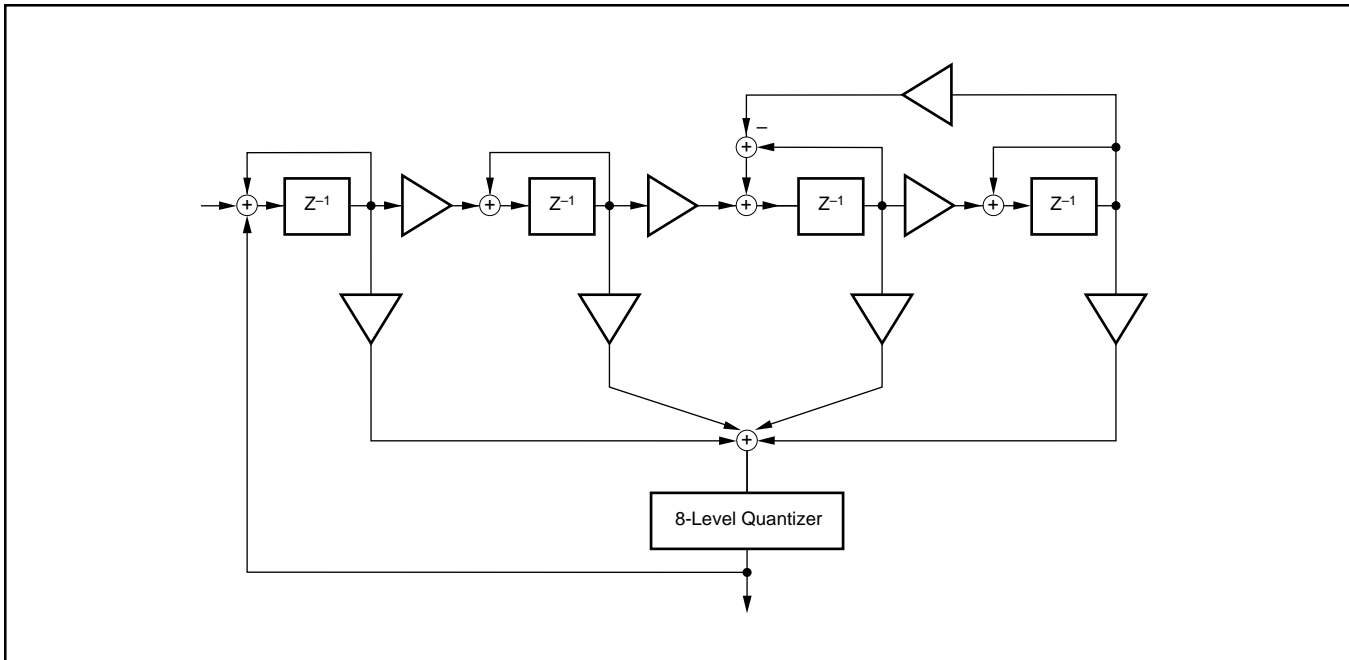


FIGURE 9. 8-Level Delta-Sigma Modulator.

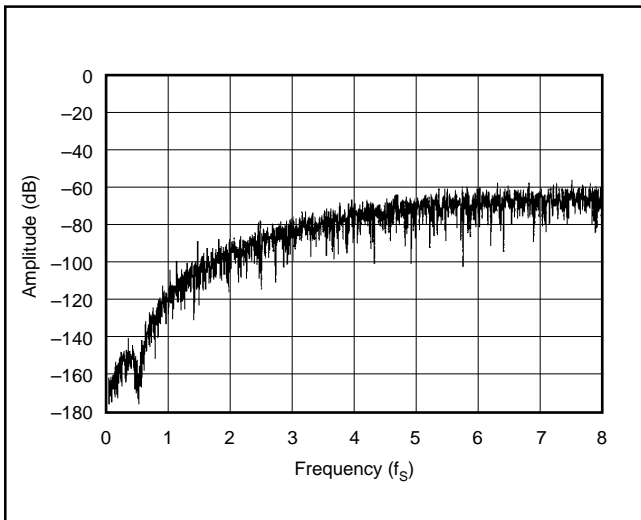


FIGURE 10. Quantization Noise Spectrum.

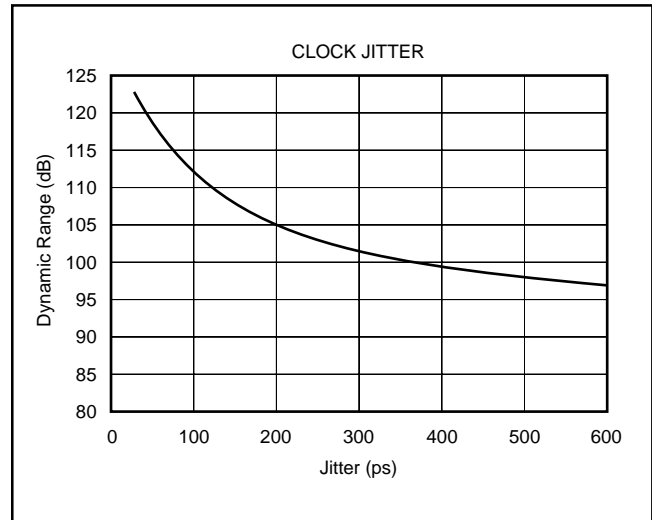


FIGURE 11. Jitter Sensitivity.

APPLICATION CONSIDERATIONS

DELAY TIME

There is a finite delay time in delta-sigma converters. In A/D converters, this is commonly referred to as latency. For a delta-sigma D/A converter, delay time is determined by the order number of the FIR filter stage, and the chosen sampling rate. The following equation expresses the delay time of PCM1716:

$$T_D = 30 \times 1/f_S$$

For $f_S = 44.1\text{kHz}$, $T_D = 30/44.1\text{kHz} = 680\mu\text{s}$

Applications using data from a disc or tape source, such as CD audio, DVD audio, Video CD, DAT, Minidisc, etc., generally are not affected by delay time. For some professional applications such as broadcast audio for studios, it is important for total delay time to be less than 2ms.

OUTPUT FILTERING

For testing purposes all dynamic tests are done on the PCM1716 using a 20kHz low pass filter. This filter limits the measured bandwidth for THD+N, etc. to 20kHz. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the specifications. The low pass filter removes out of band noise. Although it is not audible, it may affect dynamic specification numbers.

The performance of the internal low pass filter from DC to 40kHz is shown in Figure 12. The higher frequency roll-off of the filter is shown in Figure 13. If the user's application has the PCM1716 driving a wideband amplifier, it is recommended to use an external low pass filter.

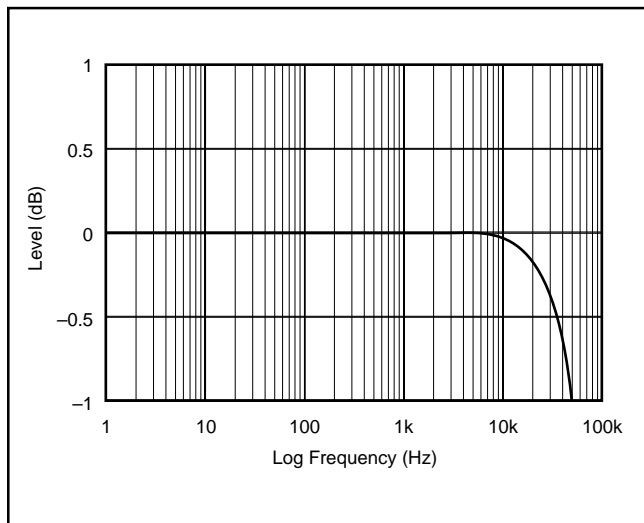


FIGURE 12. Low Pass Filter Response.

BYPASSING POWER SUPPLIES

The power supplies should be bypassed as close as possible to the unit. Refer to Figure 15 for optimal values of bypass capacitors.

POWER SUPPLY CONNECTIONS

PCM1716 has three power supply connections: digital (V_{DD}), and analog (V_{CC}). Each connection also has a separate ground. If the power supplies turn on at different times, there is a possibility of a latch-up condition. To avoid this condition, it is recommended to have a common connection between the digital and analog power supplies. If separate supplies are used without a common connection, the delta between the two supplies during ramp-up time must be less than 0.1V.

An application circuit to avoid a latch-up condition is shown in Figure 14.

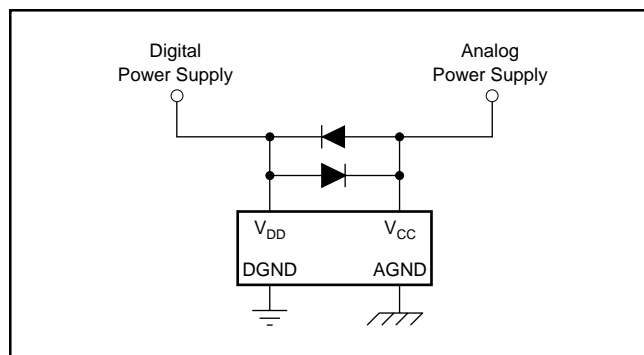


FIGURE 14. Latch-Up Prevention Circuit.

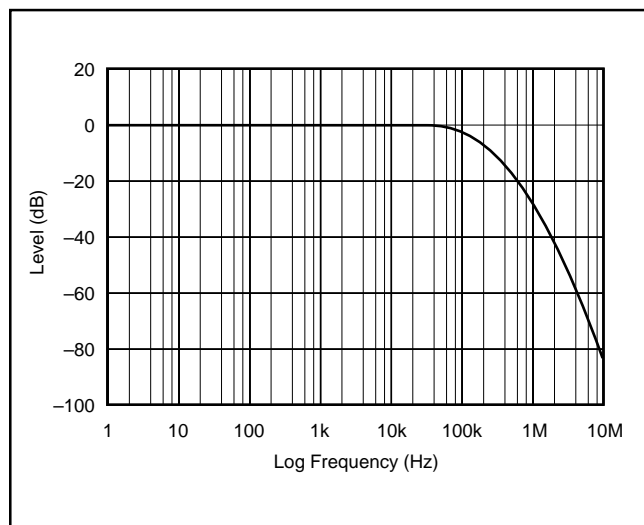


FIGURE 13. Low Pass Filter Response.

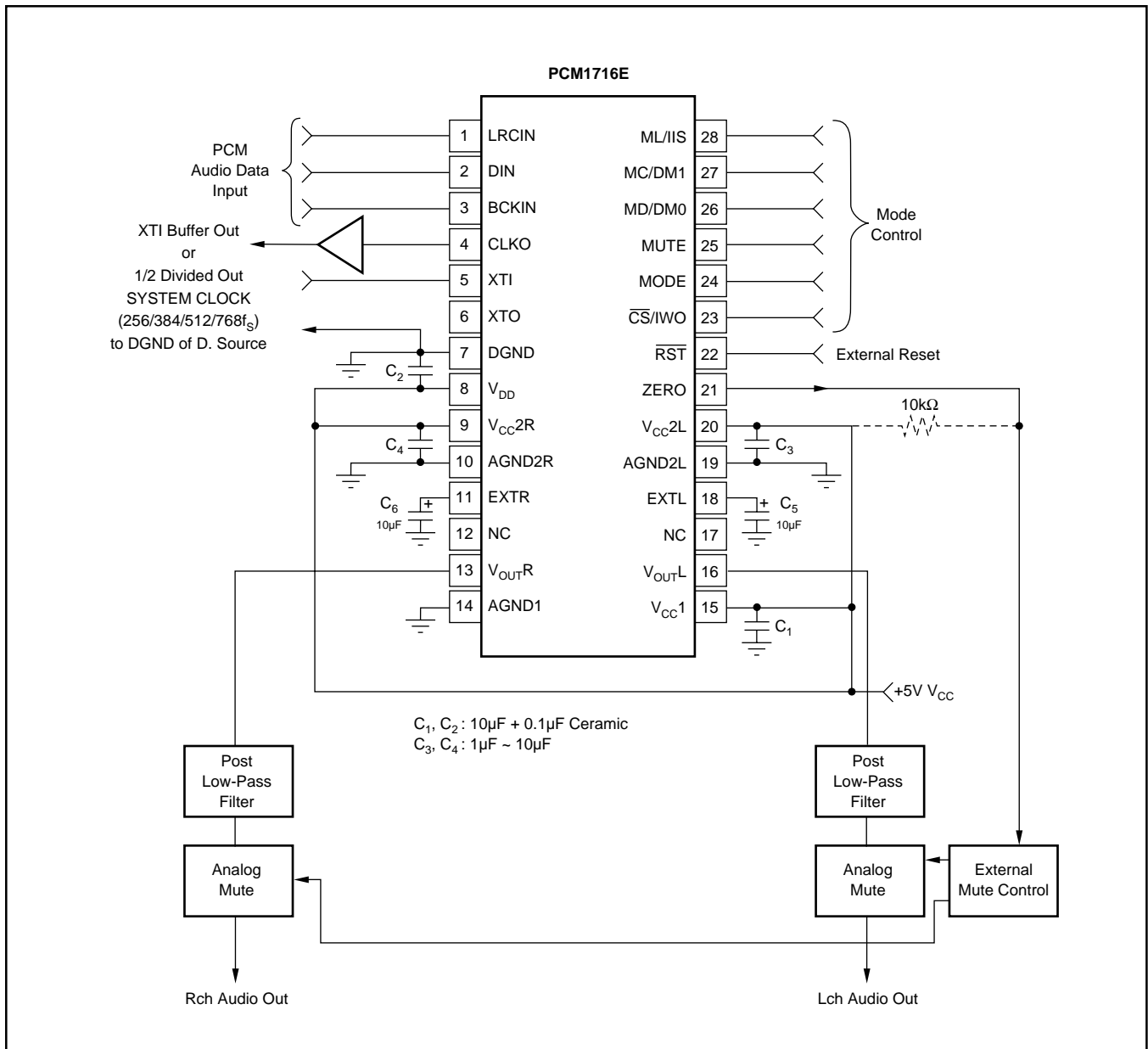


FIGURE 15. Typical Circuit Connection Diagram.

PACKAGING INFORMATION

| ORDERABLE DEVICE | STATUS(1) | PACKAGE TYPE | PACKAGE DRAWING | PINS | PACKAGE QTY |
|------------------|-----------|--------------|-----------------|------|-------------|
| PCM1716E | ACTIVE | SSOP | DB | 28 | 47 |
| PCM1716E/2K | ACTIVE | SSOP | DB | 28 | 2000 |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

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