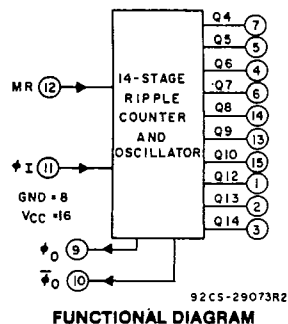


Technical Data

CD54/74HC4060, CD54/74HCT4060

T-45-23-17



14-Stage Binary Counter with Oscillator

Type Features:

- Onboard oscillator
- Common reset
- Negative edge clocking
- Typical $f_{MAX} = 50 \text{ MHz @ } V_{CC} = 5 \text{ V, } C_L = 15 \text{ pF}$

The RCA-CD54/74HC4060 and CD54/74HCT4060 each consists of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC or crystal oscillator circuits. A Master Reset input is provided which resets the counter to the all-0's state and disables the oscillator. A high level on the MR line accomplishes the reset function. All counter stages are master-slave flip-flops. The state of the counter is advanced one step in binary order on the negative transition of ϕ_1 (and ϕ_0). All inputs and outputs are buffered. Schmitt trigger action on the input-pulse line permits unlimited rise and fall times.

In order to achieve a symmetrical waveform in the oscillator section the HCT4060 input pulse switchpoints are the same as in the HC4060; only the MR input in the HCT4060 has TTL switching levels.

The CD54HC4060 and CD54HCT4060 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC4060 and CD74HCT4060 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- Fanout (Over Temperature Range):
Standard Outputs - 10 LSTTL Loads
Bus Driver Outputs - 15 LSTTL Loads
- Wide Operating Temperature Range:
CD74HC/HCT/HCU: -40 to +85° C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- Alternate Source is Philips/Signetics
- CD54HC/CD74HC Types:
2 to 6 V Operation
High Noise Immunity:
 $N_{IL}=30\%, N_{IH}=30\%$ of V_{CC} : @ $V_{CC}=5 \text{ V}$
- CD 54HCT/CD74HCT Types:
4.5 to 5.5 V Operation
Direct LSTTL Input Logic Compatibility
 $V_{IL}=0.8 \text{ V Mas.}, V_{IH}=2 \text{ V Min.}$
CMOS Input Compatibility
 $I_1 \leq 1 \mu\text{A @ } V_{OL}, V_{OH}$

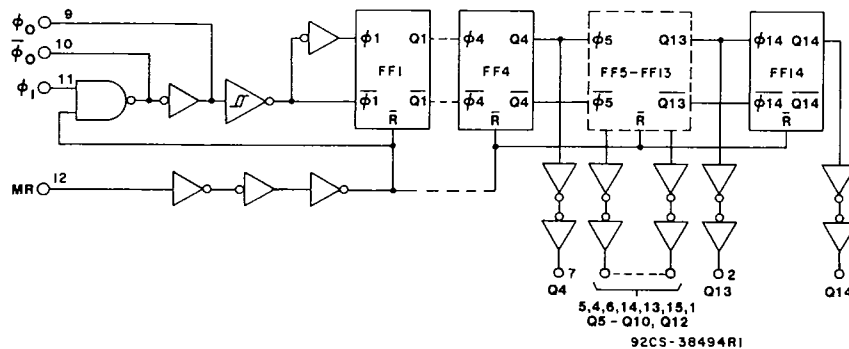


Fig. 1 - Logic block diagram.

Advance Information/
Preliminary Data

File Number 1654

CD54/74HC4060, CD54/74HCT4060

TRUTH TABLE 7-45-23-17

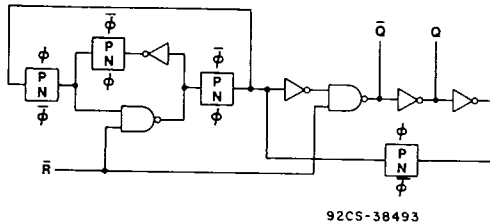


Fig. 2 - Flip-flop detail.

ϕ I	MR	OUTPUT STATE
	L	No Change
	L	Advance to Next State
X	H	All Outputs are Low

H = high level (steady state)
L = low level (steady state)
X = don't care

MAXIMUM RATINGS, Absolute-Maximum Values:

- DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) -0.5 to +7 V
- DC INPUT DIODE CURRENT, I_{IK} (FOR $V_i < -0.5$ V OR $V_i > V_{CC} + 0.5$ V) ± 20 mA
- DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC} + 0.5$ V) ± 20 mA
- DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR -0.5 V $< V_o < V_{CC} + 0.5$ V) ± 25 mA
- DC V_{CC} OR GROUND CURRENT, (I_{CC}) ± 50 mA
- POWER DISSIPATION PER PACKAGE (P_o):
For $T_A = -40$ to $+60^\circ$ C (PACKAGE TYPE E) 500 mW
For $T_A = +60$ to $+85^\circ$ C (PACKAGE TYPE E) Derate Linearly at 8 mW/ $^\circ$ C to 300 mW
For $T_A = -55$ to $+100^\circ$ C (PACKAGE TYPE F, H) 500 mW
For $T_A = +100$ to $+125^\circ$ C (PACKAGE TYPE F, H)¹ Derate Linearly at 8 mW/ $^\circ$ C to 300 mW
For $T_A = -40$ to $+60^\circ$ C (PACKAGE TYPE M) 300 mW
For $T_A = +60$ to $+85^\circ$ C (PACKAGE TYPE M) Derate Linearly at 5 mW/ $^\circ$ C to 175 mW
- OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H -55 to $+125^\circ$ C
PACKAGE TYPE E, M -40 to $+85^\circ$ C
- STORAGE TEMPERATURE (T_{stg}) -65 to $+150^\circ$ C
- LEAD TEMPERATURE (DURING SOLDERING):
At distance $1/16 \pm 1/32$ in. (1.59 ± 0.79 mm) from case for 10 s max. $+265^\circ$ C
Unit inserted into a PC Board (min. thickness $1/16$ in., 1.59 mm) with solder contacting lead tips only $+300^\circ$ C

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A =Full Package-Temperature Range) V_{CC} .* CD54/74HC Types CD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_i, V_o	0	V_{CC}	V
Operating Temperature T_A : CD74 Types CD54 Types	-40 -55	+85 +125	$^\circ$ C
Input Rise and Fall Times t_r, t_f at 2 V at 4.5 V at 6 V	0 0 0	1000 500 400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC4060, CD54/74HCT4060

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC4060, CD54HC4060										CD74HCT4060, CD54HCT4060										UNITS
	TEST CONDITIONS		V _{CC} V	74HC/54HC TYPES			74HC TYPE		54HC TYPE		TEST CONDITIONS		V _{CC} V	74HCT/54HCT TYPES			74HCT TYPE		54HCT TYPE		
	V _I V	I _O mA		+25°C			-40/ +85°C		-55/ +125°C		V _I V	V _{CC} V		+25°C			-40/ +85°C		-55/ +125°C		
			Min	Typ	Max	Min	Max	Min	Max	Min			Typ	Max	Min	Max	Min	Max			
High-Level Input Voltage V _{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5									
			4.5	3.15	—	—	3.15	—	3.15	—	—	to	2	—	—	2	—	2	—	—	V
			6	4.2	—	—	4.2	—	4.2	—	—	5.5									
Low-Level Input Voltage V _{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5									
			4.5	—	—	1.35	—	1.35	—	1.35	—	to	—	—	0.8	—	0.8	—	0.8	—	V
			6	—	—	1.8	—	1.8	—	1.8	—	5.5									
High-Level Output Voltage V _{OH} Q Outputs CMOS Loads	V _{IL} or V _{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V _{IL} ** or V _{IH}	4.5	4.4	—	—	4.4	—	4.4	—	—	V
			4.5	4.4	—	—	4.4	—	4.4	—	or	4.5	3.98	—	—	3.84	—	3.7	—	—	V
			6	5.9	—	—	5.9	—	5.9	—	V _{IH}										
High-Level Output Voltage V _{OH} Q Outputs TTL Loads	V _{IL} or V _{IH}										V _{IL} ** or V _{IH}	4.5	3.98	—	—	3.84	—	3.7	—	—	V
		-4	4.5	3.98	—	—	3.84	—	3.7	—	or	4.5	3.98	—	—	3.84	—	3.7	—	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—	V _{IH}										
Low-Level Output Voltage V _{OL} Q Outputs CMOS Loads	V _{IL} or V _{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V _{IL} ** or V _{IH}	4.5	—	—	0.1	—	0.1	—	0.1	—	V
			4.5	—	—	0.1	—	0.1	—	0.1	or	4.5	—	—	0.1	—	0.1	—	0.1	—	V
			6	—	—	0.1	—	0.1	—	0.1	V _{IH}										
Low-Level Output Voltage V _{OL} Q Outputs TTL Loads	V _{IL} or V _{IH}										V _{IL} ** or V _{IH}	4.5	—	—	0.26	—	0.33	—	0.4	—	V
		4	4.5	—	—	0.26	—	0.33	—	0.4	or	4.5	—	—	0.26	—	0.33	—	0.4	—	V
		5.2	6	—	—	0.26	—	0.33	—	0.4	V _{IH}										

**For Pin 11 V_{IH}=3.15 V, V_{IL}=0.9 V.

CD54/74HC4060, CD54/74HCT4060

T-45-23-17

STATIC ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	CD74HC4060, CD54HC4060										CD74HCT4060, CD54HCT4060								UNITS		
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPE		54HCT TYPE			
	V _I V	I _O mA	V _{CC} V	+25° C			-40/ +85° C		-55/ +125° C		V _I V	V _{CC} V	+25° C			-40/ +85° C		-55/ +125° C			
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min		Max	
High-Level Output Voltage V _{OH} φ _O Output (Pin 10) CMOS Loads	V _{CC}	-0.02		2	1.9	—	—	1.9	—	1.9	—	V _{CC}	4.5	4.4	—	—	4.4	—	4.4	—	
	or			4.5	4.4	—	—	4.4	—	4.4	—										
	Gnd			6	5.9	—	—	5.9	—	5.9	—										
High-Level Output Voltage V _{OH} φ _O Output (Pin 10) TTL Loads	V _{CC}	-2.6	4.5	3.98	—	—	—	3.84	—	3.7	—	V _{CC}	4.5	3.98	—	—	3.84	—	3.7	—	
	or			6	5.48	—	—	5.34	—	5.2	—										
	Gnd			3.3	6	—	—	0.26	—	0.33	—	0.4									—
Low-Level Output Voltage V _{OL} φ _O Output (Pin 10) CMOS Loads	V _{CC}	0.02		2	—	—	0.1	—	0.1	—	0.1	V _{CC}	4.5	—	—	0.1	—	0.1	—	0.1	
	or			4.5	—	—	0.1	—	0.1	—	0.1	—									
	Gnd			6	—	—	0.1	—	0.1	—	0.1	—									
Low-Level Output Voltage V _{OL} φ _O Output (Pin 10) TTL Loads	V _{CC}	2.6	4.5	—	—	—	0.26	—	0.33	—	0.4	V _{CC}	4.5	—	—	0.26	—	0.33	—	0.4	
	or			6	—	—	0.26	—	0.33	—	0.4	—									
	Gnd			3.3	6	—	—	0.26	—	0.33	—	0.4									—
High-Level Output Voltage V _{OH} φ _O Output (Pin 9) TTL Loads	V _{IL}	-3.2	4.5	3.98	—	—	—	3.84	—	3.7	—	V _{IL} **	4.5	3.98	—	—	3.84	—	3.7	—	
	or			6	5.48	—	—	5.34	—	5.2	—										
	V _{IH}			4.2	6	—	—	0.26	—	0.33	—	0.4									—
Low-Level Output Voltage V _{OL} φ _O Output (Pin 9) TTL Loads	V _{IL}	3.2	4.5	—	—	—	0.26	—	0.33	—	0.4	V _{IL} **	4.5	—	—	0.26	—	0.33	—	0.4	
	or			6	—	—	0.26	—	0.33	—	0.4	—									
	V _{IH}			4.2	6	—	—	0.26	—	0.33	—	0.4									—
Input Leakage Current I _I	V _{CC}		6	—	—	±0.1	—	±1	—	±1	—	Any Voltage between V _{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
or	Gnd																				
Quiescent Device Current I _{CC}	V _{CC}	0	6	—	—	8	—	80	—	160	—	V _{CC}	5.5	—	—	8	—	80	—	160	μA
or	Gnd																				
Additional Quiescent Device Current per input pin: 1 unit load ΔI _{CC} *												V _{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

**Pin II V_{IL} = 0.9V, V_{IH} = 3.15V

◇Limits not valid when pin 12 (instead of pin 11) is used as control input.

HCT INPUT LOADING

INPUT	UNIT LOADS*
MR	0.35

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25° C.

CD54/74HC4060, CD54/74HCT4060

SWITCHING CHARACTERISTICS (V_{CC}=5 V, T_A=25°C, Input t_i, t_r=6 ns)

CHARACTERISTIC	Symbol	C _L pF	Typical		UNITS
			HC	HCT	
Propagation Delay φ ₁ to Q ₄	t _{PLH} t _{PHL}	15	25	25	ns
Propagation Delay Q _n to Q _{n+1}	t _{PLH} t _{PHL}	15	6	6	ns
Propagation Delay MR to Q _n Output	t _{PHL}	15	17	17	ns
Propagation Dissipation Capacitance*	C _{PD}	—	40	40	pF

C_{PD} is used to determine the dynamic power consumption, per package.

PD = C_{PD} V_{CC}² f_i + Σ (C_L V_{CC}² f_i/M) where:

M = 2¹, 2², 2³,...2ⁿ

C_L = output load capacitance

f_i = input frequency

Prerequisite for Switching Function

CHARACTERISTIC	SYMBOL	V _{CC}	25°C		-40°C to +85°C				-55°C to +125°C				UNITS		
			HC		HCT		74HC		74HCT		54HC			54HCT	
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		Min.	Max.
Maximum Input Pulse Frequency	t _{MAX}	2	6	—	—	—	—	5	—	—	—	4	—	—	MHz
		4.5	30	—	30	—	25	—	25	—	20	—	20	—	
		6	35	—	—	—	29	—	—	—	23	—	—	—	
Input Pulse Width (Figure 4)	t _w	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	16	—	20	—	20	—	24	—	24	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Reset Removal Time (Figure 5)	t _{REM}	2	100	—	—	—	125	—	—	—	150	—	—	—	ns
		4.5	20	—	26	—	25	—	33	—	30	—	39	—	
		6	17	—	—	—	21	—	—	—	26	—	—	—	
Reset Pulse Width (Figure 5)	t _w	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	28	—	20	—	35	—	24	—	42	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_i, t_r = 6ns)

CHARACTERISTIC	SYMBOL	V _{CC}	25°C		-40°C to +85°C				-55°C to +125°C				UNITS		
			HC		HCT		74HC		74HCT		54HC			54HCT	
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		Min.	Max.
Propagation Delay φ ₁ to Q ₄ Output (Figure 4)	t _{PLH}	2	—	300	—	—	—	375	—	—	—	450	—	—	ns
	t _{PHL}	4.5	—	60	—	66	—	75	—	83	—	90	—	100	
	—	6	—	51	—	—	—	64	—	—	—	78	—	—	
Propagation Delay Q _n to Q _{n+1} (Figure 4)	t _{PLH}	2	—	80	—	—	—	100	—	—	—	120	—	—	ns
	t _{PHL}	4.5	—	16	—	16	—	20	—	20	—	24	—	24	
	—	6	—	14	—	—	—	17	—	—	—	20	—	—	
Propagation Delay MR to Q _n Output (Figure 5)	t _{PHL}	2	—	200	—	—	—	250	—	—	—	300	—	—	ns
	—	4.5	—	40	—	44	—	50	—	55	—	60	—	66	
	—	6	—	34	—	—	—	43	—	—	—	51	—	—	
Output Transition Time (Figure 4)	t _{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
	t _{THL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	
	—	6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C _i *														

*TBD

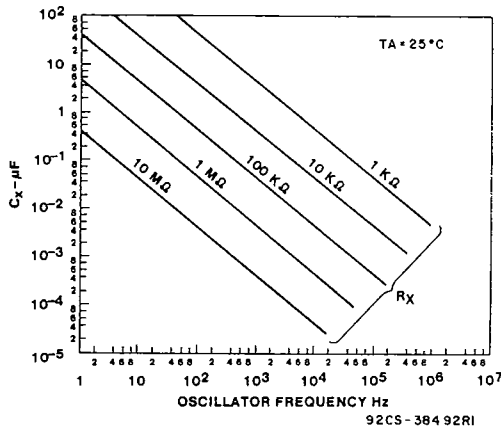
CD54/74HC4060, CD54/74HCT4060

TYPICAL LIMIT VALUES FOR R_x AND C_x

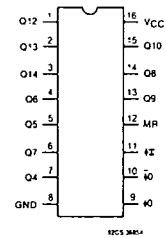
T-45-23-17

CHARACTERISTIC	TEST CONDITIONS	VOLTAGE	TYPICAL MAXIMUM LIMITS
R_x Min.	$C_x > 1000 \text{ pF}$	2	1 K Ω
	$C_x > 10 \text{ pF}$	4.5	
	$C_x > 10 \text{ pF}$	6	
R_x Max.	$C_x > 10 \text{ pF}$	2	20 M Ω
	$C_x > 10 \text{ pF}$	4.5	
	$C_x > 10 \text{ pF}$	6	
C_x Min.	$R_x > 10 \text{ K}\Omega$	2	10 pF
	$R_x > 10 \text{ K}\Omega$	4.5	
	$R_x > 10 \text{ K}\Omega$	6	
	$R_x = 1 \text{ K}\Omega$	2	1000 pF
	$R_x = 1 \text{ K}\Omega$	4.5	10 pF
	$R_x = 1 \text{ K}\Omega$	6	10 pF
Maximum Astable Oscillator Frequency	$C_x = 1000 \text{ pF}, R_x = 1 \text{ K}\Omega$	2	0.5 MHz*
	$C_x = 100 \text{ pF}, R_x = 1 \text{ K}\Omega$	4.5	3 MHz*
	$C_x = 100 \text{ pF}, R_x = 1 \text{ K}\Omega$	6	3 MHz*

*At very high frequencies $f = 1/2.2 R_x C_x$ no longer gives an accurate approximation.



OSC FREQUENCY = $1/2.2 R_x C_x$
 FOR $1 \text{ M}\Omega > R_x > 1 \text{ K}\Omega$,
 $C_x > 10 \text{ pF}, f < 1 \text{ MHz}$



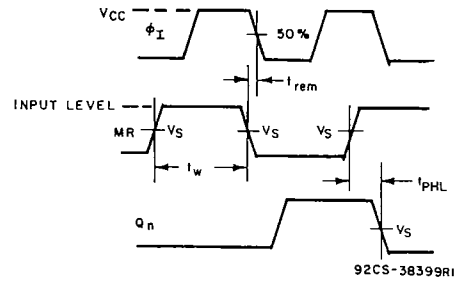
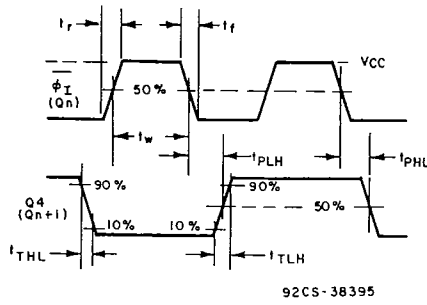
TERMINAL ASSIGNMENT

Fig. 3 - Frequency of on-board oscillator as a function of C_x and R_x .

Technical Data

T-45-23-17

CD54/74HC4060, CD54/74HCT4060



	54/74HC	54/74HCT
MR Input Level	VCC	3 V
Switching Voltage, Vs	50% VCC	1.3 V

Fig. 4 - Input pulse pre-requisite times, propagation delays and output transition times for both HC and HCT types.

Fig. 5 - Master Reset pre-requisite and propagation delays.