

# CY54FCT646T, CY74FCT646T 8-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

SCCS031A – JULY 1994 – REVISED OCTOBER 2001

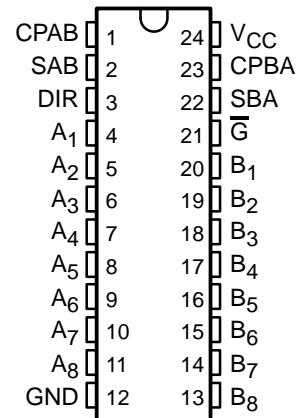
- Function, Pinout, and Drive Compatible With FCT and F Logic
- Reduced  $V_{OH}$  (Typically = 3.3 V) Versions of Equivalent FCT Functions
- Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Matched Rise and Fall Times
- Fully Compatible With TTL Input and Output Logic Levels
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
- Independent Register for A and B Buses
- CY54FCT646T
  - 48-mA Output Sink Current
  - 12-mA Output Source Current
- CY74FCT646T
  - 64-mA Output Sink Current
  - 32-mA Output Source Current
- 3-State Outputs

## description

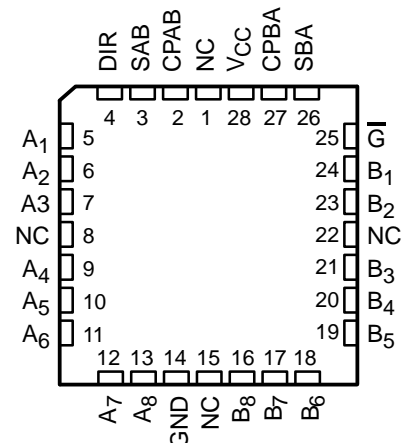
The 'FCT646T devices consist of a bus transceiver circuit with 3-state, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus is clocked into the registers as the appropriate clock pin goes to a high logic level. Output-enable ( $\overline{G}$ ) and direction (DIR) inputs control the transceiver function. In the transceiver mode, data present at the high-impedance port can be stored in either the A or B register, or in both. Select controls (SAB, SBA) can multiplex stored and real-time (transparent mode) data. DIR determines which bus receives data when  $\overline{G}$  is low. In the isolation mode ( $\overline{G}$  is high), A data can be stored in the B register and/or B data can be stored in the A register.

These devices are fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

CY54FCT646T . . . D PACKAGE  
CY74FCT646T . . . Q OR SO PACKAGE  
(TOP VIEW)



CY54FCT646T . . . L PACKAGE  
(TOP VIEW)



NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

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**PIN DESCRIPTION**

NAME	DESCRIPTION
A	Data register A inputs, data register B outputs
B	Data register B inputs, data register A outputs
CPAB, CPBA	Clock-pulse inputs
SAB, SBA	Output data-source-select inputs
DIR, $\overline{G}$	Output-enable inputs

**ORDERING INFORMATION**

T <sub>A</sub>	PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
-40°C to 85°C	QSOP – Q	Tape and reel	5.4	CY74FCT646CTQCT	FCT646C	
	SOIC – SO	Tube	5.4	CY74FCT646CTSOC	FCT646C	
		Tape and reel	5.4	CY74FCT646CTSOCT		
	QSOP – Q	Tape and reel	6.3	CY74FCT646ATQCT	FCT646A	
		SOIC – SO	Tube	6.3	CY74FCT646ATSOC	FCT646A
	Tape and reel		6.3	CY74FCT646ATSOCT		
	-55°C to 125°C	QSOP – Q	Tape and reel	9	CY74FCT646TQCT	FCT646
		SOIC – SO	Tube	9	CY74FCT646TSOC	FCT646
Tape and reel			9	CY74FCT646TSOCT		
LCC – L		Tube	6	CY54FCT646CTLMB		
-55°C to 125°C	CDIP – D	Tube	7.7	CY54FCT646ATDMB		
	LCC – L	Tube	7.7	CY54FCT646ATLMB		
		Tube	11	CY54FCT646TLMB		

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

**FUNCTION TABLE**

INPUTS						DATA I/O‡		OPERATION OR FUNCTION
$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA	A <sub>1</sub> –A <sub>8</sub>	B <sub>1</sub> –B <sub>8</sub>	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	↑	↑	X	X	Input	Input	Store A and B data
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to B bus

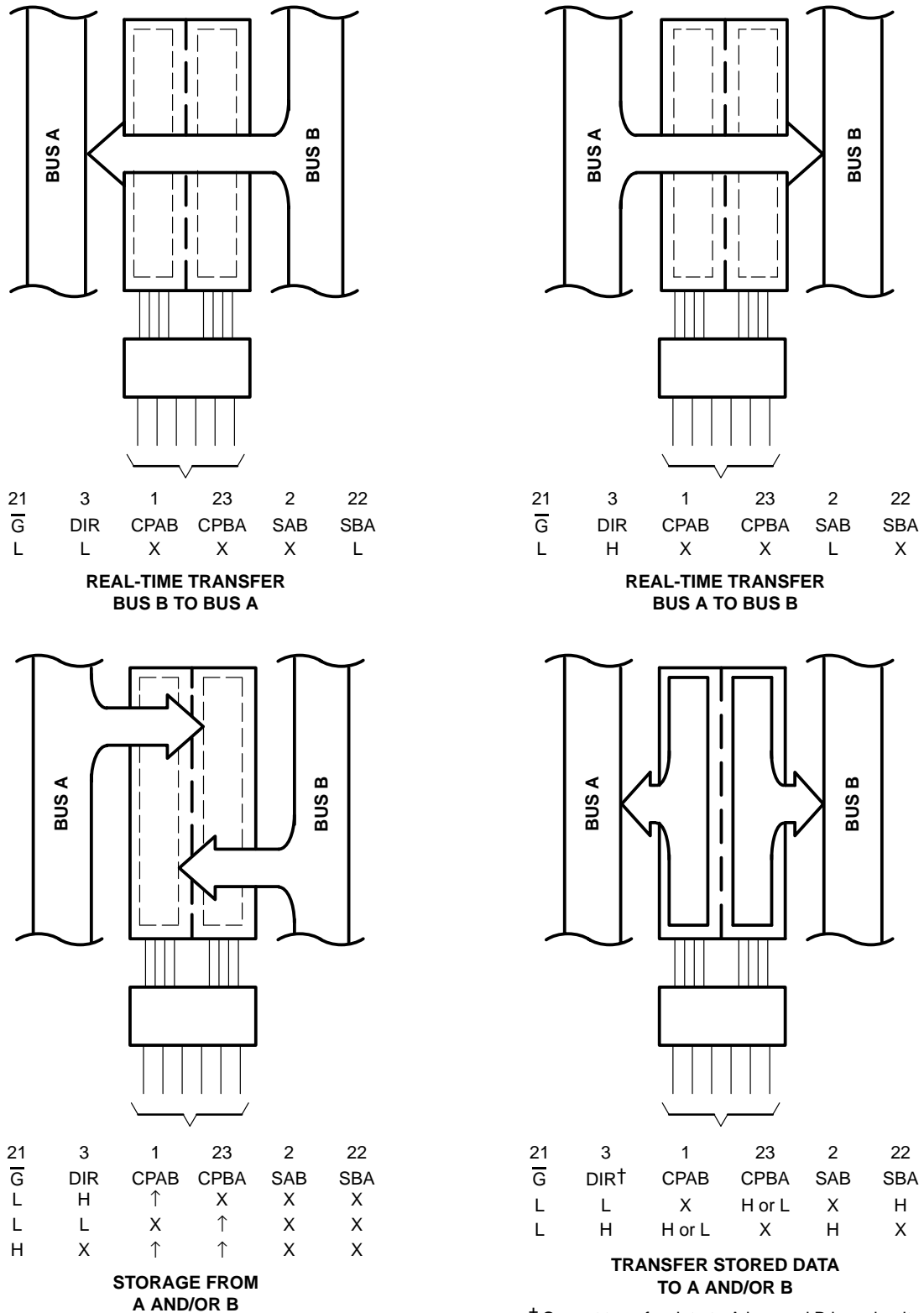
H = High logic level, L = Low logic level, ↑ = Low-to-high transition, X = Don't care

‡ The data output functions can be enabled or disabled by various signals at the  $\overline{G}$  or DIR inputs. Data input functions always are enabled, i.e., data at the bus pins is stored on every low-to-high transition of the clock inputs.



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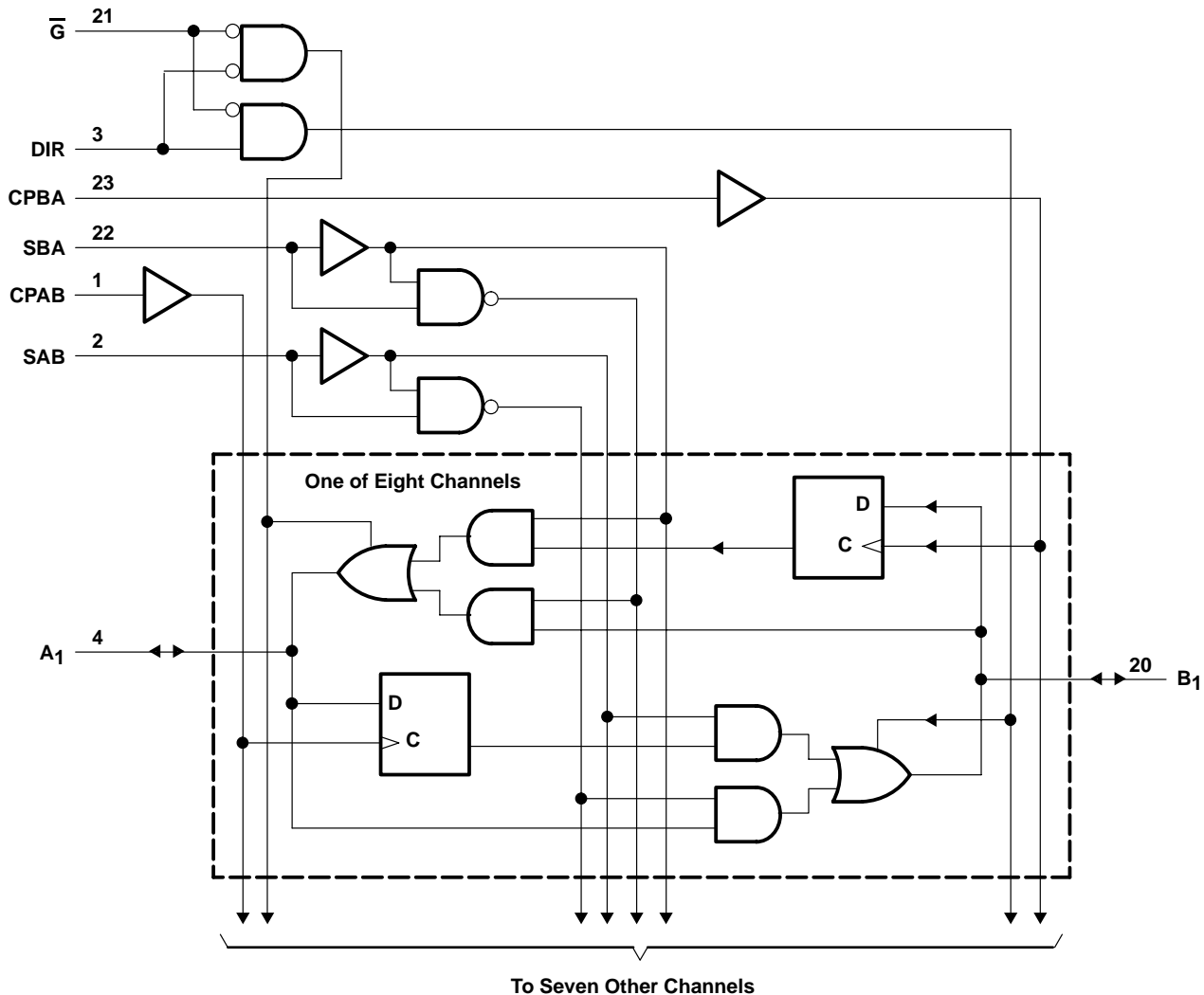
† Cannot transfer data to A bus and B bus simultaneously.

**Figure 1. Bus-Management Functions**

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**logic diagram (positive logic)**



Pin numbers shown are for the Q and SO packages.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>**

Supply voltage range to ground potential .....	-0.5 V to 7 V
DC input voltage range .....	-0.5 V to 7 V
DC output voltage range .....	-0.5 V to 7 V
DC output current (maximum sink current/pin) .....	120 mA
Package thermal impedance, $\theta_{JA}$ (see Note 1): Q package .....	61°C/W
SO package .....	46°C/W
Ambient temperature range with power applied, $T_A$ .....	-65°C to 135°C
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.



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**recommended operating conditions (see Note 2)**

	CY54FCT646T			CY74FCT646T			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub> Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub> High-level input voltage	2			2			V
V <sub>IL</sub> Low-level input voltage			0.8			0.8	V
I <sub>OH</sub> High-level output current			-12			-32	mA
I <sub>OL</sub> Low-level output current			48			64	mA
T <sub>A</sub> Operating free-air temperature	-55		125	-40		85	°C

NOTE 2: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation.



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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	CY54FCT646T			CY74FCT646T			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>IN</sub> = -18 mA	-0.7	-1.2					V
	V <sub>CC</sub> = 4.75 V, I <sub>IN</sub> = -18 mA				-0.7	-1.2		
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -12 mA	2.4	3.3					V
	V <sub>CC</sub> = 4.75 V	I <sub>OH</sub> = -32 mA			2			
		I <sub>OH</sub> = -15 mA			2.4	3.3		
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 48 mA	0.3	0.55					V
	V <sub>CC</sub> = 4.75 V, I <sub>OL</sub> = 64 mA				0.3	0.55		
V <sub>hys</sub>	All inputs	0.2			0.2			V
I <sub>I</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = V <sub>CC</sub>			5				μA
	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> = V <sub>CC</sub>					5		
I <sub>IH</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 2.7 V			±1				μA
	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> = 2.7 V					±1		
I <sub>IL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0.5 V			±1				μA
	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> = 0.5 V					±1		
I <sub>OZH</sub>	V <sub>CC</sub> = 5.5 V, V <sub>OUT</sub> = 2.7 V			10				μA
	V <sub>CC</sub> = 5.25 V, V <sub>OUT</sub> = 2.7 V					10		
I <sub>OZL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>OUT</sub> = 0.5 V			-10				μA
	V <sub>CC</sub> = 5.25 V, V <sub>OUT</sub> = 0.5 V					-10		
I <sub>OS</sub> ‡	V <sub>CC</sub> = 5.5 V, V <sub>OUT</sub> = 0 V	-60	-120	-225				mA
	V <sub>CC</sub> = 5.25 V, V <sub>OUT</sub> = 0 V				-60	-120	-225	
I <sub>off</sub>	V <sub>CC</sub> = 0 V, V <sub>OUT</sub> = 4.5 V			±1			±1	μA
I <sub>CC</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> ≤ 0.2 V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V		0.1	0.2				mA
	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> ≤ 0.2 V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V					0.1	0.2	
ΔI <sub>CC</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 3.4 V§, f <sub>1</sub> = 0, Outputs open		0.5	2				mA
	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> = 3.4 V§, f <sub>1</sub> = 0, Outputs open					0.5	2	
I <sub>CCD</sub> ¶	V <sub>CC</sub> = 5.5 V, One input switching at 50% duty cycle, Outputs open, $\overline{G}$ = DIR = GND, SAB = $\overline{SBA}$ = GND, V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V		0.06	0.12				mA/ MHz
	V <sub>CC</sub> = 5.25 V, One input switching at 50% duty cycle, Outputs open, $\overline{G}$ = DIR = GND, SAB = $\overline{SBA}$ = GND, V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V					0.06	0.12	

† Typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

§ Per TTL-driven input (V<sub>IN</sub> = 3.4 V); all other inputs at V<sub>CC</sub> or GND

¶ This parameter is derived for use in total power-supply calculations.



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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)**

PARAMETER	TEST CONDITIONS			CY54FCT646T		CY74FCT646T		UNIT
				MIN	TYP†	MAX	MIN	
I <sub>C</sub> <sup>#</sup>	V <sub>CC</sub> = 5.5 V, f <sub>0</sub> = 10 MHz, Outputs open, $\overline{G} = \overline{DIR} = \overline{GND}$ , SAB = $\overline{SBA} = \overline{GND}$	One bit switching at f <sub>1</sub> = 5 MHz at 50% duty cycle	V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2 V	0.7	1.4			mA
			V <sub>IN</sub> = 3.4 V or GND	1.2	3.4			
		Eight bits switching at f <sub>1</sub> = 5 MHz at 50% duty cycle	V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2 V	2.8	5.6			
			V <sub>IN</sub> = 3.4 V or GND	5.1	14.6			
	V <sub>CC</sub> = 5.25 V, f <sub>0</sub> = 10 MHz, Outputs open, $\overline{G} = \overline{DIR} = \overline{GND}$ , SAB = $\overline{SBA} = \overline{GND}$	One bit switching at f <sub>1</sub> = 5 MHz at 50% duty cycle	V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2 V			0.7	1.4	mA
			V <sub>IN</sub> = 3.4 V or GND			1.2	3.4	
		Eight bits switching at f <sub>1</sub> = 5 MHz at 50% duty cycle	V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2 V			2.8	5.6	
			V <sub>IN</sub> = 3.4 V or GND			5.1	14.6	
C <sub>i</sub>				6	10	6	10	pF
C <sub>o</sub>				8	12	8	12	pF

<sup>#</sup> I<sub>C</sub> = I<sub>CC</sub> + ΔI<sub>CC</sub> × D<sub>H</sub> × N<sub>T</sub> + I<sub>CCD</sub>(f<sub>0</sub>/2 + f<sub>1</sub> × N<sub>1</sub>)

Where:

I<sub>C</sub> = Total supply current

I<sub>CC</sub> = Power-supply current with CMOS input levels

ΔI<sub>CC</sub> = Power-supply current for a TTL high input (V<sub>IN</sub> = 3.4 V)

D<sub>H</sub> = Duty cycle for TTL inputs high

N<sub>T</sub> = Number of TTL inputs at D<sub>H</sub>

I<sub>CCD</sub> = Dynamic current caused by an input transition pair (HLH or LHL)

f<sub>0</sub> = Clock frequency for registered devices, otherwise zero

f<sub>1</sub> = Input signal frequency

N<sub>1</sub> = Number of inputs changing at f<sub>1</sub>

All currents are in milliamperes and all frequencies are in megahertz.

|| Values for these conditions are examples of the I<sub>CC</sub> formula.

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**timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)**

		CY54FCT646T		CY54FCT646AT		CY54FCT646CT		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_w$	Pulse duration	6		5		5		ns
$t_{su}$	Setup time, data before CPAB $\uparrow$ or CPBA $\uparrow$	4.5		2		2		ns
$t_h$	Hold time, data after CPAB $\uparrow$ or CPBA $\uparrow$	2		1.5		1.5		ns

**timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)**

		CY74FCT646T		CY74FCT646AT		CY74FCT646CT		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_w$	Pulse duration	6		5		5		ns
$t_{su}$	Setup time, data before CPAB $\uparrow$ or CPBA $\uparrow$	4		2		2		ns
$t_h$	Hold time, data after CPAB $\uparrow$ or CPBA $\uparrow$	2		1.5		1.5		ns

**switching characteristics over operating free-air temperature range (see Figure 2)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY54FCT646T		CY54FCT646AT		CY54FCT646CT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A or B	B or A	2	11	2	7.7	1.5	6	ns
$t_{PHL}$			2	11	2	7.7	1.5	6	
$t_{PZH}$	DIR	A or B	2	15	2	10.5	1.5	8.9	ns
$t_{PZL}$			2	15	2	10.5	1.5	8.9	
$t_{PHZ}$	$\bar{G}$ and DIR	A or B	2	11	2	7.7	1.5	7.7	ns
$t_{PLZ}$			2	11	2	7.7	1.5	7.7	
$t_{PLH}$	CPAB or CPBA	A or B	2	10	2	7	1.5	6.3	ns
$t_{PHL}$			2	10	2	7	1.5	6.3	
$t_{PLH}$	SBA or SAB	A or B	2	12	2	8.4	1.5	7	ns
$t_{PHL}$			2	12	2	8.4	1.5	7	

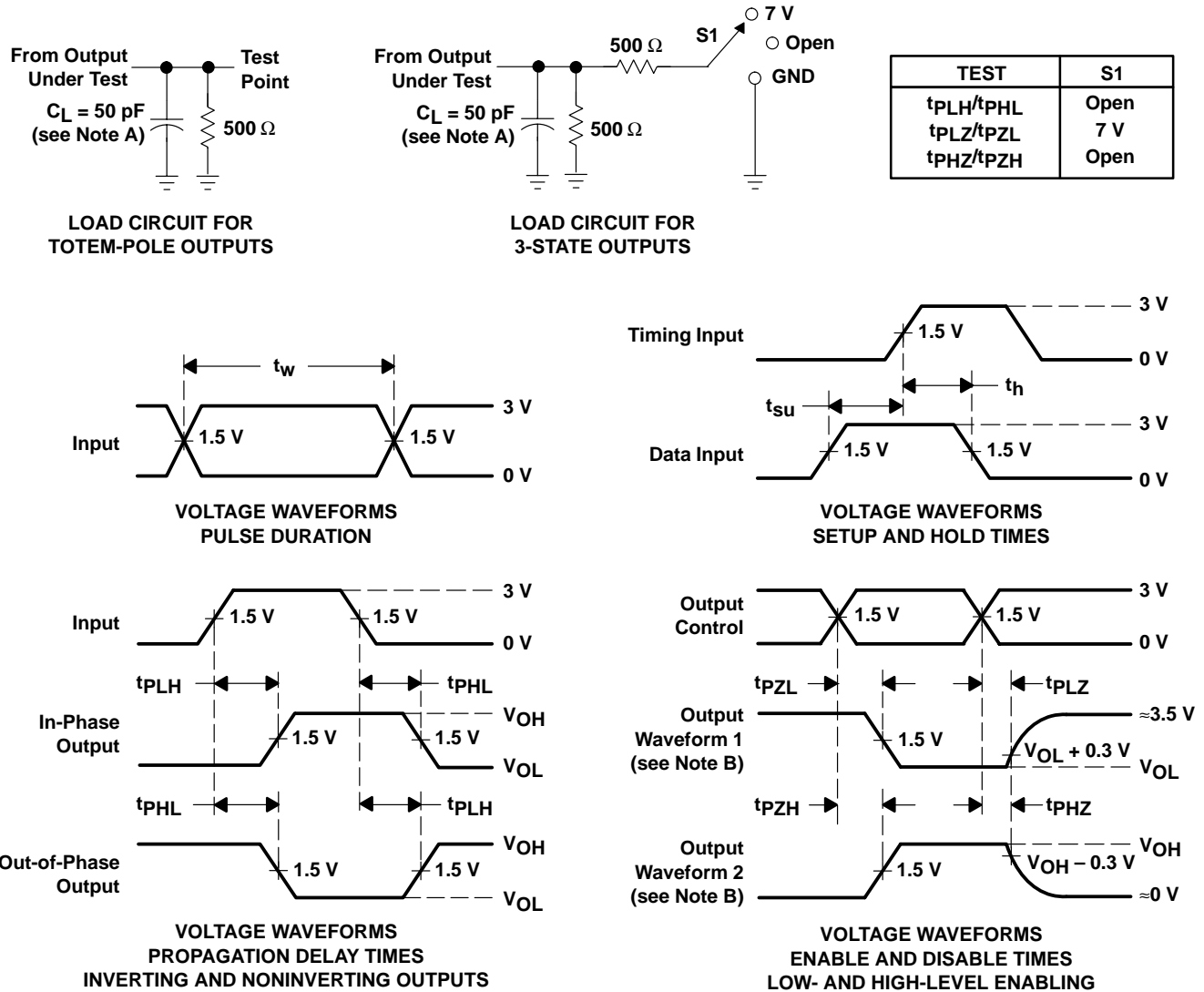
**switching characteristics over operating free-air temperature range (see Figure 2)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY74FCT646T		CY74FCT646AT		CY74FCT646CT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A or B	B or A	1.5	9	1.5	6.3	1.5	5.4	ns
$t_{PHL}$			1.5	9	1.5	6.3	1.5	5.4	
$t_{PZH}$	DIR	A or B	1.5	14	1.5	9.8	1.5	7.8	ns
$t_{PZL}$			1.5	14	1.5	9.8	1.5	7.8	
$t_{PHZ}$	$\bar{G}$ and DIR	A or B	1.5	9	1.5	6.3	1.5	6.3	ns
$t_{PLZ}$			1.5	9	1.5	6.3	1.5	6.3	
$t_{PLH}$	CPAB or CPBA	A or B	1.5	9	1.5	6.3	1.5	5.7	ns
$t_{PHL}$			1.5	9	1.5	6.3	1.5	5.7	
$t_{PLH}$	SBA or SAB	A or B	1.5	11	1.5	7.7	1.5	6.2	ns
$t_{PHL}$			1.5	11	1.5	7.7	1.5	6.2	





PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9222301M3A	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9222301M3A	<a href="#">Samples</a>
5962-9222303M3A	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9222303M3A CY54FCT 646ATLMB	<a href="#">Samples</a>
5962-9222303MLA	ACTIVE	CDIP	JT	24	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-9222303ML A CY54FCT646ATDM B	<a href="#">Samples</a>
5962-9222305M3A	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9222305M3A CY54FCT 646CTLMB	<a href="#">Samples</a>
CY54FCT646ATDMB	ACTIVE	CDIP	JT	24	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-9222303ML A CY54FCT646ATDM B	<a href="#">Samples</a>
CY54FCT646ATLMB	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9222303M3A CY54FCT 646ATLMB	<a href="#">Samples</a>
CY54FCT646CTLMB	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9222305M3A CY54FCT 646CTLMB	<a href="#">Samples</a>
CY74FCT646ATQCT	ACTIVE	SSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT646A	<a href="#">Samples</a>
CY74FCT646ATSOC	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT646A	<a href="#">Samples</a>
CY74FCT646ATSOCT	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT646A	<a href="#">Samples</a>
CY74FCT646ATSOCTE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT646A	<a href="#">Samples</a>
CY74FCT646CTSOC	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT646C	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CY74FCT646TSOC	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT646	<a href="#">Samples</a>
CY74FCT646TSOCT	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT646	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CY74FCT646ATQCT	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT646ATSOCT	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
CY74FCT646TSOCT	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CY74FCT646ATQCT	SSOP	DBQ	24	2500	367.0	367.0	38.0
CY74FCT646ATSOCT	SOIC	DW	24	2000	350.0	350.0	43.0
CY74FCT646TSOCT	SOIC	DW	24	2000	350.0	350.0	43.0

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
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