LTC4284
–48V, 1500W Hot Swap Controller with Telemetry and EEPROM

DESCRIPTION

DC2909A showcases the LTC®4284 high power, negative hot swap controller with telemetry and EEPROM in a –48V, 31A (1500W) application. DC2909A is configured for parallel mode, which offers reliable low cost hot plug solution for high power systems where input steps are imminent.

Included on board is isolation for power good control pins, to enable downstream power converters. LEDs indicate the presence of –48V input and output as well as the state of both supply feeds and power good signaling. High voltage layout rules are followed throughout for best long-term product reliability.

Headers are provided for three I^2C interfaces, providing instant access to voltage, current, power, energy, fault log, and board temperature data.

Design files for this circuit board are available.

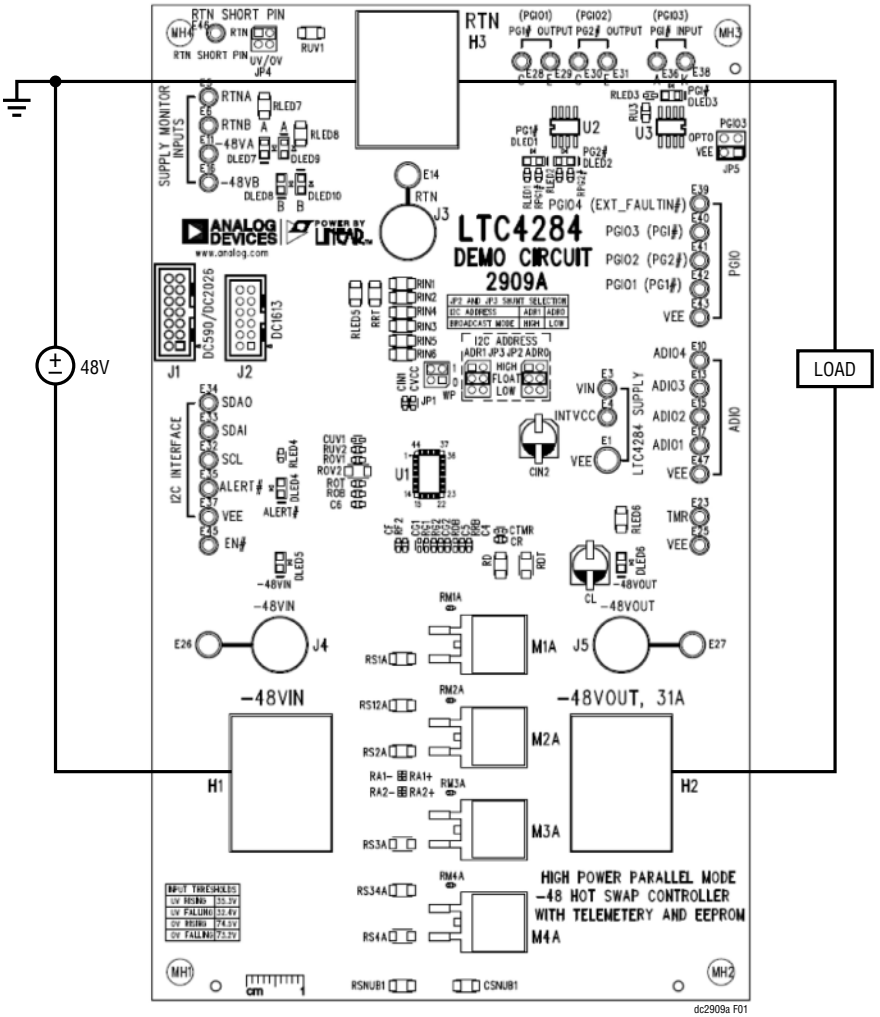

Figure 1. DC2909A Setup

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C

PARAMETER	MIN	TYP	MAX	UNITS
Input Valid Operating Voltage	–35.3	–48	–74.5	V
Output Power			1500	W
Output Capacitor			1500	µF
Current Limit (at –48V Input)	44.55	45	45.45	A

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Board Layout

The board is divided into several planes, each separated by a 60mil gap for DC standoff up to 100V. In addition to the basic planes (RTN, –48VIN, VEE and –48VOUT), there are small subplanes for the MOSFET sources. Other isolated regions include the areas around the supply monitor inputs, RTN short pin, and the power good opto-isolators.

Power Connections

Use 4 AWG (19mm^2) welding cable for power supply and load connections. Suitable welding cable is available from Anixter (877-467-9473). Order ToughFlex #4 heavy duty welding cable, part number WC4BK.

The resistance of 4 AWG welding cable is 263µΩ per foot, resulting in a power dissipation of 253mW and a voltage drop of 8.15mV, per foot at 31A. While the voltage drop may be negligible in a 48V system, the power dissipation will cause a noticeable temperature rise in the cable and can also contribute to board heating.

For power connections to the PCB, large pads are provided with Panduit S4-14R ring terminals. These are designed for use with 4 AWG welding cable. Crimp all ring terminals using a Thomas & Betts WT115 or equivalent compression crimper. Do not solder.

The ring terminals are attached to the board with stainless ¼-28 mounting hardware. To prevent damage to the PCB, do not exceed a torque of 5 ft-lbs (6.8Nm). The cap screws require a 3/16" Allen wrench, and the nuts require a 7/16" nut driver. Stainless hardware is subject to galling; lubricate the threads with Lucas Oil Products white lithium grease (product number 10533), or with an equivalent product that meets the NLGI #2 specification.

Power flows through DC2909A from the –48VIN terminal to –48VOUT, through the load and returns to the positive terminal of the power supply. It is not necessary for power to flow through DC2909A in the return path; for this reason, there is only one RTN connection on the PCB. Surprisingly, the PCB's return connection can be made with a small test lead to either the load or the power supply.

For minimum loss, the load and power supply returns should be connected together directly, through the shortest possible length of cable. Nevertheless, a high current RTN pad is included to provide a convenient point at which the load and power supply returns can be joined together, in the case where separate cables present themselves.

Power Good Control

DC2909A includes two power good outputs, as well as a power good input, using the PGIO1, PGIO2 and PGIO3 pins of the LTC4284. Initially, 256ms after a successful power-up, Power Good 1 (PG1#) goes low. 256ms later Power Good 2 (PG2#) goes low. The intent of these two outputs is to sequentially enable downstream DC-DC converters, after the MOSFETs are fully on. PG1# and PG2# outputs are the photo transistors of U2. These pull low in the "power good" condition and can sink up to 1mA.

Power good input (PGI# INPUT, implemented with the PGIO3 pin) must be asserted within 512ms after PG2# goes low, as verification that the secondary supplies have successfully reached regulation. If PGI# INPUT is not asserted in time, the LTC4284 will shut down.

Normally the PGI# INPUT signal is obtained from a supply monitor, or just simply tied to a secondary supply output. PGI# INPUT (turrets A and K) drives a green indicator LED

QUICK START PROCEDURE

and the LED in opto isolator U3, each through a 1kΩ resistor, so that PGI# INPUT can be tied directly to a 3.3V or 5V supply (A = +, K = –) to assert a power good condition.

Higher supplies can be monitored with the addition of 500Ω/V in series with PGI# INPUT's A and K turrets. To avoid the need for PGI# feedback during initial testing, jumper JP7 is provided so that PGIO3 can be forced low (PGIO3 set to VEE position).

J1, J2 Digital Interface

The LTC4284 features an I^2C interface to control the device and to retrieve measurements, status, and fault information. Because the LTC4284 uses –48VIN as its "ground" reference, the I^2C lines must be isolated in order to communicate with a truly ground-referred control processor. This isolation is not included on DC2909A. Instead, headers are made available for DC590, DC1613 and DC2026 interface boards, all of which feature full galvanic isolation and USB communication with a host computer. A ribbon cable connects J1 or J2 to the interface board; do not use J1 and J2 simultaneously.

An LTpowerPlay® GUI is available for download. This GUI operates with DC1613, supplied separately. A 24LC025 EEPROM (U4) located on DC2909A communicates with LTpowerPlay, permitting it to load the corresponding GUI without user input.

Jumpers

JP1: WP. This write protect blocks writes (position 1) to the LTC4284 on-chip EEPROM. 0 enables writes. WP does not block fault logging.

JP2, JP3: I^2C Address. These jumpers program the LTC4284's address at the ADR1 and ADR0 pins. Default FLOAT-FLOAT stuffing selects address 2Ah. HIGH-LOW selects broadcast mode (see data sheet for information on broadcast mode).

JP4: UV/OV. The UV and OV divider strings are joined together and serve as a RTN short pin input. For testing purposes, the short pin function can be bypassed by moving the jumper to the RTN position. To avoid permanent connector damage, high power applications must use a short pin for on/off control during insertion and extraction.

JP5: PGIO3. PGIO3 is configured as a PGI# input (power good input) and is controlled by the PGI# INPUT via opto-isolator U3. JP7 bypasses the PGI# function when the jumper is set to the VEE position. Doing so ties PGIO3 low, indicating "power is good" and allowing the LTC4284 to remain on after a successful power-up.

Supply Monitor Inputs

The ADIN1-4 pins are used to measure the individual supply feed terminal voltages relative to the V_{REF} pin (and ultimately, VEE), in a two-supply system. ADIO3 is configured to measure the chassis voltage, also relative to V_{REF}. Thus, in a redundant feed system, a total of five connections between DC2909A and RTNA, RTNB, –48VA, –48VB, and CHASSIS are necessary to use this feature. Precision 101:1 dividers connect to these potentials, to measure their respective voltages. The bottom of the dividers is connected to V_{REF}, allowing measurement of up to ±100V relative to VEE. Feed voltage is inferred by subtracting associated –48V and RTN readings. Absolute terminal voltages, relative to chassis, are obtained by subtracting the chassis reading (ADIO3) from the individual terminal readings (ADIN1-4). LTpowerPlay takes care of calculations and shows the differential voltage of the two feeds, and the individual feed terminal voltages relative to ground. The operation of the feed monitor circuit is explained in the data sheet and illustrated in Figure 23, Feed Voltage and Open Fuse Monitoring. If unused, these connections may be simply left open circuit.

Board Temperature

An NTC thermistor (RTHA) and linearizing circuit is connected to the LTC4284's ADIO4 pin, to measure board temperature. The ADIO4 pin is configured as an ADC input. The LTpowerPlay GUI calculates temperature using the ADC measurement of ADIO4's voltage.

QUICK START PROCEDURE

Altered Register Values

Table 1 shows the changes that have been made to the default register values as they are listed in the data sheet.

Table 1. DC2909A Specific Register Values

PARAMETER NAME	REGISTER VALUE	
I_{LIM}	0010	17mV
FB	11	10%
FTBD_DL	01	512ms
Cooling Delay	100	8.19s
DVDT Control During Start-Up	Unchecked	
Power Good Reset	Unchecked	

Basic Operation

Set JP4 to RTN, and JP7 to VEE. These are the default stuffing positions. Connect an interface cable to DC1613 via J2 and connect a PC to DC1613 via its USB interface.

After first verifying that the supply is off and the load is disabled, connect a 48V supply capable of at least 50A to –48VIN and RTN, and connect a load across –48VOUT and RTN. As previously described, the load RTN may be connected directly to the supply, and DC2909A's RTN terminal connected through a small test lead.

Turn on the supply. The LTC4284 is configured to turn on autonomously after application of power. Once the output is up, as indicated by the –48VOUT LED (DLED6) and the PG1# and PG2# LEDs (DLED1 and DLED2), the load may be enabled. The LTpowerPlay GUI may be started at any time.

If two supplies are available, the Supply Monitor Inputs may be connected to the appropriate terminals ahead of the ORing diodes. The matching negative-side diode OR board is DC2180A, which features the LTC4371.

A Note About Grounding

"Ground" reference for DC2470A is –48VIN and the attached V_{EE} plane, whereas in an actual system RTN closely tracks Earth and chassis ground. For bench testing where the input supply is floating, $–48V_{IN}$ and VEE can serve as the reference ground, such as for oscilloscope probing.

The DC590, DC1613 and DC2026 interface boards are fully isolated and can be used regardless of whether –48VIN or RTN is ground referenced.

DC2909A IEC61000-4-5 SURGE IMMUNITY TEST

IEC61000-4-5 SURGE IMMUNITY

The DC2909A is capable of handling IEC61000-4-5 surges. The DC2909A was tested for IEC61000-4-5 differential surge of 6kV with 42Ω impedance. The board set up was made as shown in Figure 2

The surge generator used for this test is Teseq NSG 3060. The surge generator has an output impedance of 2Ω. Module A has two 80Ω resistors in parallel which provides an equivalent resistance of 40Ω to make total impedance of 42Ω. Module B are gas arrestors which are installed to block any DC voltage generated by surge generator to travel to the DC2909A. Module C is a coupling decoupling network with a 1A fuse. This network makes sure that the surge current does not go towards battery. Due to limitations of Module C, DC2909A was modified for a current limit of 2A. The output capacitor was also scaled down to 100µF in order to produce similar decay in output voltage as it would be with 30A current limit and 1500µF output capacitor. A 3-wire cable module was installed to scale down the current by 3 so that it can be measured using lab equipment. The board has foot prints for two SMDJ75A diodes which can clamp the voltage at $75V_{DC}$. For this test, these diodes were populated on the board. The board was biased using a 48V lead acid battery and a load of 1A was applied to its output. With this setup a 6kV, 1.2µs/50µs surge was applied between RTN terminal and –48VIN terminal of the board. –48VIN Voltage, Gate to Source voltage, –48VOUT voltage and Surge current were monitored during this test. Upon injection of the 6kV surge, the LTC4284 hits current limit due to the inrush current that charges the output capacitor. As a result, the Gate pin pulls low. During this time, output load is provided by the 100µF capacitor installed at the output. Within 4µs the Gate voltage recovers quickly and attempts to go into regulation. Once the surge event expires, the gate voltage starts to fully enhance the MOSFETs. The circuit was able to ride through the surge without browning out the output and with no damage to the board. Figure 3, Figure 4 and Figure 5 show the various waveforms from this test.

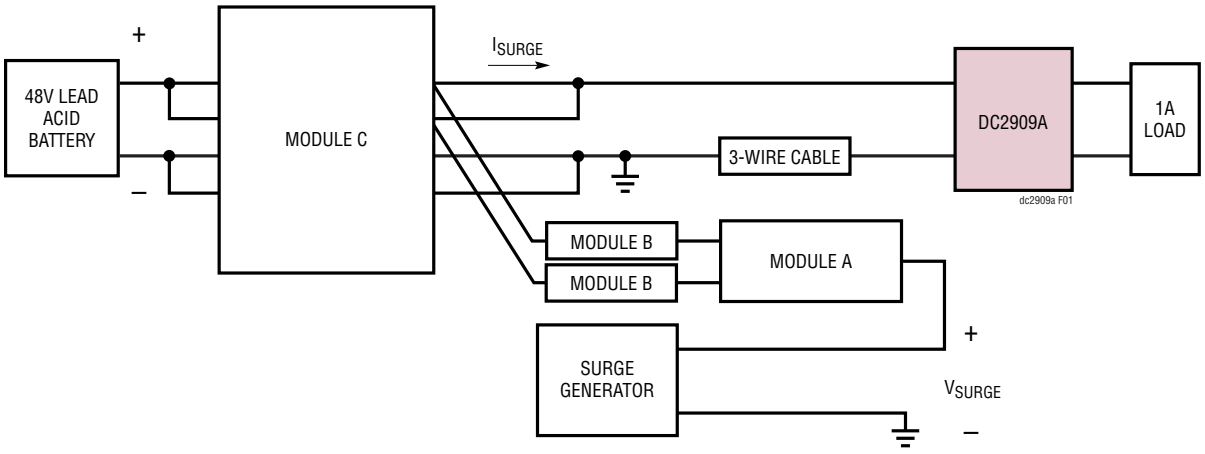
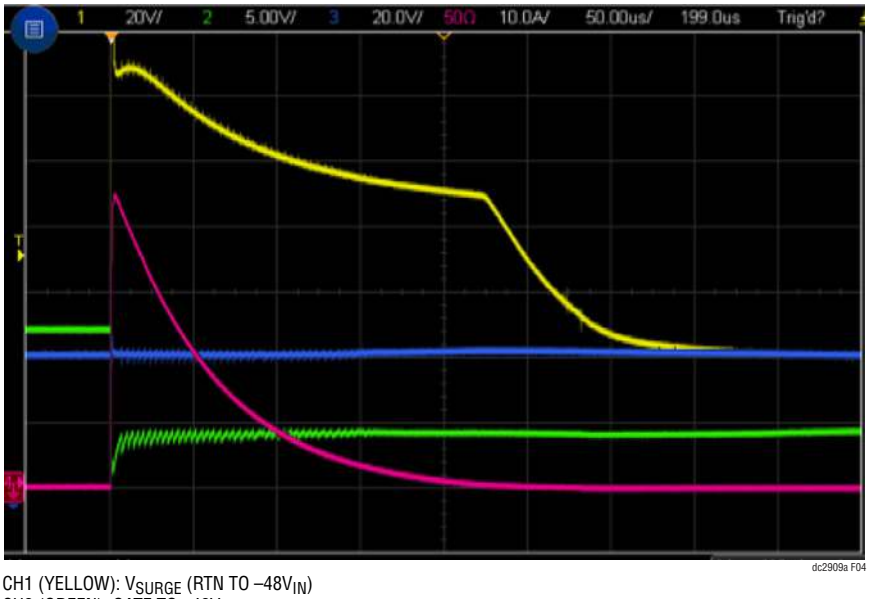


Figure 2. DC2909A IEC61000-4-5 Surge Test Setup

DC2909A IEC61000-4-5 SURGE IMMUNITY TEST

CH1 (YELLOW): V_{SURGE} (RTN TO $-48V_{IN}$)
CH2 (GREEN): GATE TO $-48V_{IN}$
CH3 (BLUE): V_{OUT} (RTN TO $-48V_{OUT}$)
CH4 (PINK): I_{SURGE} (1/3 OF TOTAL)

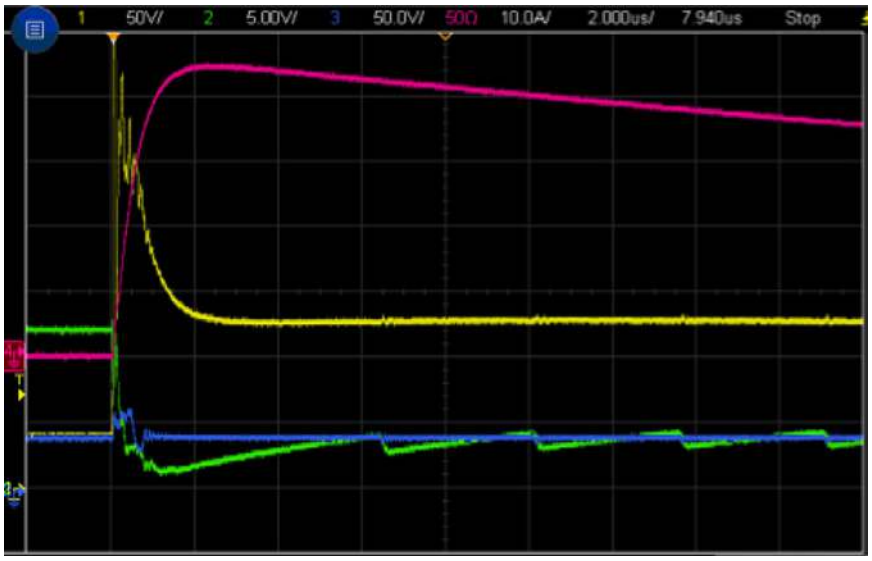
Figure 3. IEC61000-4-5 Surge Test Waveforms (Zoom = 5msec/Div)



CH1 (YELLOW): V_{SURGE} (RTN TO $-48V_{IN}$)
CH2 (GREEN): GATE TO $-48V_{IN}$
CH3 (BLUE): V_{OUT} (RTN TO $-48V_{OUT}$)
CH4 (PINK): I_{SURGE} (1/3 OF TOTAL)

Figure 4. IEC61000-4-5 Surge Test Waveforms (Zoom = 50usec/Div)

DC2909A IEC61000-4-5 SURGE IMMUNITY TEST



CH1 (YELLOW): V_{SURGE} (RTN TO $-48V_{IN}$)
CH2 (GREEN): GATE TO $-48V_{IN}$
CH3 (BLUE): V_{OUT} (RTN TO $-48V_{OUT}$)
CH4 (PINK): I_{SURGE} (1/3 OF TOTAL)

Figure 5. IEC61000-4-5 Surge Test Waveforms (Zoom = 2usec/Div)

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.