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January 2015

FAN6604
Highly Integrated Green-Mode PWM Controller

Features

- High-Voltage Startup
- AC Input Brownout Protection with Hysteresis
- Line Compensation by Current Limit
- Low Operating Current: 1.5 mA
- Linearly Decreasing PWM Frequency to 22 kHz with Cycle Skipping
- Frequency Hopping to Reduce EMI Emission
- Fixed PWM Frequency: 65 kHz
- Peak-Current-Mode Control
- Cycle-by-Cycle Current Limiting
- Leading-Edge Blanking (LEB)
- Internal Open-Loop Protection
- GATE Output Maximum Voltage Clamp: 13 V
- V_{DD} Under-Voltage Lockout (UVLO)
- V_{DD} Over-Voltage Protection (OVP)
- Programmable Over-Temperature Protection (OTP)
- Internal Latch Circuit (OVP, OTP)
- Open-Loop Protection (OLP); Restart for FAN6604MRMX, Latch for FAN6604MLMX
- SENSE Short-Circuit Protection (SSCP)
- Built-in 8 ms Soft-Start Function

Applications

General-purpose switch-mode power supplies (SMPS) and flyback power converters, including:

- Power Adapters

Description

The highly integrated FAN6604 PWM controller provides several features to enhance the performance of flyback converters. To minimize standby power consumption, a proprietary Green-Mode function provides off-time modulation to continuously decrease the switching frequency under light-load conditions.

Under zero-load and very light-load conditions, FAN6604 saves PWM pulses by entering "deep" Burst Mode. Burst Mode enables the power supply to meet international power conservation requirements.

FAN6604 also integrates a frequency-hopping function that helps reduce EMI emission of a power supply with minimum line filters. The built-in synchronized slope compensation helps achieve stable peak-current control. Add in current limit to keep constant output power over universal AC input range. The gate output is clamped at 13 V to protect the external MOSFET from over-voltage damage.

Other protection functions include AC input brownout protection with hysteresis, sense pin short-circuit protection, and V_{DD} over-voltage protection. For over-temperature protection, an external NTC thermistor can be applied to sense the external switcher's temperature. When V_{DD} OVP or OTP are activated, an internal latch circuit is used to latch-off the controller. The Latch Mode is reset when the V_{DD} supply is removed.

FAN6604 is available in an 8-pin SOP package.

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FAN6604MRMX	-40 to +105°C	8-Pin, Small Outline Package (SOP)	Tape & Reel
FAN6604MLMX			

Application Diagram

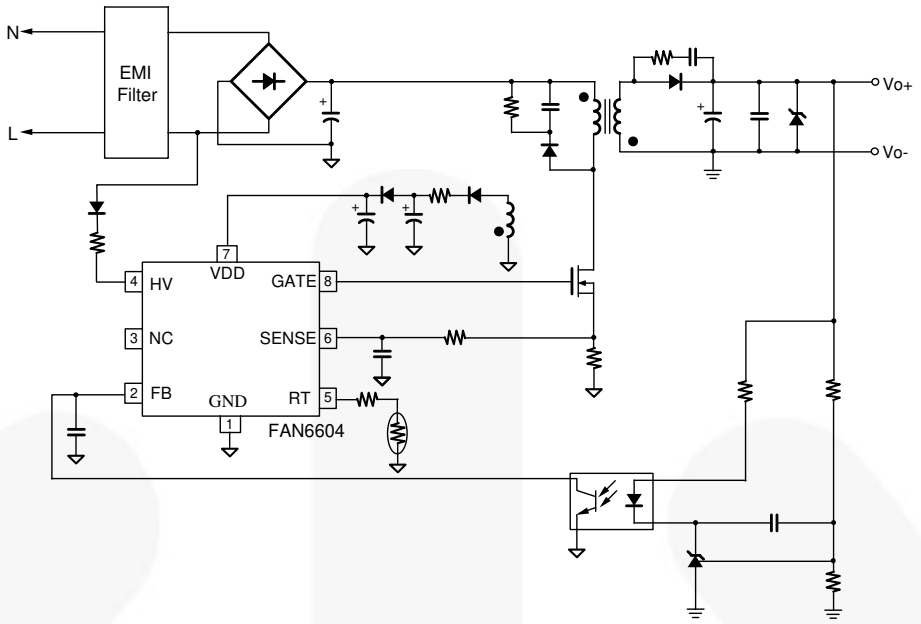


Figure 1. Typical Application

Internal Block Diagram

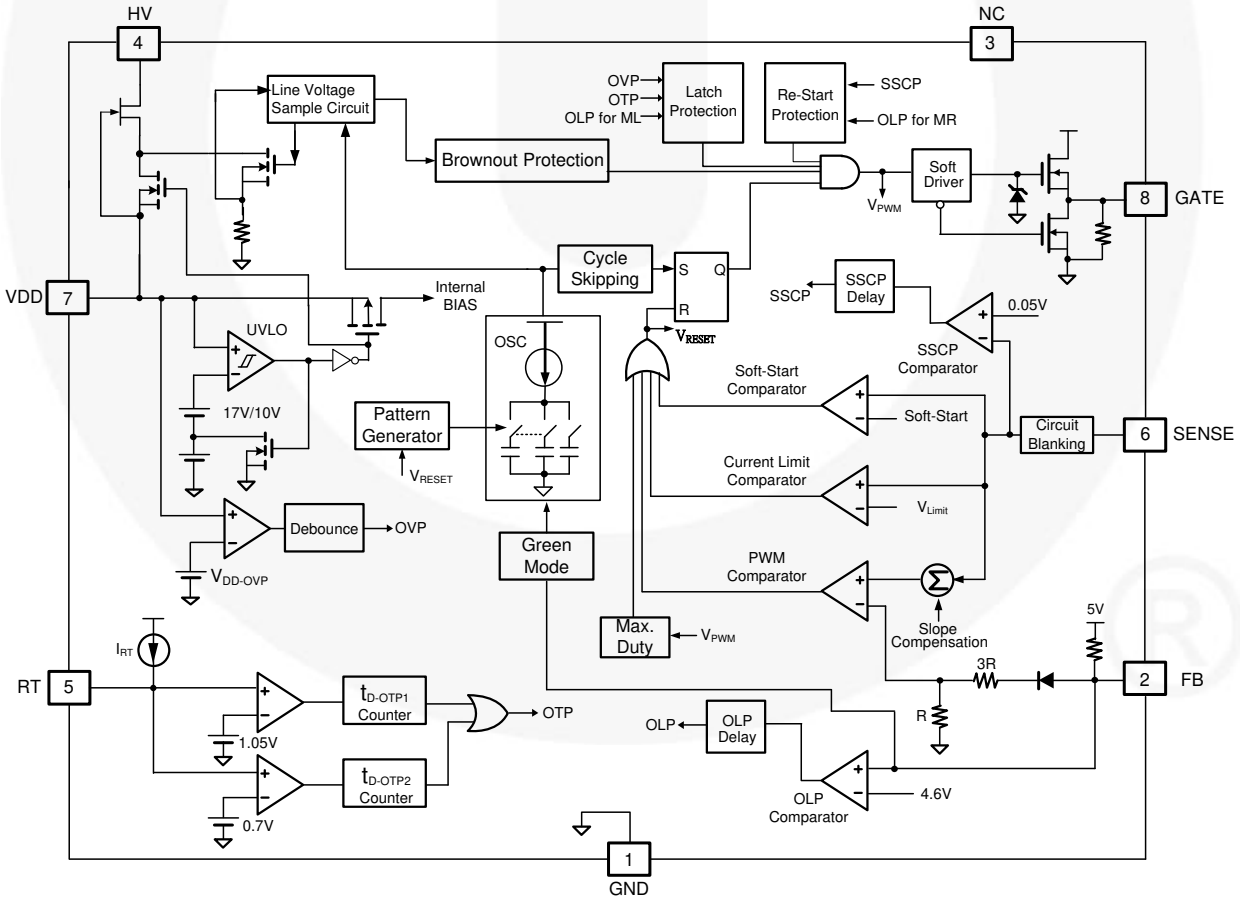
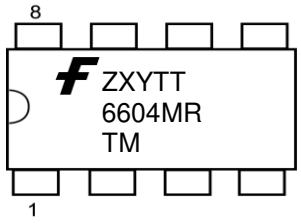
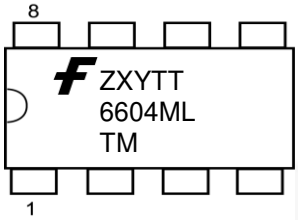


Figure 2. Functional Block Diagram

Marking Information





F - Fairchild Logo
Z - Plant Code
X - 1-Digit Year Code
Y - 1-Digit Week Code
TT - 2-Digit Die Run Code
T - Package Type (M=SOP)
M - Manufacture Flow Code

Figure 3. Top Mark

Pin Configuration

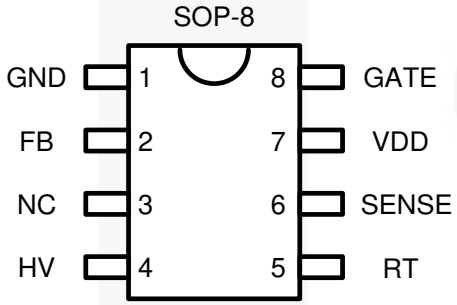


Figure 4. Pin Configuration (Top View)

Pin Definitions

Pin #	Name	Description
1	GND	**Ground**. This pin is used for the ground potential of all the pins. A 0.1 µF decoupling capacitor placed between VDD and GND is recommended.
2	FB	**Feedback**. The output voltage feedback information from the external compensation circuit is fed into this pin. The PWM duty cycle is determined by this pin and the current-sense signal from Pin 6. FAN6604 performs open-loop protection (OLP); if the FB voltage is higher than a threshold voltage (around 4.6 V) for more than 56 ms, the controller latches off the PWM.
3	NC	**No Connection**
4	HV	**High-Voltage Startup**. This pin is connected to the line input via a 1N4007 and 200 kΩ resistor to achieve brownout. Once the voltage on the HV pin is lower than the brownout voltage, PWM output turns off.
5	RT	**Over-Temperature Protection**. An external NTC thermistor is connected from this pin to GND. The impedance of the NTC decreases at high temperatures. Once the voltage on the RT pin drops below the threshold voltage, the controller latches off the PWM. If RT pin is not connected to an NTC resistor for Over-Temperature Protection, a 100 kΩ resistor is recommend to connect the RT pin to the GND pin. This pin is limited by an internal clamping circuit.
6	SENSE	**Current Sense**. This pin is used to sense the MOSFET current for the current-mode PWM and current limiting. To achieve high/low line compensation, current limit is built-in.
7	VDD	**Supply Voltage**. IC operating current and MOSFET driving current are supplied using this pin. This pin is connected to an external bulk capacitor of typically 47 µF. The threshold voltages for turn-on and turn-off are 17 V and 10 V, respectively. The operating current is lower than 2 mA.
8	GATE	**Gate Drive Output**. The totem-pole output driver for the power MOSFET. It is internally clamped below 13 V.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{VDD}	DC Supply Voltage[1,2]			30	V
V_{FB}	FB Pin Input Voltage		-0.3	6.0	V
V_{SENSE}	SENSE Pin Input Voltage		-0.3	6.0	V
V_{RT}	RT Pin Input Voltage		-0.3	6.0	V
V_{HV}	HV Pin Input Voltage			500	V
P_D	Power Dissipation ($T_A < 50°C$)			400	mW
Θ_{JA}	Thermal Resistance (Junction-to-Air)			150	°C/W
T_J	Operating Junction Temperature		-40	+125	°C
T_{STG}	Storage Temperature Range		-55	+150	°C
T_L	Lead Temperature (Wave Soldering or IR, 10 Seconds)			+260	°C
ESD	Electrostatic Discharge Capability, All Pins Except HV Pin	Human Body Model; JESD22-A114		5000	V
		Charged Device Model; JESD22-C101		2000	

Notes:
1. All voltage values, except differential voltages, are given with respect to the network ground terminal.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
3. ESD with HV pin: CDM=1000 V and HBM=1000 V.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
R_{HV}	HV Startup Resistor	150	200	250	kΩ

Electrical Characteristics

V_{DD}=11~24 V and T_A=-40~105°C unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD} Section						
V_{OP}	Continuously Operating Voltage				24	V
V_{DD-ON}	Start Threshold Voltage		16	17	18	V
V_{DD-OFF}	Minimum Operating Voltage		9	10	11	V
V_{DD-OLP}	I_{DD-OLP} Off Voltage		5	6.5	8	V
V_{DD-LH}	Threshold Voltage on VDD Pin for Latch-Off Release Voltage		3.5	4.0	4.5	V
V_{DD-AC}	Threshold Voltage on VDD Pin for Disable AC Recovery to Avoid Startup Failed		V_{DD-OFF} +2.8	V_{DD-OFF} +3.3	V_{DD-OFF} +3.8	V
I_{DD-ST}	Startup Current	V_{DD-ON} – 0.16 V			30	µA
I_{DD-OP1}	Operating Supply Current, PWM Operation	V_{DD}=20 V, FB=3 V Gate Open		1.5	2.0	mA
I_{DD-OP2}	Operating Supply Current, Gate Stop	V_{DD}=20 V, FB=3 V		1.0	1.5	mA
I_{LH}	Operating Current at PWM-Off Phase Under Latch-Off Conduction	V_{DD}=5 V	30	60	90	µA
I_{DD-OLP}	Internal Sink Current Under Latch-Off Conduction	V_{DD-OLP}+0.1 V, T_A=25°C	150	180	210	µA
V_{DD-OVP}	V_{DD} Over-Voltage Protection		24	25	26	V
$t_{D-VDDOVP}$	V_{DD} Over-Voltage Protection Debounce Time		90	180	270	µs
HV Section						
I_{HV}	Supply Current from HV Pin	V_{AC}=90 V (V_{DC}=120 V), V_{DD}=0 V, T_A=25°C	2.0	3.5	5.0	mA
I_{HV-LC}	Leakage Current after Startup	HV=500 V, V_{DD}=V_{DD-OFF}+1 V		1	20	µA
V_{AC-OFF}	Brownout Threshold	DC Source Series R=200 kΩ to HV Pin *See Equation* (1)	92	102	112	V
V_{AC-ON}	Brown-In Threshold	DC Source Series R=200 kΩ to HV Pin *See Equation* (2)	104	114	124	V
ΔV_{AC}	V_{AC-ON} - V_{AC-OFF}	DC Source Series R=200 kΩ to HV Pin	6	12	18	V
$t_{S-CYCLE}$	Line Voltage Sample Cycle[4]	FB > V_{FB-N}		220		µs
		FB < V_{FB-G}		650		
t_{H-TIME}	Line Voltage Hold Period[4]			20		µs
$t_{D-AC-OFF}$	PWM Turn-off Debounce Time	FB > V_{FB-N}	58	70	82	ms
		FB < V_{FB-G}	150	200	250	ms

Note:

4. Guaranteed by design.

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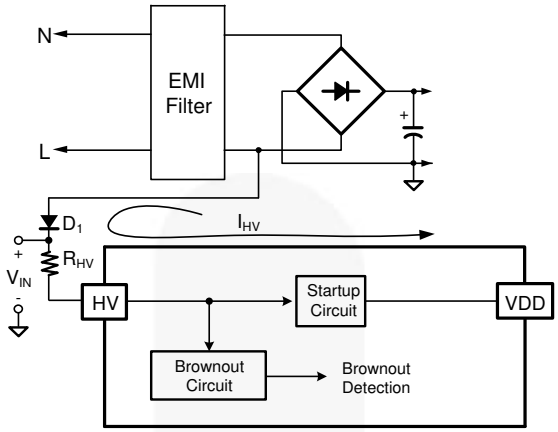

Figure 5. Brownout Circuit

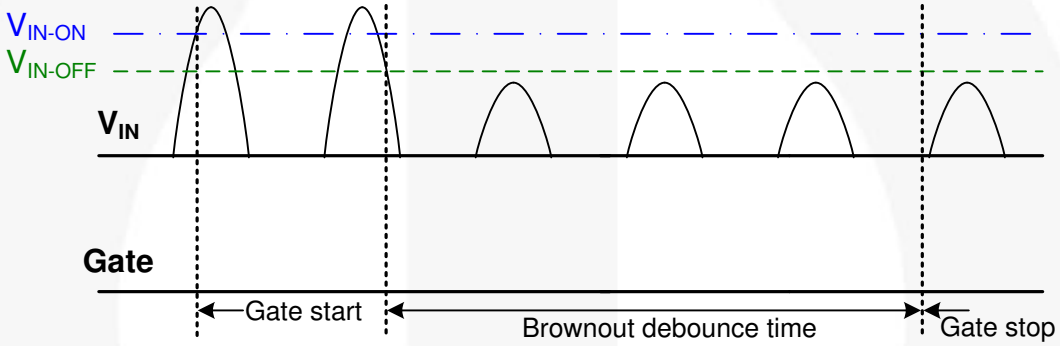

Figure 6. Brownout Behavior

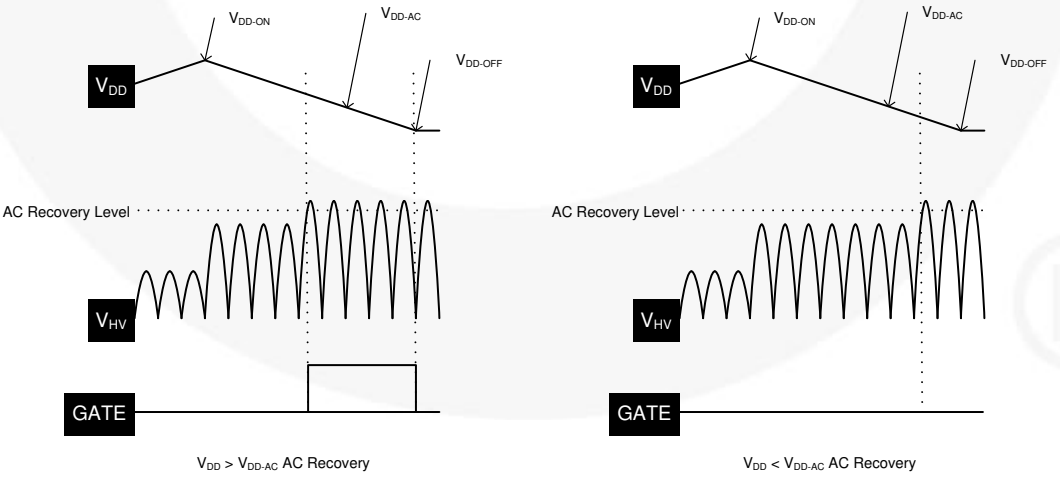

Figure 7. V_{DD-AC} and AC Recovery

Electrical Characteristics (Continued)

V_{DD}=11~24 V and T_A=-40~105°C unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Oscillator Section						
f_{OSC}	Frequency in Normal Mode	Center Frequency, T_A=25°C	61	65	69	kHz
		Hopping Range	±3.7	±4.2	±4.7	
t_{HOP}	Hopping Period		12.0	13.5	15.0	ms
f_{OSC-G}	Green-Mode Frequency		19	22	25	kHz
f_{DV}	Frequency Variation vs. V_{DD} Deviation	V_{DD}=11 V to 22 V			5	%
f_{DT}	Frequency Variation vs. Temperature Deviation	T_A=-40 to +105°C			5	%
Feedback Input Section						
A_V	Input Voltage to Current-Sense Attenuation		1/4.5	1/4.0	1/3.5	V/V
Z_{FB}	Input Impedance		13	15	17	kΩ
$V_{FB-OPEN}$	Output High Voltage	FB Pin Open	4.8	5.0	5.2	V
V_{FB-OLP}	FB Open-Loop Trigger Level		4.3	4.6	4.9	V
t_{D-OLP}	Delay Time of FB Pin Open-Loop Protection		50	57	64	ms
V_{FB-N}	Green-Mode Entry FB Voltage	Pin, FB Voltage (FB=V_{FB-N}), T_A=25°C	2.6	2.8	3.0	V
		Hopping Range	±3.7	±4.2	±4.7	kHz
V_{FB-G}	Green-Mode Ending FB Voltage	Pin, FB Voltage (FB=V_{FB-G})	2.1	2.3	2.5	V
		Hopping Range[5]	±1.27	±1.45	±1.62	kHz
$V_{FB-SKIP}$	FB Threshold Voltage for Cycle Skipping Period Divide[5]	(V_{FB-N}+V_{FB-G})/2	2.35	2.55	2.75	V
t_{SKIP-N}	Cycle Skipping Period[5]	$V_{FB-SKIP}$ < V_{FB} < V_{FB-N}	180	200	220	ms
t_{SKIP-G}	Cycle Skipping Period[5]	V_{FB-G} < V_{FB} < $V_{FB-SKIP}$	90	100	110	ms
$V_{FB-ZDCR}$	FB Threshold Voltage for Zero-Duty Recovery		1.9	2.1	2.3	V
V_{FB-ZDC}	FB Threshold Voltage for Zero-Duty		1.8	2.0	2.2	V

Note:

5. Guaranteed by design.

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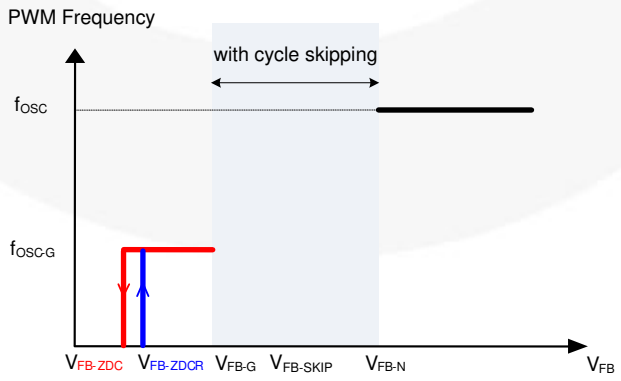


Figure 8. V_{FB} vs. PWM Frequency

Electrical Characteristics (Continued)

V_{DD}=11~24 V and T_A=-40~105°C unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Current-Sense Section						
t_{PD}	Delay to Output			100	250	ns
t_{LEB}	Leading-Edge Blanking Time		210	260	310	ns
V_{STHFL}	Flat Threshold Voltage for Current Limit	Duty>62%, FB > V_{FB-N}	0.46	0.50	0.54	V
V_{STHVA}	Valley Threshold Voltage for Current Limit	Duty=0%	0.31	0.34	0.37	V
V_{SSCP}	Threshold Voltage for Sense Short-Circuit Protection		0.03	0.05	0.07	V
$t_{ON-SSCP}$	On Time for V_{SSCP} Checking		3.85	4.40	4.95	µs
t_{D-SSCP}	Delay for Sense Short-Circuit Protection	V_{SENSE}<0.05 V	60	120	180	µs
t_{SS}	Soft-Start Time	Startup Time	5.5	7.5	9.5	ms
GATE Section						
DCY_{MAX}	Maximum Duty Cycle		75.0	82.5	90.0	%
V_{GATE-L}	Gate Low Voltage	V_{DD}=15 V, I_O=50 mA			1.5	V
V_{GATE-H}	Gate High Voltage	V_{DD}=12 V, I_O=50 mA	8			V
$I_{GATE-SINK}$	Gate Sink Current[5]	V_{DD}=15 V	300			mA
$I_{GATE-SOURCE}$	Gate Source Current[5]	V_{DD}=15 V, GATE=6 V	250			mA
t_r	Gate Rising Time	V_{DD}=15 V, C_L=1 nF		100		ns
t_f	Gate Falling Time	V_{DD}=15 V, C_L=1 nF		50		ns
$V_{GATE-CLAMP}$	Gate Output Clamping Voltage	V_{DD}=22 V	9	13	17	V
RT Section						
I_{RT}	Output Current from RT Pin		92	100	108	µA
V_{RTTH1}	Over-Temperature Protection Threshold Voltage	0.7 V < V_{RT} < 1.05 V, after 12 ms Latch Off	1.000	1.035	1.070	V
V_{RTTH2}		V_{RT} < 0.7 V, After 100 µs Latch Off	0.65	0.70	0.75	
t_{D-OTP1}	Over-Temperature Latch-Off Debounce	V_{RTTH2} < V_{RT} < V_{RTTH1} FB > V_{FB-N}	12	16	20	ms
		V_{RTTH2} < V_{RT} < V_{RTTH1} FB < V_{FB-G}	35.5	46.5	57.5	
t_{D-OTP2}		V_{RT}< V_{RTTH2}, FB > V_{FB-N}	110	185	260	µs
		V_{RT}< V_{RTTH2}, FB < V_{FB-G}	215	500	785	

Note:

6. Guaranteed by design.

Typical Performance Characteristics

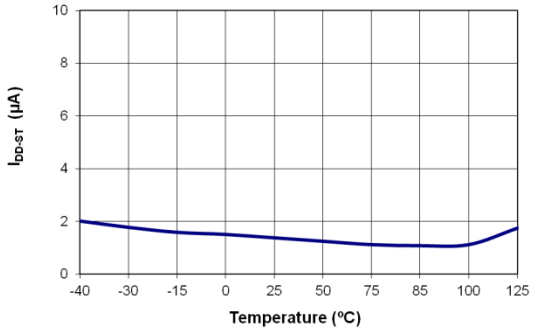


Figure 9. Startup Current (I_{DD-ST}) vs. Temperature

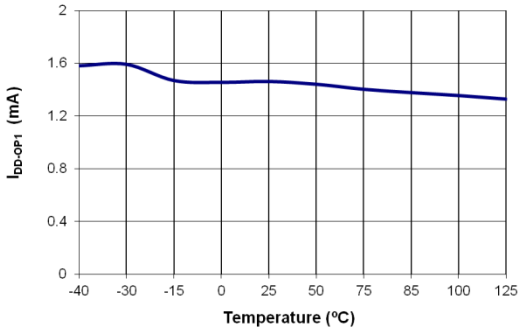


Figure 10. Operation Supply Current (I_{DD-OP1}) vs. Temperature

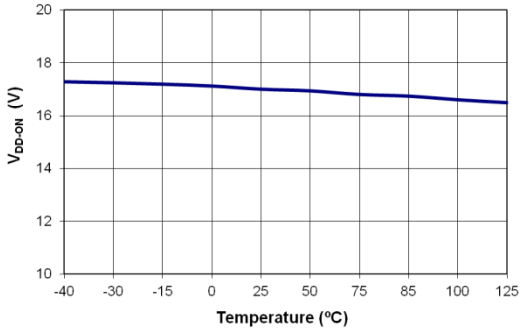


Figure 11. Start Threshold Voltage (V_{DD-ON}) vs. Temperature

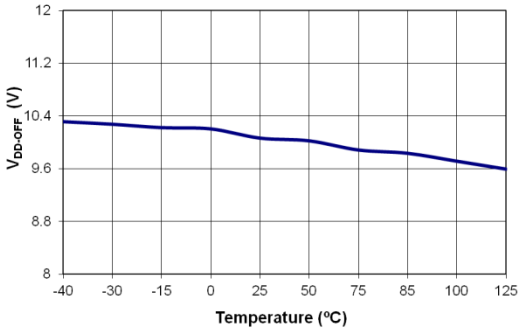


Figure 12. Minimum Operating Voltage (V_{DD-OFF}) vs. Temperature

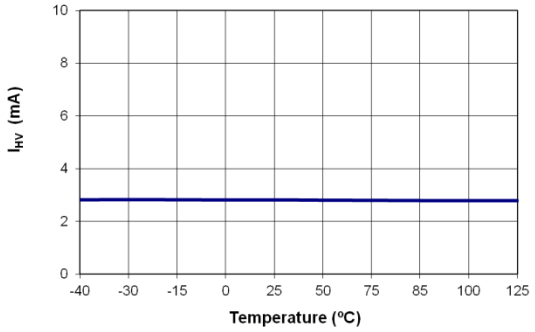


Figure 13. Supply Current Drawn from HV Pin (I_{HV}) vs. Temperature

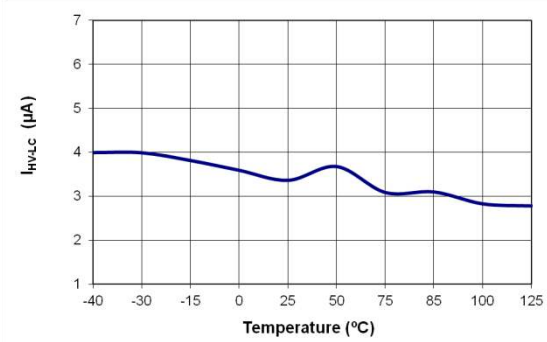


Figure 14. HV Pin Leakage Current After Startup (I_{HV-LC}) vs. Temperature

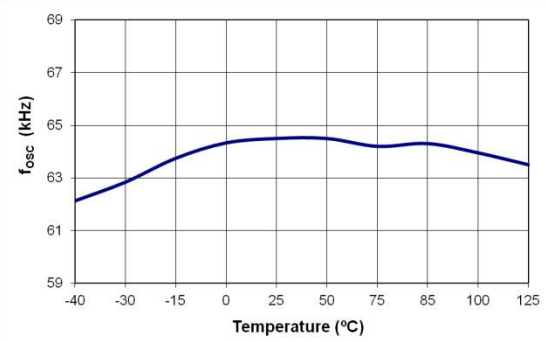


Figure 15. Frequency in Normal Mode (f_{OSC}) vs. Temperature

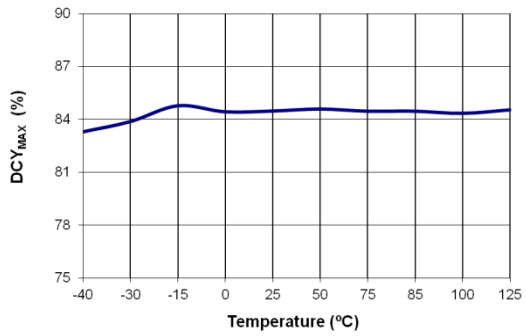


Figure 16. Maximum Duty Cycle (DCY_{MAX}) vs. Temperature

Typical Performance Characteristics (Continued)

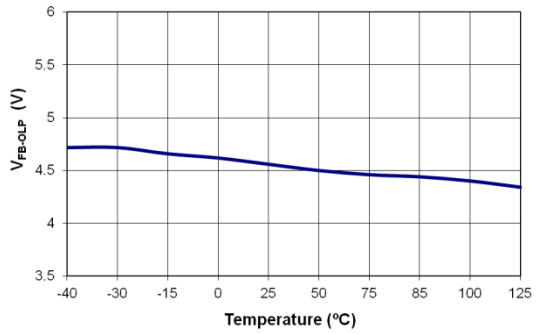


Figure 17. FB Open-Loop Trigger Level (V_{FB-OLP}) vs. Temperature

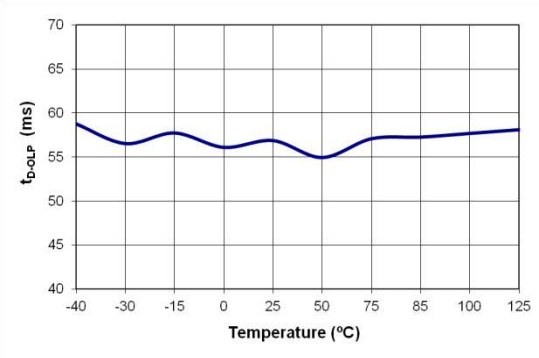


Figure 18. Delay Time of FB Pin Open-Loop Protection (t_{D-OLP}) vs. Temperature

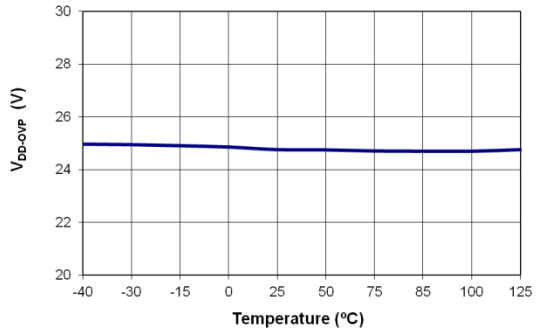


Figure 19. V_{DD} Over-Voltage Protection (V_{DD-OVP}) vs. Temperature

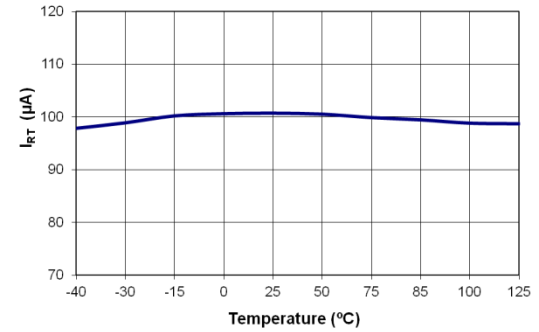


Figure 20. Output Current from RT Pin (I_{RT}) vs. Temperature

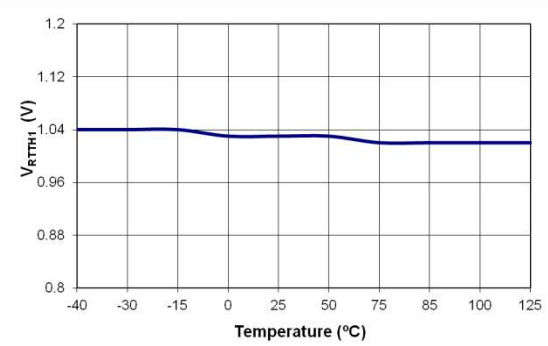


Figure 21. Over-Temperature Protection Threshold Voltage (V_{RTTH1}) vs. Temperature

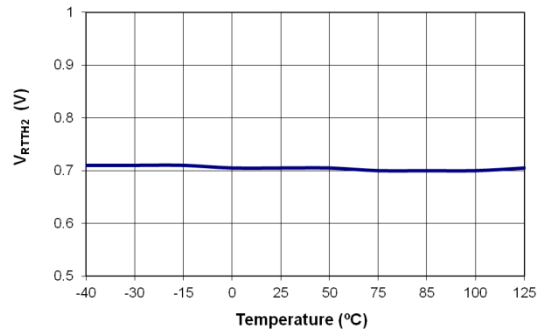


Figure 22. Over-Temperature Protection Threshold Voltage (V_{RTTH2}) vs. Temperature

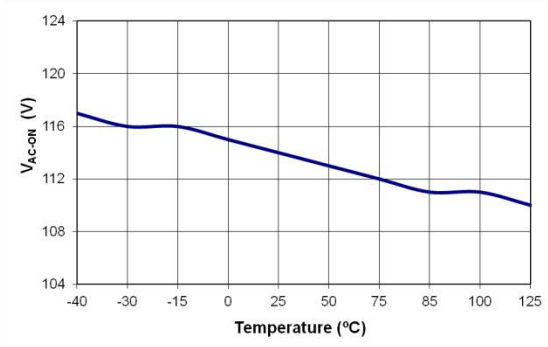


Figure 23. Brown-In (V_{AC-ON}) vs. Temperature

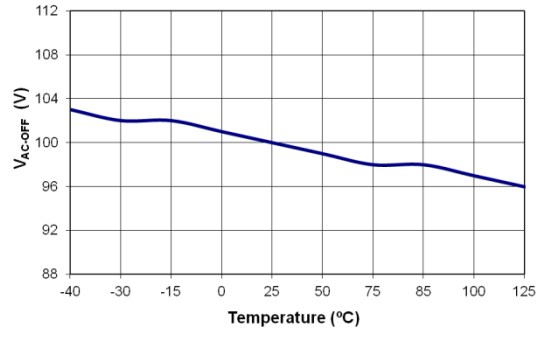


Figure 24. Brownout (V_{AC-OFF}) vs. Temperature

Functional Description

Startup Current

For startup, the HV pin is connected to the line input through an external diode and resistor; R_{HV}, (1N4007 / 200 kΩ recommended). Peak startup current drawn from the HV pin is $(V_{AC} \times \sqrt{2})$ / R_{HV} and charges the hold-up capacitor through the diode and resistor. When the V_{DD} capacitor level reaches $V_{DD\text{-}ON}$, the startup current switches off. At this moment, the V_{DD} capacitor only supplies the FAN6604 to keep the V_{DD} until the auxiliary winding of the main transformer provides the operating current.

Operating Current

Operating current is around 1.5 mA. The low operating current enables better efficiency and reduces the requirement of V_{DD} hold-up capacitance.

Green-Mode Operation

The proprietary Green-Mode function provides off-time modulation to reduce the switching frequency in light-load and no-load conditions. V_{FB}, which is derived from the voltage feedback loop, is taken as the reference. Once V_{FB} is lower than the threshold voltage ($V_{FB\text{-}N}$), the switching frequency is continuously decreased to the minimum Green-Mode frequency of around 22 kHz with cycle skipping.

Current Sensing / PWM Current Limiting

Peak-current-mode control is utilized to regulate output voltage and provide pulse-by-pulse current limiting. The switch current is detected by a sense resistor into the SENSE pin. The PWM duty cycle is determined by this current-sense signal and V_{FB}, the feedback voltage. When the voltage on the SENSE pin reaches around V_{COMP} = (V_{FB}–0.6)/4, the switch cycle is terminated immediately.

Leading-Edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn-on spike occurs on the sense-resistor. To avoid premature termination of the switching pulse, a leading-edge blanking time is built in. During this blanking period, the current-limit comparator is disabled and cannot switch off the gate driver.

Under-Voltage Lockout (UVLO)

The turn-on and turn-off thresholds are fixed internally at 17 V and 10 V, respectively. During startup, the hold-up capacitor must be charged to 17 V through the startup resistor to enable the IC. The hold-up capacitor continues to supply V_{DD} until the energy can be delivered from auxiliary winding of the main transformer. V_{DD} must not drop below 10 V during startup. This UVLO hysteresis window ensures that hold-up capacitor is adequate to supply V_{DD} during startup.

Gate Output / Soft Driving

The BiCMOS output stage is a fast totem-pole gate driver. Cross conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability. The output driver is clamped by an internal 13 V Zener diode to protect power MOSFET transistors against undesirable gate over voltage. A soft driving waveform is implemented to minimize EMI.

Soft-Start

For many applications, it is necessary to minimize the inrush current at startup. The built-in 8 ms soft-start circuit significantly reduces the startup current spike and output voltage overshoot.

Slope Compensation

The sensed voltage across the current-sense resistor is used for peak-current-mode control and cycle-by-cycle current limiting. Built-in slope compensation improves stability and prevents sub-harmonic oscillation. FAN6604 inserts a synchronized, positive-going, ramp at every switching cycle.

Constant Output Power Limit

When the SENSE voltage across sense resistor R_{SENSE} reaches the threshold voltage, the output GATE drive is turned off after a small delay, t_{PD}. This delay introduces an additional current proportional to $t_{PD} \bullet V_{IN} / L_P$. Since the delay is nearly constant, regardless of the input voltage V_{IN}, higher input voltage results in larger additional power. Therefore, the maximum output power at high line is higher than that of low line. To compensate this variation for a wide AC input range, a current limit uses to solve the unequal power-limit problem. The power limiter is fed to the inverting input of the current limiting comparator. This results in a lower current limit at high-line inputs than at low-line inputs.

Brownout by the HV Pin

Unlike previous PWM controllers, the FAN6604 HV pin can detect the AC line voltage to perform brownout protection. Using a fast diode and startup resistor to sample the AC line voltage, the peak value refreshes and is stored in a register at each sampling cycle. When internal update time is met, this peak value is used for brownout and current-limit level judgment. Equation (1) and (2) calculate the level of brown-in or brownout converted to RMS value. For power saving, FAN6604 enlarges the sampling cycle to lower the power loss from HV sampling at light-load condition.

$$V_{AC\text{-}ON}\,(RMS) = \left(0.9V \times \frac{(R_{HV} + 1.6)}{1.6}\right) / \sqrt{2} \quad (1)$$

$$V_{AC\text{-}OFF}\,(RMS) = \left(0.81V \times \frac{(R_{HV} + 1.6)}{1.6}\right) / \sqrt{2} \quad (2)$$

where R_{HV} is in kΩ.

V_{DD} Over-Voltage Protection (OVP)

V_{DD} over-voltage protection prevents damage due to abnormal conditions. If the V_{DD} voltage exceeds the over-voltage protection level (V_{DD-OVP}) and lasts for $t_{D-VDDOVP}$, the PWM pulses are disabled and V_{DD} begins to drop. As V_{DD} drops to V_{DD-OLP}, the internal HV startup circuit is activated and V_{DD} is charged to V_{DD-ON} to restart IC. Over-voltage conditions are usually caused by open feedback loops.

Sense-Pin Short-Circuit Protection

The FAN6604 provides safety protection for Limited Power Source (LPS) tests. When the sense resistor is shorted by soldering during production, the pulse-by-pulse current limiting loses efficiency for the purpose of providing over-power protection for the unit. The unit may be damaged when the loading is larger than the maximum load. To protect against a short circuit across the current-sense resistor, the controller is designed to immediately shut down if a continuously low voltage (around 0.05 V/120 µs) on the SENSE pin is detected.

Thermal Protection

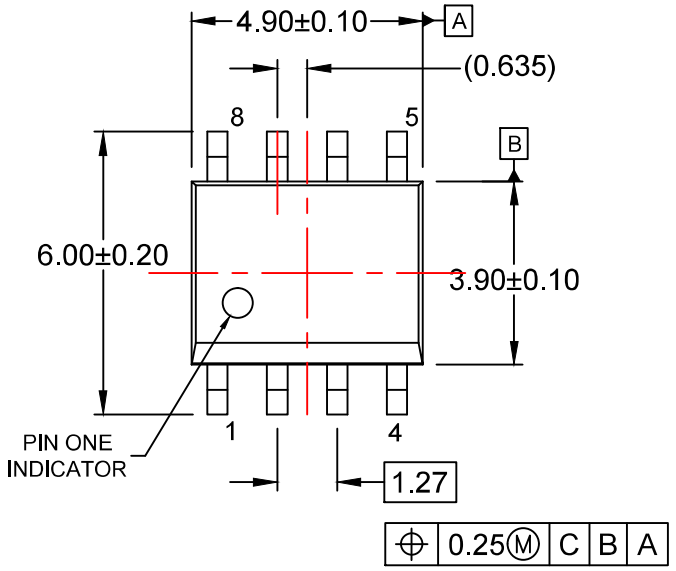
An NTC thermistor, R_{NTC}, in series with resistor R_A, can be connected from the RT pin to ground. A constant current, I_{RT}, is output from the RT pin. The voltage on the RT pin can be expressed as $V_{RT}=I_{RT} \bullet (R_{NTC} + R_{PTC})$, where I_{RT} is 100 µA. At high ambient temperature, the R_{NTC} is smaller and so that V_{RT} decreased. When V_{RT} is less than 1.035 V (V_{RTTH1}), the PWM turns off after 16 ms (t_{D-OTP1}). If V_{RT} is less than 0.7 V (V_{RTTH2}), the PWM turns off after 185 µs (t_{D-OTP2}). If the RT pin is not connected to NTC resistor for over-temperature protection, connecting a series one 100 kΩ resistor to ground to prevent from noise interference is recommended. This pin is limited by an internal clamping circuit.

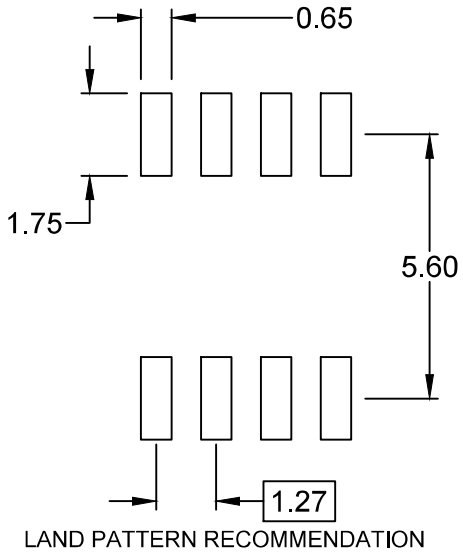
Limited Power Control

The FB voltage is pulled HIGH once the power supply cannot sustain the output load, such as during output-short or overload conditions. If the FB voltage remains higher than a built-in threshold for longer than t_{D-OLP}, PWM output is turned off. As PWM output is turned off, V_{DD} begins decreasing. When V_{DD} goes below the turn-off threshold (10 V) the controller is totally shut down and V_{DD} is continuously discharged to V_{DD-OLP} (6.5 V) by I_{DD-OLP} to lower the average input power. This is called two-level UVLO. V_{DD} is cycled again. This protection feature continues as long as the overloading condition persists. This prevents the power supply from overheating due to overloading conditions.

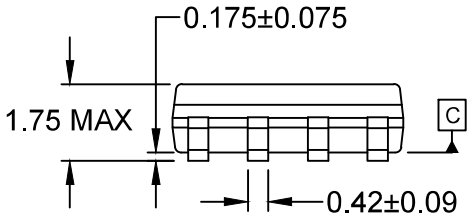
Noise Immunity

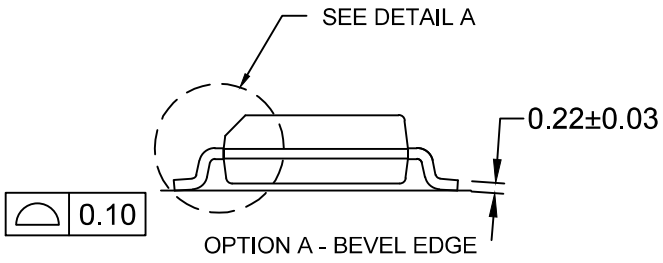
Noise on the current sense or control signal may cause significant pulse-width jitter, particularly in continuous-conduction mode. Slope compensation helps alleviate this problem. Good placement and layout practices should be followed. Avoiding long PCB traces and component leads, locating compensation and filter components near the FAN6604, and increasing the power MOS gate resistance improve performance.



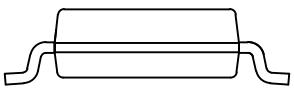


LAND PATTERN RECOMMENDATION

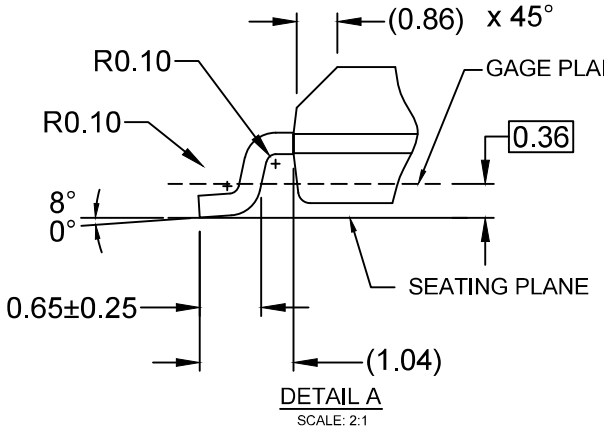




OPTION A - BEVEL EDGE



OPTION B - NO BEVEL EDGE



DETAIL A
SCALE: 2:1

NOTES:

A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
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E) DRAWING FILENAME: M08Arev16

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