

MOSFET

OptiMOS™3 Power-Transistor, 200 V

Features

- N-channel, normal level
- 175 °C rated
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- Pb-free lead plating; RoHS compliant
- Qualified according to JEDEC¹⁾ for target application
- Halogen-free according to IEC61249-2-21
- Ideal for high-frequency switching and synchronous rectification

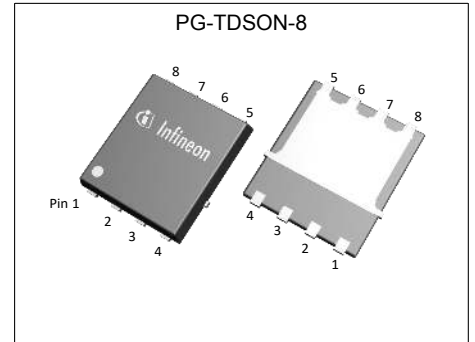
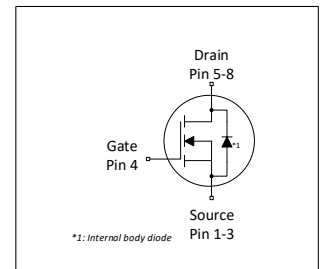


Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	200	V
$R_{DS(on),max}$	35	mΩ
I_D	35	A



RoHS

Type / Ordering Code	Package	Marking	Related Links
BSC350N20NSFD	PG-TDSON-8	350N20NF	-

¹⁾ J-STD20 and JESD22

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1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	-	-	35 27	A	$T_C=25\text{ °C}$ $T_C=100\text{ °C}$
Pulsed drain current ¹⁾	$I_{D,pulse}$	-	-	140	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse	E_{AS}	-	-	97	mJ	$I_D=27.2\text{ A}$, $R_{GS}=25\text{ }\Omega$
Reverse diode peak dv/dt	dv/dt	-	-	60	kV/ μ s	$I_D=68\text{ A}$, $V_{DS}=100\text{ V}$, $di/dt=1500\text{ A}/\mu\text{s}$, $T_{j,max}=175\text{ °C}$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	150	W	$T_C=25\text{ °C}$
Operating and storage temperature	T_j , T_{stg}	-55	-	175	°C	-

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	0.6	1	K/W	-
Thermal resistance, junction - ambient, minimal footprint	R_{thJA}	-	-	75	K/W	-
Thermal resistance, junction - ambient, 6 cm ² cooling area ²⁾	R_{thJA}	-	-	50	K/W	-

3 Electrical characteristics

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	200	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2	3	4	V	$V_{DS}=V_{GS}$, $I_D=90\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.1 10	1 100	μA	$V_{DS}=160\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=160\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	1	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	31	35	m Ω	$V_{GS}=10\text{ V}$, $I_D=35\text{ A}$
Gate resistance	R_G	-	3.3	5	Ω	-
Transconductance	g_{fs}	29	57	-	S	$ V_{DS} >2 I_D R_{DS(on)max}$, $I_D=35\text{ A}$

¹⁾ See Diagram 3

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μ m thick) copper area for drain connection. PCB is vertical in still air.

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	1810	2410	pF	$V_{GS}=0\text{ V}$, $V_{DS}=100\text{ V}$, $f=1\text{ MHz}$
Output capacitance ¹⁾	C_{oss}	-	137	182	pF	$V_{GS}=0\text{ V}$, $V_{DS}=100\text{ V}$, $f=1\text{ MHz}$
Reverse transfer capacitance	C_{rss}	-	5.4	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=100\text{ V}$, $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	8.0	-	ns	$V_{DD}=100\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=17\text{ A}$, $R_{G,ext}=1.6\ \Omega$
Rise time	t_r	-	4.8	-	ns	$V_{DD}=100\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=17\text{ A}$, $R_{G,ext}=1.6\ \Omega$
Turn-off delay time	$t_{d(off)}$	-	17	-	ns	$V_{DD}=100\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=17\text{ A}$, $R_{G,ext}=1.6\ \Omega$
Fall time	t_f	-	4.8	-	ns	$V_{DD}=100\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=17\text{ A}$, $R_{G,ext}=1.6\ \Omega$

Table 6 Gate charge characteristics²⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	8.6	-	nC	$V_{DD}=100\text{ V}$, $I_D=35\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge	Q_{gd}	-	3.0	-	nC	$V_{DD}=100\text{ V}$, $I_D=35\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Switching charge	Q_{sw}	-	6.2	-	nC	$V_{DD}=100\text{ V}$, $I_D=35\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total ¹⁾	Q_g	-	22	30	nC	$V_{DD}=100\text{ V}$, $I_D=35\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	4.7	-	V	$V_{DD}=100\text{ V}$, $I_D=35\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Output charge	Q_{oss}	-	54	-	nC	$V_{DD}=100\text{ V}$, $V_{GS}=0\text{ V}$

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	35	A	$T_C=25\text{ °C}$
Diode pulse current ³⁾	$I_{S,pulse}$	-	-	140	A	$T_C=25\text{ °C}$
Diode hard commutation current ⁴⁾	$I_{S,hard}$	-	-	68	A	$T_C=25\text{ °C}$, $di_F/dt=1500\text{ A}/\mu\text{s}$
Diode forward voltage	V_{SD}	-	1.0	1.2	V	$V_{GS}=0\text{ V}$, $I_F=35\text{ A}$, $T_j=25\text{ °C}$
Reverse recovery time ¹⁾	t_{rr}	-	70	140	ns	$V_R=100\text{ V}$, $I_F=24\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge ¹⁾	Q_{rr}	-	93	186	nC	$V_R=100\text{ V}$, $I_F=24\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$

¹⁾ Defined by design. Not subject to production test.

²⁾ See "Gate charge waveforms" for parameter definition

³⁾ Diode pulse current is defined by thermal and/or package limits

⁴⁾ Maximum allowed hard-commutated current through diode at $di/dt=1500\text{ A}/\mu\text{s}$

4 Electrical characteristics diagrams

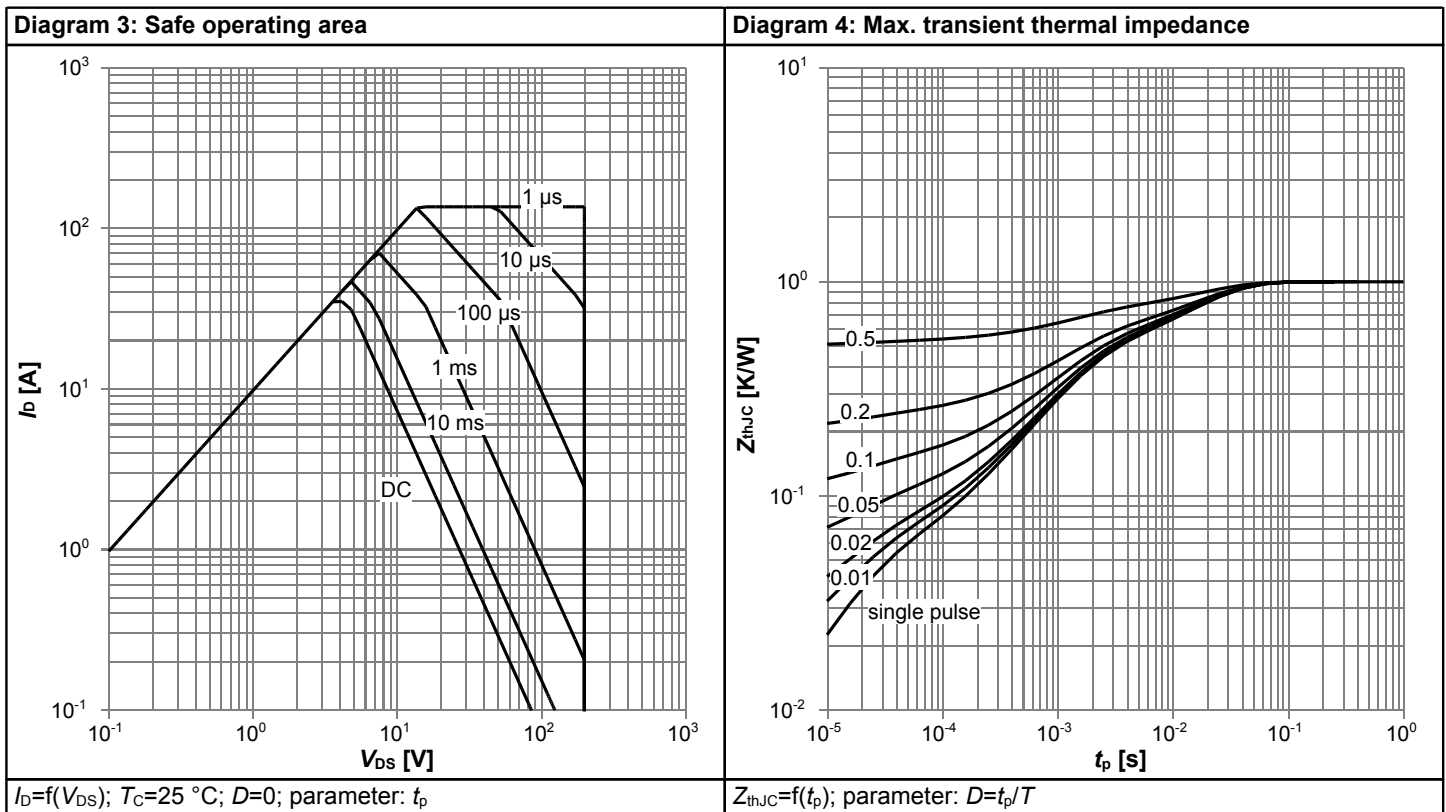
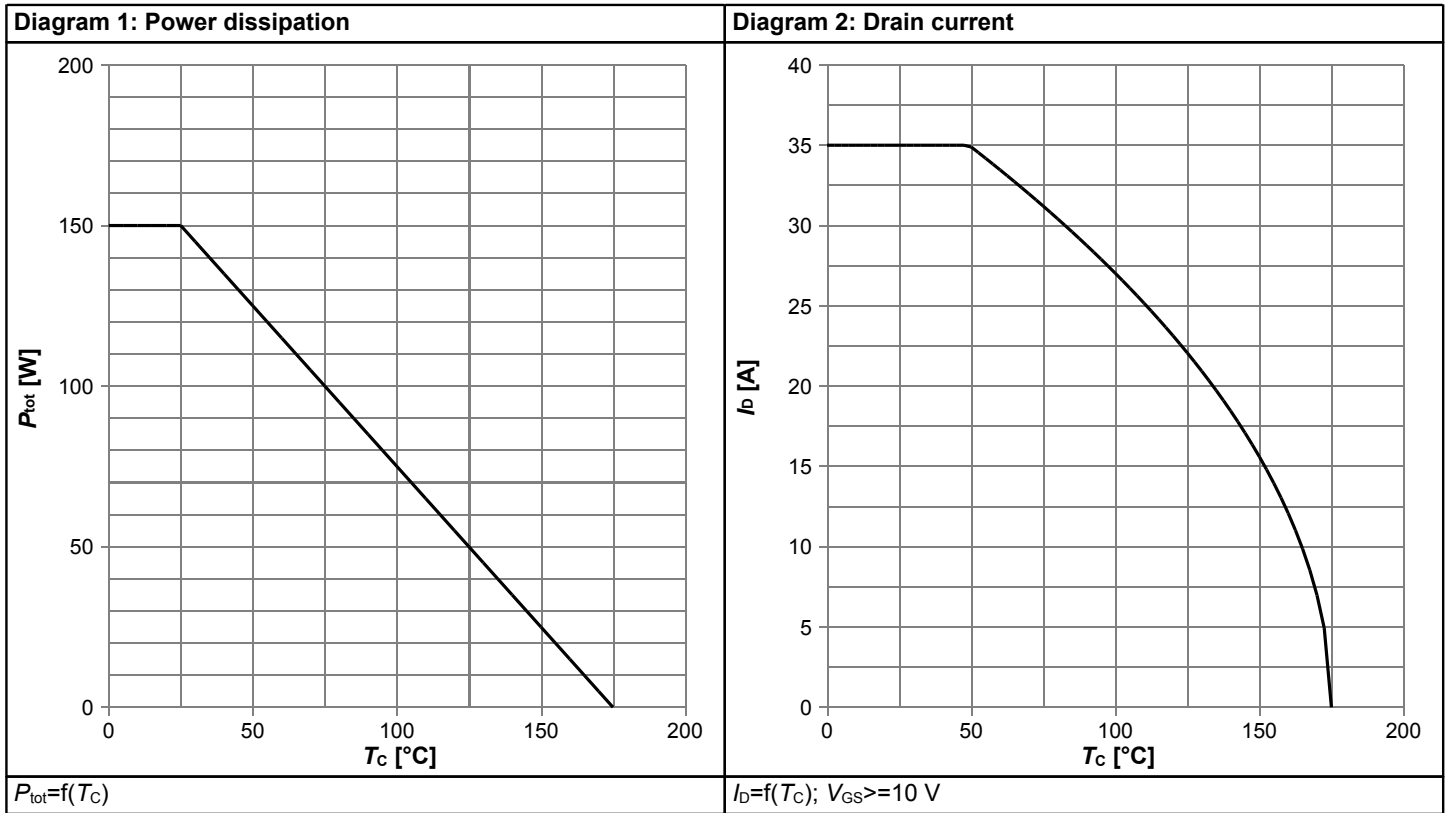
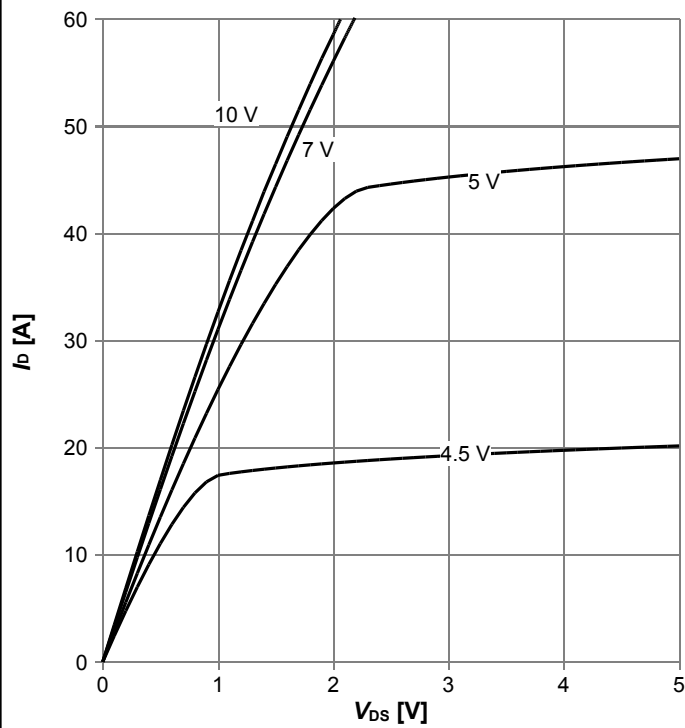
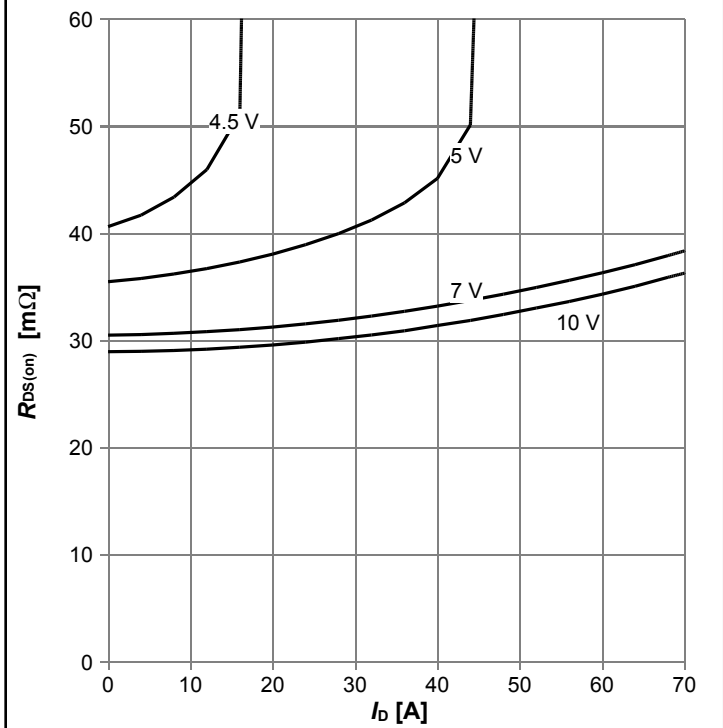


Diagram 5: Typ. output characteristics



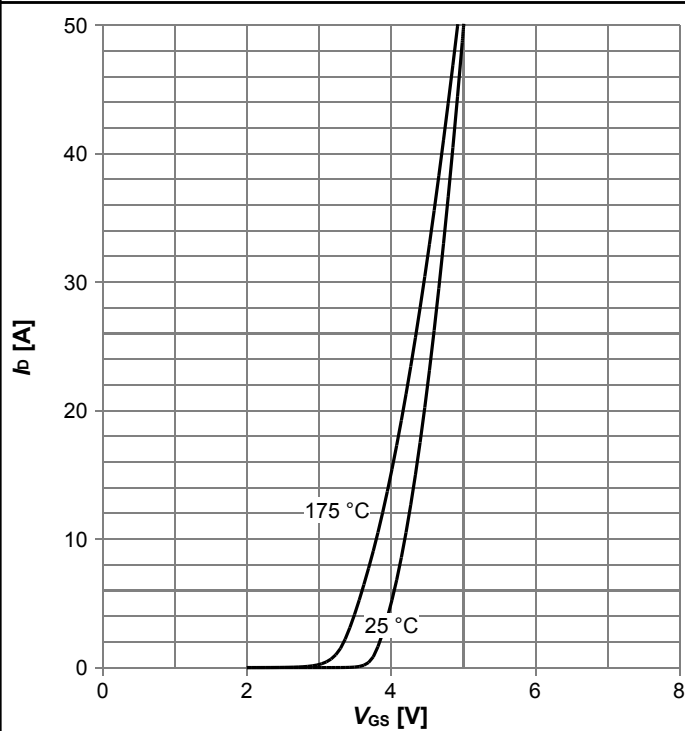
$I_D = f(V_{DS})$; $T_j = 25\text{ °C}$; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



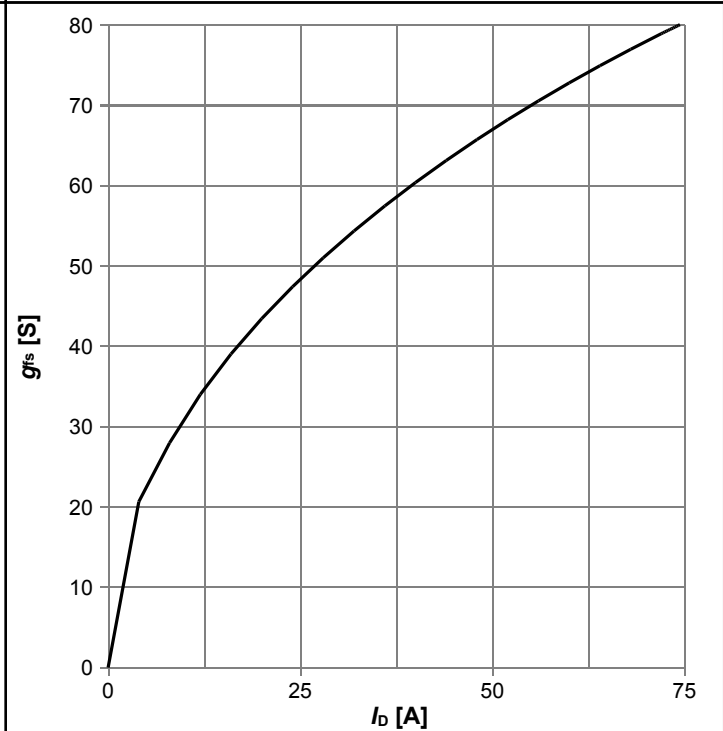
$R_{DS(on)} = f(I_D)$; $T_j = 25\text{ °C}$; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



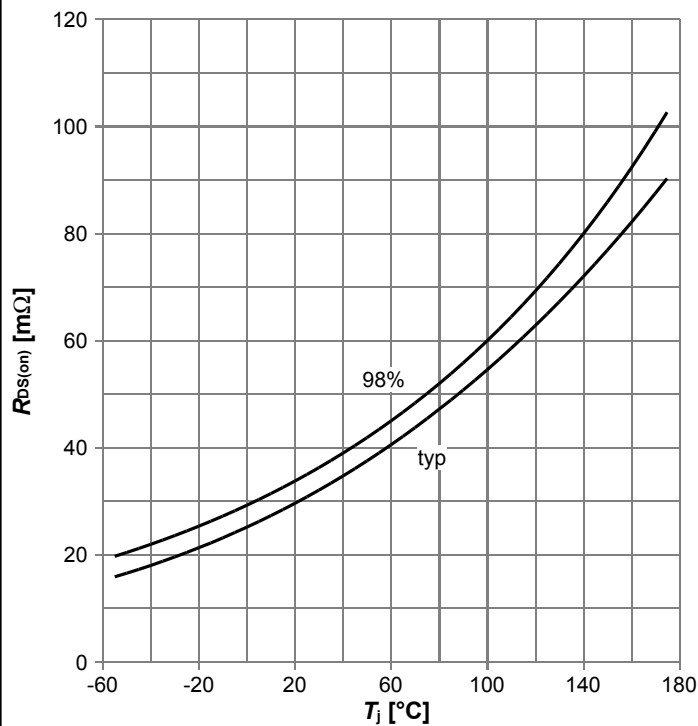
$I_D = f(V_{GS})$; $|V_{DS}| > 2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. forward transconductance



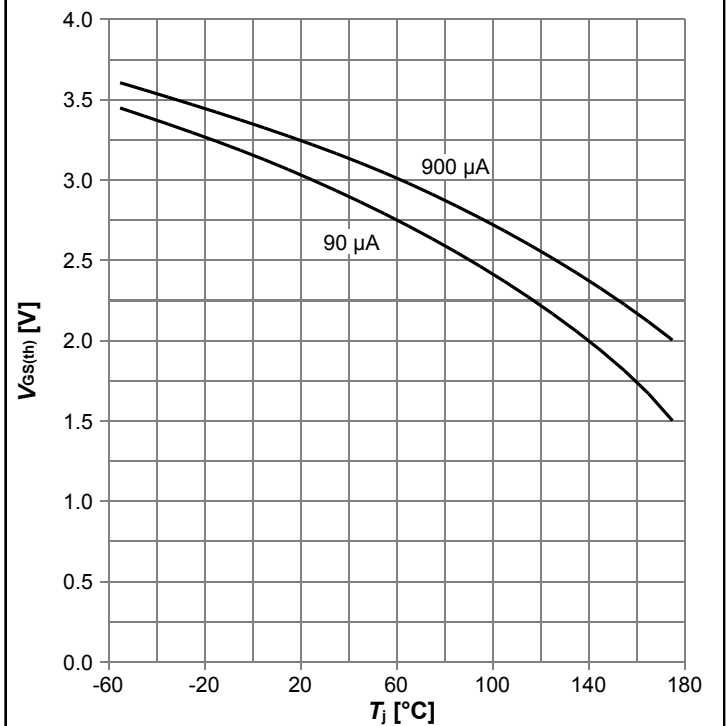
$g_{fs} = f(I_D)$; $T_j = 25\text{ °C}$

Diagram 9: Drain-source on-state resistance



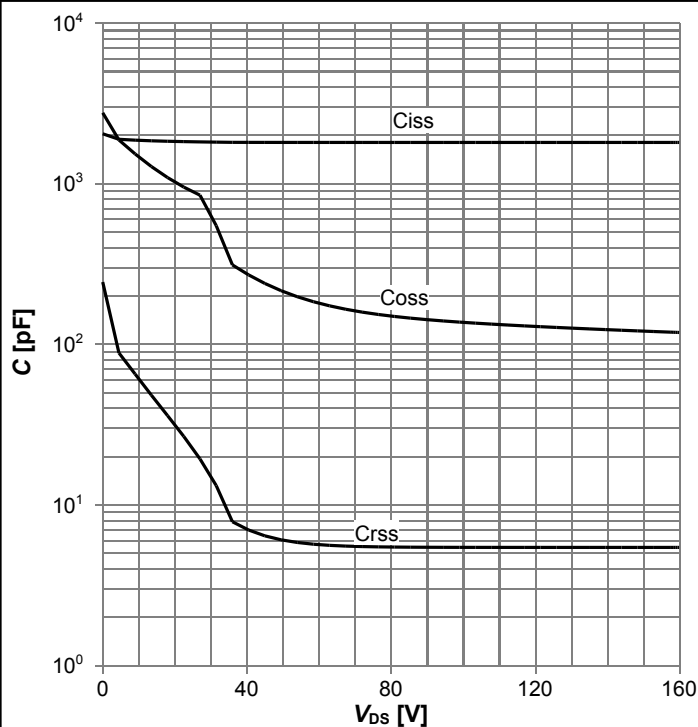
$R_{DS(on)}=f(T_j)$; $I_D=35\text{ A}$; $V_{GS}=10\text{ V}$

Diagram 10: Typ. gate threshold voltage



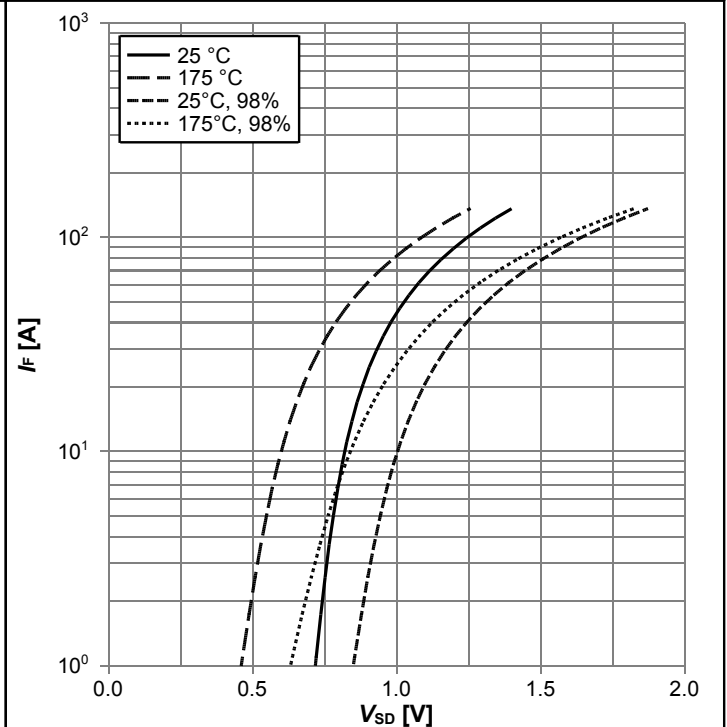
$V_{GS(th)}=f(T_j)$; $V_{GS}=V_{DS}$; parameter: I_D

Diagram 11: Typ. capacitances



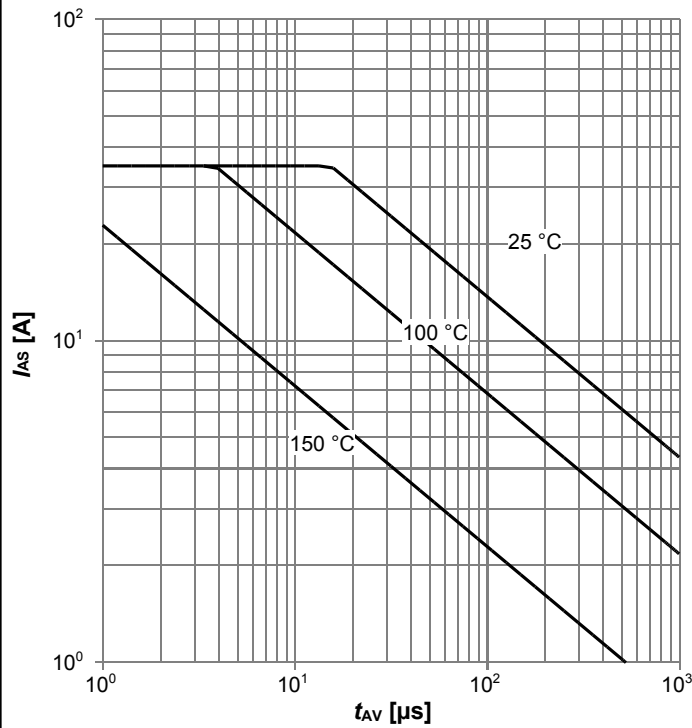
$C=f(V_{DS})$; $V_{GS}=0\text{ V}$; $f=1\text{ MHz}$

Diagram 12: Forward characteristics of reverse diode



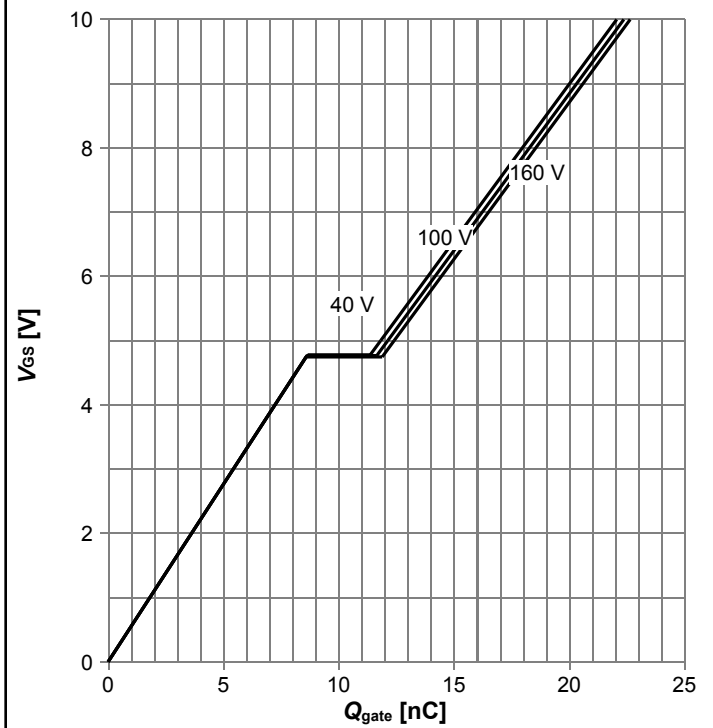
$I_F=f(V_{SD})$; parameter: T_j

Diagram 13: Avalanche characteristics



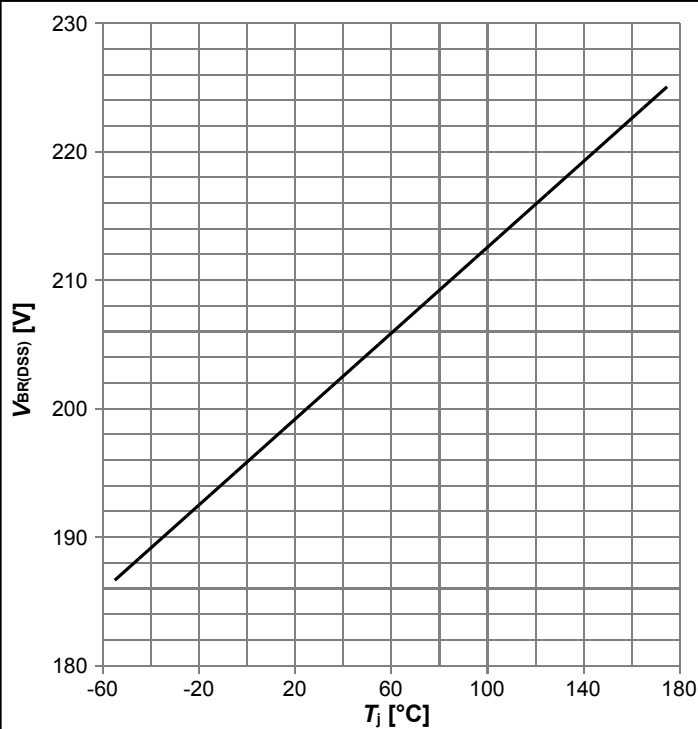
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$; parameter: $T_{j(start)}$

Diagram 14: Typ. gate charge



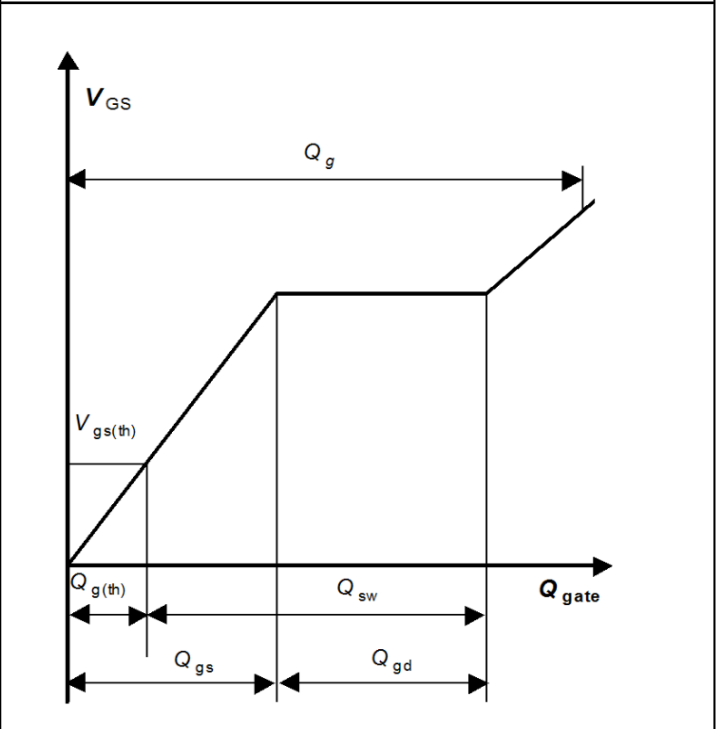
$V_{GS}=f(Q_{gate}); I_D=35 \text{ A pulsed}$; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage

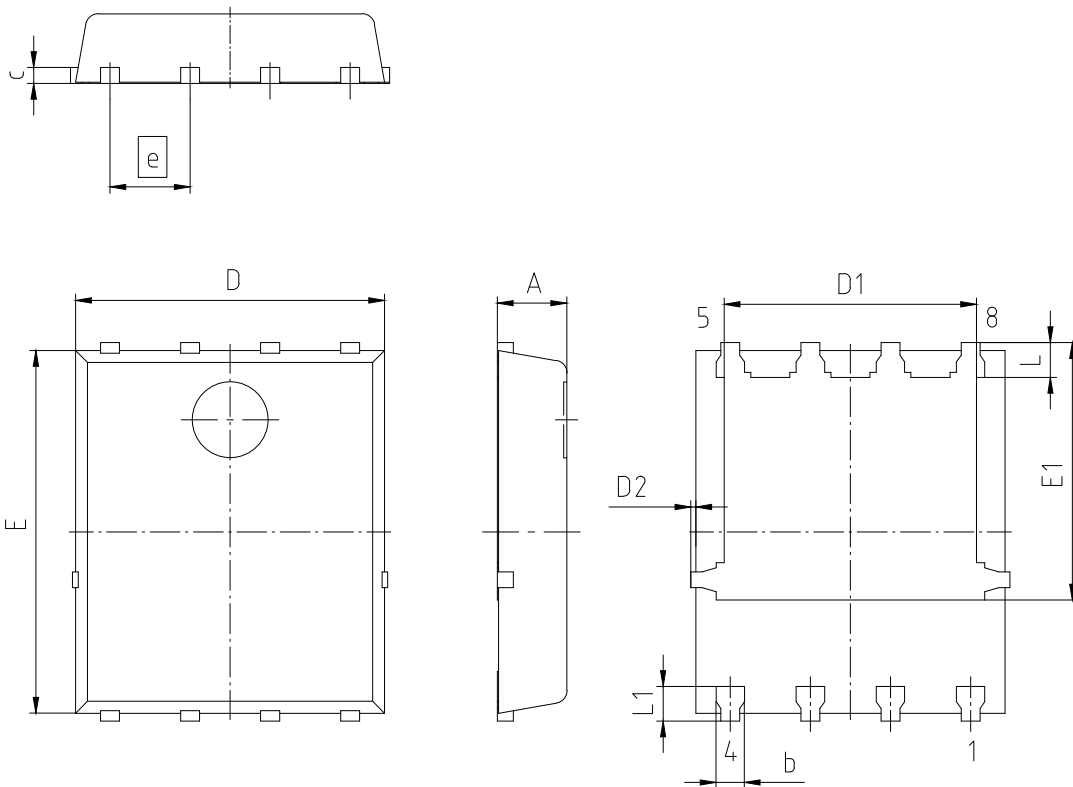


$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

Diagram Gate charge waveforms



5 Package Outlines



PACKAGE - GROUP NUMBER:		PG-TDSON-8-U08	
DIMENSIONS	MILLIMETERS		
	MIN.	MAX.	
A	0.90	1.20	
b	0.34	0.54	
c	0.15	0.35	
D	4.80	5.35	
D1	3.90	4.40	
D2	0.00	0.22	
E	5.70	6.10	
E1	4.05	4.25	
e	1.27		
L	0.45	0.65	
L1	0.45	0.65	

- 1) EXCLUDING MOLD FLASH
- 2) REMOVAL ON MOLD GATE
INTRUSION 0.1 MM
PROTRUSION 0.1 MM
- 3) ALL METAL SURFACES ARE PLATED,
EXCEPT AREA OF CUT

Figure 1 Outline PG-TDSON-8, dimensions in mm

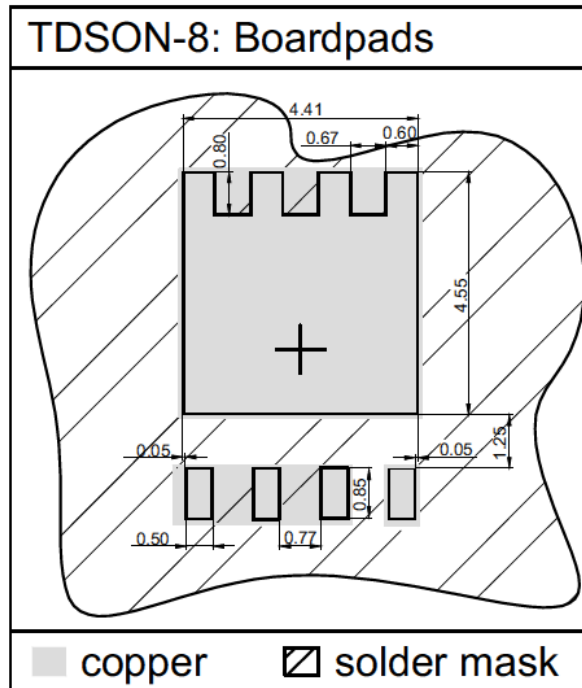


Figure 2 Outline Footprint (TDSO-8)

Revision History

BSC350N20NSFD

Revision: 2022-11-09, Rev. 2.2

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2016-10-21	Release of final version
2.1	2016-12-05	Update Eas
2.2	2022-11-09	Update package outline drawing

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