TEXAS INSTRUMENTS

Translator/Oscillator Buffer
Evaluation Module

User's Guide

September 2004

HPL-D Interface

SLLU086A

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It is important to operate this EVM within the supply voltage range of 3 V to 3.6 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 125°C. The EVM is designed to operate properly with certain components above 125°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Preface

Read This First

About This Manual

This EVM user's guide provides information about the translator/oscillator buffer evaluation module.

How to Use This Manual

This document contains the following chapters:

- Chapter 1 — Introduction
- Chapter2 — Bills of Materials and Schematic

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This book may contain cautions and warnings.

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Data Sheet:	Literature Number:
SN65LVDS16/17/SN65LVP16/17	SLLS625
SN65LVDS18/19/SN65LVP18/19	SLLS624
SN65LVDS20/SN65LVP20	SLLS620

FCC Warning

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

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Chapter 1

Introduction

The translator/oscillator buffer evaluation module (EVM) allows evaluation of the SN65LVDS16/17/18/19/20 and SN65LVP16/17/18/19/20 repeaters/translators/oscillators. This user's guide provides a brief overview of the EVM, operation instructions, and output results.

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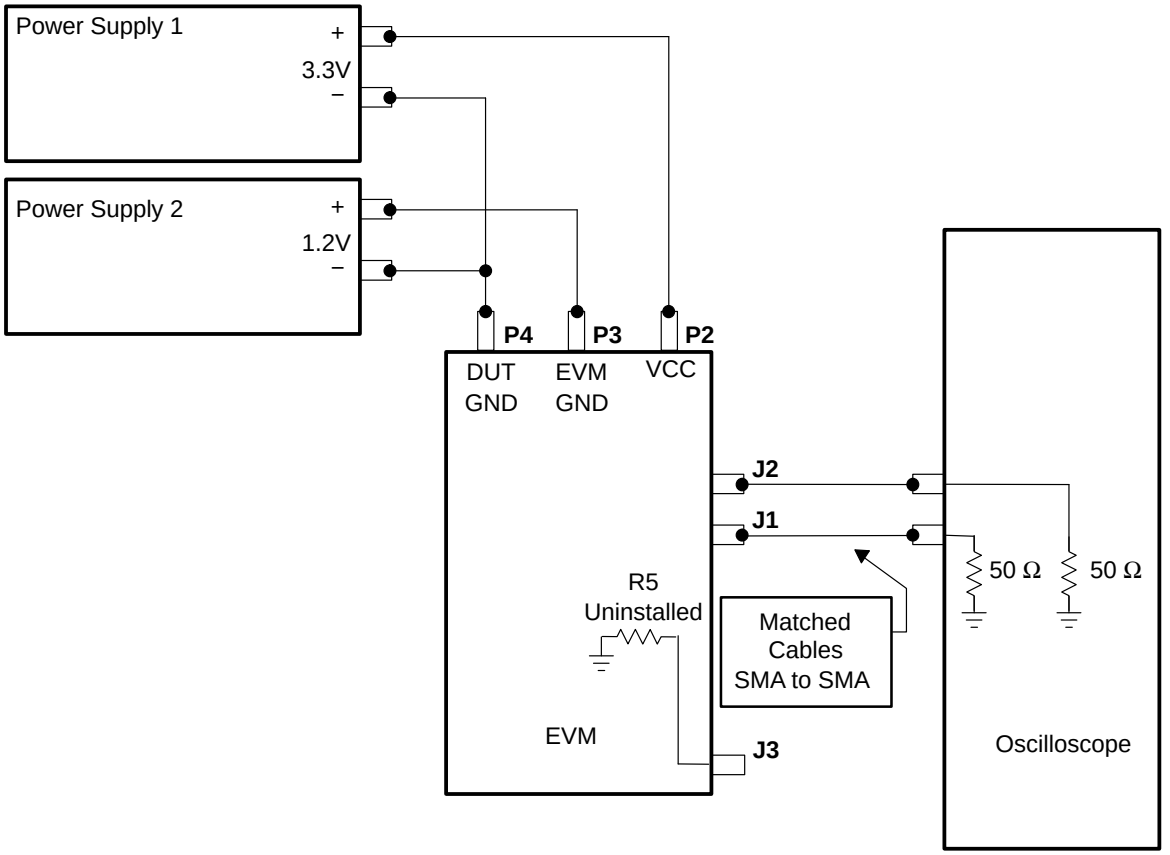
1.1 Evaluation Module U1

Figure 1−1. Power Connections for Evaluation Module U1



Warning

Power jacks P2, P3, and P4 are not insulated on the backside of the EVM. Place the EVM on a nonconductive surface.

1.2 Applying an Input to EVM U1

For the oscillator gain stage/buffer the only requirement is to simply apply power to the EVM. The EVM has a crystal onboard that when powered up supplies a signal to the SN65LVDS16, SN65LVP16, SN65LVDS18, or SN65LVP18 which provides a very clean 155.52 MHz signal at J1 and J2.

1.3 Observing an EVM U1 Output

The outputs are available at J1 and J2 for direct connection to oscilloscope inputs. Matched length cables must be used when connecting the EVM to a scope to avoid inducing skew between the noninverting (+) and inverting (−) outputs.

The three power jacks (P2, P3, and P4) are used to provide power and a ground reference for the EVM. The power connections to the EVM determine the common-mode load to the device. When connecting the EVM outputs directly to oscilloscope inputs, setting of the oscilloscope common-mode offset voltage is required, as the oscilloscope presents low common-mode load impedance to the device.

Returning to Figure 1−1, Power Supply 1 is used to provide the required 3.3 V to the EVM. Power Supply 2 is used to offset the EVM ground relative to the DUT ground. The EVM ground is connected to the oscilloscope ground through the returns on SMA connectors J1 and J2. With power applied, the common-mode voltage seen by the SN65LVDS16 or SN65LVDS18 is approximately equal to the reference voltage being used inside the device preventing significant common-mode current to flow. Optimum device setup can be confirmed by adjusting the voltage on Power Supply 2 until its current is minimized. It is important to note that use of the dual supplies, and offsetting the EVM ground relative to the DUT ground are simply steps needed for test and evaluation of devices. Actual designs would include high-impedance receivers, which would not require the setup steps outlined above.

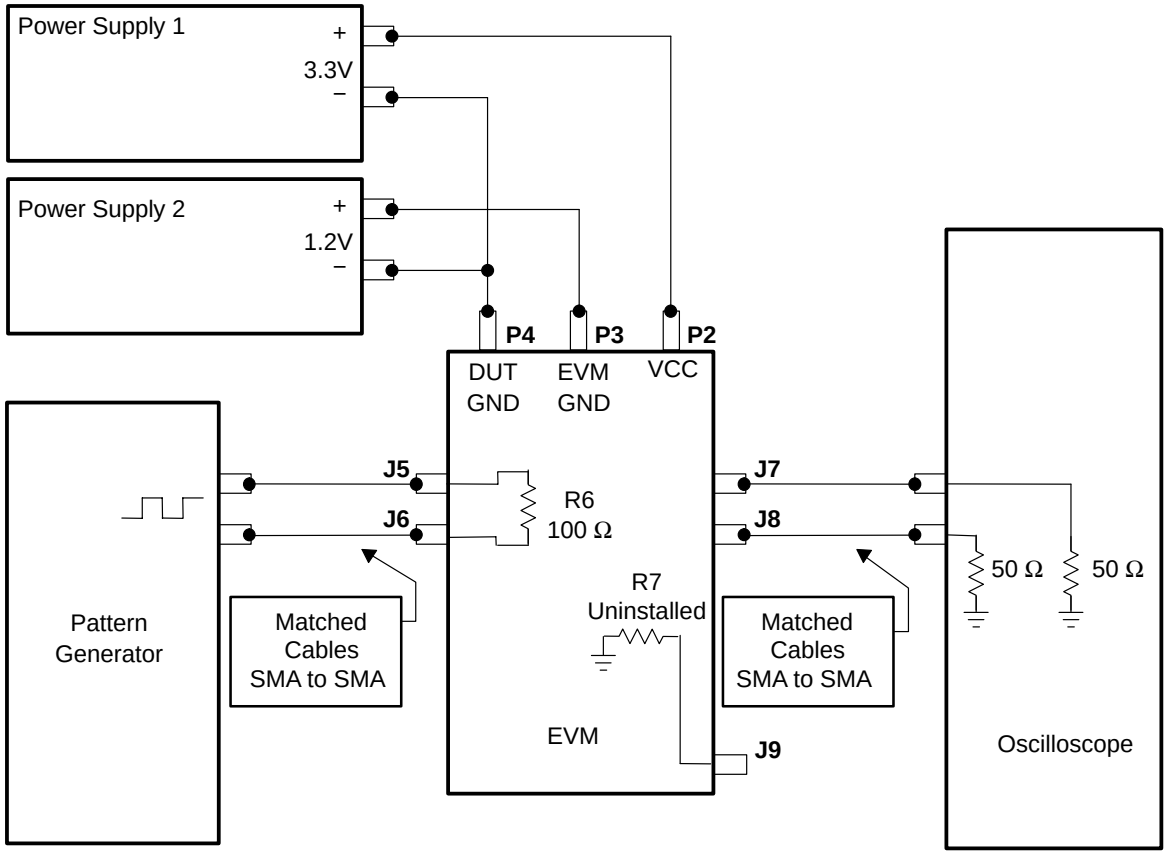
LVPECL drivers need a 50-Ω termination to V_{TT}. A modification of Figure 1−1 and the above instructions are used when evaluating a SN65LVP16 or SN65LVP18 with a direct connection to a 50-Ω oscilloscope. With Power Supply 1 in Figure 1−1 set to 3.3 V, Power Supply 2 should be set to 1.3 V (2 V below V_{CC}) to provide the correct termination voltage.

Note:

Power Supply 2 must be able to sink current.

1.4 Evaluation Module U2

Figure 1−2. Power Connections for Evaluation Module U2



Warning

Power jacks P2, P3, and P4 are not insulated on the backside of the EVM. Place the EVM on a nonconductive surface.

1.5 Applying an Input to EVM U2

Inputs should be applied to SMA connectors J5 and J6, while keeping R6 installed. The EVM comes with a 100-Ω termination resistor (R6) installed across the differential inputs for terminating the transmission line.

When using a general-purpose signal generator with 50-Ω output impedance, make sure that the signal levels are between 0 V to V_{CC} with respect to P4. V_{ID} cannot exceed 2 V. A signal generator such as the Advantest D3186 can simulate LVPECL, LVDS, or CML inputs.

LVPECL levels can be obtained with 100-Ω differential input termination by setting the input generator to a common-mode of 0.7 V.

1.6 Observing an EVM U2 Output

The outputs are available at J8 and J7 for direct connection to oscilloscope inputs. Matched length cables must be used when connecting the EVM to a scope to avoid inducing skew between the noninverting (+) and inverting (−) outputs.

The three power jacks (P2, P3, and P4) are used to provide power and a ground reference for the EVM. The power connections to the EVM determine the common-mode load to the device. When connecting the EVM outputs directly to oscilloscope inputs, setting of the oscilloscope common-mode offset voltage is required, as the oscilloscope presents low common-mode load impedance to the device.

Returning to Figure 1−2, Power Supply 1 is used to provide the required 3.3 V to the EVM. Power Supply 2 is used to offset the EVM ground relative to the DUT ground. The EVM ground is connected to the oscilloscope ground through the returns on SMA connectors J8 and J7. With power applied, the common-mode voltage seen by the SN65LVDS20, SN65LVDS17, or SN65LVDS19 is approximately equal to the reference voltage being used inside the device preventing significant common-mode current to flow. Optimum device setup can be confirmed by adjusting the voltage on Power Supply 2 until its current is minimized. It is important to note that use of the dual supplies, and offsetting the EVM ground relative to the DUT ground are simply steps needed for test and evaluation of devices. Actual designs would include high-impedance receivers, which would not require the setup steps outlined above.

LVPECL drivers need a 50-Ω termination to V_{TT}. A modification of Figure 1−1 and the above instructions are used when evaluating a SN65LVP20, SN65LVP17, or SN65LVP19 with a direct connection to a 50-Ω oscilloscope. With Power Supply 1 in Figure 1−2 set to 3.3 V, Power Supply 2 should be set to 1.3 V (2 V below V_{CC}) to provide the correct termination voltage.

Note:

Power Supply 2 must be able to sink current.

Chapter 2

Bill of Materials and Schematic

This chapter contains the bill of materials and schematic.

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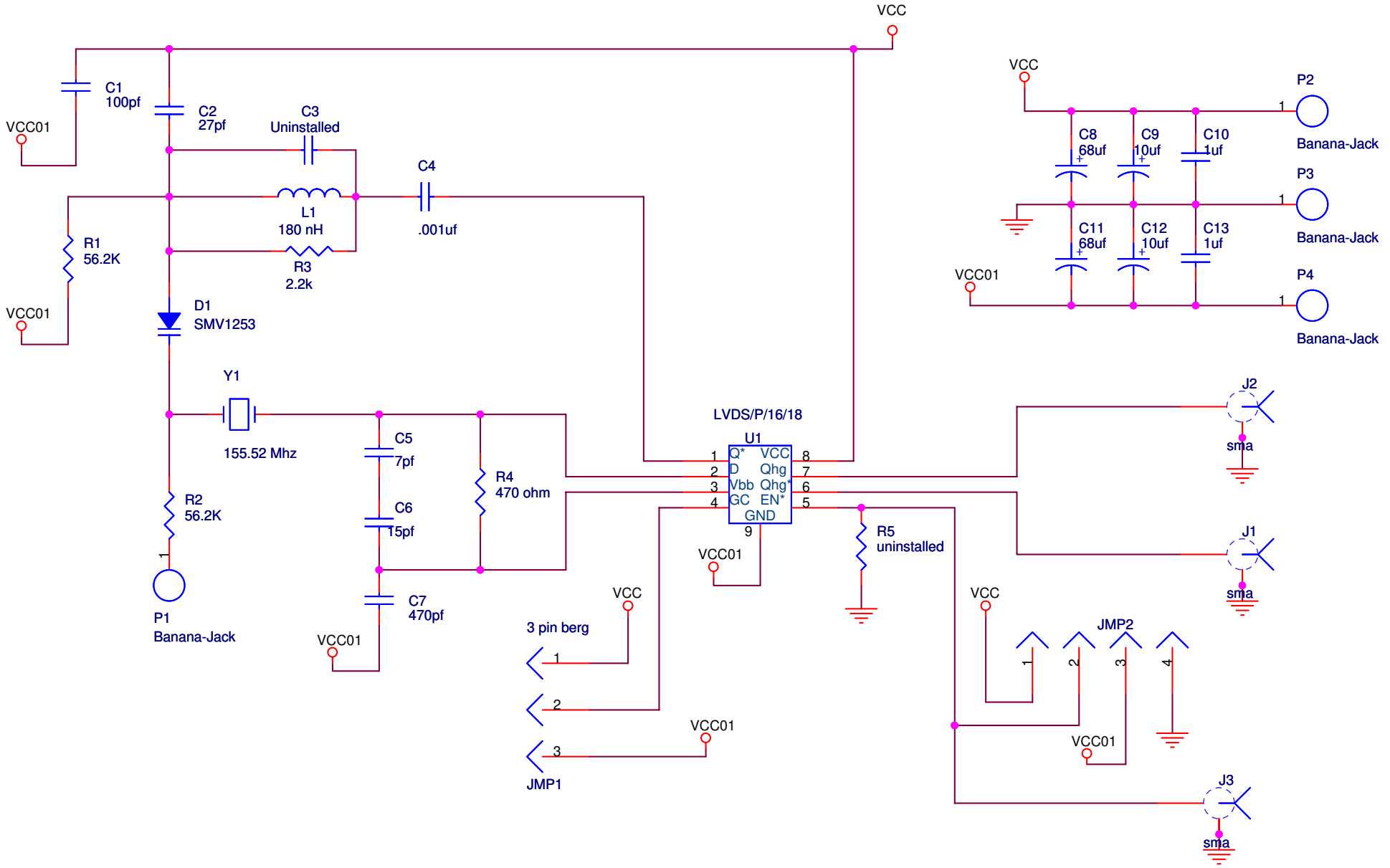
2.2 Schematic 2-3

2.1 Bill of Materials

Item	Quantity −1	Quantity −2	Reference	Value	Part No.
1	1	−	C1	0.01 μF	ECJ−1VB1H103K
2	1	−	C2	27 pF	ECJ−OEC1H270J
3	1	−	C3	Uninstalled	Uninstalled
4	1	−	C4	0.001 μF	ECJ−OEB1H102K
5	1	−	C5	7 pF	ECJ−OEC1H070D
6	1	−	C6	15 pF	ECJ−OEC1H150J
7	1	−	C7	470 pF	ECJ−OEB1H471K
8	2	2	C8, C11	68 μF	592D686X0010R2T
9	2	2	C9, C12	10 μF	293D106X0035D2W
10	2	2	C10, C13	1 μF	12063G105ZATRA
11	−	1	C14	0.01 μF	ECJ−OEB1E103K
12	1	−	D1	SMV1253	SMV1253−079 Skyworks Solutions Inc.
13	1	1	JMP1, JMP3		3 Pin berg (Make from AMP 4−103239−0)
14	1	1	JMP2, JMP4		4 Pin berg (Make from AMP 4−103239−0)
15	3	5	J1, J2, J3, J4, J5, J6, J7, J8, J9	SMA	142−0701−801
16	1	−	L1	180 nH	ELJ−RER18JF3
17	4	4	P1, P2, P3, P4	Banana−jack	3267
18	2	−	R1, R2	56.2 kΩ	ERJ−2RKF5622X
19	1	−	R3	2.21 kΩ	ERJ−2RKF2211X
20	1	−	R4	470 Ω	ERJ−2RKF4700X
21	1	1	R5, R7	49.9 Ω	ERJ−3EKF49R9V (Uninstalled)
22	−	1	R6	100 Ω	ERJ−2RKF1000X
23	1	−	U1	LVP/16/18	SN65LVDS/P16/18
24	−	1	U2	LVDS/P	SN65LVDS/P/17/19/20
25	1	−	Y1	155.52 MHz	CWI45−B Conner−Winfield Corp.
26	4	4	NA	Rubber feet	SJ5303−7−ND
27	1	1	NA	PWB	6464145

2.2 Schematic

The schematic for this device is attached.



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Size A	Document Number 6464145	Rev A
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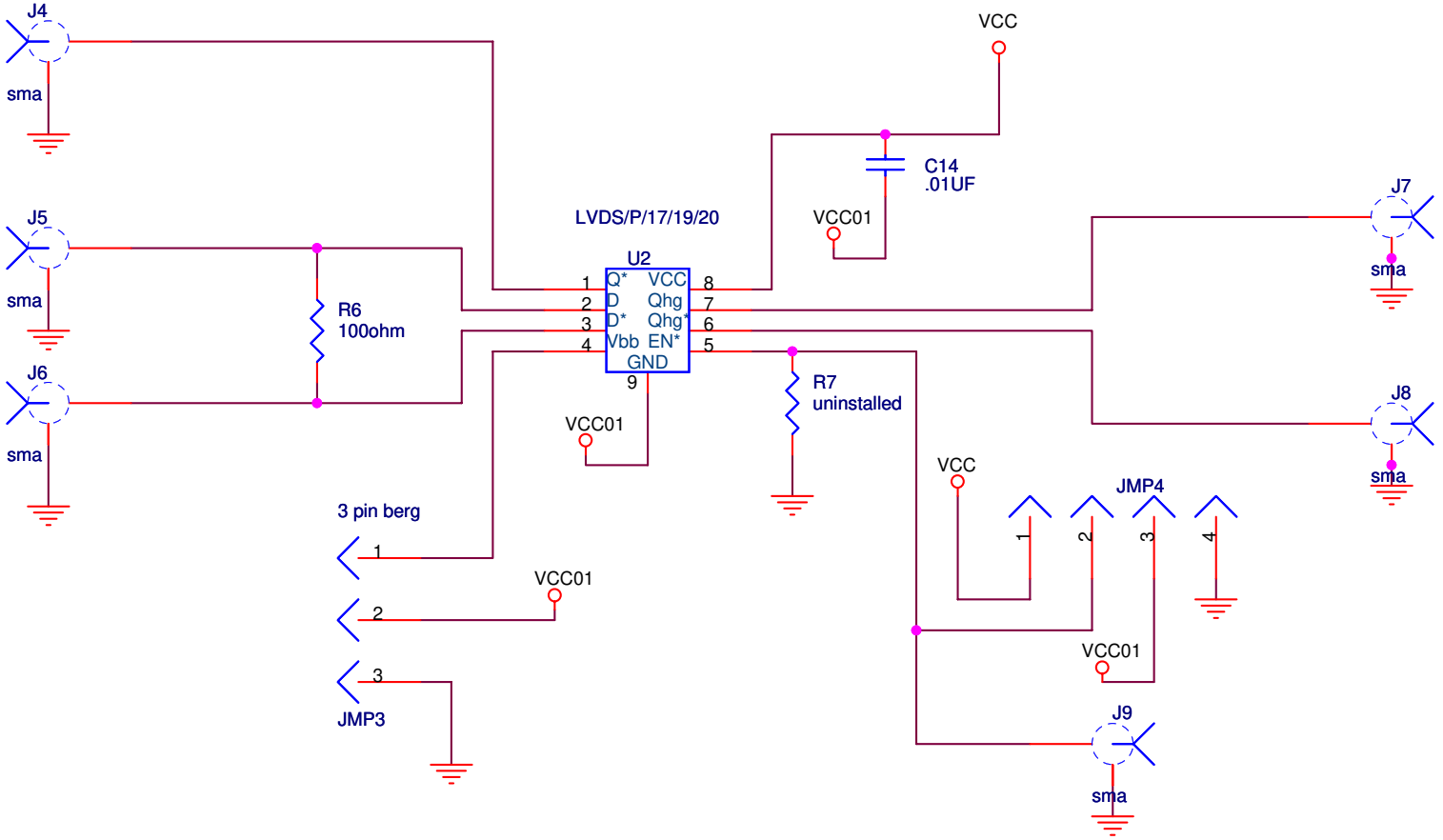

Title	LVDS/P/16/17/18/19/20 EVM	
Size A	Document Number 6464145	Rev A
Date: Friday, August 27, 2004	Sheet 2 of 2	