ZL50211

256 Channel Voice Echo Canceller

Data Sheet

January 2006

Features

- ZL50211 has eight Echo Voice Processors in a single BGA package. This single device provides 256 channels of 64 msec echo cancellation or 128 channels at 128 msec echo cancellation
- Each Echo Voice Processor has the capability of cancelling echo over 32 channels
- Each Echo Voice Processor (EVP) shares the address bus and data bus with each other
- Fully compliant to ITU-T G.165, G.168 (2000) and (2002) specifications
- Passed all AT&T voice quality tests for carrier grade echo canceller
- The ZL50211 provides more than 58% board space savings when compared with the eight Echo Voice Processors packaged devices
- Each EVP has a Patented Advanced Non-Linear Processor with high quality subjective performance
- Each EVP has protection against narrow band signal divergence and instability in high echo environments

Ordering Information

ZL50211GBC	535 Ball BGA	Trays
ZL50211GBG2	535 Ball BGA**	Trays

**Pb Free Tin/Silver/Copper

-40°C to +85°C

- Each EVP can be programmed independently in any mode e.g., Back-to-Back or Extended Delay to provide capability of cancelling different echo tails
- Each EVP has 0 to -12 dB level adjusters at all signal ports (Rin, Sin, Sout and Rout)
- Each EVP has the same JTAG identification code

Applications

- Voice over IP network gateways
- Voice over ATM, Frame Relay
- T1/E1/J1 multichannel echo cancellation
- Wireless base stations
- Echo Canceller pools
- DCME, satellite and multiplexer system

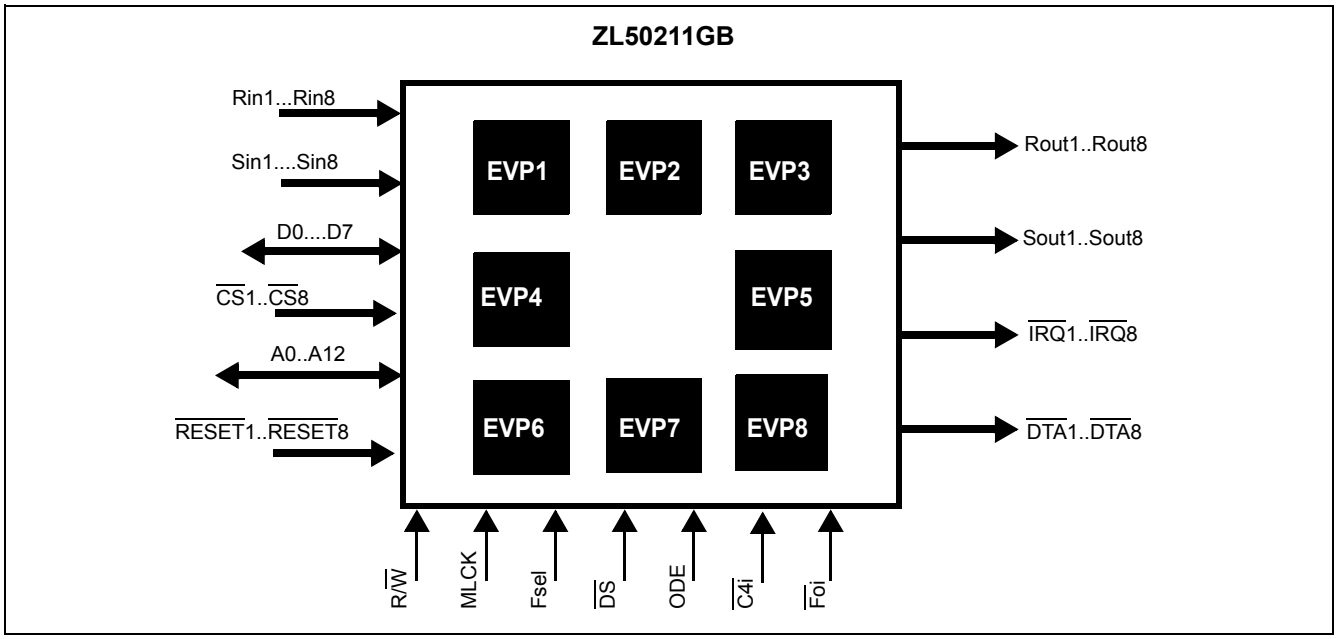


Figure 1 - ZL50211 Device Overview

Description

The ZL50211 Voice Echo Canceller implements a cost effective solution for telephony voice-band echo cancellation conforming to ITU-T G.168 requirements. The ZL50211 architecture contains 128 groups of two echo cancellers (ECA and ECB) which can be configured to provide two channels of 64 milliseconds or one channel of 128 milliseconds echo cancellation. This provides 256 channels of 64 milliseconds to 128 channels of 128 milliseconds echo cancellation or any combination of the two configurations. The ZL50211 supports ITU-T G.165 and G.164 tone disable requirements.

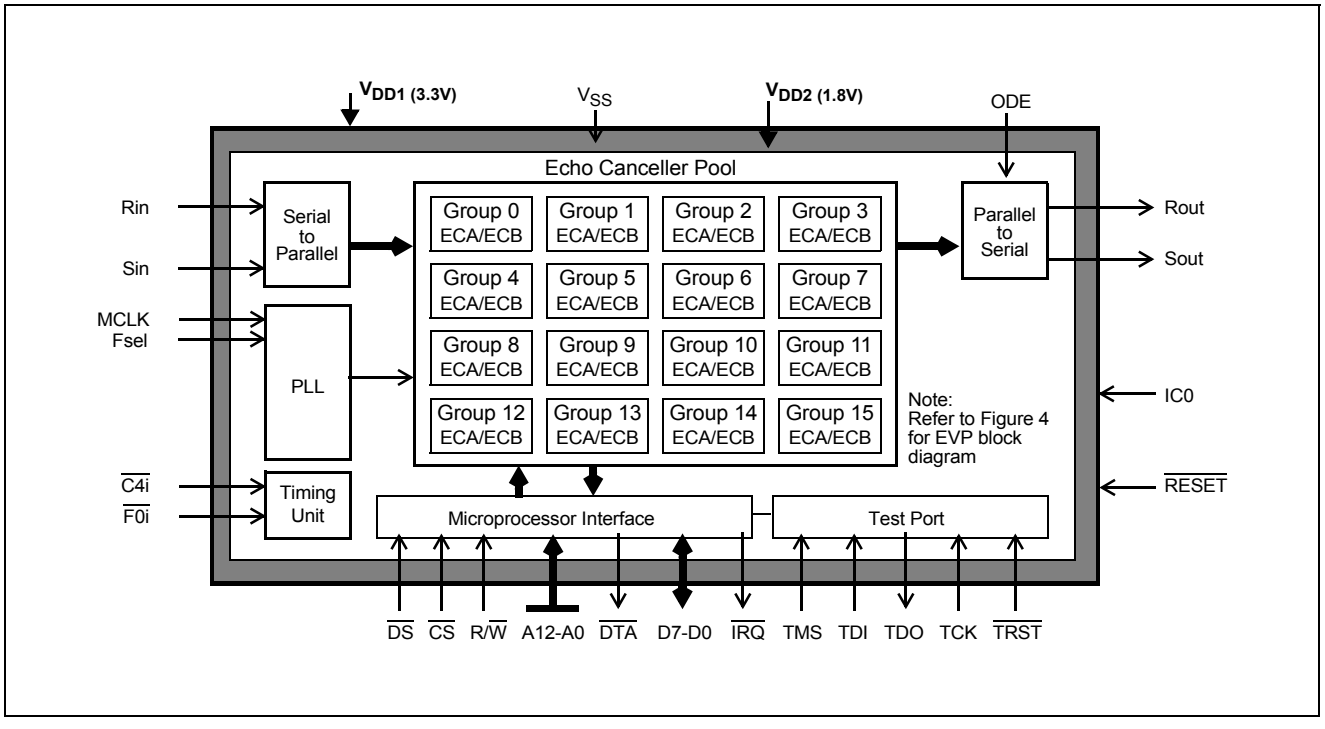


Figure 2 - Single Echo Voice Processor (EVP) Overview

Features of Echo Voice Processor (EVP)

- Each EVP can cancel echo tails of 64 ms (32 channels) to 128 ms (16 channels) with the ability to mix channels at 128 ms or 64 ms in any combination
- Independent Power Down mode for each group of 2 channels for power management
- Fully compliant to ITU-T G.165, G.168 (2000) and (2002) specifications
- Passed all AT&T voice quality tests for carrier grade echo canceller
- Compatible to ST-BUS and GCI interface at 2 Mb/s serial PCM
- PCM coding, μ/A-Law ITU-T G.711 or sign magnitude
- Per channel Fax/Modem G.164 2100 Hz or G.165 2100 Hz phase reversal Tone Disable
- Per channel echo canceller parameters control
- Transparent data transfer and mute
- Fast reconvergence on echo path changes
- Fully programmable convergence speeds
- Patented Advanced Non-Linear Processor with high quality subjective performance
- Protection against narrow band signal divergence and instability in high echo environments
- 0 dB to -12 dB level adjusters (3 dB steps) at all signal ports
- Offset nulling of all PCM channels
- 10 MHz or 20 MHz master clock operation
- 3.3 V pads and 1.8 V Logic core operation with 5-Volt tolerant inputs
- IEEE-1149.1 (JTAG) Test Access Port

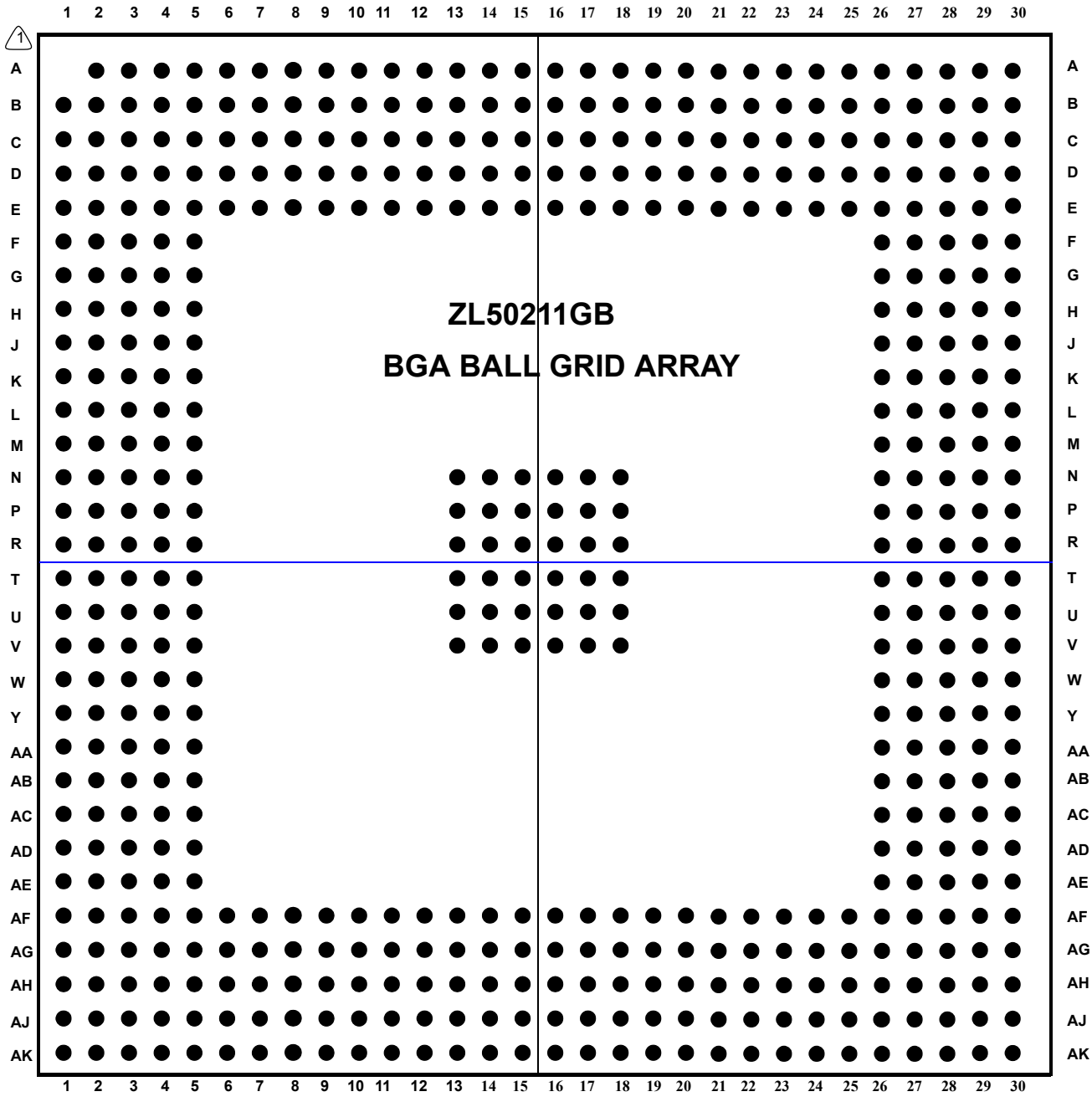


Figure 3 - 535 Ball BGA Ball Grid Array

Pin Description

Signal Name	Signal Type	BGA Ball #	Signal Description
V_{DD1} = 3.3V (V_{DD_IO})	Power	AC5,AC26,AC27,AD26,AD5,AE5,AF12,AF13,AF14,AF17,AF18,AF19,AF24,AF6,AF7,AF8,AG24,AH24,E13,E14,E17,E18,E19,E23,E24,E25,E6,E7,E8,F5,G26,G27,G5,H26,H5,M26,M5,N26,N5,P26,P27, P4,P5,U26,U27,U4,U5,V26,V5,W26,W5	**Positive Power Supply.** Nominally 3.3 volt (I/O voltage).
V_{DD2} = 1.8V (V_{DD_Core})	Power	AA26,AA28,AA3,AA5,AB26,AB28,AB3,AB5,AF11,AF20,AG10,AG21,AG22,AH10,AH11,AH22,AJ15,AJ16,AJ9,AK9,C10,C11,C22,C23,C9,D10,D23,D9,E11,E20,E21,E22,J26,J27,J4,J5,K26,K27,K3,K5,L26,L27,L3,L5,Y26, Y27,Y3,Y5	**Positive Power Supply.** Nominally 1.8 volt (Core voltage).
VSS	Power	A29,A30,AF5,AG15,AG16,AG26,AG27,AG4,AH15, AH16,AH21,AH28,AH3,AJ2,AJ21,AJ29,AK1,AK30,B1,B15,B16,B2,B29,C15,C16,C28,C3,D15,D16,D27,D4,E26,E5,N13,N14,N15,N16,N17,N18,P13,P14,P15,P16,P17,P18,R13,R14,R15,R16,R17,R18,R2,R27,R28,R29,R3,R4,T13,T14,T15,T16,T17,T18,T2,T27,T28,T29,T3,T4,U13,U14,U15,U16,U17,U18,V13,V14,V15,V16, V17,V18	**Ground**
TEST PINS			
TE1, TE2, TE3, TE4, TE5, TE6, TE7, TE8	Test Mode Pins	M4,AK26,M3,AJ4,AK4,AK25,K30,N28	**Internal Connection.** Connected to VSS for normal operation.
OUTPUT TEST PINS	Test pins	D8,P28,C12,AK10,AH12,AD29,H28,J29,AC28,D12,P29,E9,AJ11,AK11,AD30,G28,H29,AB27,A3,P2,A2,Y1,AA1,AJ17,C20,B21,AK17,B3,P1,D3,AA2,AB1,AK18,B22,D21,AJ18,C2,R1,E3,AB2,AB4,AH18,D19,A22,AK19,D2,T1,E4,AC1,AC2,AG18,A21,B20,AJ19,C1,U1,F4,AC4,AD1,AK20,C19,A20,AH19,F3,U2,E2,AC3,AD2,AK21,B19,A19,AG19,E10,P30,B12,AJ12,AG13,AC29,J30,G29,AC30,A11,N30,D11,AH13,AK12,AB29,H30,G30,AB30,A10,N27,B11,AJ13,AG14,AA27,F29,F30,AA29,A9,A14,B10,AG11,AG12,Y28,E29,E28,AA30,A8,A13,B9,AJ10,AF10,Y29,D29,E30,Y30,C8,B14,B8,AG9,AH9,W28,D26,D28,W29,C4,E12,C5,AA4,Y4,R30,A23,B23,T30,B4,P3,A4,Y2,W1,AG17,D20,C21,AH17	**No connection.** These pins must be left open for normal operation.

Pin Description (continued)

Signal Name	Signal Type	BGA Ball #	Signal Description
INPUT TEST PINS	SC_EN, SC_FCLK, SC_IN, SC_M_MCLK, SC_RESET, SC_SET, SC_T_MCLK,	A27,D5,A25,A26,A24,B24,A28	**Internal Connection.** Connected to VSS for normal operation.
THalt and TStep	Halt Step	C14, D14	**Internal Connection.** Connected to VSS for normal operation.

Signal Name	Signal Type	BGA Ball #	Signal Description
User Signal Pins			
D0, D1, D2, D3, D4, D5, D6, D7	User Signals	AK7,AJ8,AK8, AJ27,AK29,AJ28, AH27, AJ30	**Data Bus D0 to D7 (Bidirectional).** These pins form the 8-bit bidirectional data bus of the microprocessor port. They are connected to all the EVP's.
A0,A1,A2,A3,A4,A5, A6,A7, A8, A9, A10,A11,A12	User Signals	AG28,AH29, AH30,AG29,AF28, AG30,AE28,AF29, AE29,AF30,AD27, AE30,AD28	**Address A0 to A12 (Input).** These inputs provide the A12 - A0 address lines to the internal registers. They are connected to all the EVP's.
$\overline{CS}$1,$\overline{CS}$2,$\overline{CS}$3, $\overline{CS}$4, $\overline{CS}$5, $\overline{CS}$6, $\overline{CS}$7, $\overline{CS}$8	User Signals	R5,L28,T5,AF15, AF16,E16,T26, R26	**Chip Select (Input).** These active low inputs are used enable the microprocessor interface of each EVP.
$\overline{RESET}$1 $\overline{RESET}$2, $\overline{RESET}$3, $\overline{RESET}$4, $\overline{RESET}$5, $\overline{RESET}$6, $\overline{RESET}$7, $\overline{RESET}$8	User Signals	M2,AH23,M1,AH5, AJ5,AJ23,N29,M30	**EVP Reset (Schmitt Trigger Input).** An active low resets the device and puts the Voice Processor into a low-power stand-by mode. When the $\overline{RESET}$ pin is returned to logic high and a clock is applied to the MCLK pin, the EVP will automatically execute initialization routines, which preset all the Control and Status Registers to their default power-up values. Each reset pin controls a single processor. A user can connect all of them together if required.
Rin1,Rin2,Rin3, Rin4,Rin5,Rin6, Rin7,Rin8	User Signals	C6,V27,B5,AG5, AH6,U28,B27,B28	**Receive PCM Signal Inputs (Input).** Port 1 TDM data input streams. Each Rin pin receives serial TDM data streams at 2.048 Mb/s with 32 channels per stream.
Sin1,Sin2,Sin3,Sin4, Sin5,Sin6,Sin7,Sin8	User Signals	C7,U30,B6,AG7, AG6,U29,B30,C27	**Send PCM Signal Inputs (Input).** Port 2 TDM data input streams. Each Sin pin receives serial TDM data streams at 2.048 Mb/s with 32 channels per stream.

Signal Name	Signal Type	BGA Ball #	Signal Description
Rout1,Rout2,Rout3, Rout4,Rout5,Rout6, Rout7,Rout8,	User Signals	A5,V30,A6,AH7, AG8,V28,C26,C30	**Receive PCM Signal Outputs (Output).** Port 2 TDM data output streams. Each Rout pin outputs serial TDM data streams at 2.048 Mb/s with 32 channels per stream.
Sout1,Sout2,Sout3, Sout4,Sout5,Sout6, Sout7,Sout8	User Signals	B7,W27,A7,AH8, AF9,W30,C29,D30	**Send PCM Signal Outputs (Output).** Port 1 TDM data output streams. Each Sout pin outputs serial TDM data streams at 2.048 Mb/s with 32 channels per stream.
$\overline{\text{DS}}$	User Signal	K29	**Data Strobe (Input).** This active low input works in conjunction with $\overline{\text{CS}}$ to enable the read and write operations. This signal is connected to all processors.
R/$\overline{\text{W}}$	User Signal	M29	**Read/Write (Input).** This input controls the direction of the data bus lines (D7-D0) during a microprocessor access. This signal is connected to all processors.
$\overline{\text{DTA}}$1, $\overline{\text{DTA}}$2, $\overline{\text{DTA}}$3, $\overline{\text{DTA}}$4, $\overline{\text{DTA}}$5, $\overline{\text{DTA}}$6, DTA7, DTA8	User Signals	N2,AK28,N1,AK6, AJ7,AK27,M28, M27	**Data Transfer Acknowledgment (Open Drain Output).** These active low outputs indicate that a data bus transfer is completed. A pull-up resistor (1 K typical) is required at these outputs.
ODE	User Signal	V29	**Output Drive Enable (Input).** This input pin is logically AND'd with the ODE bit-6 of the Main Control Register. When both ODE bit and ODE input pin are high, the Rout and Sout ST-BUS outputs are enabled. When the ODE bit is low or the ODE input pin is low, the Rout and Sout ST-BUS outputs are high impedance. This signal is connected to all processors.
$\overline{\text{F0i}}$	User Signal	B26	**Frame Pulse (Input).** This input accepts and automatically identifies frame synchronization signals formatted according to ST-BUS or GCI interface specifications.This signal is connected to all processors.
$\overline{\text{C4i}}$	User Signal	B25	**Serial Clock (Input).** 4.096 MHz serial clock for shifting data in/out on the serial streams (Rin, Sin, Rout, Sout).This signal is connected to all processors.
Fsel	User Signal	A15	**Frequency select (Input).** This input selects the Master Clock frequency operation. When Fsel pin is low, nominal 20 MHz Master Clock input must be applied. When Fsel pin is high, nominal 10 MHz Master Clock input must be applied.This signal is connected to all processors.
MCLK	User Signal	A16	**Master Clock (Input).** Nominal 10 MHz or 20 MHz Master Clock input. May be connected to an asynchronous (relative to frame signal) clock source.This signal is connected to all processors.

Signal Name	Signal Type	BGA Ball #	Signal Description
$\overline{\text{IRQ}}$1, $\overline{\text{IRQ}}$2, $\overline{\text{IRQ}}$3, $\overline{\text{IRQ}}$4, $\overline{\text{IRQ}}$5, $\overline{\text{IRQ}}$6, $\overline{\text{IRQ}}$7, $\overline{\text{IRQ}}$8	User Signals	N4,AJ26,N3,AK5, AJ6,AG23,L30,L29	**Interrupt Request (Open Drain Output).** These outputs go low when an interrupt occurs in any channel. Each $\overline{\text{IRQ}}$ returns high when all the interrupts have been read from the Interrupt FIFO Register of respective EVP. A pull-up resistor (1 K typical) is required at these outputs.
Extra Device Pins	-	W3,E15,V4,AK16, AK15,AK14,D13, C13,V3,A12,B13, AK13,AH14,U3,V2, AJ14	**No connection.** The ball pins must be left open for normal operation.
JTAG SIGNAL PINS			
TMS	JTAG Signal	K2	**Test Mode Select (3.3 V Input).** JTAG signal that controls the state transitions of the TAP controller. This pin is pulled high by an internal pull-up when not driven. This signal is connected to all processors.
TCK	JTAG Signal	D6	**Test Clock (3.3 V Input).** Provides the clock to the JTAG test logic.This signal is connected to all processors.
$\overline{\text{TRST}}$	JTAG Signal	D7	**Test Reset (3.3 V Input).** Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin should be pulsed low on power-up or held low, to ensure that all the EVP's are in the normal functional mode. This pin is pulled by an internal pull-down when not driven. This signal is connected to all EVP's.
TDI1,TDI2,TDI3,TDI4, TDI5,TDI6,TDI7,TDI8	JTAG Signals	K1,AK23,L2,AK2, AJ3,AH20,F27,H27	**Test Serial Data In (3.3 V Input).** JTAG serial test instructions and data are shifted in on these pins. These pins are pulled high by an internal pull-up when not driven.
TDO1,TDO2,TDO3, TDO4,TDO5,TDO6 TDO7,TDO8	JTAG Signals	L1,AJ22,L4,AH4, AK3,AK24,J28,K28	**Test Serial Data Out (Output).** JTAG serial data is outputted on these pins on the falling edge of TCK. These pins are held in high impedance state when JTAG scan is not enabled.
PLL SIGNAL PINS			
$PLLV_{DD2}$ = 1.8V	PLL Power	H3,V1,H4,AE3, AG2,AE26,D22, C24, AE27	**PLL Power Supply.** Must be connected to $PLLV_{DD2}$ = 1.8V.
$PLLV_{SS1}$ $PLLV_{SS2}$	PLL Power	J3,W2,H2,AF4, AF3,AF27,D24, C25,AF26,H1,W4, J2, AH1,AG3,AF22, D25,E27,AF21	**PLL Ground.** Must be connected to VSS.

Signal Name	Signal Type	BGA Ball #	Signal Description
T1M1, T1M2, T1M3, T1M4, T1M5, T1M6, T1M7, T1M8	PLL Test Signals	D1,AH26,E1,AE1, AD4,AK22,D18, C18	**Internal Connection.** Connected to VSS for normal operation.
T2M1, T2M2, T2M3, T2M4, T2M5, T2M6, T2M7, T2M8	PLL Test Signals	F2,AG25,G3,AF1, AD3,AF25,B18,A18	**Internal Connection.** Connected to VSS for normal operation.
SG1, SG2, SG3, SG4, SG5, SG6, SG7, SG8	PLL Test Signals	G4,AJ25,F1,AE2, AG1, AH25,B17,C17	**Internal Connection.** Connected to VSS for normal operation.
DT1, DT2, DT3, DT4, DT5, DT6, DT7, DT8	PLL Test Signals	G2,AF23,G1,AF2, AE4,AJ24,D17, A17	**No connection.** These pins must be left open for normal operation.
AT1, AT2, AT3, AT4, AT5, AT6, AT7, AT8	PLL Test Signals	K4,AJ20,J1, AH2,AJ1,AG20, F28,F26	**No connection.** These pins must be left open for normal operation.

The following description applies to a single EVP (Echo Voice Processor). Note that the ZL50211 contains eight EVP's.

1.0 Single Echo Voice Processor (EVP) Description

Each single Echo Voice Processor (EVP) contains 32 echo cancellers divided into 16 groups. Each group has two echo cancellers, Echo Canceller A (ECA) and Echo Canceller B (ECB). Each group can be configured in Normal, Extended Delay or Back-to-Back configurations. In **Normal configuration**, a group of echo cancellers provides two channels of 64 ms echo cancellation, which run independently on different channels. In **Extended Delay** configuration, a group of echo cancellers achieves 128 ms of echo cancellation by cascading the two echo cancellers (A & B). In **Back-to-Back** configuration, the two echo cancellers from the same group are positioned to cancel echo coming from both directions in a single channel, providing full-duplex 64 ms echo cancellation.

Each Echo Voice Processor contains the following main elements (see Figure 4).

- Adaptive Filter for estimating the echo channel
- Subtractor for cancelling the echo
- Double-Talk detector for disabling the filter adaptation during periods of double-talk
- Path Change detector for fast reconvergence on major echo path changes
- Instability Detector to combat instability in very low ERL environments
- Patented Advanced Non-Linear Processor for suppression of residual echo, with comfort noise injection
- Disable Tone Detectors for detecting valid disable tones at send and receive path inputs
- Narrow-Band Detector for preventing Adaptive Filter divergence from narrow-band signals
- Offset Null filters for removing the DC component in PCM channels
- 0 to -12 dB level adjusters at all signal ports
- Parallel controller interface compatible with Motorola microcontrollers
- PCM encoder/decoder compatible with μ/A-Law ITU-T G.711 or Sign-Magnitude coding

- Each echo canceller in the EVP has four functional states: Mute, Bypass, Disable Adaptation and Enable Adaptation. These are explained in the section entitled Echo Canceller Functional States.

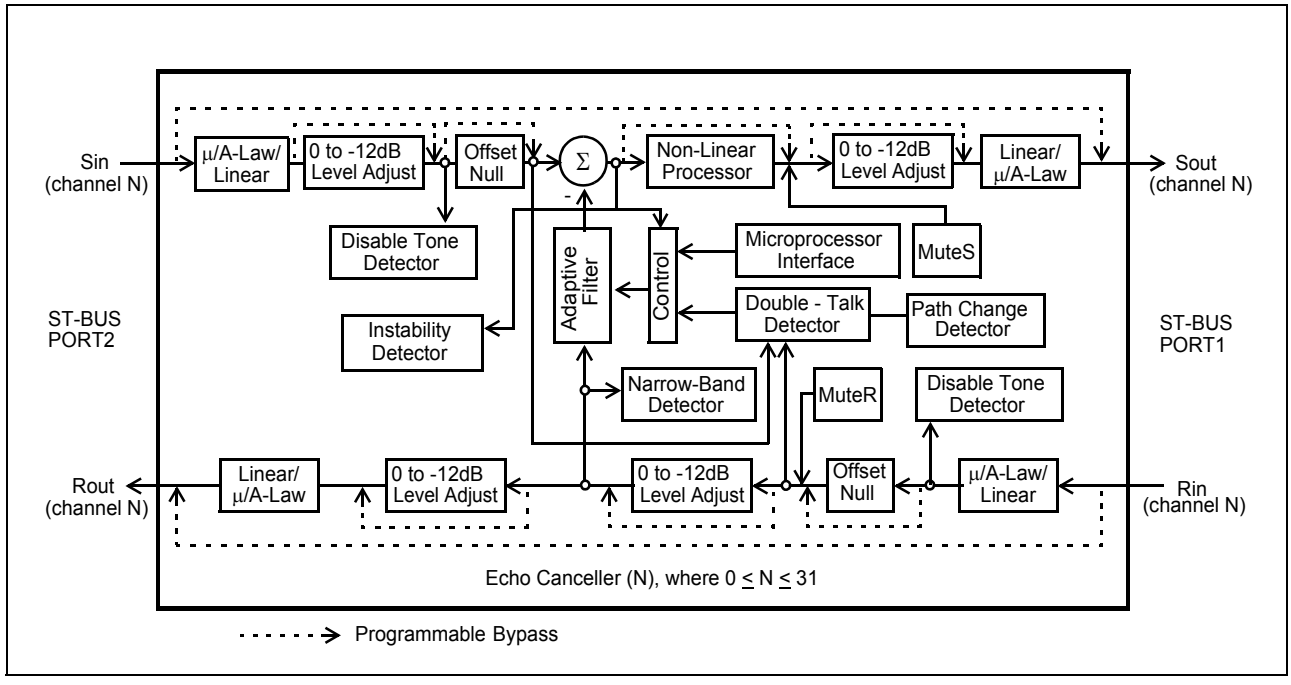


Figure 4 - Functional Block Diagram of an Echo Canceller

1.1 Adaptive Filter

The adaptive filter adapts to the echo path and generates an estimate of the echo signal. This echo estimate is then subtracted from Sin. For each group of echo cancellers, the Adaptive Filter is a 1024 tap FIR adaptive filter which is divided into two sections. Each section contains 512 taps providing 64 ms of echo estimation. In **Normal configuration**, the first section is dedicated to channel A and the second section to channel B. In **Extended Delay configuration**, both sections are cascaded to provide 128 ms of echo estimation in channel A. In **Back-to-Back configuration**, the first section is used in the receive direction and the second section is used in the transmit direction for the same channel.

1.2 Double-Talk Detector

Double-Talk is defined as those periods of time when signal energy is present in both directions simultaneously. When this happens, it is necessary to disable the filter adaptation to prevent divergence of the Adaptive Filter coefficients. Note that when double-talk is detected, the adaptation process is halted but the echo canceller continues to cancel echo using the previous converged echo profile. A double-talk condition exists whenever the relative signal levels of Rin (Lrin) and Sin (Lsin) meet the following condition:

$$Lsin > Lrin + 20log_{10}(DTDT)$$

where DTDT is the Double-Talk Detection Threshold. Lsin and Lrin are signal levels expressed in dBm0.

A different method is used when it is uncertain whether Sin consists of a low level double-talk signal or an echo return. During these periods, the adaptation process is slowed down but it is not halted. The slow convergence speed is set using the Slow sub-register in Control Register 4. During slow convergence, the adaptation speed is reduced by a factor of 2^{Slow} relative to normal convergence for non-zero values of Slow. If Slow equals zero, adaptation is halted completely.

In the G.168 standard, the echo return loss is expected to be at least 6 dB. This implies that the Double-Talk Detector Threshold (DTDT) should be set to 0.5 (-6 dB). However, in order to achieve additional guardband, the DTDT is set internally to 0.5625 (-5 dB).

In some applications the return loss can be higher or lower than 6 dB. The EVP allows the user to change the detection threshold to suit each application's need. This threshold can be set by writing the desired threshold value into the DTDT register.

The DTDT register is 16 bits wide. The register value in hexadecimal can be calculated with the following equation:

$$DTDT_{(hex)} = hex(DTDT_{(dec)} * 32768)$$

where $0 < DTDT_{(dec)} < 1$

Example:For DTDT = 0.5625 (-5 dB), the hexadecimal value becomes $hex(0.5625 * 32768) = 4800_{hex}$

1.3 Path Change Detector

Integrated into the EVP is a Path Change Detector. This permits fast reconvergence when a major change occurs in the echo channel. Subtle changes in the echo channel are also tracked automatically once convergence is achieved, but at a much slower speed.

The Path Change Detector is activated by setting the PathDet bit in Control Register 3 to "1". An optional path clearing feature can be enabled by setting the PathClr bit in Control Register 3 to "1". With path clearing turned on, the existing echo channel estimate will also be cleared (i.e., the adaptive filter will be filled with zeroes) upon detection of a major path change.

1.4 Non-Linear Processor (NLP)

After echo cancellation, there is always a small amount of residual echo which may still be audible. The EVP uses **Zarlink's patented Advanced NLP** to remove residual echo signals which have a level lower than the Adaptive Suppression Threshold (TSUP in G.168). This threshold depends upon the level of the Rin (Lrin) reference signal as well as the programmed value of the Non-Linear Processor Threshold register (NLPTHR). TSUP can be calculated by the following equation:

$$TSUP = Lrin + 20log_{10}(NLPTHR)$$

where NLPTHR is the Non-Linear Processor Threshold register value and Lrin is the relative power level expressed in dBm0. The NLPTHR register is 16 bits wide. The register value in hexadecimal can be calculated with the following equation:

$$NLPTHR_{(hex)} = hex(NLPTHR_{(dec)} * 32768)$$

where $0 < NLPTHR_{(dec)} < 1$

When the level of residual error signal falls below TSUP, the NLP is activated further attenuating the residual signal by an additional 30 dB. To prevent a perceived decrease in background noise due to the activation of the NLP, a spectrally-shaped comfort noise, equivalent in power level to the background noise, is injected. This keeps the perceived noise level constant. Consequently, the user does not hear the activation and de-activation of the NLP.

The NLP processor can be disabled by setting the NLPDis bit to "1" in Control Register 2.

The comfort noise injector can be disabled by setting the INJDis bit to "1" in Control Register 1. It should be noted that the NLPTHR is valid and the comfort noise injection is active only when the NLP is enabled.

The patented Advanced NLP provides a number of new and improved features over the original NLP found in previous generation devices. The differences between the Advanced NLP and the original NLP are summarized in Table 1.

Feature	Register or Bit(s)	Advanced NLP Default Value	Original NLP Default Value
NLP Selection	NLPSel (Control Register 3)	1	0 (feature not supported)
Reject uncancelled echo as noise	NLRun1 (Control Register 3)	1	0 (feature not supported)
Reject double-talk as noise	NLRun2 (Control Register 3)	1	0 (feature not supported)
Noise level estimator ramping scheme	InjCtrl (Control Register 3)	1	0 (feature not supported)
Noise level ramping rate	NLInc (Noise Control)	5(hex)	C(hex)
Noise level scaling	Noise Scaling	16(hex)	74(hex)

Table 1 - Comparison of NLP Types

The NLPSel bit in Control Register 3 selects which NLP is used. A “1” will select the Advanced NLP, “0” selects the original NLP.

The Advanced NLP uses a new noise ramping scheme to quickly and more accurately estimate the background noise level. The noise ramping method of the original NLP can also be used. The InjCtrl bit in Control Register 3 selects the ramping scheme.

The NLInc sub-register in Noise Control is used to set the ramping speed. When InjCtrl = 1 (such as with the Advanced NLP), a lower value will give faster ramping. When InjCtrl = 0 (such as with the original NLP), a higher value will give faster ramping. NLInc is a 4-bit value, so only values from 0 to F(hex) are valid.

The Noise Scaling register can be used to adjust the relative volume of the comfort noise. Lowering this value will scale the injected noise level down, conversely, raising the value will scale the comfort noise up. Due to differences in the noise estimator operation, the Advanced NLP requires a different scaling value than the original NLP.

Important Note: NLInc and the Noise Scaling register have been pre-programmed with G.168 compliant values. Changing these values may result in undesirable comfort noise performance!

The Advanced NLP also contains safeguards to prevent double-talk and uncancelled echo from being mistaken for background noise. These features were not present in the original NLP. They can be disabled by setting the NLRun1 and NLRun2 bits in Control Register 3 to “0”.

1.5 Disable Tone Detector

The G.165 recommendation defines the disable tone as having the following characteristics: 2100 Hz (±21 Hz) sine wave, a power level between -6 to -31 dBm0, and a phase reversal of 180 degrees (± 25 degrees) every 450 ms (±25 ms). If the disable tone is present for a minimum of one second with at least one phase reversal, the Tone Detector will trigger.

The G.164 recommendation defines the disable tone as a 2100 Hz (±21 Hz) sine wave with a power level between 0 to -31 dBm0. If the disable tone is present for a minimum of 400 ms, with or without phase reversal, the Tone Detector will trigger.

Each EVP has two Tone Detectors per channels (for a total of 64) in order to monitor the occurrence of a valid disable tone on both Rin and Sin. Upon detection of a disable tone, TD bit of the Status Register will indicate logic high and an interrupt is generated (i.e., $\overline{IRQ}$ pin low). Refer to Figure 5 and to the **Interrupts** section.

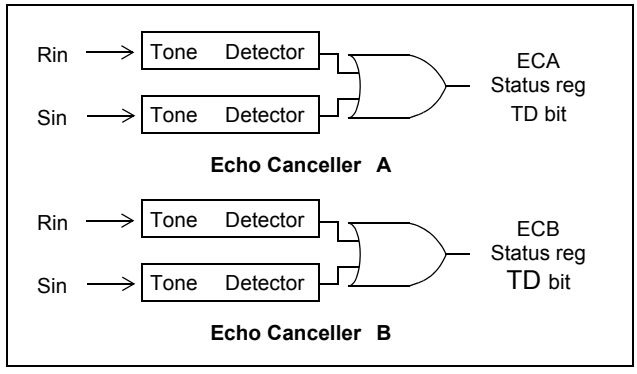


Figure 5 - Disable Tone Detection

Once a Tone Detector has been triggered, there is no longer a need for a valid disable tone (G.164 or G.165) to maintain Tone Detector status (i.e., TD bit high). The Tone Detector status will only release (i.e. TD bit low) if the signals Rin and Sin fall below -30 dBm0, in the frequency range of 390 Hz to 700 Hz, and below -34 dBm0, in the frequency range of 700 Hz to 3400 Hz, for at least 400 ms. Whenever a Tone Detector releases, an interrupt is generated (i.e., $\overline{IRQ}$ pin low).

The selection between G.165 and G.164 tone disable is controlled by the PHDis bit in Control Register 2 on a per channel basis. When the PHDis bit is set to “1”, G.164 tone disable requirements are selected.

In response to a valid disable tone, the echo canceller must be switched from the Enable Adaptation state to the Bypass state. This can be done in two ways, automatically or externally. In automatic mode, the Tone Detectors internally control the switching between Enable Adaptation and Bypass states. The automatic mode is activated by setting the AutoTD bit in Control Register 2 to high. In external mode, an external controller is needed to service the interrupts and poll the TD bits in the Status Registers. Following the detection of a disable tone (TD bit high) on a given channel, the external controller must switch the echo canceller from Enable Adaptation to Bypass state.

1.6 Instability Detector

In systems with very low echo channel return loss (ERL), there may be enough feedback in the loop to cause stability problems in the Adaptive Filter. This instability can result in variable pitched ringing or oscillation. Should this ringing occur, the Instability Detector will activate and suppress the oscillations.

The Instability Detector is activated by setting the RingClr bit in Control Register 3 to “1”.

1.7 Narrow Band Signal Detector (NBSD)

Single or dual frequency tones (i.e. DTMF tones) present in the receive input (Rin) of the echo canceller for a prolonged period of time may cause the Adaptive Filter to diverge. The Narrow Band Signal Detector (NBSD) is designed to prevent this by detecting single or dual tones of arbitrary frequency, phase, and amplitude. When narrow band signals are detected, adaptation is halted but the echo canceller continues to cancel echo.

The NBSD will be active regardless of the EVP functional state. However the NBSD can be disabled by setting the NBDis bit to “1” in Control Register 2.

1.8 Offset Null Filter

Adaptive filters in general do not operate properly when a DC offset is present at any input. To remove the DC component, each EVP incorporates Offset Null filters in both Rin and Sin inputs.

The offset null filters can be disabled by setting the HPFDis bit to “1” in Control Register 2.

1.9 Adjustable Level Pads

Each EVP provides adjustable level pads at Rin, Rout, Sin and Sout. This setup allows signal strength to be adjusted both inside and outside the echo path. Each signal level may be independently scaled with anywhere from 0 to -12 dB level, in 3 dB steps. Level values are set using the Gains register.

CAUTION: Gain adjustment can help interface the ZL50211 to a particular system in order to provide optimum echo cancellation, but it can also degrade performance if not done carefully. Excessive loss may cause low signal levels and slow convergence. Exercise great care when adjusting these values.

The -12 dB PAD bit in Control Register 1 is still supported as a legacy feature. Setting this bit will provide 12 dB of attenuation at Rin, and override the values in the Gains register.

1.10 ITU-T G.168 Compliance

The ZL50211 has been certified G.168 (1997), (2000) and (2002) compliant in all 64 ms cancellation modes (i.e. Normal and Back-to-Back configurations) by in-house testing with the DSPG ECT-1 echo canceller tester.

The ZL50211 has also been tested for G.168 compliance and all voice quality tests at AT&T Labs. The ZL50211 was classified as “carrier grade” echo canceller.

2.0 EVP Configuration

The EVP architecture contains 32 echo cancellers divided into 16 groups. Each group has two echo cancellers which can be individually controlled (Echo Canceller A (ECA) and Echo Canceller B (ECB). They can be set in three distinct configurations: **Normal, Back-to-Back,** and **Extended Delay**. See Figures 6, 7, and 8.

2.1 Normal Configuration

In Normal configuration, the two echo cancellers (Echo Canceller A and B) are positioned in parallel, as shown in Figure 6, providing 64 milliseconds of echo cancellation in two channels simultaneously.

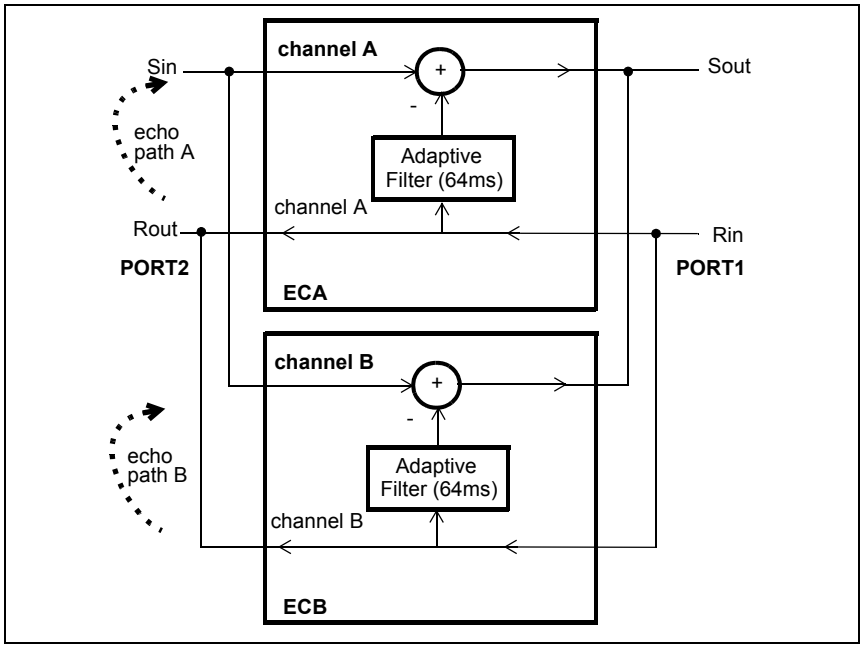


Figure 6 - Normal Device Configuration (64 ms)

2.2 Back-to-Back Configuration

In Back-to-Back configuration, the two echo cancellers from the same group are positioned to cancel echo coming from both directions in a single channel providing full-duplex 64ms echo cancellation. See Figure 7. This configuration uses only one timeslot on PORT1 and PORT2 and the second timeslot normally associated with ECB contains zero code. Back-to-Back configuration allows a no-glue interface for applications where bidirectional echo cancellation is required.

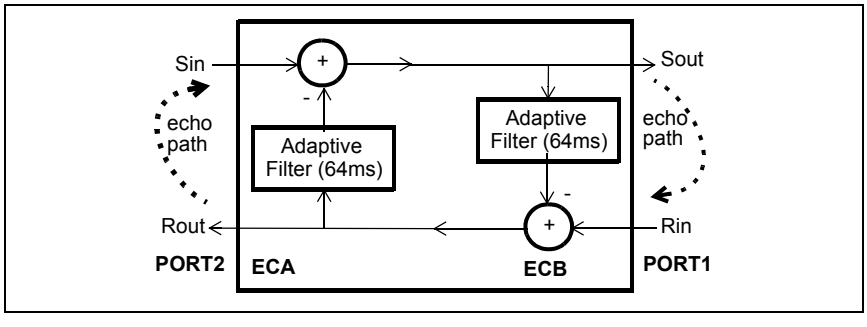


Figure 7 - Back-to-Back Device Configuration (64 ms)

Back-to-Back configuration is selected by writing a “1” into the BBM bit of Control Register 1 for **both** Echo Canceller A and Echo Canceller B for a given group of echo canceller. Table 4 shows the 16 groups of 2 cancellers that can be configured into Back-to-Back.

Examples of Back-to-Back configuration include positioning one group of echo cancellers between a codec and a transmission device or between two codecs for echo control on analog trunks.

2.3 Extended Delay Configuration

In this configuration, the two echo cancellers from the same group are internally cascaded into one 128 milliseconds echo canceller. See Figure 8. This configuration uses only one timeslot on PORT1 and PORT2 and the second timeslot normally associated with ECB contains quiet code.

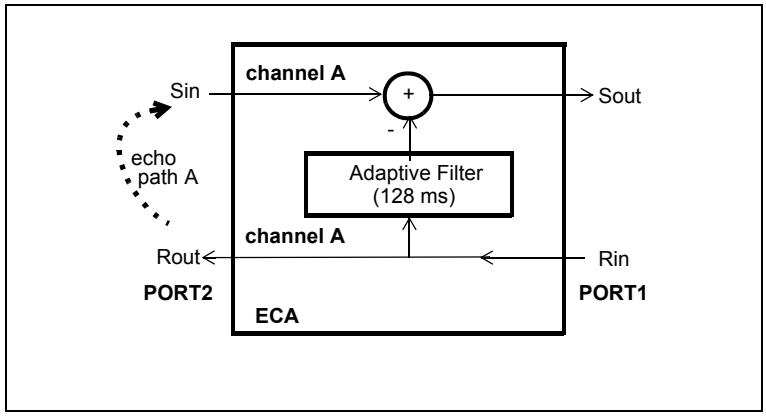


Figure 8 - Extended Delay Configuration (128 ms)

Extended Delay configuration is selected by writing a “1” into the ExtDl bit in Echo Canceller A, Control Register 1. For a given group, only Echo Canceller A, Control Register 1, has the ExtDl bit. For Echo Canceller B Control Register 1, Bit 0 must always be set to zero.

Table 4 shows the 16 groups of 2 cancellers that can each be configured into 64 ms or 128 ms echo tail capacity.

3.0 Echo Canceller Functional States

Each echo canceller has four functional states: **Mute, Bypass, Disable Adaptation** and **Enable Adaptation**.

3.1 Mute

In Normal and in Extended Delay configurations, writing a “1” into the MuteR bit replaces Rin with quiet code which is applied to both the Adaptive Filter and Rout. Writing a “1” into the MuteS bit replaces the Sout PCM data with quiet code.

	LINEAR 16 bits 2’s complement	SIGN/ MAGNITUDE μ-Law A-Law	CCITT (G.711)	
			μ-Law	A-Law
+Zero (quiet code)	0000_{hex}	80_{hex}	FF_{hex}	$D5_{hex}$

Table 2 - Quiet PCM Code Assignment

In Back-to-Back configuration, writing a “1” into the MuteR bit of Echo Canceller A, Control Register 2, causes quiet code to be transmitted on Rout. Writing a “1” into the MuteS bit of Echo Canceller A, Control Register 2, causes quiet code to be transmitted on Sout.

In Extended Delay and in Back-to-Back configurations, MuteR and MuteS bits of Echo Canceller B must always be “0”. Refer to Figure 4 and to Control Register 2 for bit description.

3.2 Bypass

The Bypass state directly transfers PCM codes from Rin to Rout and from Sin to Sout. **When Bypass state is selected, the Adaptive Filter coefficients are reset to zero.** Bypass state must be selected for at least one frame (125 μs) in order to properly clear the filter.

3.3 Disable Adaptation

When the Disable Adaptation state is selected, the Adaptive Filter coefficients are frozen at their current value. The adaptation process is halted, however, the echo canceller continues to cancel echo.

3.4 Enable Adaptation

In Enable Adaptation state, the Adaptive Filter coefficients are continually updated. This allows the echo canceller to model the echo return path characteristics in order to cancel echo. This is the normal operating state.

The echo canceller functions are selected in Control Register 1 and Control Register 2 through four control bits: MuteS, MuteR, Bypass and AdaptDis. Refer to the EVP Registers Description for details.

4.0 Echo Voice Processor (EVP) Throughput Delay

The throughput delay of the EVP varies according to the device configuration. For all device configurations, Rin to Rout has a delay of two frames and Sin to Sout has a delay of three frames. In Bypass state, the Rin to Rout and Sin to Sout paths have a delay of two frames.

5.0 Serial PCM I/O Channels

There are four TDM I/O streams, each with channels numbered from 0 to 31. One input stream is for Receive (Rin) channels, and the other input stream is for Send (Sin) channels. Likewise, two output streams is for Rout PCM channels, and Sout PCM channels. See Figure 9 for channel allocation.

5.1 Serial Data Interface Timing

The ZL50211 provides ST-BUS and GCI interface timing. The Serial Interface clock frequency, $\overline{C4i}$, is 4.096 MHz. The input and output data rate of the ST-BUS and GCI bus is 2.048 Mb/s.

The 8 KHz input frame pulse can be in either ST-BUS or GCI format. The EVP automatically detects the presence of an input frame pulse and identifies it as either ST-BUS or GCI. In ST-BUS format, every second falling edge of the $\overline{C4i}$ clock marks a bit boundary, and the data is clocked in on the rising edge of $\overline{C4i}$, three quarters of the way into the bit cell (See Figure 11). In GCI format, every second rising edge of the $\overline{C4i}$ clock marks the bit boundary, and data is clocked in on the second falling edge of $\overline{C4i}$, half the way into the bit cell (see Figure 12).

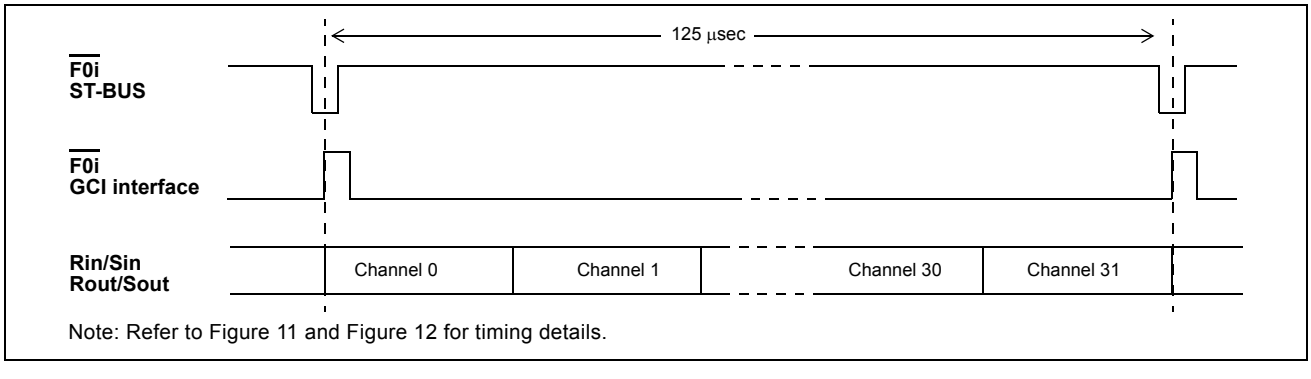


Figure 9 - ST-BUS and GCI Interface Channel Assignment for 2 Mb/s Data Streams

Base Address +		Echo Canceller A		Base Address +		Echo Canceller B
MS Byte	LS Byte			MS Byte	LS Byte	
-	00_{hex}	Control Reg 1		-	20_{hex}	Control Reg 1
-	01_{hex}	Control Reg 2		-	21_{hex}	Control Reg 2
-	02_{hex}	Status Reg		-	22_{hex}	Status Reg
-	03_{hex}	Reserved		-	23_{hex}	Reserved
-	04_{hex}	Flat Delay Reg		-	24_{hex}	Flat Delay Reg
-	05_{hex}	Reserved		-	25_{hex}	Reserved
-	06_{hex}	Decay Step Size Reg		-	26_{hex}	Decay Step Size Reg
-	07_{hex}	Decay Step Number		-	27_{hex}	Decay Step Number
-	08_{hex}	Control Reg 3		-	28_{hex}	Control Reg 3
-	09_{hex}	Control Reg 4		-	29_{hex}	Control Reg 4
-	$0A_{hex}$	Noise Scaling		-	$2A_{hex}$	Noise Scaling
-	$0B_{hex}$	Noise Control		-	$2B_{hex}$	Noise Control
$0D_{hex}$	$0C_{hex}$	Rin Peak Detect Reg		$2D_{hex}$	$2C_{hex}$	Rin Peak Detect Reg
$0F_{hex}$	$0E_{hex}$	Sin Peak Detect Reg		$2F_{hex}$	$2E_{hex}$	Sin Peak Detect Reg
11_{hex}	10_{hex}	Error Peak Detect Reg		31_{hex}	30_{hex}	Error Peak Detect Reg
13_{hex}	12_{hex}	Reserved		33_{hex}	32_{hex}	Reserved
15_{hex}	14_{hex}	DTDT Reg		35_{hex}	34_{hex}	DTDT Reg
17_{hex}	16_{hex}	Reserved		37_{hex}	36_{hex}	Reserved
19_{hex}	18_{hex}	NLPTHR		39_{hex}	38_{hex}	NLPTHR
$1B_{hex}$	$1A_{hex}$	Step Size, MU		$3B_{hex}$	$3A_{hex}$	Step Size, MU
$1D_{hex}$	$1C_{hex}$	Gains		$3D_{hex}$	$3C_{hex}$	Gains
$1F_{hex}$	$1E_{hex}$	Reserved		$3F_{hex}$	$3E_{hex}$	Reserved

Table 3 - Memory Mapping of Per Channel Control and Status Registers

6.0 Memory Mapped Control and Status Registers

Internal memory and registers are memory mapped into the address space of the HOST interface. The internal dual ported memory is mapped into segments on a “per channel” basis to monitor and control each individual echo canceller and associated PCM channels. For example, in **Normal configuration**, echo canceller #5 makes use of Echo Canceller B from group 2. It occupies the internal address space from $0A0_{hex}$ to $0BF_{hex}$ and interfaces to PCM channel #5 on all serial PCM I/O streams.

As illustrated in Table 3, the “per channel” registers provide independent control and status bits for each echo canceller. Figure 10 shows the memory map of the control/status register blocks for all echo cancellers of the EVP.

When **Extended Delay** or **Back-to-Back** configuration is selected, Control Register 1 of ECA and ECB and Control Register 2 of the selected group of echo cancellers require special care. Refer to the EVP Register description section.

Table 4 is a list of the channels used for the 16 groups of echo cancellers when they are configured as **Extended Delay** or **Back-to-Back.**

7.0 Normal Configuration

For a given group (group 0 to 15), 2 PCM I/O channels are used. For example, group 1 Echo Cancellers A and B, channels 2 and 3 are active.

Group	Channels	Group	Channels
0	0, 1	8	16, 17
1	2, 3	9	18, 19
2	4, 5	10	20, 21
3	6, 7	11	22, 23
4	8, 9	12	24, 25
5	10, 11	13	26, 27
6	12, 13	14	28, 29
7	14, 15	15	30, 31

Table 4 - Group and Channel Allocation

7.1 Extended Delay Configuration

For a given group (group 0 to 15), only one PCM I/O channel is active (Echo Canceller A) and the other channel carries quiet code. For example, group 2, Echo Canceller A (Channel 4) will be active and Echo Canceller B (Channel 5) will carry quiet code.

7.2 Back-to-Back Configuration

For a given group (group 0 to 15), only one PCM I/O channel is active (Echo Canceller A) and the other channel carries quiet code. For example, group 5, Echo Canceller A (Channel 10) will be active and Echo Canceller B (Channel 11) will carry quiet code.

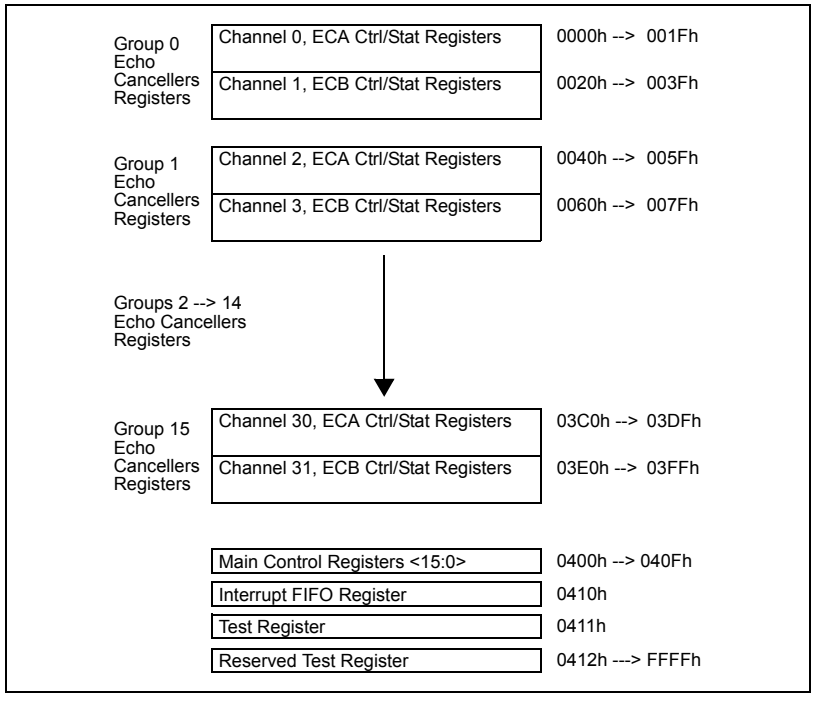


Figure 10 - Memory Mapping

7.3 Power Up Sequence

On power up, the $\overline{\text{RESET}}$ pin must be held low for 100 µs. Forcing the $\overline{\text{RESET}}$ pin low will put each EVP in power down state. In this state, all internal clocks are halted, D<7:0>, Sout, Rout, $\overline{\text{DTA}}$ and $\overline{\text{IRQ}}$ pins are tristated. The 16 Main Control Registers, the Interrupt FIFO Register and the Test Register are reset to zero.

When the $\overline{\text{RESET}}$ pin returns to logic high and a valid MCLK is applied, the user must wait 500 µs for the PLL to lock. $\overline{\text{C4i}}$ and $\overline{\text{F0i}}$ can be active during this period. Once the PLL has locked, the user must power up the 16 groups of echo cancellers individually, by writing a “1” into the PWUP bit in each group of echo canceller’s Main Control Register.

For each group of echo cancellers, when the PWUP bit toggles from zero to one, echo cancellers A and B execute their initialization routine. The initialization routine sets their registers, Base Address+00_{hex} to Base Address+$3F_{hex}$, to the default power-up value and clears the Adaptive Filter coefficients. Two frames are necessary for the initialization routine to execute properly.

Once the initialization routine is executed, the user can set the per channel Control Registers, Base Address+00_{hex} to Base Address+$3F_{hex}$, for the specific application.

7.4 Power Management

Each group of echo cancellers can be placed in Power Down mode by writing a “0” into the PWUP bit in their respective Main Control Register. When a given group is in Power Down mode, the corresponding PCM data are bypassed from Rin to Rout and from Sin to Sout with two frames delay. Refer to the Main Control Register section for description.

The typical power consumption can be calculated with the following equation:

$$P_C = 9 * Nb\_of\_groups + 3.6, \text{ in mW}$$

where $0 \leq Nb\_of\_groups \leq 16$.

7.5 Call Initialization

To ensure fast initial convergence on a new call, it is important to clear the Adaptive Filter. This is done by putting the echo canceller in bypass mode for at least one frame (125 μs) and then enabling adaptation.

Since the Narrow Band Detector is “ON” regardless of the functional state of the Echo Canceller it is recommended that the Echo Cancellers are reset before any call progress tones are applied.

7.6 Interrupts

The EVP provides an interrupt pin ($\overline{IRQ}$) to indicate to the HOST processor when a G.164 or G.165 Tone Disable is detected and released.

Although each EVP may be configured to react automatically to tone disable status on any input PCM voice channels, the user may want for the external HOST processor to respond to Tone Disable information in an appropriate application-specific manner.

Each echo canceller will generate an interrupt when a Tone Disable occurs and will generate another interrupt when a Tone Disable releases.

Upon receiving an $\overline{IRQ}$, the HOST CPU should read the Interrupt FIFO Register. This register is a FIFO memory containing the channel number of the echo canceller that has generated the interrupt.

All pending interrupts from any of the echo cancellers and their associated input channel number are stored in this FIFO memory. The $\overline{IRQ}$ always returns high after a read access to the Interrupt FIFO Register. The $\overline{IRQ}$ pin will toggle low for each pending interrupt.

After the HOST CPU has received the channel number of the interrupt source, the corresponding per channel Status Register can be read from internal memory to determine the cause of the interrupt (see Table 3 for address mapping of Status register). The TD bit indicates the presence of a Tone Disable.

The MIRQ bit 5 in the Main Control Register 0 masks interrupts from the EVP. To provide more flexibility, the MTDBI (bit-4) and MTDAI (bit-3) bits in the Main Control Register<15:0> allow Tone Disable to be masked or unmasked from generating an interrupt on a per channel basis. Refer to the Registers Description section.

8.0 JTAG Support

The EVP JTAG interface conforms to the Boundary-Scan standard IEEE1149.1. This standard specifies a design-for-testability technique called Boundary-Scan test (BST). The operation of the Boundary Scan circuitry is controlled by an Test Access Port (TAP) controller. JTAG inputs are **3.3 Volts** compliant only.

8.1 Test Access Port (TAP)

The TAP provides access to many test functions of the EVP. It consists of four input pins and one output pin. The following pins are found on the TAP.

- Test Clock Input (TCK)
  The TCK provides the clock for the test logic. The TCK does not interfere with any on-chip clock and thus remains independent. The TCK permits shifting of test data into or out of the Boundary-Scan register cells concurrent with the operation of the device and without interfering with the on-chip logic.
- Test Mode Select Input (TMS)
  The logic signals received at the TMS input are interpreted by the TAP Controller to control the test operations. The TMS signals are sampled at the rising edge of the TCK pulse. This pin is internally pulled to V_{DD1} when it is not driven from an external source.
- Test Data Input (TDI)
  Serial input data applied to this port is fed either into the instruction register or into a test data register, depending on the sequence previously applied to the TMS input. Both registers are described in a

subsequent section. The received input data is sampled at the rising edge of TCK pulses. This pin is internally pulled to V_{DD1} when it is not driven from an external source.

- Test Data Output (TDO)
  Depending on the sequence previously applied to the TMS input, the contents of either the instruction register or data register are serially shifted out towards the TDO. The data from the TDO is clocked on the falling edge of the TCK pulses. When no data is shifted through the Boundary Scan cells, the TDO driver is set to a high impedance state.
- Test Reset ($\overline{TRST}$)
  This pin is used to reset the JTAG scan structure. This pin is internally pulled to V_{SS}.

8.2 Instruction Register

In accordance with the IEEE 1149.1 standard, the EVP uses public instructions. The JTAG Interface contains a 3-bit instruction register. Instructions are serially loaded into the instruction register from the TDI when the TAP Controller is in its shifted-IR state. Subsequently, the instructions are decoded to achieve two basic functions: to select the test data register that will operate while the instruction is current, and to define the serial test data register path, which is used to shift data between TDI and TDO during data register scanning.

8.3 Test Data Registers

As specified in IEEE 1149.1, each of the Echo Voice Processor's JTAG Interface contains three test data registers:

- Boundary-Scan register
  The Boundary-Scan register consists of a series of Boundary-Scan cells arranged to form a scan path around the boundary of each EVP core logic.
- Bypass Register
  The Bypass register is a single stage shift register that provides a one-bit path from TDI to TDO.
- Device Identification register
  The Device Identification register provides access to the following encoded information:
  device version number, part number and manufacturer's name.

Absolute Maximum Ratings*

	Parameter	Symbol	Min.	Max.	Units
1	I/O Supply Voltage (V_{DD1})	V_{DD_IO}	-0.5	5.0	V
2	Core Supply Voltage (V_{DD2})	V_{DD_CORE}	-0.5	2.5	V
3	Input Voltage	V_{I3}	V_{SS} - 0.5	V_{DD1}+0.5	V
4	Input Voltage on any 5 V Tolerant I/O pins	V_{I5}	V_{SS} - 0.3	7.0	V
5	Continuous Current at digital outputs	I_o		20	mA
6	Package power dissipation	P_D		3.0	W
7	Storage temperature	T_S	-55	150	°C

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (Vss) unless otherwise stated

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units
1	Operating Temperature	T_{OP}	-40		+85	°C
2	I/O Supply Voltage (V_{DD_IO})	V_{DD1}	3.0	3.3	3.6	V
3	Core Supply Voltage (V_{DD_CORE})	V_{DD2}	1.6	1.8	2.0	V
4	Input High Voltage on 3.3 V tolerant I/O	V_{IH3}	$0.7V_{DD1}$		V_{DD1}	V
5	Input High Voltage on 5 V tolerant I/O pins	V_{IH5}	$0.7V_{DD1}$		5.5	V
6	Input Low Voltage	V_{IL}			$0.3V_{DD1}$	V

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing

DC Electrical Characteristics† - Voltages are with respect to ground (V_{ss}) unless otherwise stated.

		Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1		Static Supply Current	I_{CC}			250	µA	$\overline{RESET}$ = 0
		IDD_IO (V_{DD1} = 3.3 V) Single EV Processor	I_{DD_IO}		10		mA	32 channels of **single** EVP are active
		IDD_CORE (V_{DD2} = 1.8 V) Single EV Processor	I_{DD_CORE}		65		mA	32 channels of **single** EVP are active
2		Power Consumption	P_C		1.2		W	All EVP's i.e.,**256** channels are active
3	INPUTS	Input High Voltage	V_{IH}	$0.7V_{DD1}$			V	
4		Input Low Voltage	V_{IL}			$0.3V_{DD1}$	V	
5		Input Leakage Input Leakage on Pullup Input Leakage on Pulldown	I_{IH}/I_{IL} I_{LU} I_{LD}		10 -100 100		µA µA µA	$V_{IN}=V_{SS}$ to V_{DD1}or 5.5 V $V_{IN}=V_{SS}$ $V_{IN}=V_{DD1}$
6		Input Pin Capacitance	C_I			10	pF	
7	OUTPUTS	Output High Voltage	V_{OH}	$0.8V_{DD1}$			V	I_{OH} = 12 mA
8		Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
9		High Impedance Leakage	I_{OZ}			10	µA	$V_{IN}=V_{SS}$ to 5.5 V
10		Output Pin Capacitance	C_O			10	pF	

† Characteristics are over recommended operating conditions unless otherwise stated
‡ Typical figures are at 25°C, V_{DD1} =3.3 V and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - Timing Parameter Measurement Voltage Levels

- Voltages are with respect to ground (V_{ss}) unless otherwise stated.

	Characteristics	Sym.	Level	Units	Conditions
1	CMOS Threshold	V_{TT}	$0.5V_{DD1}$	V	
2	CMOS Rise/Fall Threshold Voltage High	V_{HM}	$0.7V_{DD1}$	V	
3	CMOS Rise/Fall Threshold Voltage Low	V_{LM}	$0.3V_{DD1}$	V	

† Characteristics are over recommended operating conditions unless otherwise stated

AC Electrical Characteristics† - Frame Pulse and $\overline{C4i}$

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	Frame pulse width (ST-BUS, GCI)	t_{FPW}	20		2* t_{CP}-20	ns	
2	Frame Pulse Setup time before $\overline{C4i}$ falling (ST-BUS or GCI)	t_{FPS}	10	122	150	ns	
3	Frame Pulse Hold Time from $\overline{C4i}$ falling (ST-BUS or GCI)	t_{FPH}	10	122	150	ns	
4	$\overline{C4i}$ Period	t_{CP}	190	244	300	ns	
5	$\overline{C4i}$ Pulse Width High	t_{CH}	85		150	ns	
6	$\overline{C4i}$ Pulse Width Low	t_{CL}	85		150	ns	
7	$\overline{C4i}$ Rise/Fall Time	t_r, t_f			10	ns	

† Characteristics are over recommended operating conditions unless otherwise stated
‡ Typical figures are at 25°C, V_{DD1} = 3.3 V and for design aid only: not guaranteed and not subject to production testing

AC Electrical Characteristics† - Serial Streams for ST-BUS and GCI Backplanes

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Rin/Sin Set-up Time	t_{SIS}	10			ns	
2	Rin/Sin Hold Time	t_{SIH}	10			ns	
3	Rout/Sout Delay - Active to Active	t_{SOD}			60	ns	
4	Output Data Enable (ODE) Delay	t_{ODE}			30	ns	

† Characteristics are over recommended operating conditions unless otherwise stated
‡ Typical figures are at 25°C, V_{DD1} = 3.3 V and for design aid only: not guaranteed and not subject to production testing

AC Electrical Characteristics† - Master Clock - Voltages are with respect to ground (V_{SS}). unless otherwise stated.

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	Master Clock Frequency, - Fsel = 0 - Fsel = 1	 f_{MCF0} f_{MCF1}	 19.0 9.5	 20.0 10.0	 21.0 10.5	 MHz MHz	
2	Master Clock Low	t_{MCL}	20			ns	
3	Master Clock High	t_{MCH}	20			ns	

† Characteristics are over recommended operating conditions unless otherwise stated
‡ Typical figures are at 25°C, V_{DD1} = 3.3 V and for design aid only: not guaranteed and not subject to production testing

AC Electrical Characteristics† - Motorola Non-Multiplexed Bus Mode

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	$\overline{CS}$ setup from DS falling	t_{CSS}	0			ns	
2	R/$\overline{W}$ setup from DS falling	t_{RWS}	0			ns	
3	Address setup from DS falling	t_{ADS}	0			ns	
4	$\overline{CS}$ hold after DS rising	t_{CSH}	0			ns	
5	R/$\overline{W}$ hold after DS rising	t_{RWH}	0			ns	
6	Address hold after DS rising	t_{ADH}	0			ns	
7	Data delay on read	t_{DDR}			79	ns	
8	Data hold on read	t_{DHR}	3		15	ns	
9	Data setup on write	t_{DSW}	0			ns	
10	Data hold on write	t_{DHW}	0			ns	
11	Acknowledgment delay	t_{AKD}			80	ns	
12	Acknowledgment hold time	t_{AKH}	0		8	ns	
13	$\overline{IRQ}$ delay	t_{IRD}	20		65	ns	

† Characteristics are over recommended operating conditions unless otherwise stated
‡ Typical figures are at 25°C, V_{DD1} = 3.3 V and for design aid only: not guaranteed and not subject to production testing

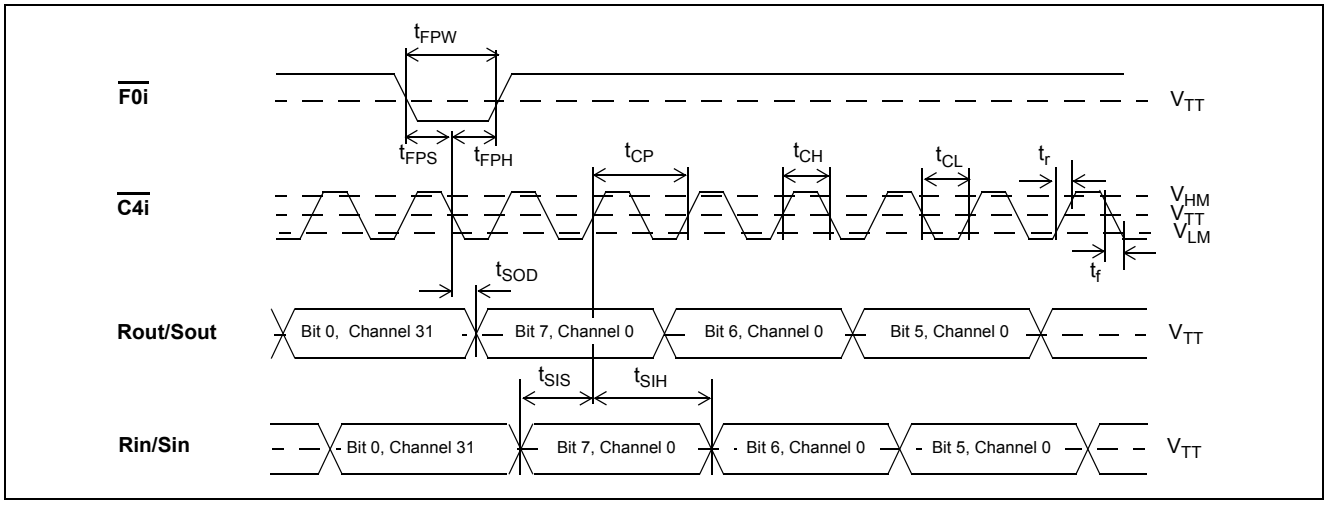


Figure 11 - ST-BUS Timing at 2.048 Mb/s

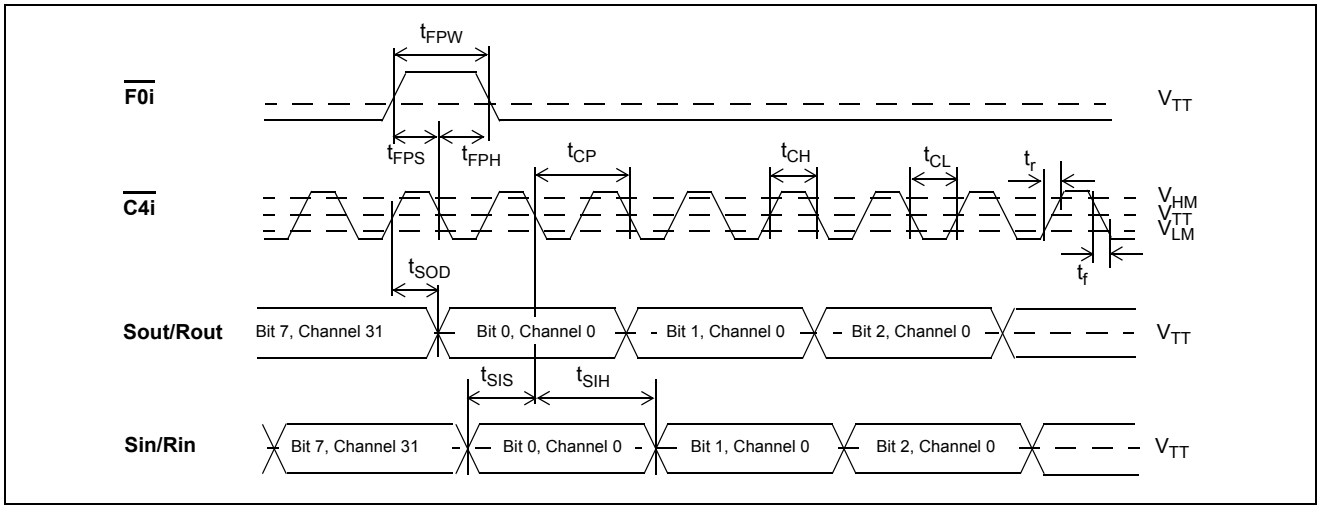


Figure 12 - GCI Interface Timing at 2.048 Mb/s

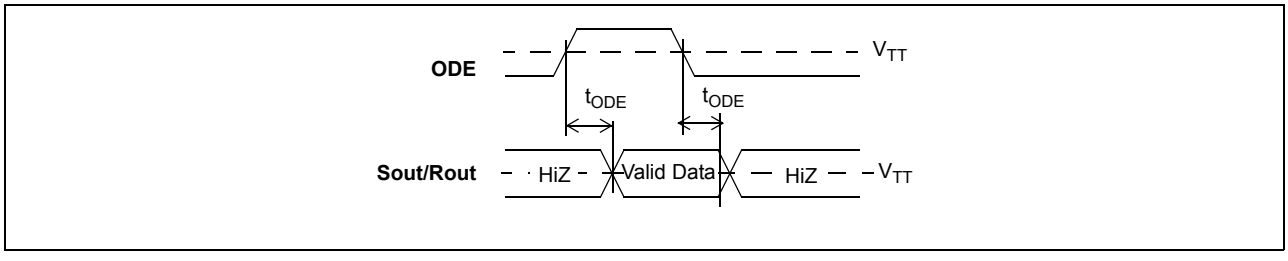


Figure 13 - Output Driver Enable (ODE)

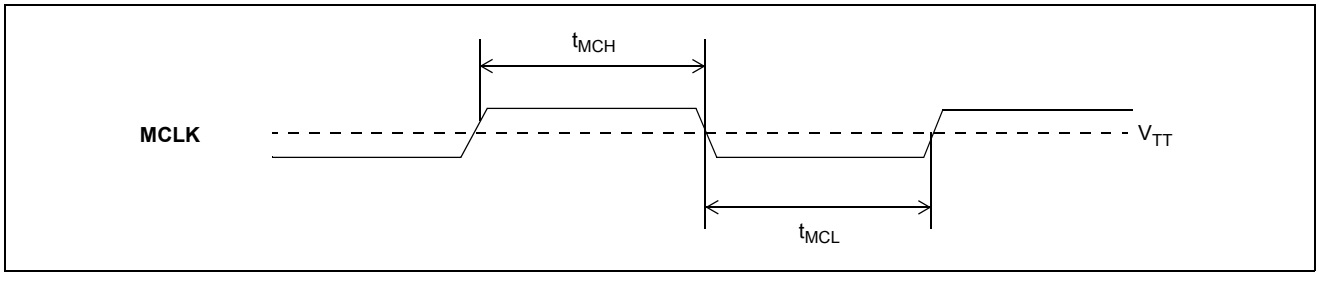


Figure 14 - Master Clock

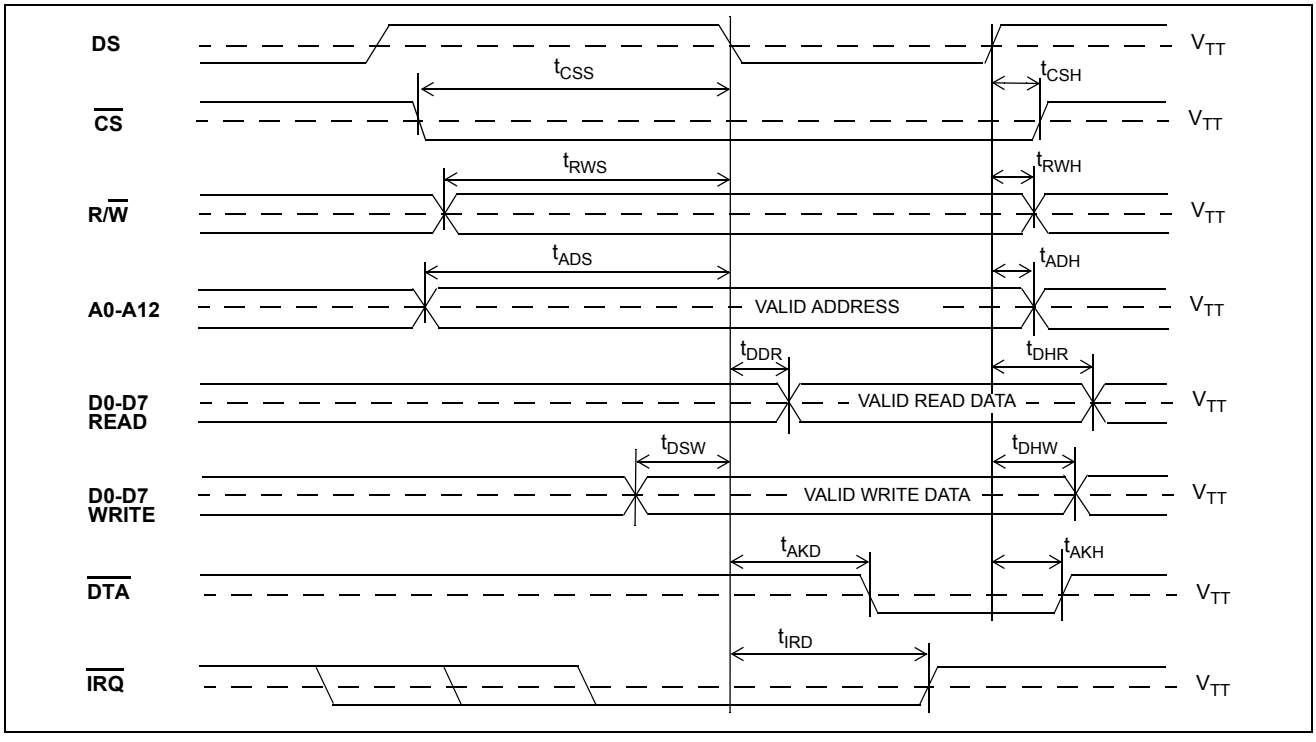


Figure 15 - Motorola Non-Multiplexed Bus Timing

9.0 EVP Registers Description

Echo Canceller A (ECA): Control Register 1							
Power-up 00_{hex}				**R/W Address: 00_{hex} + Base Address**			
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset	**INJDis**	**BBM**	**PAD**	**Bypass**	**AdpDis**	**0**	**ExtDl**
Functional Description of Register Bits							
Reset	When high, the power-up initialization is executed. This presets all register bits including this bit and clears the Adaptive Filter coefficients.						
INJDis	When high, the noise injection process is disabled. When low noise injection is enabled.						
BBM	When high, the Back to Back configuration is enabled. When low, the Normal configuration is enabled. Note: Do not enable Extended-Delay and BBM configurations at the same time. Always set **both** BBM bits of the two echo cancellers (Control Register 1) of the same group to the same logic value to avoid conflict.						
PAD	When high, 12 dB of attenuation is inserted into the Rin to Rout path. When low, the Gains register controls the signal levels.						
Bypass	When high, Sin data is by-passed to Sout and Rin data is by-passed to Rout. The Adaptive Filter coefficients are set to zero and the filter adaptation is stopped. When low, output data on both Sout and Rout is a function of the echo canceller algorithm.						
AdpDis	When high, echo canceller adaptation is disabled. The Voice Processor cancels echo. When low, the echo canceller dynamically adapts to the echo path characteristics.						
0	Bits marked as “1” or “0” are reserved bits and should be written as indicated.						
ExtDl	When high, Echo Cancellers A and B of the same group are internally cascaded into one 128 ms echo canceller. When low, Echo Cancellers A and B of the same group operate independently.						

Echo Canceller B (ECB): Control Register 1							
Power-up 02_{hex}				**R/W Address: 20_{hex} + Base Address**			
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset	**INJDis**	**BBM**	**PAD**	**Bypass**	**AdpDis**	**1**	**0**
Functional Description of Register Bits							
Reset	When high, the power-up initialization is executed which presets all register bits including this bit and clears the Adaptive Filter coefficients.						
INJDis	When high, the noise injection process is disabled. When low, noise injection is enabled.						
BBM	When high, the Back to Back configuration is enabled. When low, the Normal configuration is enabled. Note: Do not enable Extended-Delay and BBM configurations at the same time. Always set **both** BBM bits of the two echo cancellers (Control Register 1) of the same group to the same logic value to avoid conflict.						
PAD	When high, 12 dB of attenuation is inserted into the Rin to Rout path. When low, the Gains register controls the signal levels.						
Bypass	When high, Sin data is by-passed to Sout and Rin data is by-passed to Rout. The Adaptive Filter coefficients are set to zero and the filter adaptation is stopped. When low, output data on both Sout and Rout is a function of the echo canceller algorithm.						
AdpDis	When high, echo canceller adaptation is disabled. The Voice Processor cancels echo. When low, the echo canceller dynamically adapts to the echo path characteristics.						
1	Bits marked as “1” or “0” are reserved bits and should be written as indicated.						
0	Control Register 1 (Echo Canceller B) Bit 0 is a reserved bit and should be written “0”.						

Power-up 00_{hex}		ECA: Control Register 2				R/W Address: 01_{hex} + Base Address	
		ECB: Control Register 2				R/W Address: 21_{hex} + Base Address	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TDis	**PHDis**	**NLPDis**	**AutoTD**	**NBDis**	**HPFDis**	**MuteS**	**MuteR**

Functional Description of Register Bits	
TDis	When high, tone detection is disabled. When low, tone detection is enabled. When both Echo Cancellers A and B TDis bits are high, Tone Disable processors are disabled entirely and are put into Power Down mode.
PHDis	When high, the tone detectors will trigger upon the presence of a 2100 Hz tone regardless of the presence/absence of periodic phase reversals. When low, the tone detectors will trigger only upon the presence of a 2100 Hz tone with periodic phase reversals.
NLPDis	When high, the non-linear processor is disabled. When low, the non-linear processors function normally. Useful for G.165 conformance testing.
AutoTD	When high, the echo canceller puts itself in Bypass mode when the tone detectors detect the presence of 2100 Hz tone. See PHDis for qualification of 2100 Hz tones. When low, the echo canceller algorithm will remain operational regardless of the state of the 2100 Hz tone detectors.
NBDis	When high, the narrow-band detector is disabled. When low, the narrow-band detector is enabled.
HPFDis	When high, the offset nulling high pass filters are bypassed in the Rin and Sin paths. When low, the offset nulling filters are active and will remove DC offsets on PCM input signals.
MuteS	When high, data on Sout is muted to quiet code. When low, Sout carries active code.
MuteR	When high, data on Rout is muted to quiet code. When low, Rout carries active code.

Note: In order to correctly write to Control Register 1 and 2 of ECB, it is necessary to write the data twice to the register, one immediately after another. The two writes must be separated by at least 350 ns and no more than 20 us.

Power-up 00_{hex}		ECA: Status Register				R/W Address: 02_{hex} + Base Address	
		ECB: Status Register				R/W Address: 22_{hex} + Base Address	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserve	**TD**	**DTDet**	**Reserve**	**Reserve**	**Reserve**	**TDG**	**NB**

Functional Description of Register Bits	
Reserve	Reserved bit.
TD	Logic high indicates the presence of a 2100 Hz tone.
DTDet	Logic high indicates the presence of a double-talk condition.
Reserve	Reserved bit.
Reserve	Reserved bit.
Reserve	Reserved bit.
TDG	Tone detection status bit gated with the AutoTD bit. (Control Register 2). Logic high indicates that AutoTD has been enabled and the tone detector has detected the presence of a 2100 Hz tone.
NB	Logic high indicates the presence of a narrow-band signal on Rin.

Power-up 00_{hex}		ECA: Flat Delay Register (FD)				R/W Address: 04_{hex} + Base Address	
		ECB: Flat Delay Register (FD)				R/W Address: 24_{hex} + Base Address	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FD7	**FD6**	**FD5**	**FD4**	**FD3**	**FD2**	**FD1**	**FD0**

Power-up 00_{hex}		ECA: Decay Step Number Register (NS)				R/W Address: 07_{hex} + Base Address	
		ECB: Decay Step Number Register (NS)				R/W Address: 27_{hex}+ Base Address	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NS7	**NS6**	**NS5**	**NS4**	**NS3**	**NS2**	**NS1**	**NS0**

Power-up 00_{hex}		ECA: Decay Step Size Control Register (SSC)				R/W Address: 06_{hex} + Base Address	
		ECB: Decay Step Size Control Register (SSC)				R/W Address: 26_{hex} + Base Address	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	**0**	**0**	**0**	**0**	**SSC2**	**SSC1**	**SSC0**

Note: Bits marked with “0” are reserved bits and should be written “0”

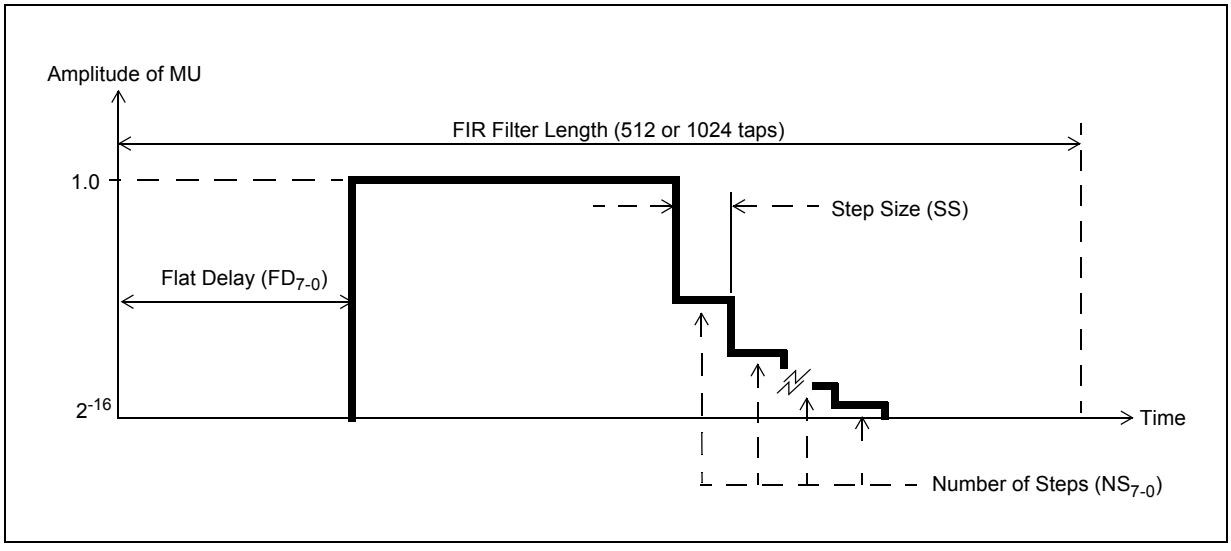


Figure 16 - The MU Profile

Functional Description of Register Bits

The Exponential Decay registers (Decay Step Number and Decay Step Size) and Flat Delay register allow the LMS adaptation step-size (MU) to be programmed over the length of the FIR filter. A programmable MU profile allows the performance of the echo canceller to be optimized for specific applications. For example, if the characteristic of the echo response is known to have a flat delay of several milliseconds and a roughly exponential decay of the echo impulse response, then the MU profile can be programmed to approximate this expected impulse response thereby improving the convergence characteristics of the Adaptive Filter. Note that in the following register descriptions, one tap is equivalent to 125 μs (64 ms/512 taps).

FD_{7-0} **Flat Delay**: This register defines the flat delay of the MU profile, (i.e., where the MU value is 2^{-16}). The delay is defined as FD_{7-0} x 8 taps. For example; If FD_{7-0} = 5, then MU=2^{-16} for the first 40 taps of the echo canceller FIR filter. The valid range of FD_{7-0} is: $0 \leq FD_{7-0} \leq 64$ in normal mode and $0 \leq FD_{7-0} \leq 128$ in extended-delay mode. The default value of FD_{7-0} is zero.

SSC_{2-0} **Decay Step Size Control**: This register controls the step size (SS) to be used during the exponential decay of MU. The decay rate is defined as a decrease of MU by a factor of 2 every SS taps of the FIR filter, where SS = 4 x$2^{SSC_{2-0}}$. For example; If SSC_{2-0} = 4, then MU is reduced by a factor of 2 every 64 taps of the FIR filter. The default value of SSC_{2-0} is 04_{hex}.

NS_{7-0} **Decay Step Number**: This register defines the number of steps to be used for the decay of MU where each step has a period of SS taps (see SSC_{2-0}). The start of the exponential decay is defined as: Filter Length (512 or 1024) - [Decay Step Number (NS_{7-0}) x Step Size (SS)] where SS = 4 x$2^{SSC_{2-0}}$.
For example; If NS_{7-0}=4 and SSC_{2-0}=4, then the exponential decay start value is 512 - [NS_{7-0} x SS] = 512 - [4 x (4x2^4)] = 256 taps for a filter length of 512 taps.

Power-up FB_{hex}		ECA: Control Register 3				R/W Address: 08_{hex} + Base Address	
		ECB: Control Register 3				R/W Address: 28_{hex} + Base Address	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NLRun2	**InjCtrl**	**NLRun1**	**RingClr**	**Reserve**	**PathClr**	**PathDet**	**NLPSel**
Functional Description of Register Bits							
NLRun2	When high, the comfort noise level estimator actively rejects double-talk as being background noise. When low, the noise level estimator makes no such distinction.						
InjCtrl	Selects which noise ramping scheme is used. See Table below.						
NLRun1	When high, the comfort noise level estimator actively rejects uncancelled echo as being background noise. When low, the noise level estimator makes no such distinction.						
RingClr	When high, the instability detector is activated. When low, the instability detector is disabled.						
Reserve	Reserved bit. Must always be set to one for normal operation.						
PathClr	When high, the current echo channel estimate will be cleared and the echo canceller will enter fast convergence mode upon detection of a path change. When low, the echo canceller will keep the current path estimate but revert to fast convergence mode upon detection of a path change. Note: this bit is ignored if PathDet is low.						
PathDet	When high, the path change detector is activated. When low, the path change detector is disabled.						
NLPSel	When high, the Advanced NLP is selected. When low, the original NLP is selected.						

Table 5 below is the same Table shown on page 9.

Feature	Register or Bit(s)	Advanced NLP Default Value	Original NLP Default Value
NLP Selection	NLPSel (Control Register 3)	1	0 (feature not supported)
Reject uncancelled echo as noise	NLRun1 (Control Register 3)	1	0 (feature not supported)
Reject double-talk as noise	NLRun2 (Control Register 3)	1	0 (feature not supported)
Noise level estimator ramping scheme	InjCtrl (Control Register 3)	1	0 (feature not supported)
Noise level ramping rate	NLInc (Noise Control)	5_{hex}	C_{hex}
Noise level scaling	Noise Scaling	16_{hex}	74_{hex}

Table 5 - Comparison of the NLP Types

Power-up 54_{hex}		ECA: Control Register 4				R/W Address: 09_{hex} + Base Address	
		ECB: Control Register 4				R/W Address: 29_{hex} + Base Address	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	**SD2**	**SD1**	**SD0**	**0**	**Slow2**	**Slow1**	**Slow0**
Functional Description of Register Bits							
0	Must be set to zero.						
SupDec	These three bits (SD2,SD1,SD0) control how long the echo canceller remains in a fast convergence state following a path change, Reset or Bypass operation. A value of zero will keep the echo canceller in fast convergence indefinitely.						
0	Must be set to zero.						
Slow	Slow convergence mode speed adjustment.(Bits Slow2, Slow1,Slow0) For Slow = 1, 2,..., 7, slow convergence speed is reduced by a factor of 2^{Slow} as compared to normal adaptation. For Slow = 0, no adaptation occurs during slow convergence.						

Power-up 16_{hex}		ECA: Noise Scaling (NS)				R/W Address: $0A_{hex}$ + Base Address	
		ECB: Noise Scaling (NS)				R/W Address: $2A_{hex}$ + Base Address	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NS7	**NS6**	**NS5**	**NS4**	**NS3**	**NS2**	**NS1**	**NS0**
Functional Description of Register Bits							
This register is used to scale the comfort noise up or down. Larger values will increase the relative level of comfort noise. The default value of 16_{hex} will provide G.168 compliance with the Advanced NLP. A value of 74_{hex} is recommended if the original NLP is used.							

Power-up 45_{hex}		ECA: Noise Control				R/W Address: $0B_{hex}$ + Base Address	
		ECB: Noise Control				R/W Address: $2B_{hex}$ + Base Address	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserve	**Reserve**	**Reserve**	**Reserve**	**NLInc3**	**NLInc2**	**NLInc1**	**NLInc0**
Functional Description of Register Bits							
Reserve	Reserved bits. Must be set to 4_{hex} for normal operation.						
NLInc	Noise level estimator ramping rate. When InjCtrl = 1, a lower value will give faster ramping. When InjCtrl = 0, a higher value will give faster ramping. The default value of 5_{hex} will provide G.168 compliance with InjCtrl = 1. A value of C_{hex} is recommended if InjCtrl = 0.						

Power-up N/A		ECA: Rin Peak Detect Register 2 (RP)				R/W Address: $0D_{hex}$ + Base Address	
		ECB: Rin Peak Detect Register 2 (RP)				R/W Address: $2D_{hex}$ + Base Address	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RP15	**RP14**	**RP13**	**RP12**	**RP11**	**RP10**	**RP9**	**RP8**
Power-up N/A		**ECA: Rin Peak Detect Register 1 (RP)**				**R/W Address: $0C_{hex}$ + Base Address**	
		ECB: Rin Peak Detect Register 1 (RP)				**R/W Address: $2C_{hex}$ + Base Address**	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RP7	**RP6**	**RP5**	**RP4**	**RP3**	**RP2**	**RP1**	**RP0**
Functional Description of Register Bits							
These peak detector registers allow the user to monitor the receive in (Rin) peak signal level. The information is in 16-bit 2's complement linear coded format presented in two 8 bit registers for each echo canceller. The high byte is in Register 2 and the low byte is in Register 1.							

Power-up N/A		ECA: Sin Peak Detect Register 2 (SP)				R/W Address: $0F_{hex}$ + Base Address	
		ECB: Sin Peak Detect Register 2 (SP)				R/W Address: $2F_{hex}$ + Base Address	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8
Power-up N/A		**ECA: Sin Peak Detect Register 1 (SP)**				**R/W Address: $0E_{hex}$ + Base Address**	
		ECB: Sin Peak Detect Register 1 (SP)				**R/W Address: $2E_{hex}$ + Base Address**	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SP7	**SP6**	**SP5**	**SP4**	**SP3**	**SP2**	**SP1**	**SP0**
Functional Description of Register Bits							
These peak detector registers allow the user to monitor the send in (Sin) peak signal level. The information is in 16-bit 2's complement linear coded format presented in two 8 bit registers for each echo canceller. The high byte is in Register 2 and the low byte is in Register 1.							

Power-up N/A		ECA: Error Peak Detect Register 2 (EP)				R/W Address: 11_{hex} + Base Address	
		ECB: Error Peak Detect Register 2 (EP)				R/W Address: 31_{hex} + Base Address	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EP15	**EP14**	**EP13**	**EP12**	**EP11**	**EP10**	**EP9**	**EP8**
Power-up N/A		**ECA: Error Peak Detect Register 1 (EP)**				**R/W Address: 10_{hex} + Base Address**	
		ECB: Error Peak Detect Register 1 (EP)				**R/W Address: 30_{hex} + Base Address**	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EP7	**EP6**	**EP5**	**EP4**	**EP3**	**EP2**	**EP1**	**EP0**
Functional Description of Register Bits							
These peak detector registers allow the user to monitor the error signal peak level. The information is in 16-bit 2's complement linear coded format presented in two 8 bit registers for each echo canceller. The high byte is in Register 2 and the low byte is in Register 1.							

Power-up 48_{hex}		ECA: Double-Talk Detection Threshold Register 2				R/W Address: 15_{hex} + Base Address	
		ECB: Double-Talk Detection Threshold Register 2				R/W Address: 35_{hex} + Base Address	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DTDT15	**DTDT14**	**DTDT13**	**DTDT12**	**DTDT11**	**DTDT10**	**DTDT9**	**DTDT8**
Power-up 00_{hex}		**ECA: Double-Talk Detection Threshold Register 1**				**R/W Address: 14_{hex} + Base Address**	
		ECB: Double-Talk Detection Threshold Register 1				**R/W Address: 34_{hex} + Base Address**	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DTDT7	**DTDT6**	**DTDT5**	**DTDT4**	**DTDT3**	**DTDT2**	**DTDT1**	**DTDT0**
Functional Description of Register Bits							
This register allows the user to program the level of Double-Talk Detection Threshold (DTDT). The 16 bit 2's complement linear value defaults to 4800_{hex}= 0.5625 or -5 dB. The maximum value is $7FFF_{hex}$ = 0.9999 or 0 dB. The high byte is in Register 2 and the low byte is in Register 1.							

Power-up $0C_{hex}$		ECA: Non-Linear Processor Threshold Register 2 (NLPTHR)				R/W Address: 19_{hex} + Base Address	
		ECB: Non-Linear Processor Threshold Register 2 (NLPTHR)				R/W Address: 39_{hex} + Base Address	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NLP15	**NLP14**	**NLP13**	**NLP12**	**NLP11**	**NLP10**	**NLP9**	**NLP8**
Power-up $E0_{hex}$		ECA: Non-Linear Processor Threshold Register 1 (NLPTHR)				R/W Address: 18_{hex} + Base Address	
		ECB: Non-Linear Processor Threshold Register 1 (NLPTHR)				R/W Address: 38_{hex} + Base Address	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NLP7	**NLP6**	**NLP5**	**NLP4**	**NLP3**	**NLP2**	**NLP1**	**NLP0**
Functional Description of Register Bits							
This register allows the user to program the level of the Non-Linear Processor Threshold (NLPTHR). The 16 bit 2's complement linear value defaults to $0CE0_{hex}$ = 0.1 or -20.0 dB. The maximum value is $7FFF_{hex}$ = 0.9999 or 0 dB. The high byte is in Register 2 and the low byte is in Register 1.							

Power-up 40_{hex}		ECA: Adaptation Step Size Register 2 (MU)				R/W Address: $1B_{hex}$ + Base Address	
		ECB: Adaptation Step Size Register 2 (MU)				R/W Address: $3B_{hex}$ + Base Address	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MU15	**MU14**	**MU13**	**MU12**	**MU11**	**MU10**	**MU9**	**MU8**
Power-up 00_{hex}		ECA: Adaptation Step Size Register 1 (MU)				R/W Address: $1A_{hex}$ + Base Address	
		ECB: Adaptation Step Size Register 1 (MU)				R/W Address: $3A_{hex}$ + Base Address	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MU7	**MU6**	**MU5**	**MU4**	**MU3**	**MU2**	**MU1**	**MU0**
Functional Description of Register Bits							
This register allows the user to program the level of MU. MU is a 16 bit 2's complement value which defaults to 4000_{hex} = 1.0 The maximum value is $7FFF_{hex}$ or 1.9999 decimal. The high byte is in Register 2 and the low byte is in Register 1.							

Power-up 44_{hex}		ECA: Gains Register 2				R/W Address: $1D_{hex}$ + Base Address	
		ECB: Gains Register 2				R/W Address: $3D_{hex}$ + Base Address	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	**Rin2**	**Rin1**	**Rin0**	**0**	**Rout2**	**Rout1**	**Rout0**

Power-up 44_{hex}		ECA: Gains Register 1				R/W Address: $1C_{hex}$ + Base Address	
		ECB: Gains Register 1				R/W Address: $3C_{hex}$ + Base Address	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	**Sin2**	**Sin1**	**Sin0**	**0**	**Sout2**	**Sout1**	**Sout0**

Functional Description of Register Bits

This register is used to select gain values on RIN, ROUT, SIN and SOUT. Gains has the following structure:
RIN ROUT SIN SOUT
Gains = 0xxx 0xxx 0xxx 0xxx
= 0100 0100 0100 0100 (4444_{hex}) default

Gains is split into four groups of four bits. Each group maps to a different signal port (as indicated above), and has three gain bits. The following table indicates how these gain bits are used:

Bit2	Bit1	Bit0	Gain Level
1	0	0	0 dB (default)
0	1	1	-3 dB
0	1	0	-6 dB
0	0	1	-9 dB
0	0	0	-12 dB

Note that the -12 dB PAD bit in Control Register 1 provides 12 dB of attenuation in the Rin to Rout path, and will override the settings in Gains.

Main Control Register 0 (EC Group 0)							
Power-up 00_{hex}				R/W Address: 400_{hex}			
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WR_all	**ODE**	**MIRQ**	**MTDBI**	**MTDAI**	**Format**	**Law**	**PWUP**
Functional Description of Register Bits							
WR_all	Write all control bit: When high, Group 0-15 Echo Cancellers Registers are mapped into 0000_{hex} to $0003F_{hex}$ which is Group 0 address mapping. Useful to initialize the 16 Groups of Echo Cancellers as per Group 0. When low, address mapping is per Figure 10. Note: Only the Main Control Register 0 has the WR_all bit						
ODE	Output Data Enable: This control bit is logically AND'd with the ODE input pin. When both ODE bit and ODE input pin are high, the Rout and Sout outputs are enabled. When the ODE bit is low or the ODE input pin is low, the Rout and Sout outputs are high impedance. Note: Only the Main Control Register 0 has the ODE bit.						
MIRQ	Mask Interrupt: When high, all the interrupts from the Tone Detectors output are masked. The Tone Detectors operate as specified in their Echo Canceller B, Control Register 2. When low, the Tone Detectors Interrupts are active. Note: Only the Main Control Register 0 has the MIRQ bit.						
MTDBI	Mask Tone Detector B Interrupt: When high, the Tone Detector interrupt output from Echo Canceller B is masked. The Tone Detector operates as specified in Echo Canceller B, Control Register 2. When low, the Tone Detector B Interrupt is active.						
MTDAI	Mask Tone Detector A Interrupt: When high, the Tone Detector interrupt output from Echo Canceller A is masked. The Tone Detector operates as specified in Echo Canceller A, Control Register 2. When low, the Tone Detector A Interrupt is active.						
Format	ITU-T/Sign Mag: When high, both Echo Cancellers A and B for a given group, accept ITU-T (G.711) PCM code. When low, both Echo Cancellers A and B for a given group, accept sign-magnitude PCM code.						
Law	A/μ Law: When high, both Echo Cancellers A and B for a given group, accept A-Law companded PCM code. When low, both Echo Cancellers A and B for a given group, accept μ-Law companded PCM code.						
PWUP	Power-UP: When high, both Echo Cancellers A and B and Tone Detectors for a given group, are active. When low, both Echo Cancellers A and B and Tone Detectors for a given group, are placed in Power Down mode. In this mode, the corresponding PCM data are bypassed from Rin to Rout and from Sin to Sout with two frames delay. When the PWUP bit toggles from zero to one, the echo canceller A and B execute their initialization routine which presets their registers, Base Address+00_{hex} to Base Address+$3F_{hex}$, to the default power up value and clears the Adaptive Filter coefficients. Two frames are necessary for the initialization routine to execute properly. Once the initialization routine is executed, the user can set the per channel Control Registers for their specific application.						

Main Control Register 1 (EC Group 1)	R/W Address: 401_{hex}
Main Control Register 2 (EC Group 2)	R/W Address: 402_{hex}
Main Control Register 3 (EC Group 3)	R/W Address: 403_{hex}
Main Control Register 4 (EC Group 4)	R/W Address: 404_{hex}
Main Control Register 5 (EC Group 5)	R/W Address: 405_{hex}
Main Control Register 6 (EC Group 6)	R/W Address: 406_{hex}
Main Control Register 7 (EC Group 7)	R/W Address: 407_{hex}
Main Control Register 8 (EC Group 8)	R/W Address: 408_{hex}
Main Control Register 9 (EC Group 9)	R/W Address: 409_{hex}
Main Control Register 10 (EC Group 10)	R/W Address: $40A_{hex}$
Main Control Register 11 (EC Group 11)	R/W Address: $40B_{hex}$
Main Control Register 12 (EC Group 12)	R/W Address: $40C_{hex}$
Main Control Register 13 (EC Group 13)	R/W Address: $40D_{hex}$
Main Control Register 14 (EC Group 14)	R/W Address: $40E_{hex}$
Main Control Register 15 (EC Group 15)	R/W Address: $40F_{hex}$

Power-up 00_{hex}							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused	**Unused**	**Unused**	**MTDBI**	**MTDAI**	**Format**	**Law**	**PWUP**

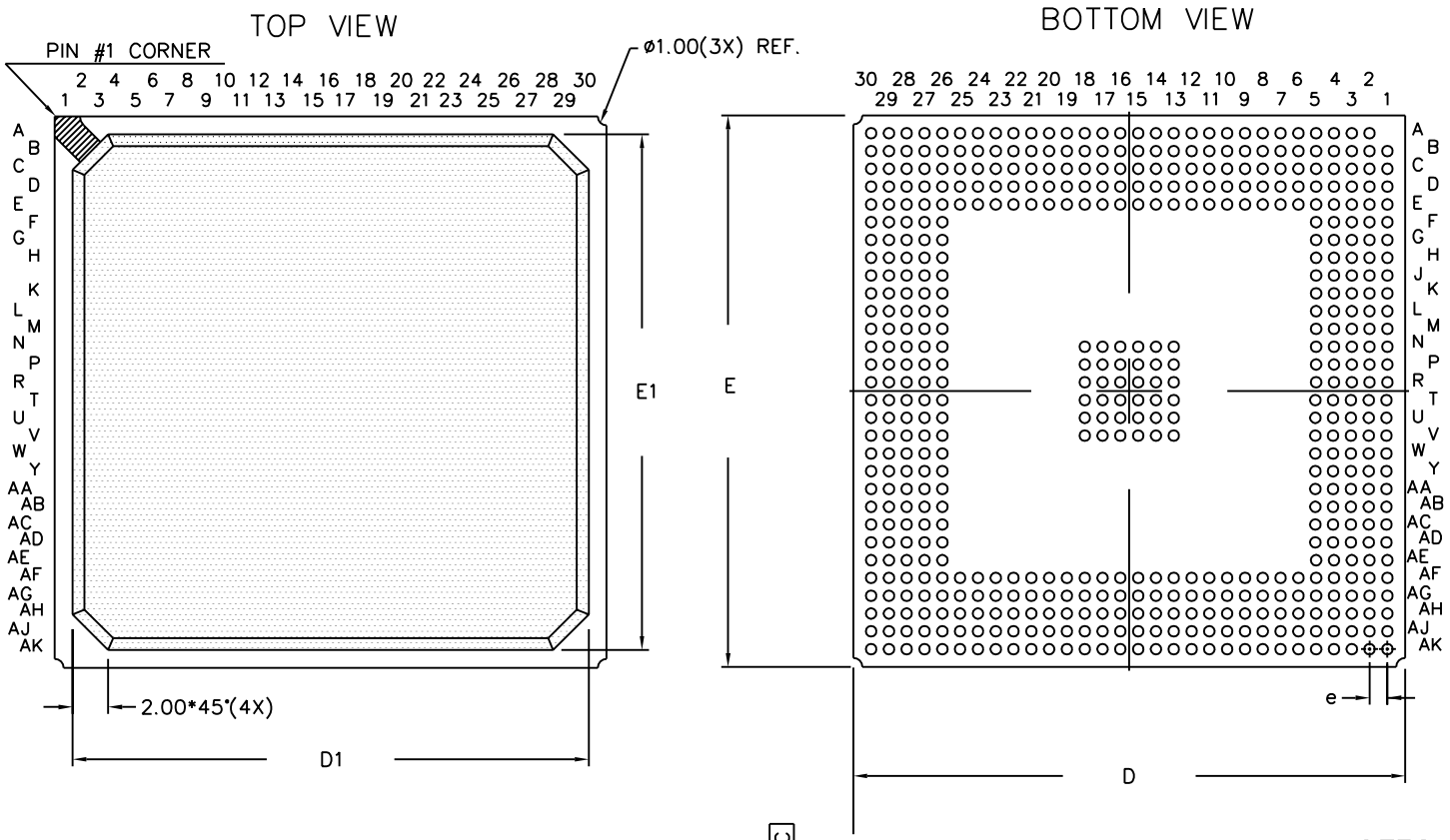
Functional Description of Register Bits	
Unused	Unused Bits.
MTDBI	Mask Tone Detector B Interrupt: When high, the Tone Detector interrupt output from Echo Canceller B is masked. The Tone Detector operates as specified in Echo Canceller B, Control Register 2. When low, the Tone Detector B Interrupt is active.
MTDAI	Mask Tone Detector A Interrupt: When high, the Tone Detector interrupt output from Echo Canceller A is masked. The Tone Detector operates as specified in Echo Canceller A, Control Register 2. When low, the Tone Detector A Interrupt is active.
Format	ITU-T/Sign Mag: When high, both Echo Cancellers A and B for a given group, select ITU-T (G.711) PCM code. When low, both Echo Cancellers A and B for a given group, select sign-magnitude PCM code.
Law	A/μ Law: When high, both Echo Cancellers A and B for a given group, select A-Law companded PCM code. When low, both Echo Cancellers A and B for a given group, select μ-Law companded PCM code.
PWUP	Power-UP: When high, both Echo Cancellers A and B and Tone Detectors for a given group, are active. When low, both Echo Cancellers A and B and Tone Detectors for a given group, are placed in Power Down mode. In this mode, the corresponding PCM data are bypassed from Rin to Rout and from Sin to Sout with two frames delay. When the PWUP bit toggles from zero to one, the echo cancellers A and B execute their initialization routine which presets their registers, Base Address+00_{hex} to Base Address+$3F_{hex}$, to the default Reset Value and clears the Adaptive Filter coefficients. Two frames are necessary for the initialization routine to execute properly. Once the initialization routine is executed, the user can set the per channel Control Registers for their specific application.

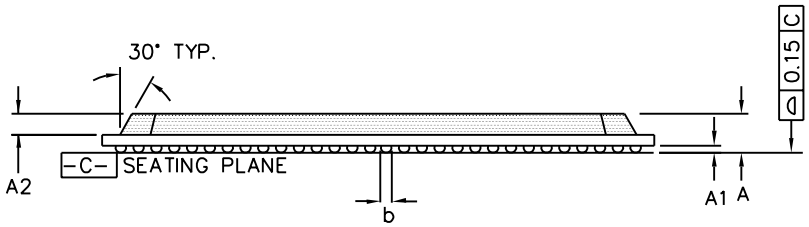
Interrupt FIFO Register							
Power-up 00_{hex}				**R/W Address: 410_{hex}**			
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IRQ	**0**	**0**	**I4**	**I3**	**I2**	**I1**	**I0**

Functional Description of Register Bits	
IRQ	Logic high indicates an interrupt has occurred. IRQ bit is cleared after the Interrupt FIFO register is read. Logic Low indicates that no interrupt is pending and the FIFO is empty.
0	Unused bit. Always zero.
0	Unused bit. Always zero.
I<4:0>	I<4:0> binary code indicates the channel number at which a Tone Detector state change has occurred. Note: Whenever a Tone Disable is detected or released, an interrupt is generated.

Test Register							
Power-up 00_{hex}				**R/W Address: 411_{hex}**			
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserve	**Reserve**	**Reserve**	**Reserve**	**Reserve**	**Reserve**	**Reserve**	**Tirq**

Functional Description of Register Bits	
Reserve	Reserved bits. Must always be set to zero for normal operation.
Tirq	Test IRQ: Useful for the application engineer to verify the interrupt service routine. When high, any change to MTDBI and MTDAI bits of the Main Control Register will cause an interrupt and its corresponding channel number will be available from the Interrupt FIFO Register. When low, normal operation is selected.





SIDE VIEW

DIMENSION	MIN	MAX
A	2.1	2.36
A1	0.40	0.60
A2	1.17 REF	
D	30.8	31.20
D1	29.00 REF	
E	30.8	31.20
E1	29.00 REF	
b	0.50	0.70
e	1.00	
N	535	
Conforms to JEDEC MS-034		

NOTES: –
1. Controlling dimensions are in MM.
2. Seating plane is defined by the spherical crown of the solder balls.
3. Not to scale.
4. N is the number of solder balls
5. Substrate thickness is 0.61 MM.
6. Mold thickness is 1.17 MM

ISSUE	1			
ACN	18Sep02			
DATE	213443			
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

Package Code GA

Package Outline for
535 Ball PBGA (31 x 31mm)

GPD00797

For more information about all Zarlink products
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www.zarlink.com

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