

## TPS3809xxx-Q1 3-Pin Supply Voltage Supervisors

### 1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C5
- 3-Pin SOT-23 Package
- Supply Current of  $9\ \mu\text{A}$  (Typical)
- Precision-Supply Voltage Monitor 2.5 V, 3 V, 3.3 V, 5 V
- Power-On Reset Generator With Fixed Delay Time of 200 ms
- Pin-For-Pin Compatible With MAX 809

### 2 Applications

- Automotive Applications With DSPs, Microcontrollers, or Microprocessors
- Automotive Camera Systems
- Automotive Radar
- USB Hubs and Charging

### 3 Description

The TPS3809 family of supervisory circuits provides circuit initialization and timing supervision, primarily for DSPs and processor-based systems.

During power-on,  $\overline{\text{RESET}}$  is asserted when the supply voltage  $V_{\text{DD}}$  becomes higher than 1.1 V. Thereafter, the supervisory circuit monitors  $V_{\text{DD}}$  and keeps  $\overline{\text{RESET}}$  active as long as  $V_{\text{DD}}$  remains below the threshold voltage  $V_{\text{IT}}$ . An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time,  $t_{\text{d(typ)}} = 200\ \text{ms}$ , starts after  $V_{\text{DD}}$  has risen above the threshold voltage  $V_{\text{IT}}$ . When the supply voltage drops below the threshold voltage  $V_{\text{IT}}$ , the output becomes active (low) again. No external components are required. All the devices of this family have a fixed sense-threshold voltage  $V_{\text{IT}}$  set by an internal voltage divider.

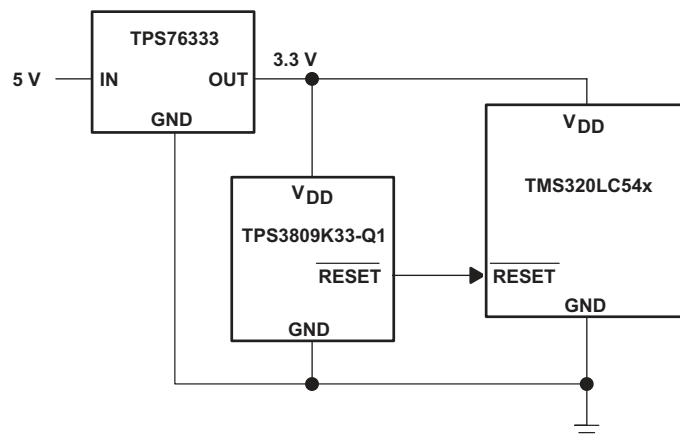
The product spectrum is designed for supply voltages of 2.5 V, 3 V, 3.3 V, and 5 V. The circuits are available in a 3-pin SOT-23. The TPS3809xxx-Q1 devices are characterized for operation over a temperature range of  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ , and are qualified in accordance with AEC-Q100 stress test qualification for integrated circuits. For more information about TI's voltage supervisor portfolio, please visit the [Supervisor and Reset IC Overview](#) web page.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS3809xxx-Q1	SOT-23 (3)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

#### Typical Application



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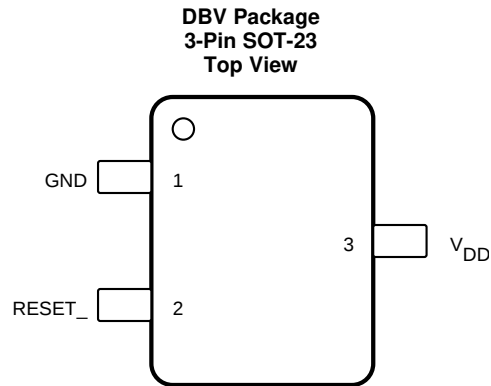
## 4 Revision History

Changes from Revision A (December 2002) to Revision B	Page
• Added AEC-Q100 Qualified information in bullets .....	1
• Changed <i>Applications</i> list items .....	1
• Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	1
• Changed device part numbers by adding -Q1 to them throughout document .....	5

## 5 Voltage Options

$T_A$	DEVICE NAME	THRESHOLD VOLTAGE	MARKING
–40°C to 125°C	TPS3809J25QDBVRQ1	2.25 V	PCZQ
	TPS3809L30QDBVRQ1	2.64 V	PDAQ
	TPS3809K33QDBVRQ1	2.93 V	PDBQ
	TPS3809I50QDBVRQ1	4.55 V	PDCQ

## 6 Pin Configuration and Functions



**Pin Functions**

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	1	—	Ground
$\overline{\text{RESET}}$	2	O	Reset output
$V_{DD}$	3	I	Supply voltage and supervising input

## 7 Specifications

### 7.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

	MIN	MAX	UNIT
Supply voltage, $V_{DD}$ <sup>(2)</sup>		7	V
All other pins <sup>(2)</sup>	-0.3	7	V
Maximum low output current, $I_{OL}$		5	mA
Maximum high output current, $I_{OH}$		-5	mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{DD}$ )	-20	20	mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{DD}$ )	-20	20	mA
Continuous total power dissipation			
Operating free-air temperature range, $T_A$	-40	125	°C
Storage temperature, $T_{stg}$	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to GND. For reliable operation the device should not be operated at 7 V for more than  $t = 1000$  h continuously.

### 7.2 ESD Ratings

		VALUE	UNIT
$V_{ESD}$ Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±2000	V
	Charged-device model (CDM), per AEC Q100-011	±750	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{DD}$	Supply voltage	2		6	V
$T_A$	Operating free-air temperature	-40		125	°C

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS3809xxx-Q1	UNIT
		DBV (SOT-23)	
		3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	232.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	187.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	104.1	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	40.5	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	104.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT		
V <sub>OH</sub>	High-level output voltage	V <sub>DD</sub> = 2.5 V to 6 V, I <sub>OH</sub> = -500 μA	V <sub>DD</sub> - 0.2			V		
		V <sub>DD</sub> = 3.3 V, I <sub>OH</sub> = -2 μA	V <sub>DD</sub> - 0.4					
		V <sub>DD</sub> = 6 V, I <sub>OH</sub> = -4 mA	T <sub>A</sub> = -40°C to +25°C	V <sub>DD</sub> - 0.4				
			T <sub>A</sub> = 125°C	V <sub>DD</sub> - 0.5				
V <sub>OL</sub>	Low-level output voltage	V <sub>DD</sub> = 2 V to 6 V, I <sub>OL</sub> = 500 μA	0.2			V		
		V <sub>DD</sub> = 3.3 V, I <sub>OL</sub> = 2 mA	0.4					
		V <sub>DD</sub> = 6 V, I <sub>OL</sub> = 4 mA	0.4					
Power-up reset voltage <sup>(1)</sup>		V <sub>DD</sub> ≥ 1.1 V, I <sub>OL</sub> = 50 μA	0.2			V		
V <sub>IT-</sub>	Negative-going input threshold voltage <sup>(2)</sup>	TPS3809J25-Q1	T <sub>A</sub> = -40°C to +125°C	2.20	2.25	2.30	V	
		TPS3809L30-Q1		2.58	2.64	2.7		
		TPS3809K33-Q1		2.87	2.93	2.99		
		TPS3809I50-Q1		T <sub>A</sub> = -40°C to +85°C	4.45	4.55		4.65
				T <sub>A</sub> = -40°C to +125°C	4.4	4.55		4.65
V <sub>hys</sub>	Hysteresis	TPS3809J25-Q1	30			mV		
		TPS3809L30-Q1	35					
		TPS3809K33-Q1	40					
		TPS3809I50-Q1	60					
I <sub>DD</sub>	Supply current	V <sub>DD</sub> = 2 V, Output unconnected	9			μA		
		V <sub>DD</sub> = 6 V, Output unconnected	20					
C <sub>i</sub>	Input capacitance	V <sub>I</sub> = 0 V to V <sub>DD</sub>	5			pF		

 (1) The lowest supply voltage at which  $\overline{\text{RESET}}$  becomes active.  $t_r$ , V<sub>DD</sub> ≥ 15 μs/V.

(2) To ensure best stability of the threshold voltage, a bypass capacitor ( 0.1 μF, ceramic) should be placed near the supply terminals.

## 7.6 Timing Requirements

 R<sub>L</sub> = 1 MΩ, C<sub>L</sub> = 50 pF, T<sub>A</sub> = 25°C

		MIN	NOM	MAX	UNIT
t <sub>w</sub>	Pulse width at V <sub>DD</sub>	V <sub>DD</sub> = V <sub>IT-</sub> + 0.2 V, V <sub>DD</sub> = V <sub>IT-</sub> - 0.2 V		3	μs

## 7.7 Switching Characteristics

 R<sub>L</sub> = 1 MΩ, C<sub>L</sub> = 50 pF, T<sub>A</sub> = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>d</sub>	Delay time	V <sub>DD</sub> ≥ V <sub>IT-</sub> + 0.2 V, See timing diagram, <a href="#">Figure 1</a>	120	200	280	ms
t <sub>PHL</sub>	Propagation (delay) time, high-to-low-level output	V <sub>DD</sub> to $\overline{\text{RESET}}$ delay V <sub>IL</sub> = V <sub>IT-</sub> - 0.2 V, V <sub>IH</sub> = V <sub>IT-</sub> + 0.2 V	1			μs

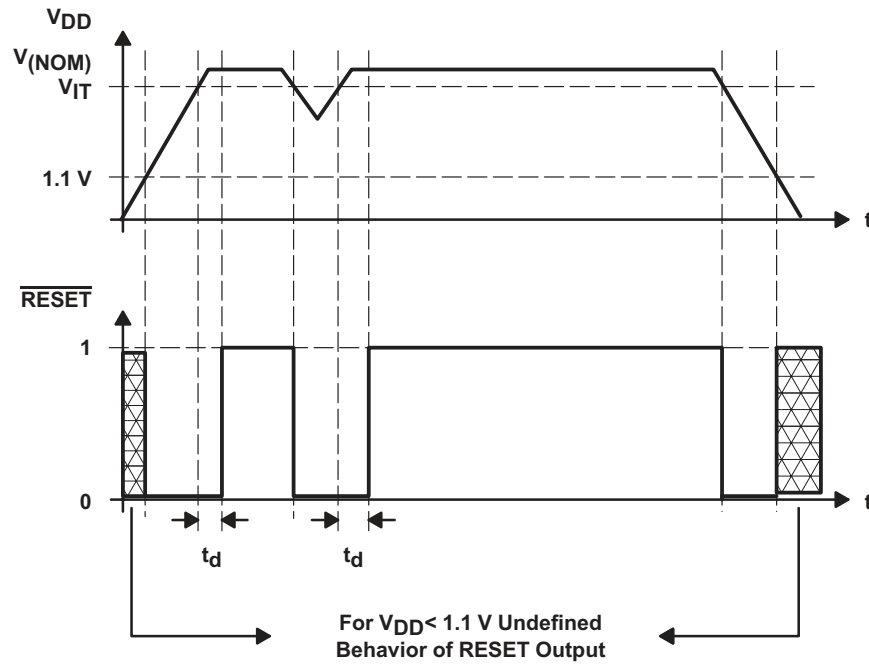


Figure 1. Timing Diagram

## 7.8 Typical Characteristics

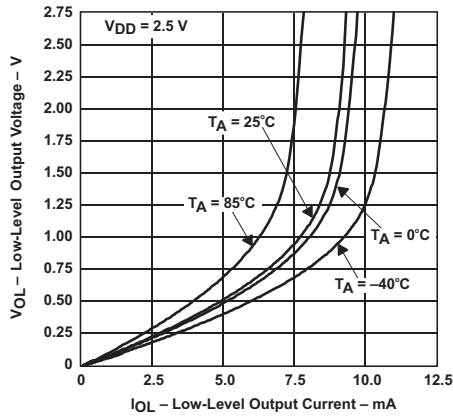


Figure 2. Low-Level Output Voltage vs Low-Level Output Current

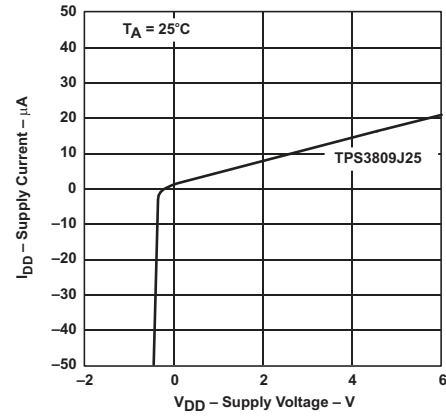
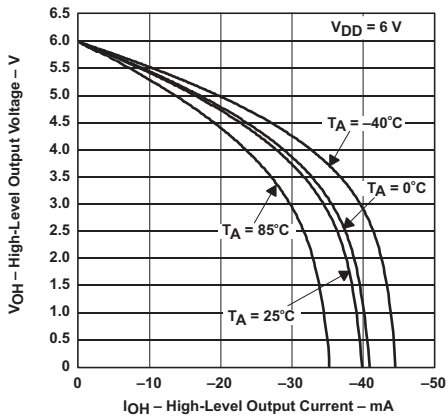
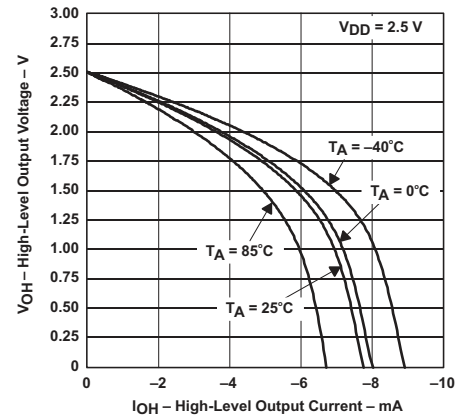


Figure 3. Supply Current vs Supply Voltage



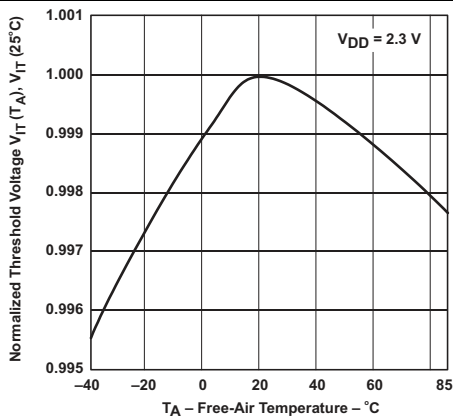
$V_{DD} = 6\text{ V}$

Figure 4. High-Level Output Voltage vs High-Level Output Current



$V_{DD} = 2.5\text{ V}$

Figure 5. High-Level Output Voltage vs High-Level Output Current



$V_{DD} = 2.3\text{ V}$

Figure 6. Normalized Input Threshold Voltage vs Free-Air Temperature at  $V_{DD}$

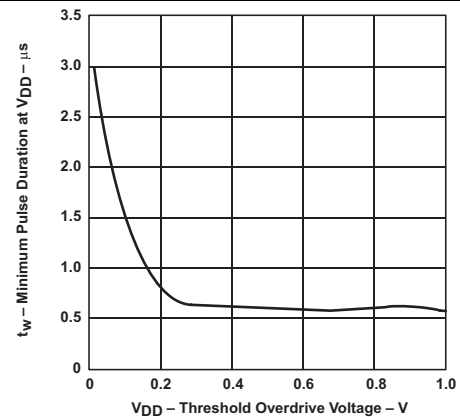


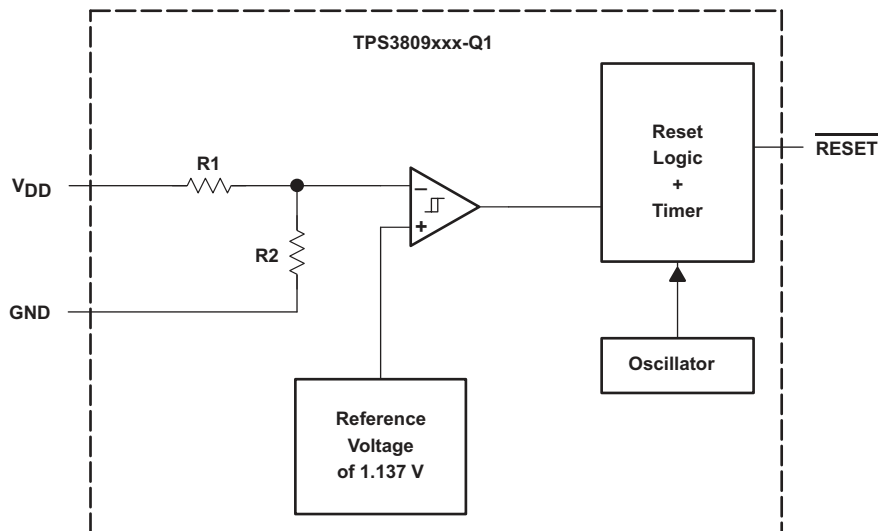
Figure 7. Minimum Pulse Duration at  $V_{DD}$  vs  $V_{DD}$  Threshold Overdrive Voltage

## 8 Detailed Description

### 8.1 Overview

The TPS3809xxx-Q1 device is a low-current supervisory circuit for monitoring system voltages above 2 V. The device asserts an active-low  $\overline{\text{RESET}}$  signal when VDD drops below a preset threshold. The  $\overline{\text{RESET}}$  output remains low until VDD returns above its threshold. The device design is also to be relatively immune to short negative transients on the VDD pin.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 V<sub>DD</sub> Monitoring

The V<sub>DD</sub> pin provides a terminal at which a system voltage can be monitored. If the voltage on this pin drops below V<sub>IT</sub>,  $\overline{\text{RESET}}$  is asserted low. The comparator has a built-in hysteresis to ensure smooth  $\overline{\text{RESET}}$  assertions and deassertions. Refer to [Voltage Options](#) to determine the V<sub>DD</sub> voltage threshold for each device.

#### 8.4 Device Functional Modes

TPS3809xxx-Q1 monitors one supply using the V<sub>DD</sub> pin. When V<sub>DD</sub> is above the V<sub>IT</sub> threshold for the device,  $\overline{\text{RESET}}$  will be high. When V<sub>DD</sub> is below the V<sub>IT</sub> threshold for the device,  $\overline{\text{RESET}}$  will be low.



## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The TPS3809xxx-Q1 voltage supervisor device design asserts an active-low RESET signal when  $V_{DD}$  drops below a voltage threshold  $V_{IT}$ . The  $\overline{RESET}$  signal remains low until the voltage returns above its threshold. The typical application is with a processor or microcontroller, which needs to be reset when the supply rail drops below a specified tolerance.

### 9.2 Typical Application

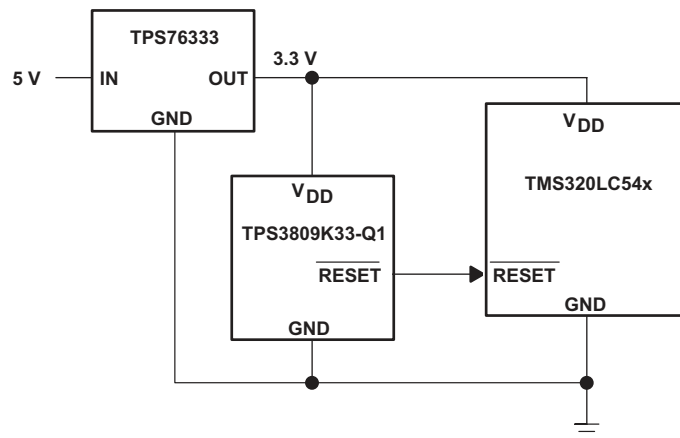


Figure 8. Typical Application Schematic

#### 9.2.1 Design Requirements

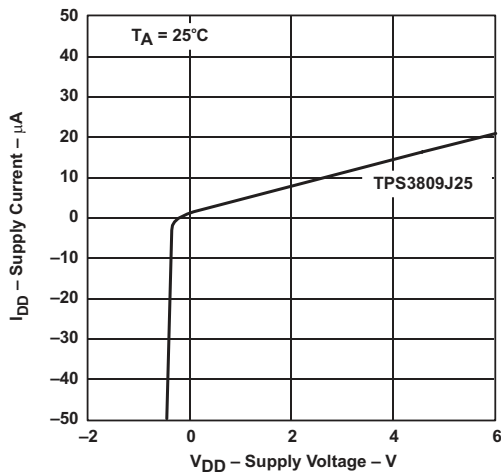
Each device has a fixed-voltage monitoring threshold, and the device should be chosen based on the voltage being monitored. Refer to [Voltage Options](#) to determine the  $V_{DD}$  voltage threshold for each device. In this example, a 3.3V supply rail to a microcontroller will be monitored.

#### 9.2.2 Detailed Design Procedure

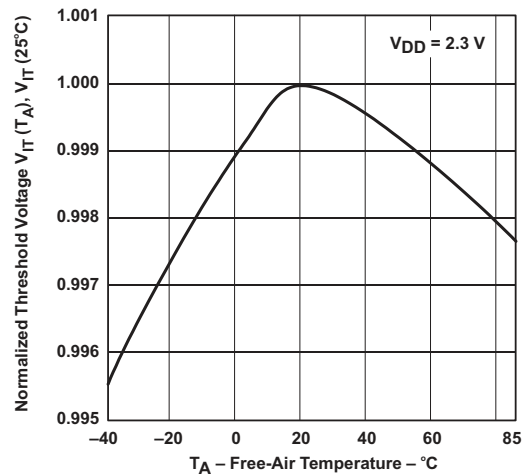
Because a 3.3-V supply rail needs to be monitored, TPS3809K33-Q1 should be used. This device has a 2.93-V threshold for reset. Connect the 3.3-V supply to the  $V_{DD}$  pin and the reset output of the supervisor to the reset pin of the microcontroller.

**Typical Application (continued)**

**9.2.3 Application Curves**



**Figure 9. Supply Current vs Supply Voltage**



**Figure 10. Normalized Input Threshold Voltage vs Free-Air Temperature at V<sub>DD</sub>**

## 10 Power Supply Recommendations

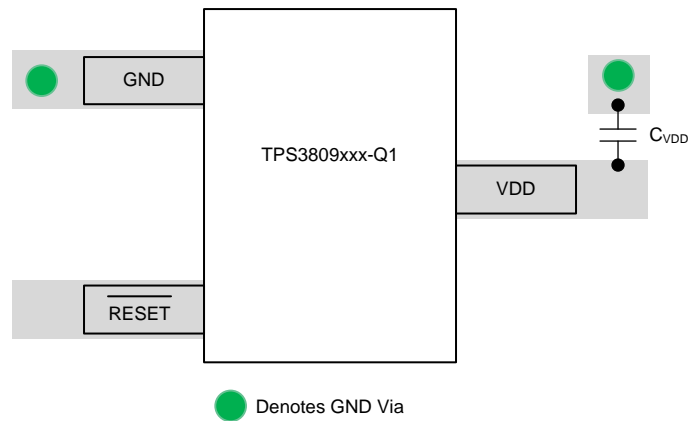
The TPS3809xxx-Q1 device design operates from an input supply from 2 V to 6 V. TI recommends placing a 0.1- $\mu$ F capacitor near the  $V_{DD}$  pin.

## 11 Layout

### 11.1 Layout Guidelines

TI recommends placing the 0.1- $\mu$ F decoupling capacitor close to the  $V_{DD}$  pin. The  $V_{DD}$  and GND traces should be able to carry 30  $\mu$ A without a significant drop in voltage.

### 11.2 Layout Example



**Figure 11. Layout Example**

## 12 Device and Documentation Support

### 12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 1. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS3809J25-Q1	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TPS3809L30-Q1	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TPS3809K33-Q1	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TPS3809I50-Q1	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.3 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.5 Glossary





[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
2T09I50QDBVRG4Q	ACTIVE	SOT-23	DBV	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PDCQ	
2T09J25QDBVRG4Q	LIFEBUY	SOT-23	DBV	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PCZQ	
2U3809K33QDBVRG4Q1	LIFEBUY	SOT-23	DBV	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PDBQ	
2U3809L30QDBVRG4Q1	LIFEBUY	SOT-23	DBV	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PDAQ	
TPS3809I50QDBVRQ1	ACTIVE	SOT-23	DBV	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PDCQ	
TPS3809J25QDBVRQ1	LIFEBUY	SOT-23	DBV	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PCZQ	
TPS3809K33QDBVRQ1	ACTIVE	SOT-23	DBV	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PDBQ	
TPS3809L30QDBVRQ1	ACTIVE	SOT-23	DBV	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PDAQ	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

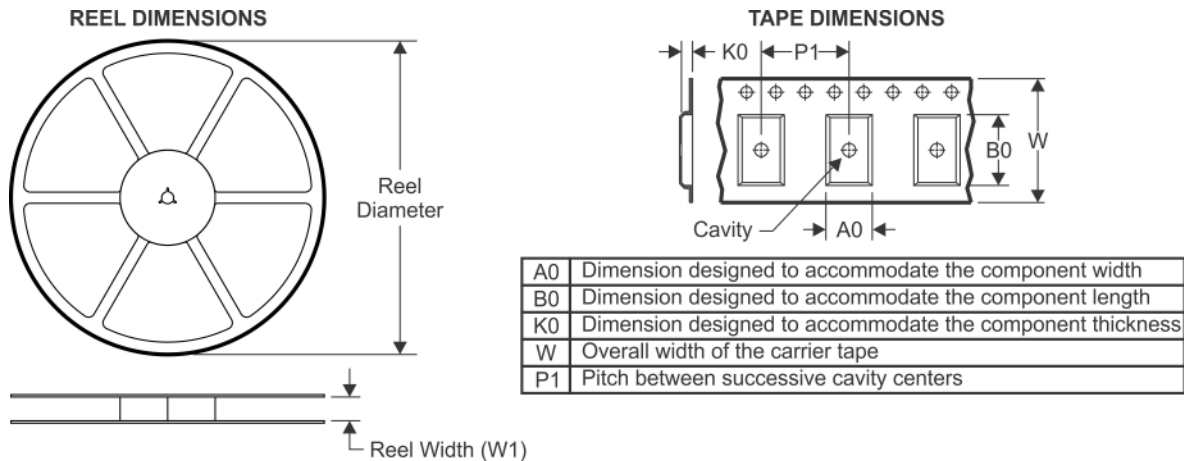
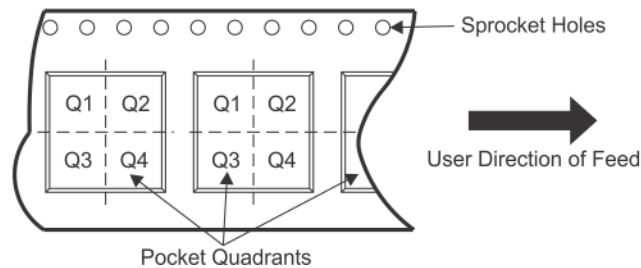
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TPS3809-Q1, TPS3809I50-Q1, TPS3809J25-Q1, TPS3809K33-Q1, TPS3809L30-Q1 :**

- Catalog: [TPS3809I50](#), [TPS3809J25](#), [TPS3809K33](#), [TPS3809L30](#)
- Enhanced Product: [TPS3809-EP](#), [TPS3809I50-EP](#), [TPS3809K33-EP](#), [TPS3809L30-EP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
2T09I50QDBVRG4Q	SOT-23	DBV	3	3000	180.0	9.0	3.3	3.2	1.47	4.0	8.0	Q3
2T09J25QDBVRG4Q	SOT-23	DBV	3	3000	180.0	9.0	3.3	3.2	1.47	4.0	8.0	Q3
2U3809K33QDBVRG4Q1	SOT-23	DBV	3	3000	180.0	9.0	3.3	3.2	1.47	4.0	8.0	Q3
2U3809L30QDBVRG4Q1	SOT-23	DBV	3	3000	180.0	9.0	3.3	3.2	1.47	4.0	8.0	Q3
TPS3809I50QDBVRQ1	SOT-23	DBV	3	3000	180.0	9.0	3.3	3.2	1.47	4.0	8.0	Q3
TPS3809J25QDBVRQ1	SOT-23	DBV	3	3000	180.0	9.0	3.3	3.2	1.47	4.0	8.0	Q3
TPS3809K33QDBVRQ1	SOT-23	DBV	3	3000	180.0	9.0	3.3	3.2	1.47	4.0	8.0	Q3
TPS3809L30QDBVRQ1	SOT-23	DBV	3	3000	180.0	9.0	3.3	3.2	1.47	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**

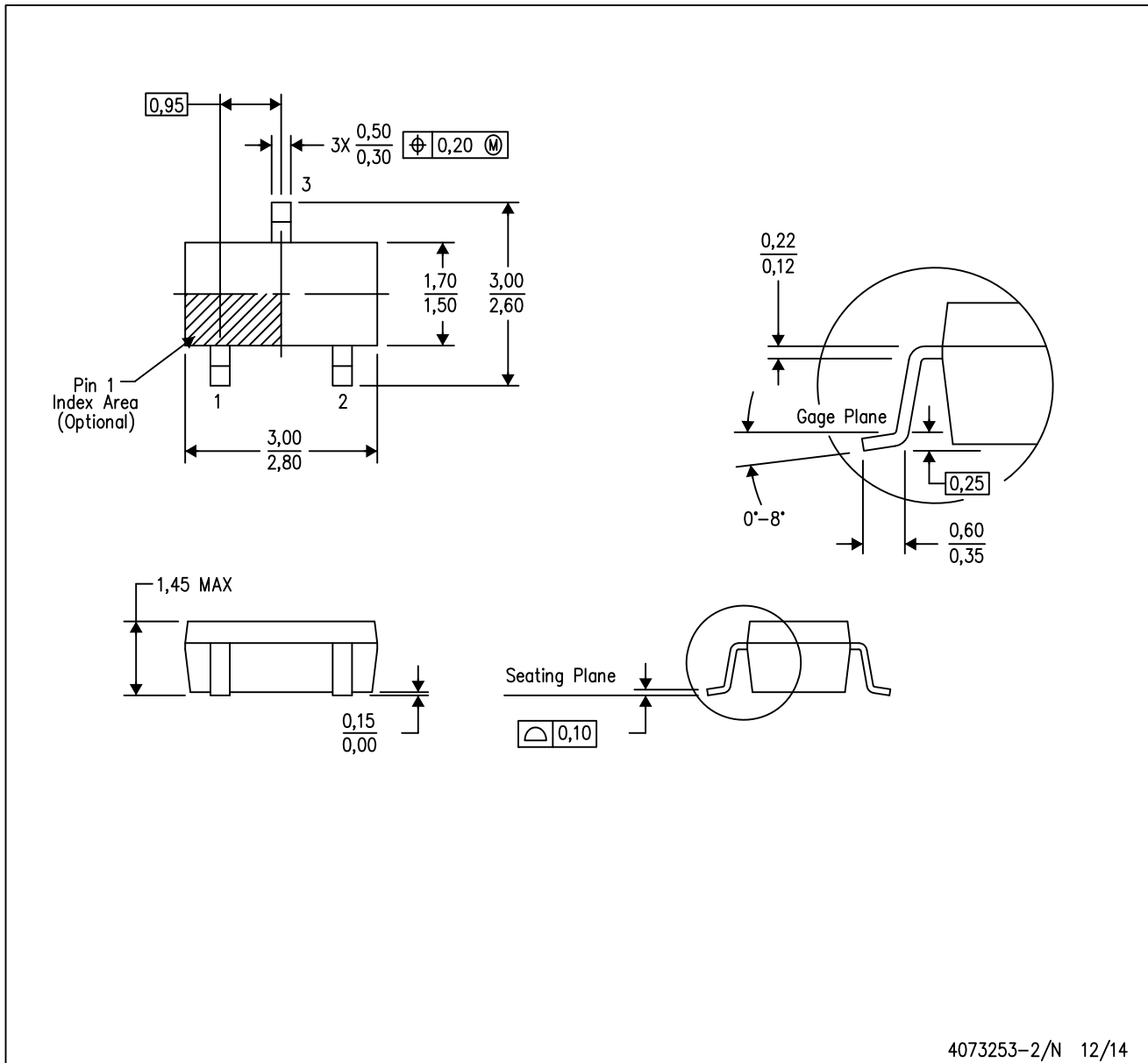

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
2T09I50QDBVRG4Q	SOT-23	DBV	3	3000	182.0	182.0	20.0
2T09J25QDBVRG4Q	SOT-23	DBV	3	3000	182.0	182.0	20.0
2U3809K33QDBVRG4Q1	SOT-23	DBV	3	3000	182.0	182.0	20.0
2U3809L30QDBVRG4Q1	SOT-23	DBV	3	3000	182.0	182.0	20.0
TPS3809I50QDBVRQ1	SOT-23	DBV	3	3000	182.0	182.0	20.0
TPS3809J25QDBVRQ1	SOT-23	DBV	3	3000	182.0	182.0	20.0
TPS3809K33QDBVRQ1	SOT-23	DBV	3	3000	182.0	182.0	20.0
TPS3809L30QDBVRQ1	SOT-23	DBV	3	3000	182.0	182.0	20.0



DBV (R-PDSO-G3)

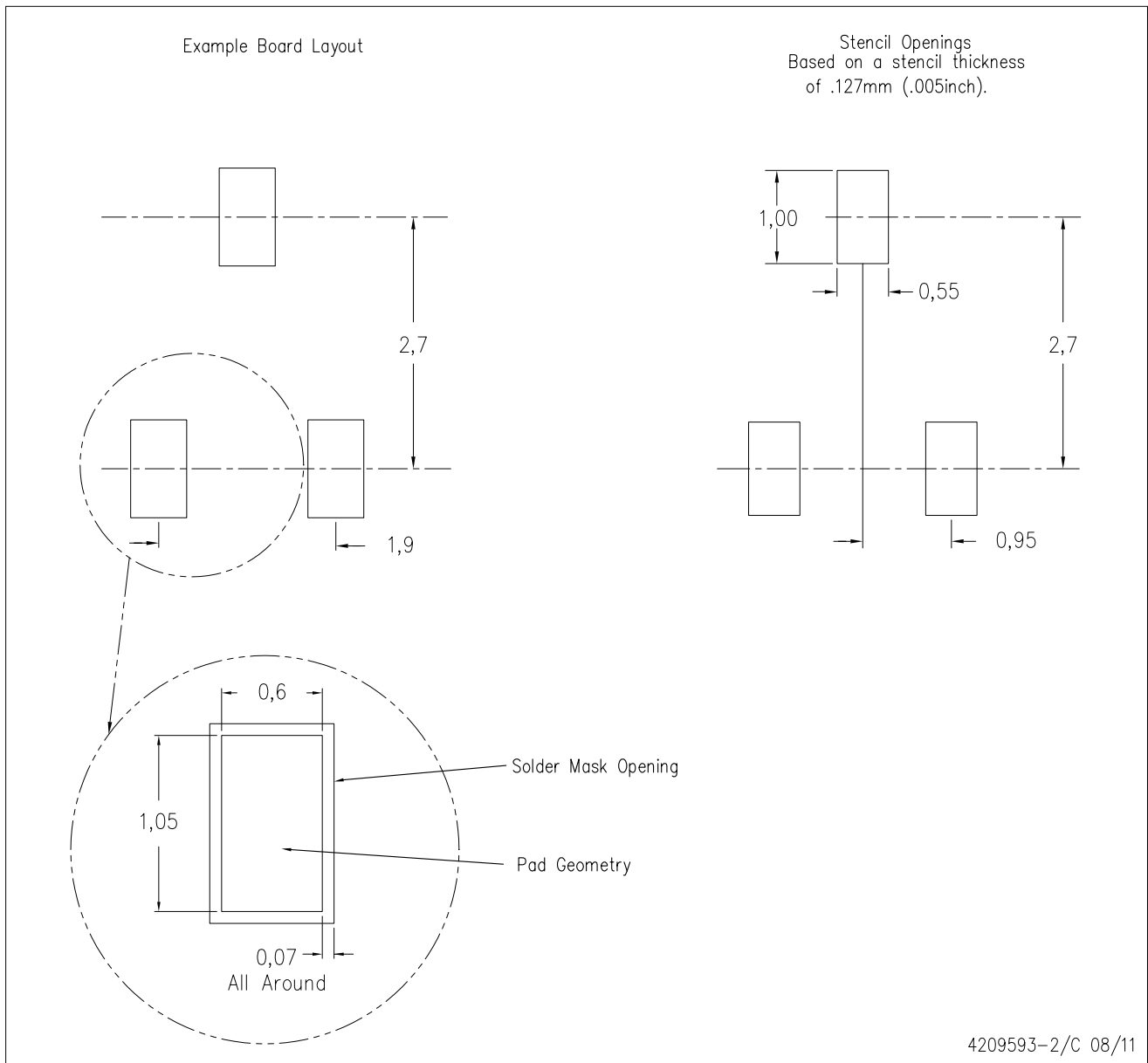
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.

DBV (R-PDSO-G3)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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