A1210, A1211, A1212, A1213, and A1214

Continuous-Time Latch Family

FEATURES AND BENEFITS

- AEC-Q100 automotive qualified
- Continuous-time operation
  - □ Fast power-on time
  - □ Low noise
- Stable operation over full operating temperature range
- Reverse-battery protection
- Solid-state reliability
- Factory-programmed at end-of-line for optimum performance
- Robust EMC performance
- High ESD rating
- Regulator stability without a bypass capacitor

PACKAGES:

Not to scale

3-pin SOT23W
(suffix LH)

3-pin SIP,
matrix HD style
(suffix UA)

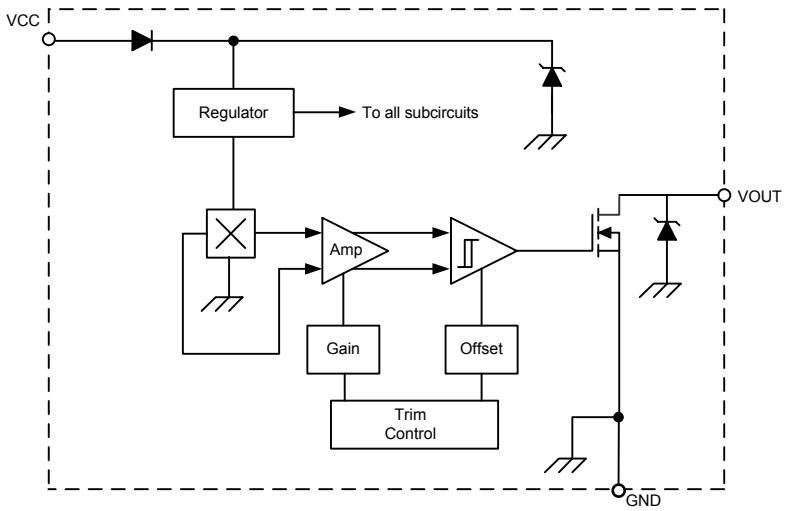
3-pin SIP,
chopper style
(suffix UA)

DESCRIPTION

The Allegro™ A1210-A1214 Hall-effect latches are next generation replacements for the popular Allegro 317x and 318x lines of latching switches. The A121x family, produced with BiCMOS technology, consists of devices that feature fast power-on time and low-noise operation. Device programming is performed after packaging, to ensure increased switch point accuracy by eliminating offsets that can be induced by package stress. Unique Hall element geometries and low-offset amplifiers help to minimize noise and to reduce the residual offset voltage normally caused by device overmolding, temperature excursions, and thermal stress.

The A1210-A1214 Hall-effect latches include the following on a single silicon chip: voltage regulator, Hall-voltage generator, small-signal amplifier, Schmitt trigger, and NMOS output transistor. The integrated voltage regulator permits operation from 3.8 to 24 V. The extensive on-board protection circuitry makes possible a ±30 V absolute maximum voltage rating for superior protection in automotive and industrial motor commutation applications, without adding external components. All devices in the family are identical except for magnetic switch point levels.

The small geometries of the BiCMOS process allow these devices to be provided in ultra small packages. The package styles available provide magnetically optimized solutions for most applications. Package LH is an SOT23W, a miniature low-profile surface-mount package, while package UA is a three-lead ultra mini SIP for through-hole mounting. Each package is lead (Pb) free, with 100% matte-tin-plated leadframes.



Functional Block Diagram

SELECTION GUIDE

Part Number	Packing [1]	Mounting	Ambient, T_A	B_{RP} (Min)	B_{OP} (Max)
A1210ELHLT-T	7-in. reel, 3000 pieces/reel	3-pin SOT23W surface mount	–40°C to 85°C	–150 G	150 G
A1210ELHLX-T	13-in. reel, 10000 pieces/reel	3-pin SOT23W surface mount			
A1210LLHLT-T	7-in. reel, 3000 pieces/reel	3-pin SOT23W surface mount	–40°C to 150°C		
A1210LLHLX-T	13-in. reel, 10000 pieces/reel	3-pin SOT23W surface mount			
A1210LUA-T [2]	Bulk, 500 pieces/bag	3-pin SIP through hole			
A1211LUA-T [2]	Bulk, 500 pieces/bag	3-pin SIP through hole	–40°C to 150°C	–180 G	180 G
A1212LLHLT-T	7-in. reel, 3000 pieces/reel	3-pin SOT23W surface mount	–40°C to 150°CMC 640 <<0C .4553 529.9502 TmTP6c50°C		

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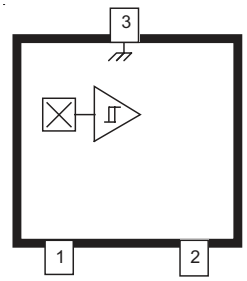
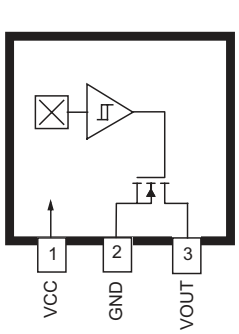


Package LH, 3-Pin SOT23W Pinout Diagram



Package UA, 3-Pin SIP Pinout Diagram

Terminal List

Name	Number		Description
	Package LH	Package UA	
VCC	1	1	Connects power supply to chip
VOUT	2	3	Output from circuit
GND	3	2	Ground

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DEVICE QUALIFICATION PROGRAM

Contact Allegro for information.

EMC (Electromagnetic Compatibility) REQUIREMENTS

Contact Allegro for information.

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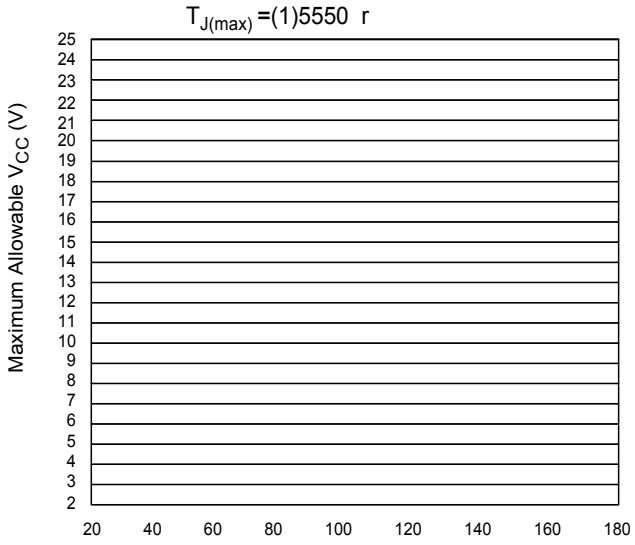
THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	Package LH, on single layer, single-sided PCB with copper limited to solder pads	228	°C/W
		Package LH, on single layer, double-sided PCB with 0.926 in^2 copper area	110	°C/W
		Package UA on single layer, single-sided PCB with copper limited to solder pads	165	°C/W



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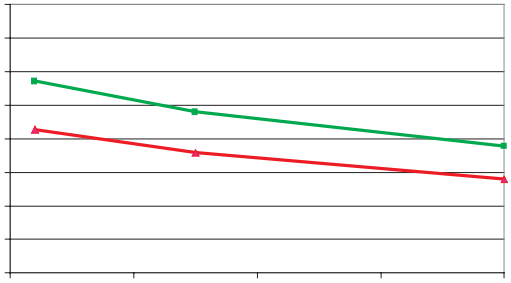
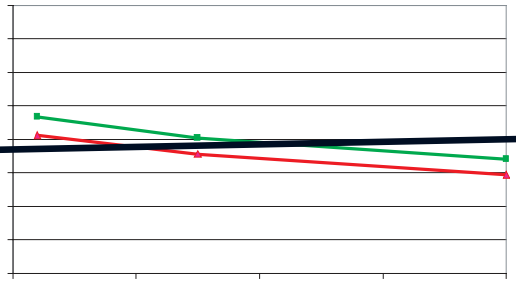
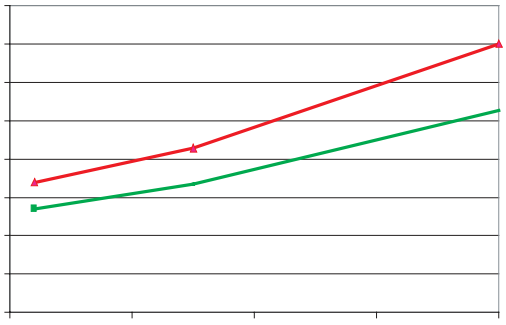
CHARACTERISTIC DATA







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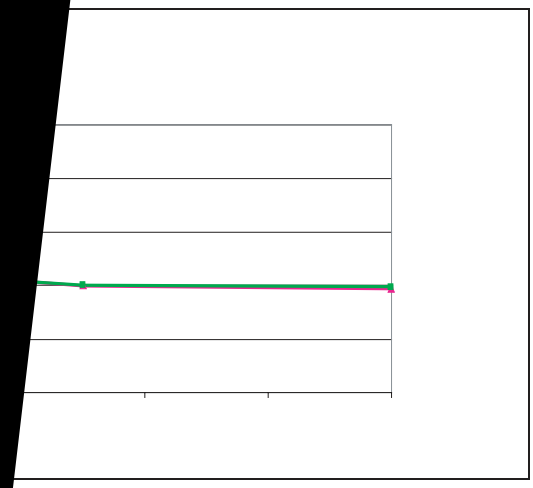
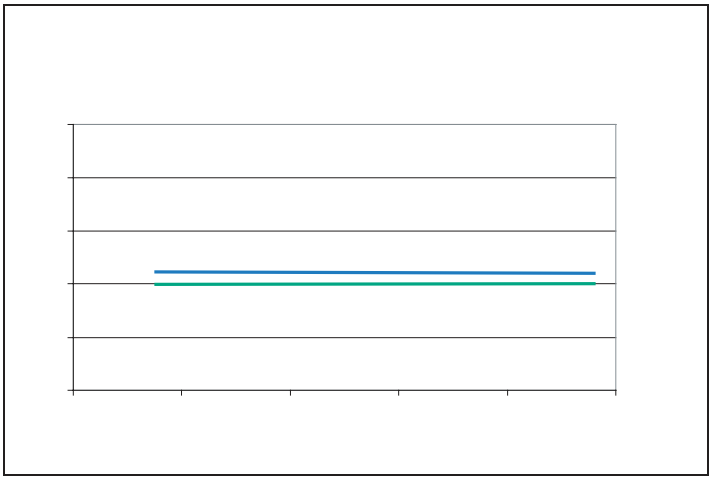
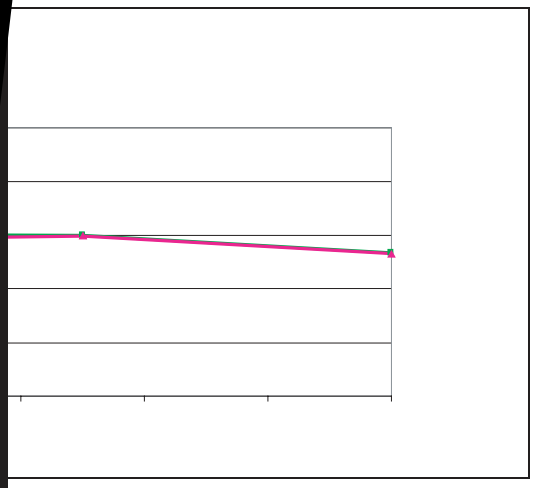
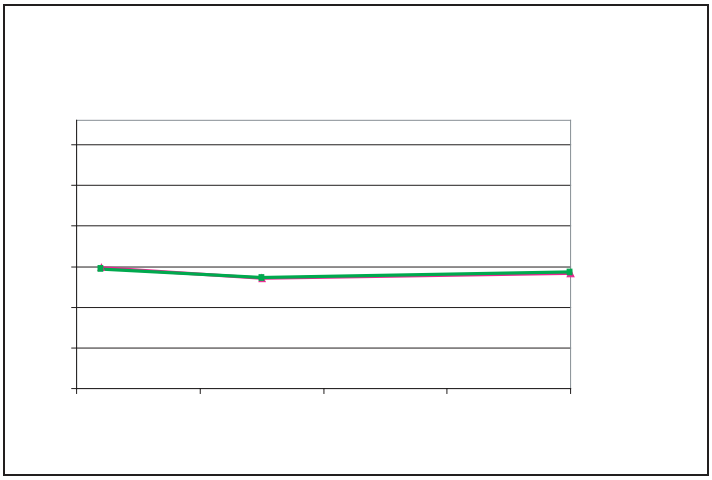
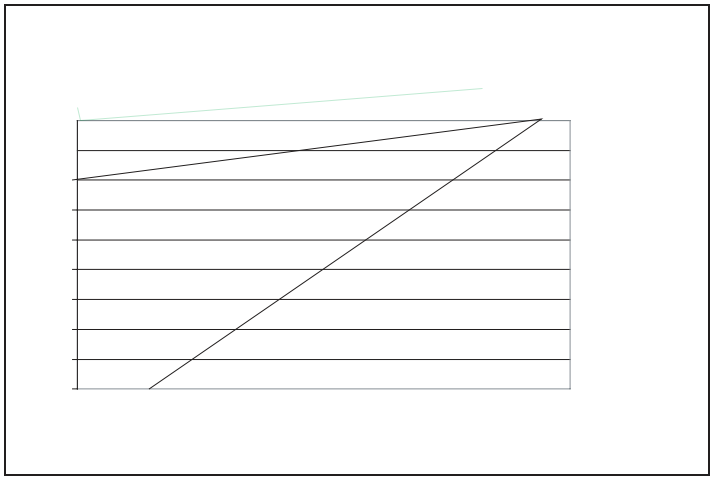
Continuous-Time Latch Family

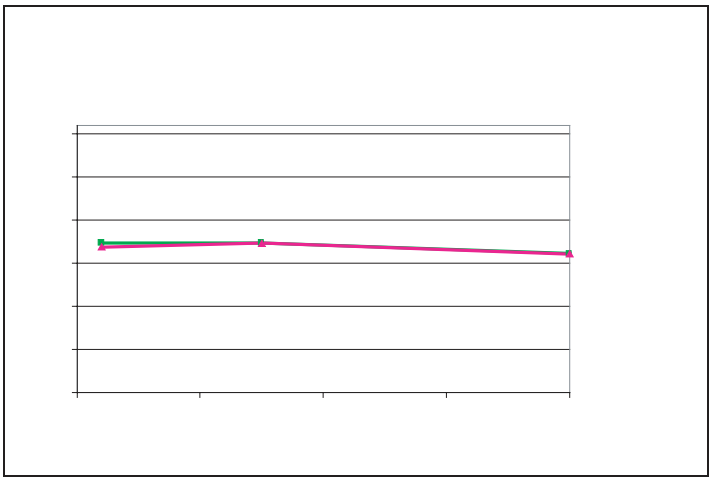


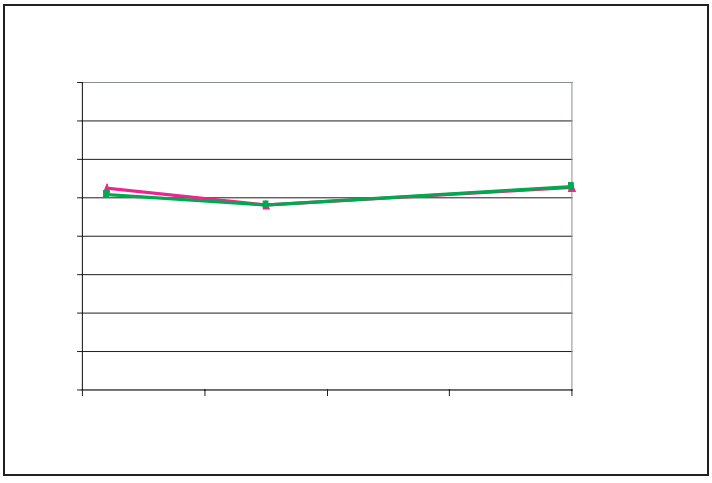












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FUNCTIONAL DESCRIPTION

Operation

The output of these devices switches low (turns on) when a magnetic field perpendicular to the Hall element exceeds the operate point threshold, B_{OP}. After turn-on, the output is capable of sinking 25 mA and the output voltage is $V_{OUT(SAT)}$. Notice that the device latches; that is, a south pole of sufficient strength towards the branded surface of the device turns the device on, and the device remains on with removal of the south pole. When the magnetic field is reduced below the release point, B_{RP}, the device output goes high (turns off). The difference in the magnetic operate and release points is the hysteresis, B_{hys}, of the device. This built-in hysteresis allows clean switching of the output, even in the presence of external mechanical vibration and electrical noise.

Powering-on the device in the hysteresis range, less than B_{OP} and higher than B_{RP}, allows an indeterminate output state. The correct state is attained after the first excursion beyond B_{OP} or B_{RP}.

Continuous-Time Benefits

Continuous-time devices, such as the A121x family, offer the fastest available power-on settling time and frequency response.

Due to offsets generated during the IC packaging process, continuous-time devices typically require programming after packaging to tighten magnetic parameter distributions. In contrast, chopper-stabilized switches employ an offset cancellation technique on the chip that eliminates these offsets without the need for after-packaging programming. The tradeoff is a longer settling time and reduced frequency response as a result of the chopper-stabilization offset cancellation algorithm.

The choice between continuous-time and chopper-stabilized designs is solely determined by the application. Battery management is an example where continuous-time is often required. In these applications, V_{CC}

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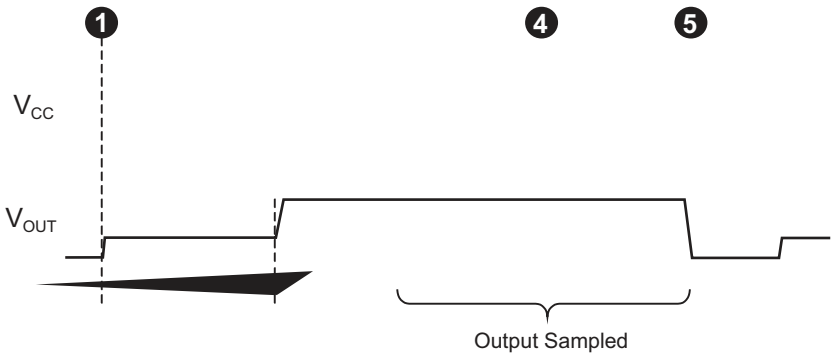

Figure 2: Continuous-Time Application, $B < B_{RP}$

This figure illustrates the use of a quick cycle for chopping V_{CC} in order to conserve battery power. Position 1, power is applied to the device. Position 2, the output assumes the correct state at a time prior to the maximum Power-On Time, $t_{PO(max)}$. The case shown is where the correct output state is HIGH. Position 3, $t_{PO(max)}$ has elapsed. The device output is valid. Position 4, after the output is valid, a control unit reads the output. Position 5, power is removed from the device.

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POWER DERATING

Power Derating

The device must be operated below the maximum junction temperature of the device, $T_{J(max)}$. Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J. (Thermal data is also available on the Allegro MicroSystems Web site.)

The Package Thermal Resistance, $R_{\theta JA}$, is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity, K, of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case, $R_{\theta JC}$, is relatively small component of $R_{\theta JA}$. Ambient air temperature, T_A, and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation, P_D), can be estimated. The following formulas represent the fundamental relationships used to estimate T_J, at P_D.

$$P_D = V_{IN} \times I_{IN} \qquad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \qquad (2)$$

$$T$$

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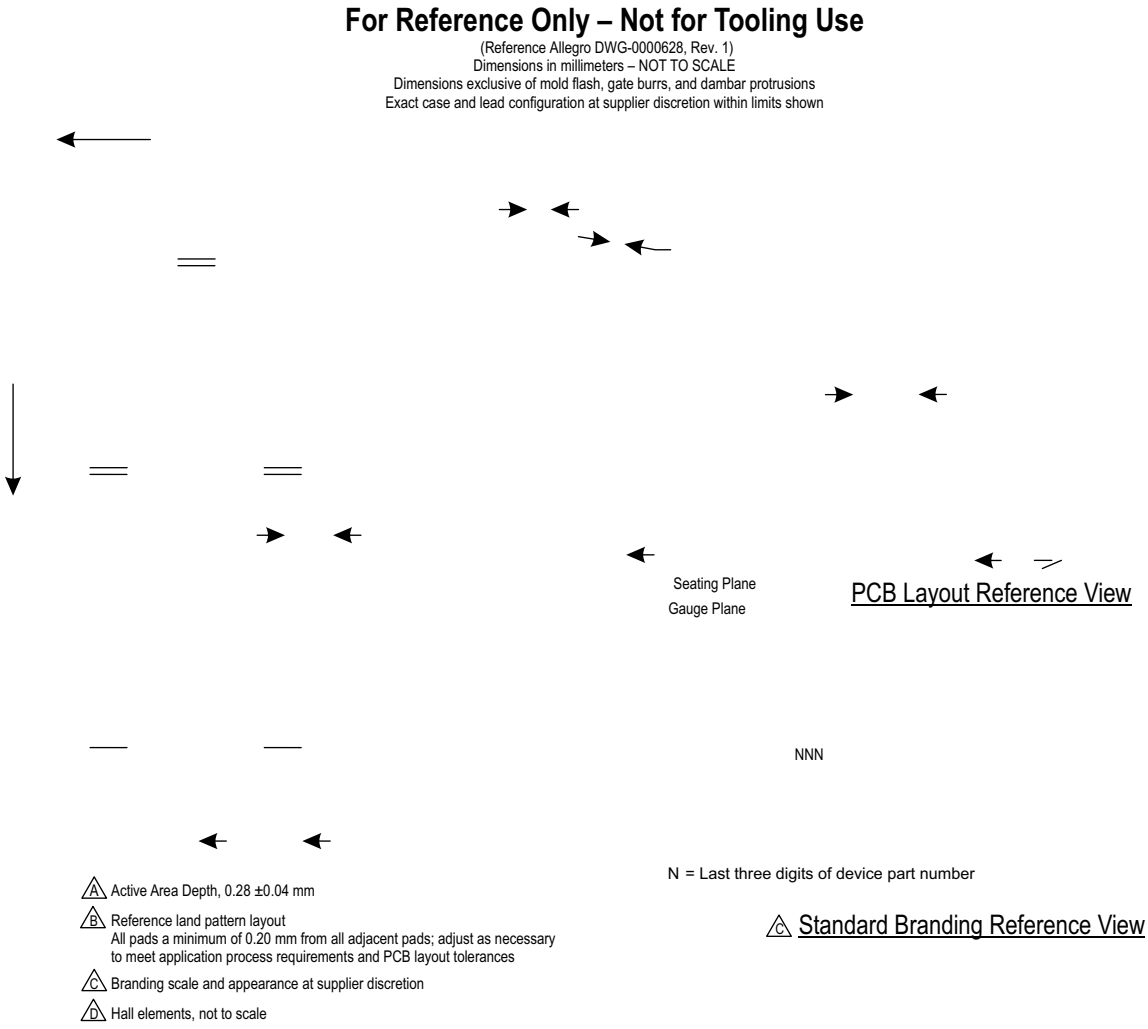

Figure 3: Package LH, 3-Pin SOT-23W

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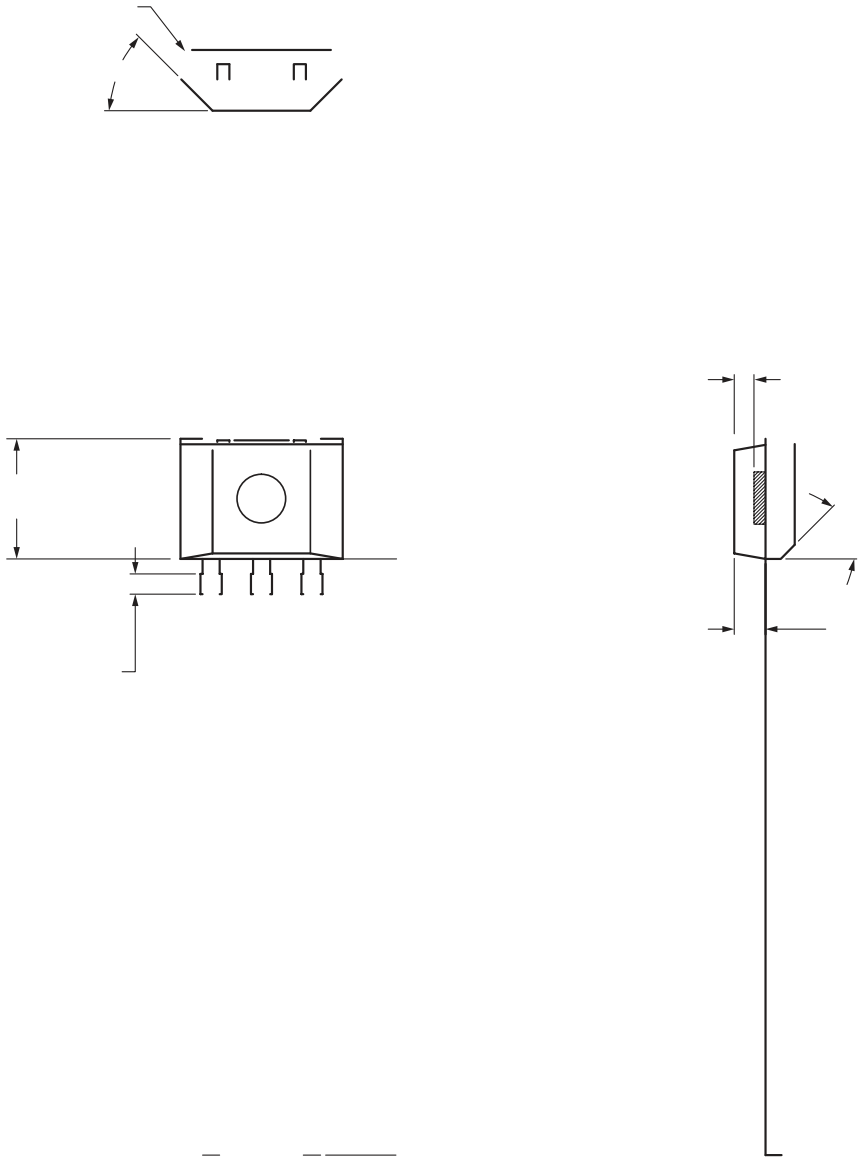

Figure 4: Package UA, 3-Pin SIP, Matrix Style

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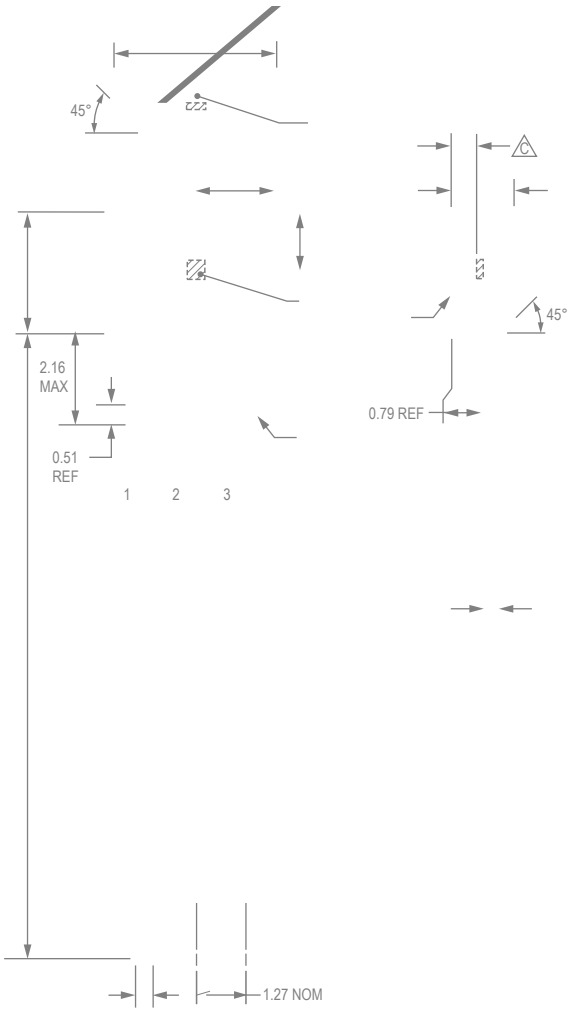

Figure 5: Package UA, 3-Pin SIP, Chopper Style

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Revision History

Number	Date	Description
10	May 29, 2012	Update UA package drawing
11	August 20, 2014	Revised Selection Guide, reformatted datasheet
12	January 1, 2015	Added LX option to Selection Guide
13	September 22, 2015	Corrected LH package Active Area Depth value; added AEC-Q100 qualification under Features and Benefits
14	November 4, 2016	Chopper-style UA package designated as not for new design
15	February 4, 2019	Updated Active Area Depth for UA matrix-style package, and minor editorial updates
16	February 12, 2020	Minor editorial updates
17	December 13, 2021	Updated package drawings and minor editorial updates

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