CY28442-2

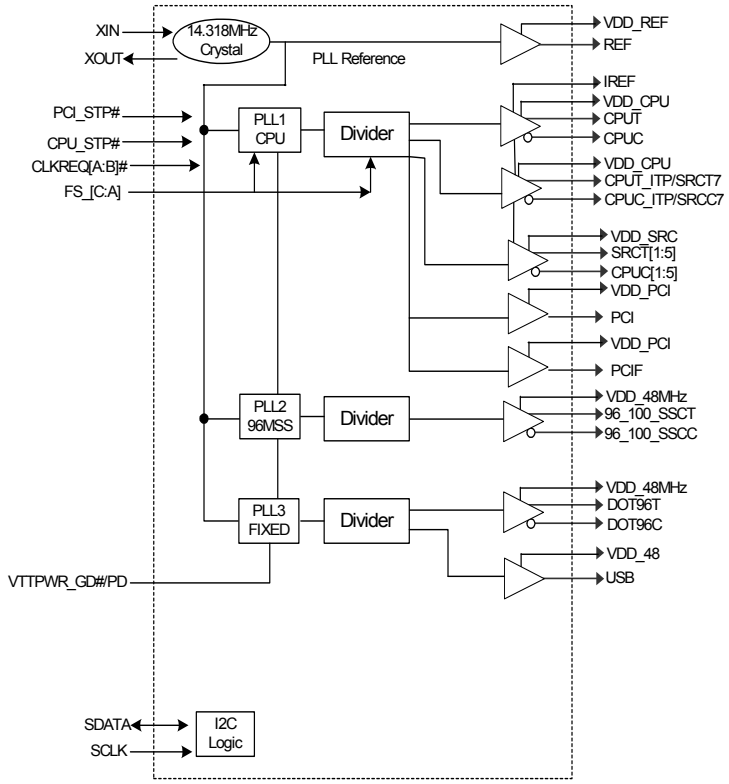
Clock Generator for Intel® Alviso Chipset

Features

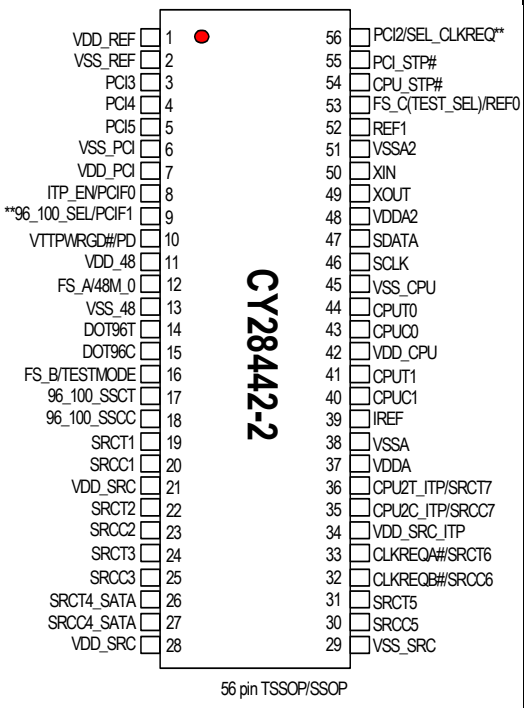
- **Compliant to Intel® CK410M**
- **Supports Intel Pentium-M CPU**
- **Selectable CPU frequencies**
- **Differential CPU clock pairs**
- **100-MHz differential SRC clocks**
- **96-MHz differential dot clock**
- **48-MHz USB clocks**
- **SRC clocks independently stoppable through CLKREQ#[A:B]**
- **96-/100-MHz Spreadable differential clock.**
- **33-MHz PCI clock**
- **Low-voltage frequency select input**
- **I^2C support with readback capabilities**
- **Ideal Lexmark Spread Spectrum profile for maximum electromagnetic interference (EMI) reduction**
- **3.3V power supply**
- **56-pin TSSOP package**

CPU	SRC	PCI	REF	DOT96	USB_48
x2 / x3	x5/6	x 6	x 2	x 2	x 1

Block Diagram



Pin Configuration



Pin Definitions

Pin No.	Name	Type	Description
1	VDD_REF	PWR	**3.3V power supply for output**
2	VSS_REF	GND	**Ground for outputs**.
33,32	CLKREQA#/SRCT6, CLKREQB#,SRCC6	I/O, PU	**3.3V LVTTL input for enabling assigned SRC clock (active LOW) or 100-MHz Serial Reference Clock.** Selectable through CLKREQA# defaults to enable/disable SRCT/C4, CLKREQB# defaults to enable/disable SRCT/C5. Assignment can be changed via SMBUS register Byte 8.
7	VDD_PCI	PWR	**3.3V power supply for outputs**.
6	VSS_PCI	GND	**Ground for outputs**.
3,4,5	PCI	O, SE	**33-MHz clock**
8	ITP_EN/PCIF0	I/O, SE	**3.3V LVTTL input to enable SRC7 or CPU2_ITP/33-MHz clock output.** (sampled on the VTT_PWRGD# assertion). 1 = CPU2_ITP, 0 = SRC7
9	PCIF1/96_100_SEL	I/O, PD,SE	**33-MHz clock/3.3V-tolerant input for 96_100M frequency selection** (sampled on the VTT_PWRGD# assertion). 1 = 100 MHz, 0 = 96 MHz
10	VTT_PWRGD#/PD	I, PU	**3.3V LVTTL input. This pin is a level sensitive strobe used to latch the FS_A, FS_B, FS_C and ITP_EN, 96MSS_SRC_SEL inputs, SEL_CLKREQ**. After VTT_PWRGD# (active LOW) assertion, this pin becomes a real-time input for asserting power-down (active HIGH).
11	VDD_48	PWR	**3.3V power supply for outputs**.
12	FS_A/48_M0	I/O	**3.3V-tolerant input for CPU frequency selection/fixed 48-MHz clock output**. *Refer to DC Electrical Specifications table for Vil_FS and Vih_FS specifications.*
13	VSS_48	GND	**Ground for outputs**.
14,15	DOT96T, DOT96C	O, DIF	**Fixed 96-MHz clock output**.
16	FS_B/TEST_MODE	I	**3.3V-tolerant input for CPU frequency selection**. Selects Ref/N or Tri-state when in test mode 0 = Tri-state, 1 = Ref/N *Refer to DC Electrical Specifications table for Vil_FS and Vih_FS specifications.*
17,18	96_100_SSC	O,DIF	**Differential 96-/100-MHz SS clock for flat-panel display**
19,20,22,23, 24,25,30,31	SRCT/C	O, DIF	**100-MHz Differential serial reference clocks**.
21,28	VDD_SRC	PWR	**3.3V power supply for outputs**.
34	VDD_SRC_ITP	PWR	**3.3V power supply for outputs**.
26,27	SRC4_SATAT, SRC4_SATAC	O, DIF	**Differential serial reference clock**. Recommended output for SATA.
29	VSS_SRC	GND	**Ground for outputs**.
36,35	CPUT2_ITP/SRCT7, CPUC2_ITP/SRCC7	O, DIF	**Selectable differential CPU or SRC clock output**. ITP_EN = 0 @ VTT_PWRGD# assertion = SRC7 ITP_EN = 1 @ VTT_PWRGD# assertion = CPU2
37	VDDA	PWR	**3.3V power supply for PLL**.
38	VSSA	GND	**Ground for PLL**.
39	IREF	I	**A precision resistor is attached to this pin**, which is connected to the internal current reference.
42	VDD_CPU	PWR	**3.3V power supply for outputs**.
44,43,41,40	CPUT/C	O, DIF	**Differential CPU clock outputs**.
45	VSS_CPU	GND	**Ground for outputs**.
46	SCLK	I	**SMBus-compatible SCLOCK**.
47	SDATA	I/O	**SMBus-compatible SDATA**.

Pin Definitions (continued)

Pin No.	Name	Type	Description
48	VDDA2	PWR	**3.3V power supply for PLL2**
49	XOUT	O, SE	**14.318-MHz crystal output**.
50	XIN	I	**14.318-MHz crystal input**.
51	VSSA2	GND	**Ground for PLL2**.
52	REF1	O	**Fixed 14.318 MHz clock output**.
53	FS_C_TEST_SEL/ REF0	I/O	**3.3V-tolerant input for CPU frequency selection/fixed 14.318 clock output**. Selects test mode if pulled to greater than 1.8V when VTT_PWRGD# is asserted LOW. *Refer to DC Electrical Specifications table for* V_{IL_FS},V_{IH_FS} *specifications.*
54	CPU_STP#	I, PU	**3.3V LVTTL input for CPU_STP# active LOW**.
55	PCI_STP#	I, PU	**3.3V LVTTL input for PCI_STP# active LOW**.
56	PCI2/SEL_CLKREQ	I/O, PD	**3.3V-tolerant input for CLKREQ pin selection/fixed 33-MHz clock output**. (sampled on the VTT_PWRGD# assertion). 1= pins 32,33 function as clk request pins, 0= pins 32,33 function as SRC outputs.

Table 1. Frequency Select Table FS_A, FS_B, and FS_C

FS_C	FS_B	FS_A	CPU	SRC	PCIF/PCI	REF0	DOT96	USB
1	0	1	100 MHz	100 MHz	33 MHz	14.318 MHz	96 MHz	48 MHz
0	0	1	133 MHz	100 MHz	33 MHz	14.318 MHz	96 MHz	48 MHz
0	1	1	166 MHz	100 MHz	33 MHz	14.318 MHz	96 MHz	48 MHz
0	1	0	200 MHz	100 MHz	33 MHz	14.318 MHz	96 MHz	48 MHz

Frequency Select Pins (FS_A, FS_B, and FS_C)

Host clock frequency selection is achieved by applying the appropriate logic levels to FS_A, FS_B, FS_C inputs prior to VTT_PWRGD# assertion (as seen by the clock synthesizer). Upon VTT_PWRGD# being sampled LOW by the clock chip (indicating processor VTT voltage is stable), the clock chip samples the FS_A, FS_B, and FS_C input values. For all logic levels of FS_A, FS_B, and FS_C, VTT_PWRGD# employs a one-shot functionality in that once a valid LOW on VTT_PWRGD# has been sampled, all further VTT_PWRGD#, FS_A, FS_B, and FS_C transitions will be ignored, except in test mode.

Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers, can be individually enabled or disabled. The registers associated with the Serial Data Interface initialize to their default setting upon power-up, and therefore use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required. The interface cannot be used during system operation for power management functions.

Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code, as described in *Table 2*.

The block write and block read protocol is outlined in *Table 3* while *Table 4* outlines the corresponding byte write and byte read protocol. The slave receiver address is 11010010 (D2h).

Table 2. Command Code Definition

Bit	Description
7	0 = Block read or block write operation, 1 = Byte read or byte write operation
(6:0)	Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be '0000000'

Table 3. Block Read and Block Write Protocol

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
8:2	Slave address – 7 bits	8:2	Slave address – 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code – 8 bits	18:11	Command Code – 8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Byte Count – 8 bits (Skip this step if I^2C_EN bit set)	20	Repeat start
28	Acknowledge from slave	27:21	Slave address – 7 bits
36:29	Data byte 1 – 8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
45:38	Data byte 2 – 8 bits	37:30	Byte Count from slave – 8 bits
46	Acknowledge from slave	38	Acknowledge
....	Data Byte /Slave Acknowledges	46:39	Data byte 1 from slave – 8 bits
....	Data Byte N – 8 bits	47	Acknowledge
....	Acknowledge from slave	55:48	Data byte 2 from slave – 8 bits
....	Stop	56	Acknowledge
		....	Data bytes from slave / Acknowledge
		....	Data Byte N from slave – 8 bits
		....	NOT Acknowledge
		....	Stop

Table 4. Byte Read and Byte Write Protocol

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
8:2	Slave address – 7 bits	8:2	Slave address – 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code – 8 bits	18:11	Command Code – 8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Data byte – 8 bits	20	Repeated start
28	Acknowledge from slave	27:21	Slave address – 7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		37:30	Data from slave – 8 bits
		38	NOT Acknowledge
		39	Stop

Control Registers

Byte 0: Control Register 0

Bit	@Pup	Name	Description
7	1	CPUT2_ITP/SRCT7 CPUC2_ITP/SRCC7	CPU[T/C]2_ITP/SRC[T/C]7 Output Enable 0 = Disable (Tri-state), 1 = Enable
6	1	SRC[T/C]6	SRC[T/C]6 Output Enable 0 = Disable (Tri-state), 1 = Enable
5	1	SRC[T/C]5	SRC[T/C]5 Output Enable 0 = Disable (Tri-state), 1 = Enable
4	1	SRC[T/C]4	SRC[T/C]4 Output Enable 0 = Disable (Tri-state), 1 = Enable
3	1	SRC[T/C]3	SRC[T/C]3 Output Enable 0 = Disable (Tri-state), 1 = Enable
2	1	SRC[T/C]2	SRC[T/C]2 Output Enable 0 = Disable (Tri-state), 1 = Enable
1	1	SRC[T/C]1	SRC[T/C]1 Output Enable 0 = Disable (Tri-state), 1 = Enable
0	1	RESERVED	RESERVED

Byte 1: Control Register 1

Bit	@Pup	Name	Description
7	1	PCIF0	PCIF0 Output Enable 0 = Disabled, 1 = Enabled
6	1	DOT_96T/C	DOT_96 MHz Output Enable 0 = Disable (Tri-state), 1 = Enabled
5	1	USB_48	USB_48 MHz Output Enable 0 = Disabled, 1 = Enabled
4	1	REF0	REF0 Output Enable 0 = Disabled, 1 = Enabled
3	1	REF1	REF1 Output Enable 0 = Disabled, 1 = Enabled
2	1	CPU[T/C]1	CPU[T/C]1 Output Enable 0 = Disable (Tri-state), 1 = Enabled
1	1	CPU[T/C]0	CPU[T/C]0 Output Enable 0 = Disable (Tri-state), 1 = Enabled
0	0	CPU	PLL1 (CPU PLL) Spread Spectrum Enable 0 = Spread off, 1 = Spread on

Byte 2: Control Register 2

Bit	@Pup	Name	Description
7	1	PCI5	PCI5 Output Enable 0 = Disabled, 1 = Enabled
6	1	PCI4	PCI4 Output Enable 0 = Disabled, 1 = Enabled
5	1	PCI3	PCI3 Output Enable 0 = Disabled, 1 = Enabled
4	1	PCI2	PCI2 Output Enable 0 = Disabled, 1 = Enabled
3	1	Reserved	Reserved, Set = 1
2	1	Reserved	Reserved, Set = 1
1	1	Reserved	Reserved, Set = 1
0	1	PCIF1	PCIF1 Output Enable 0 = Disabled, 1 = Enabled

Byte 3: Control Register 3

Bit	@Pup	Name	Description
7	0	SRC7	Allow control of SRC[T/C]7 with assertion of PCI_STP# or SW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP#
6	0	SRC6	Allow control of SRC[T/C]6 with assertion of PCI_STP# or SW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP#
5	0	SRC5	Allow control of SRC[T/C]5 with assertion of PCI_STP# or SW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP#
4	0	SRC4	Allow control of SRC[T/C]4 with assertion of PCI_STP# or SW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP#
3	0	SRC3	Allow control of SRC[T/C]3 with assertion of PCI_STP# or SW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP#
2	0	SRC2	Allow control of SRC[T/C]2 with assertion of PCI_STP# or SW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP#
1	0	SRC1	Allow control of SRC[T/C]1 with assertion of PCI_STP# or SW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP#
0	0	RESERVED	RESERVED

Byte 4: Control Register 4

Bit	@Pup	Name	Description
7	0	96_100_SSC	96_100_SSC Drive Mode 0 = Driven in PWRDWN, 1 = Tri-state
6	0	DOT96T/C	DOT_PWRDWN Drive Mode 0 = Driven in PWRDWN, 1 = Tri-state
5	0	RESERVED	RESERVED
4	0	PCIF1	Allow control of PCIF1 with assertion of SW and HW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP#
3	0	PCIF0	Allow control of PCIF0 with assertion of SW and HW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP#
2	1	CPU[T/C]2	Allow control of CPU[T/C]2 with assertion of CPU_STP# 0 = Free running, 1 = Stopped with CPU_STP#
1	1	CPU[T/C]1	Allow control of CPU[T/C]1 with assertion of CPU_STP# 0 = Free running, 1 = Stopped with CPU_STP#
0	1	CPU[T/C]0	Allow control of CPU[T/C]0 with assertion of CPU_STP# 0 = Free running, 1 = Stopped with CPU_STP#

Byte 5: Control Register 5

Bit	@Pup	Name	Description
7	0	SRC[T/C]	SRC[T/C] Stop Drive Mode 0 = Driven when PCI_STP# asserted,1 = Tri-state when PCI_STP# asserted
6	0	CPU[T/C]2	CPU[T/C]2 Stop Drive Mode 0 = Driven when CPU_STP# asserted,1 = Tri-state when CPU_STP# asserted
5	0	CPU[T/C]1	CPU[T/C]1 Stop Drive Mode 0 = Driven when CPU_STP# asserted,1 = Tri-state when CPU_STP# asserted
4	0	CPU[T/C]0	CPU[T/C]0 Stop Drive Mode 0 = Driven when CPU_STP# asserted,1 = Tri-state when CPU_STP# asserted
3	0	SRC[T/C][7:1]	SRC[T/C] PWRDWN Drive Mode 0 = Driven when PD asserted,1 = Tri-state when PD asserted
2	0	CPU[T/C]2	CPU[T/C]2 PWRDWN Drive Mode 0 = Driven when PD asserted,1 = Tri-state when PD asserted
1	0	CPU[T/C]1	CPU[T/C]1 PWRDWN Drive Mode 0 = Driven when PD asserted,1 = Tri-state when PD asserted

Byte 5: Control Register 5 (continued)

Bit	@Pup	Name	Description
0	0	CPU[T/C]0	CPU[T/C]0 PWRDWN Drive Mode 0 = Driven when PD asserted,1 = Tri-state when PD asserted

Byte 6: Control Register 6

Bit	@Pup	Name	Description
7	0	TEST_SEL	REF/N or Tri-state Select 0 = Tri-state, 1 = REF/N Clock
6	0	TEST_MODE	Test Clock Mode Entry Control 0 = Normal operation, 1 = REF/N or Tri-state mode,
5	0	RESERVED	RESERVED
4	1	REF	REF Output Drive Strength 0 = Low, 1 = High
3	1	PCI, PCIF and SRC clock outputs except those set to free running	SW PCI_STP Function 0=SW PCI_STP assert, 1= SW PCI_STP deassert When this bit is set to 0, all STOPPABLE PCI, PCIF and SRC outputs will be stopped in a synchronous manner with no short pulses. When this bit is set to 1, all STOPPED PCI, PCIF and SRC outputs will resume in a synchronous manner with no short pulses.
2	HW	FS_C	FS_C Reflects the value of the FS_C pin sampled on power-up 0 = FS_C was low during VTT_PWRGD# assertion
1	HW	FS_B	FS_B Reflects the value of the FS_B pin sampled on power-up 0 = FS_B was low during VTT_PWRGD# assertion
0	HW	FS_A	FS_A Reflects the value of the FS_A pin sampled on power-up 0 = FS_A was low during VTT_PWRGD# assertion

Byte 7: Vendor ID

Bit	@Pup	Name	Description
7	0	Revision Code Bit 3	Revision Code Bit 3
6	0	Revision Code Bit 2	Revision Code Bit 2
5	0	Revision Code Bit 1	Revision Code Bit 1
4	0	Revision Code Bit 0	Revision Code Bit 0
3	1	Vendor ID Bit 3	Vendor ID Bit 3
2	0	Vendor ID Bit 2	Vendor ID Bit 2
1	0	Vendor ID Bit 1	Vendor ID Bit 1
0	0	Vendor ID Bit 0	Vendor ID Bit 0

Byte 8: Control Register 8

Bit	@Pup	Name	Description
7	0	CLKREQ#B	SRC[T/C]7CLKREQ#B control 1 = SRC[T/C]7 stoppable by CLKREQ#B pin 0 = SRC[T/C]7 not controlled by CLKREQ#B pin
6	1	CLKREQ#B	SRC[T/C]5 CLKREQ#B control 1 = SRC[T/C]5 stoppable by CLKREQ#B pin 0 = SRC[T/C]5 not controlled by CLKREQ#B pin
5	0	CLKREQ#B	SRC[T/C]3 CLKREQ#B control 1 = SRC[T/C]3 stoppable by CLKREQ#B pin 0 = SRC[T/C]3 not controlled by CLKREQ#B pin
4	0	CLKREQ#B	SRC[T/C]1 CLKREQ#B control 1 = SRC[T/C]1 stoppable by CLKREQ#B pin 0 = SRC[T/C]1 not controlled by CLKREQ#B pin
3	0	RESERVED	RESERVED
2	1	CLKREQ#A	SRC[T/C]4 CLKREQ#A control 1 = SRC[T/C]4 stoppable by CLKREQ#A pin 0 = SRC[T/C]4 not controlled by CLKREQ#A pin

Byte 8: Control Register 8 (continued)

Bit	@Pup	Name	Description
1	0	CLKREQ#A	SRC[T/C]2 CLKREQ#A control 1 = SRC[T/C]2 stoppable by CLKREQ#A pin 0 = SRC[T/C]2 not controlled by CLKREQ#A pin
0	0	RESERVED	RESERVED

Byte 9: Control Register 9

Bit	@Pup	Name	Description
7	0	S3	96_100_SSC Spread Spectrum Selection table: S[3:0] SS% '0000' = –0.8%(Default value) '0001' = –1.0% '0010' = –1.25% '0011' = –1.5% '0100' = –1.75% '0101' = –2.0% '0110' = –2.5% '0111' = –0.5% '1000' = ±0.25% '1001' = ±0.4% '1010' = ±0.5% '1011' = ±0.6% '1100' = ±0.8% '1101' = ±1.0% '1110' = ±1.25% '1111' = ±1.5%
6	0	S2	
5	0	S1	
4	0	S0	
3	1	96_100 SEL	Software select 96_100_SSC output frequency, 0 = 96 MHz, 1 = 100 MHz.
2	1	96_100 Enable	96_100_SSC Enable, 0 = Disable, 1 = Enable.
1	1	96_100 SS Enable	96_100_SSC Spread spectrum enable. 0 = Disable, 1 = Enable.
0	0	96_100 SW HW	Select output frequency of 96_100_SSC via software or hardware 0 = Hardware, 1 = Software.

Byte 10: Control Register 10

Bit	@Pup	Name	Description
7	0	RESERVED	RESERVED
6	0	CLKREQ#B	SRC[T/C]4 CLKREQ#B control 1 = SRC[T/C]4 stoppable by CLKREQ#B pin 0 = SRC[T/C]4not controlled by CLKREQ#B pin
5	0	CLKREQ#B	SRC[T/C]2 CLKREQ#B control 1 = SRC[T/C]2 stoppable by CLKREQ#B pin 0 = SRC[T/C]2 not controlled by CLKREQ#B pin
4	0	RESERVED	RESERVED
3	0	CLKREQ#A	SRC[T/C]7CLKREQ#A control 1 = SRC[T/C]7 stoppable by CLKREQ#A pin 0 = SRC[T/C]7 not controlled by CLKREQ#A pin
2	0	CLKREQ#A	SRC[T/C]5 CLKREQ#A control 1 = SRC[T/C]5 stoppable by CLKREQ#A pin 0 = SRC[T/C]5 not controlled by CLKREQ#A pin
1	0	CLKREQ#A	SRC[T/C]3 CLKREQ#A control 1 = SRC[T/C]3 stoppable by CLKREQ#A pin 0 = SRC[T/C]3 not controlled by CLKREQ#A pin
0	0	CLKREQ#A	SRC[T/C]1 CLKREQ#A control 1 = SRC[T/C]1 stoppable by CLKREQ#A pin 0 = SRC[T/C]1 not controlled by CLKREQ#A pin

Table 5. Crystal Recommendations

Frequency (Fund)	Cut	Loading	Load Cap	Drive (max.)	Shunt Cap (max.)	Motional (max.)	Tolerance (max.)	Stability (max.)	Aging (max.)
14.31818 MHz	AT	Parallel	20 pF	0.1 mW	5 pF	0.016 pF	35 ppm	30 ppm	5 ppm

The CY28442-2 requires a Parallel Resonance Crystal. Substituting a series resonance crystal will cause the CY28442-2 to operate at the wrong frequency and violate the ppm specification. For most applications there is a 300-ppm frequency shift between series and parallel crystals due to incorrect loading.

Crystal Loading

Crystal loading plays a critical role in achieving low ppm performance. To realize low ppm performance, the total capacitance the crystal will see must be considered to calculate the appropriate capacitive loading (CL).

Figure 1 shows a typical crystal configuration using the two trim capacitors. An important clarification for the following discussion is that the trim capacitors are in series with the crystal not parallel. It's a common misconception that load capacitors are in parallel with the crystal and should be approximately equal to the load capacitance of the crystal. This is not true.

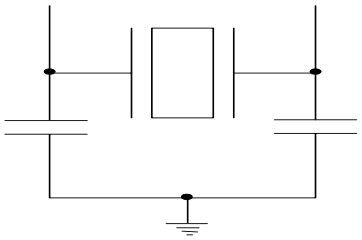


Figure 1. Crystal Capacitive Clarification

Calculating Load Capacitors

In addition to the standard external trim capacitors, trace capacitance and pin capacitance must also be considered to correctly calculate crystal loading. As mentioned previously, the capacitance on each side of the crystal is in series with the crystal. This means the total capacitance on each side of the crystal must be twice the specified crystal load capacitance (CL). While the capacitance on each side of the crystal is in series with the crystal, trim capacitors (Ce1,Ce2) should be calculated to provide equal capacitive loading on both sides.

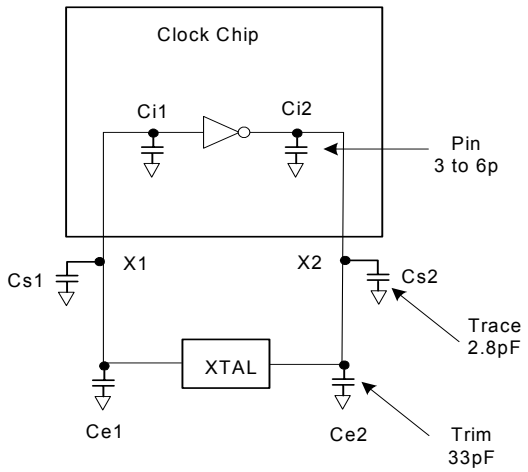


Figure 2. Crystal Loading Example

As mentioned previously, the capacitance on each side of the crystal is in series with the crystal. This mean the total capacitance on each side of the crystal must be twice the specified load capacitance (CL). While the capacitance on each side of the crystal is in series with the crystal, trim capacitors (Ce1,Ce2) should be calculated to provide equal capacitance loading on both sides.

Use the following formulas to calculate the trim capacitor values for Ce1 and Ce2.

Load Capacitance (each side)

$$Ce = 2 * CL - (Cs + Ci)$$

Total Capacitance (as seen by the crystal)

$$CLe = \frac{1}{\left(\frac{1}{Ce1 + Cs1 + Ci1} + \frac{1}{Ce2 + Cs2 + Ci2}\right)}$$

CL .....Crystal load capacitance

CLe ..... Actual loading seen by crystal using standard value trim capacitors

Ce ..... External trim capacitors

Cs .....Stray capacitance (terraced)

Ci ..... Internal capacitance (lead frame, bond wires etc.)

CLK_REQ[0:1]# Description

The CLKREQ#[A:B] signals are active LOW inputs used for clean enabling and disabling selected SRC outputs. The outputs controlled by CLKREQ#[A:B] are determined by the settings in register byte 8. The CLKREQ# signal is a de-bounced signal in that it's state must remain unchanged during two consecutive rising edges of SRCC to be recognized as a valid assertion or deassertion. (The assertion and deassertion of this signal is absolutely asynchronous).

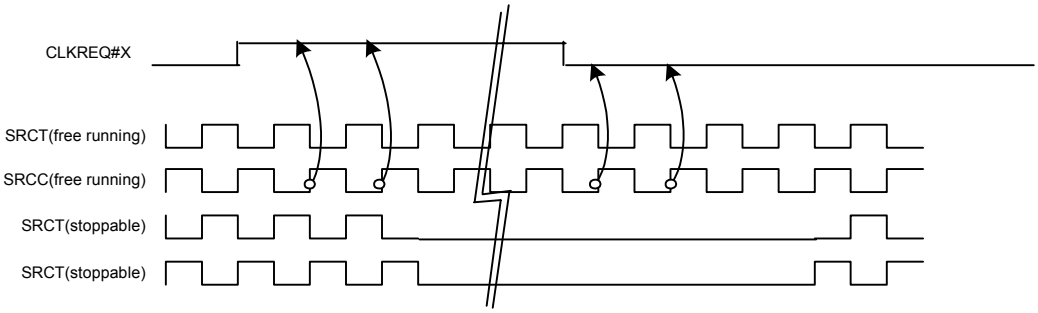


Figure 3. CLK_REQ#[A:B] Deassertion/Assertion Waveform

CLK_REQ[A:B]# Assertion (CLKREQ# -> LOW)

All differential outputs that were stopped are to resume normal operation in a glitch-free manner. The maximum latency from the assertion to active outputs is between 2 and 6 SRC clock periods (2 clocks are shown) with all SRC outputs resuming simultaneously. All stopped SRC outputs must be driven high within 10 ns of CLKREQ#[1:0] deassertion to a voltage greater than 200 mV.

CLK_REQ[A:B]# Deassertion (CLKREQ# -> HIGH)

The impact of deasserting the CLKREQ#[A:B] pins is that all SRC outputs that are set in the control registers to stoppable via deassertion of CLKREQ#[A:B] are to be stopped after their next transition. The final state of all stopped DIF signals is LOW, both SRCT clock and SRCC clock outputs will not be driven.

PD (Power-down) Clarification

The VTT_PWRGD# /PD pin is a dual-function pin. During initial power-up, the pin functions as VTT_PWRGD#. Once VTT_PWRGD# has been sampled LOW by the clock chip, the pin assumes PD functionality. The PD pin is an asynchronous active HIGH input used to shut off all clocks cleanly prior to shutting off power to the device. This signal is synchronized internal to the device prior to powering down the clock synthesizer. PD is also an asynchronous input for powering up the system. When PD is asserted HIGH, all clocks need to be driven to a LOW value and held prior to turning off the VCOs and the crystal oscillator.

PD (Power-down) Assertion

When PD is sampled HIGH by two consecutive rising edges of CPUC, all single-ended outputs will be held LOW on their next HIGH-to-LOW transition and differential clocks must held high or tri-stated (depending on the state of the control register drive mode bit) on the next diff clock# HIGH-to-LOW transition within 4 clock periods. When the SMBus PD drive mode bit corresponding to the differential (CPU, SRC, and DOT) clock output of interest is programmed to ‘0’, the clock output are held with “Diff clock” pin driven HIGH at 2 x Iref, and “Diff clock#” tri-state. If the control register PD drive mode bit corresponding to the output of interest is programmed to “1”, then both the “Diff clock” and the “Diff clock#” are tri-state. Note the example below shows CPUT = 133 MHz and PD drive mode = ‘1’ for all differential outputs. This diagram and description is applicable to valid CPU frequencies 100, 133, 166, 200, 266, 333, and 400 MHz. In the event that PD mode is desired as the initial power-on state, PD must be asserted HIGH in less than 10 μs after asserting Vtt_PwrGd#.

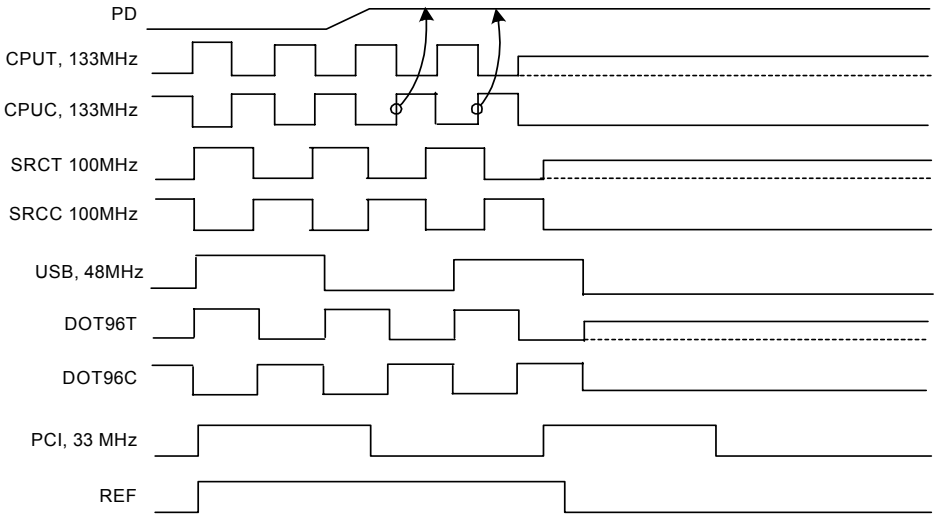


Figure 4. Power-down Assertion Timing Waveform

PD Deassertion

The power-up latency is less than 1.8 ms. This is the time from the deassertion of the PD pin or the ramping of the power supply until the time that stable clocks are output from the clock chip. All differential outputs stopped in a three-state condition resulting from power down will be driven high in less than 300 μs of PD deassertion to a voltage greater than 200 mV. After the clock chip's internal PLL is powered up and locked, all outputs will be enabled within a few clock cycles of each other. Below is an example showing the relationship of clocks coming up.

CPU_STP# Assertion

The CPU_STP# signal is an active LOW input used for synchronous stopping and starting the CPU output clocks while the rest of the clock generator continues to function. When the CPU_STP# pin is asserted, all CPU outputs that are set with the SMBus configuration to be stoppable via assertion of CPU_STP# will be stopped within two–six CPU clock periods after being sampled by two rising edges of the internal CPUC clock. The final states of the stopped CPU signals are CPUT = HIGH and CPUC = LOW. There is no change to the output drive current values during the stopped state. The CPUT is driven HIGH with a current value equal to 6 x (Iref), and the CPUC signal will be tri-stated.

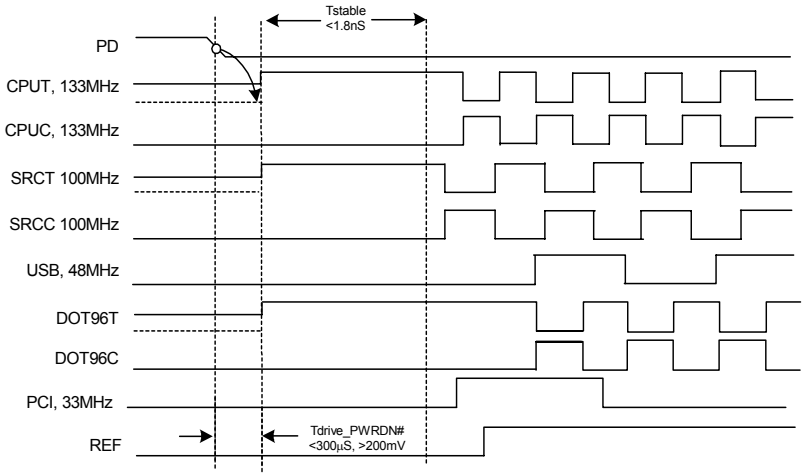


Figure 5. Power-down Deassertion Timing Waveform

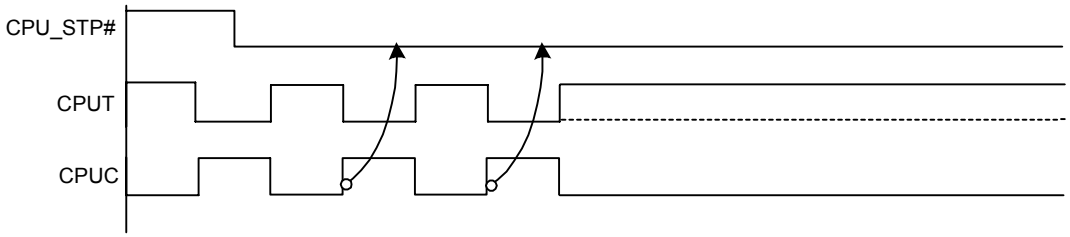


Figure 6. CPU_STP# Assertion Waveform

CPU_STP# Deassertion

The deassertion of the CPU_STP# signal will cause all CPU outputs that were stopped to resume normal operation in a synchronous manner. Synchronous manner meaning that no short or stretched clock pulses will be produce when the clock resumes. The maximum latency from the deassertion to active outputs is no more than two CPU clock cycles.

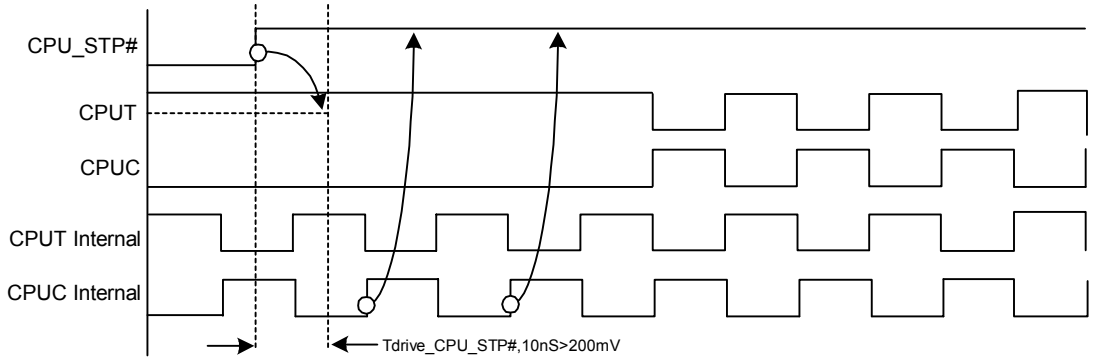


Figure 7. CPU_STP# Deassertion Waveform

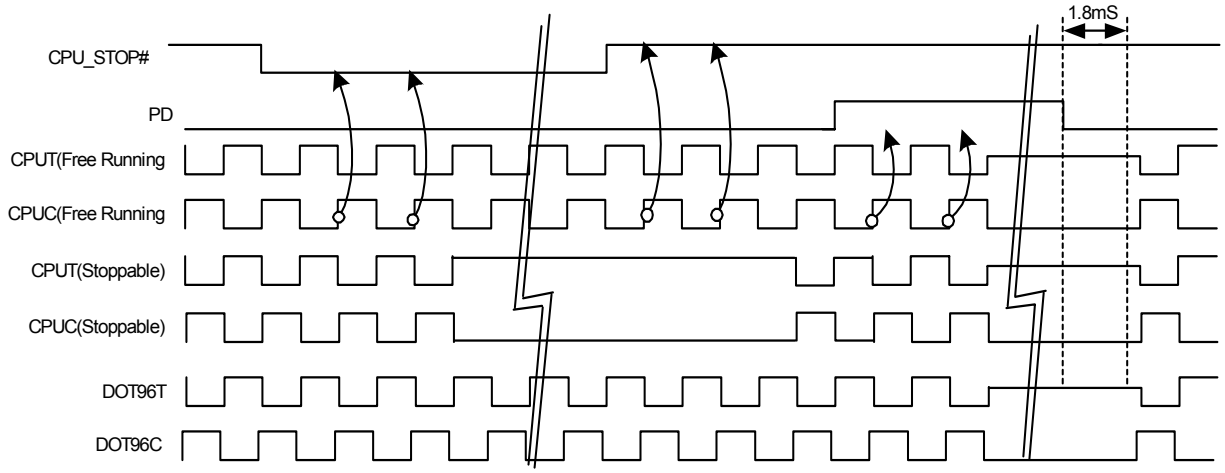


Figure 8. CPU_STP#= Driven, CPU_PD = Driven, DOT_PD = Driven

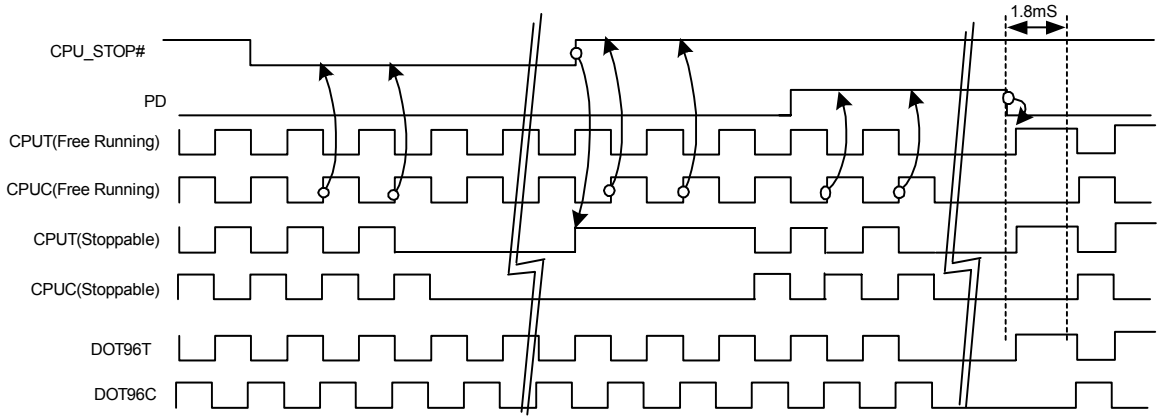


Figure 9. CPU_STP# = Tri-state, CPU_PD = Tri-state, DOT_PD = Tri-state

PCI_STP# Assertion

The PCI_STP# signal is an active LOW input used for synchronous stopping and starting the PCI outputs while the rest of the clock generator continues to function. The set-up time for capturing PCI_STP# going LOW is 10 ns (t_{SU}). (See *Figure 10.*) The PCIF clocks will not be affected by this pin if their corresponding control bit in the SMBus register is set to allow them to be free-running.

PCI_STP# Deassertion

The deassertion of the PCI_STP# signal will cause all PCI and stoppable PCIF clocks to resume running in a synchronous manner within two PCI clock periods after PCI_STP# transitions to a high level.

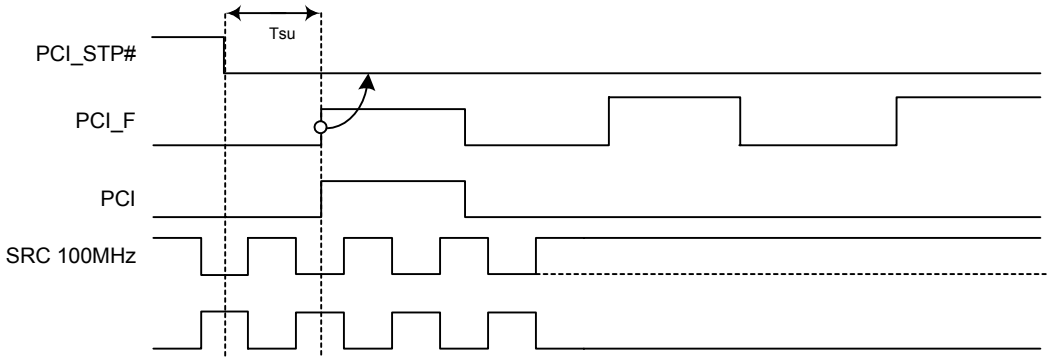


Figure 10. PCI_STP# Assertion Waveform

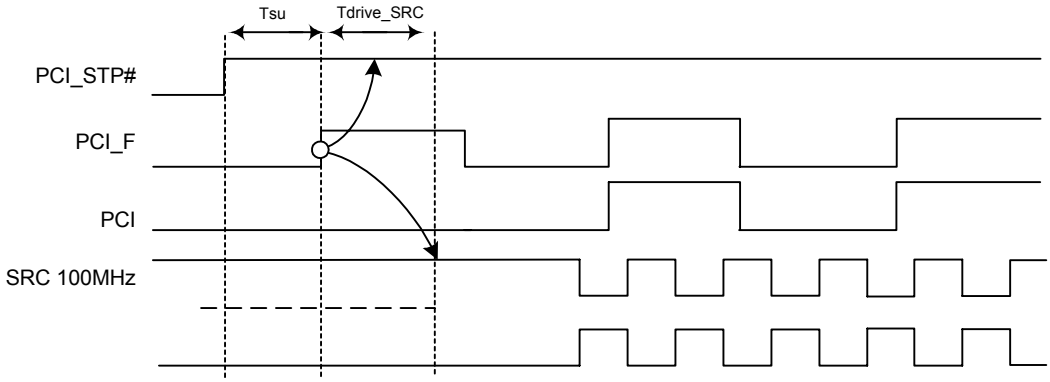


Figure 11. PCI_STP# Deassertion Waveform

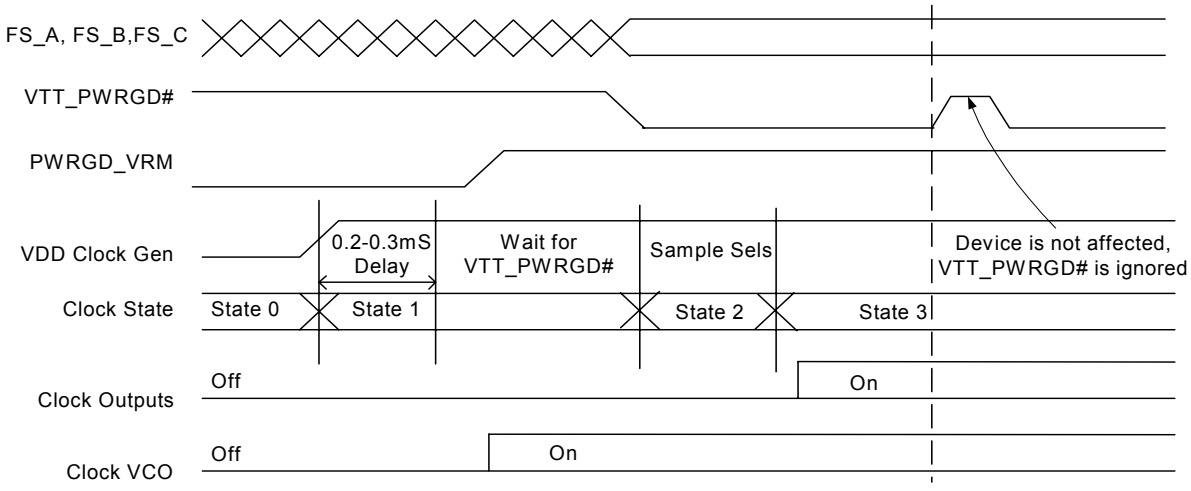


Figure 12. VTT_PWRGD# Timing Diagram

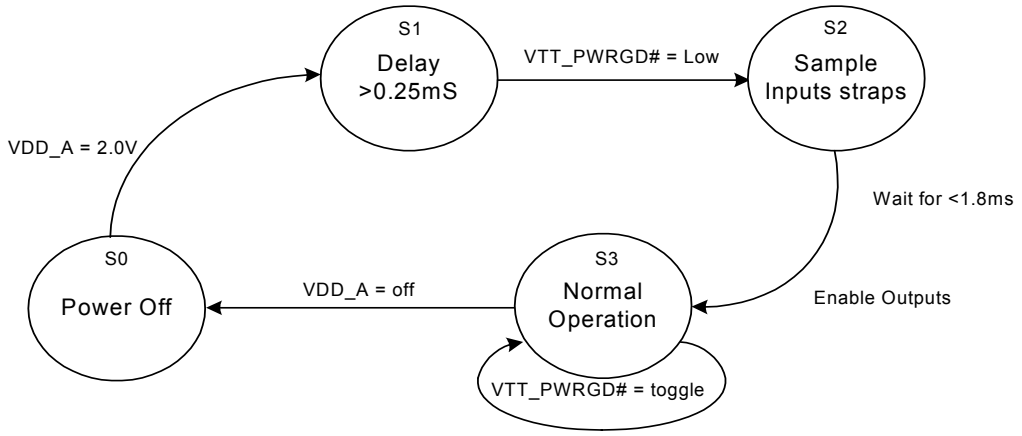


Figure 13. Clock Generator Power-up/Run State Diagram

Absolute Maximum Conditions

Parameter	Description	Condition	Min.	Max.	Unit
V_{DD}	Core Supply Voltage		–0.5	4.6	V
V_{DD_A}	Analog Supply Voltage		–0.5	4.6	V
V_{IN}	Input Voltage	Relative to V_{SS}	–0.5	V_{DD} + 0.5	VDC
T_S	Temperature, Storage	Non-functional	–65	150	°C
T_A	Temperature, Operating Ambient	Functional	0	85	°C
T_J	Temperature, Junction	Functional	–	150	°C
$Ø_{JC}$	Dissipation, Junction to Case	Mil-STD-883E Method 1012.1	–	20	°C/W
$Ø_{JA}$	Dissipation, Junction to Ambient	JEDEC (JESD 51)	–	60	°C/W
ESD_{HBM}	ESD Protection (Human Body Model)	MIL-STD-883, Method 3015	2000	–	V
UL-94	Flammability Rating	At 1/8 in.	V–0		
MSL	Moisture Sensitivity Level		1		
Multiple Supplies: The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.					

DC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
All VDDs	3.3V Operating Voltage	3.3 ± 5%	3.135	3.465	V
V_{ILI2C}	Input Low Voltage	SDATA, SCLK	–	1.0	V
V_{IHI2C}	Input High Voltage	SDATA, SCLK	2.2	–	V
V_{IL_FS}	FS_[A,B] Input Low Voltage		V_{SS} – 0.3	0.35	V
V_{IH_FS}	FS_[A,B] Input High Voltage		0.7	V_{DD} + 0.5	V
V_{ILFS_C}	FS_C Input Low Voltage		V_{SS} – 0.3	0.35	V
V_{IMFS_C}	FS_C Input Middle Voltage		0.7	1.8	V
V_{IHFS_C}	FS_C Input High Voltage		1.8	V_{DD} + 0.5	V
V_{IL}	3.3V Input Low Voltage		V_{SS} – 0.3	0.8	V
V_{IH}	3.3V Input High Voltage		2.0	V_{DD} + 0.3	V
I_{IL}	Input Low Leakage Current	Except internal pull-up resistors, $0 < V_{IN} < V_{DD}$	–5	5	µA
I_{IH}	Input High Leakage Current	Except internal pull-down resistors, $0 < V_{IN} < V_{DD}$	–	5	µA
V_{OL}	3.3V Output Low Voltage	I_{OL} = 1 mA	–	0.4	V
V_{OH}	3.3V Output High Voltage	I_{OH} = –1 mA	2.4	–	V
I_{OZ}	High-impedance Output Current		–10	10	µA
C_{IN}	Input Pin Capacitance		3	5	pF
C_{OUT}	Output Pin Capacitance		3	5	pF
L_{IN}	Pin Inductance		–	7	nH
V_{XIH}	Xin High Voltage		$0.7V_{DD}$	V_{DD}	V
V_{XIL}	Xin Low Voltage		0	$0.3V_{DD}$	V
$I_{DD3.3V}$	Dynamic Supply Current	At max. load and freq. per *Figure 15*	–	400	mA
$I_{PD3.3V}$	Power-down Supply Current	PD asserted, Outputs Driven	–	70	mA
$I_{PD3.3V}$	Power-down Supply Current	PD asserted, Outputs Tri-state	–	2	mA
I_{TRI}	Tri-state Current	Current in tri-state mode	–	100	mA

AC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
Crystal					
T_{DC}	XIN Duty Cycle	The device will operate reliably with input duty cycles up to 30/70 but the REF clock duty cycle will not be within specification	47.5	52.5	%
T_{PERIOD}	XIN Period	When XIN is driven from an external clock source	69.841	71.0	ns
T_R / T_F	XIN Rise and Fall Times	Measured between $0.3V_{DD}$ and $0.7V_{DD}$	–	10.0	ns
T_{CCJ}	XIN Cycle to Cycle Jitter	As an average over 1-μs duration	–	500	ps
L_{ACC}	Long-term Accuracy	Over 150 ms	–	300	ppm
CPU at 0.7V					
T_{DC}	CPUT and CPUC Duty Cycle	Measured at crossing point V_{OX}	45	55	%
T_{PERIOD}	100-MHz CPUT and CPUC Period	Measured at crossing point V_{OX}	9.997001	10.00300	ns
T_{PERIOD}	133-MHz CPUT and CPUC Period	Measured at crossing point V_{OX}	7.497751	7.502251	ns
T_{PERIOD}	166-MHz CPUT and CPUC Period	Measured at crossing point V_{OX}	5.998201	6.001801	ns
T_{PERIOD}	200-MHz CPUT and CPUC Period	Measured at crossing point V_{OX}	4.998500	5.001500	ns
$T_{PERIODSS}$	100-MHz CPUT and CPUC Period, SSC	Measured at crossing point V_{OX}	9.997001	10.05327	ns
$T_{PERIODSS}$	133-MHz CPUT and CPUC Period, SSC	Measured at crossing point V_{OX}	7.497751	7.539950	ns
$T_{PERIODSS}$	166-MHz CPUT and CPUC Period, SSC	Measured at crossing point V_{OX}	5.998201	6.031960	ns
$T_{PERIODSS}$	200-MHz CPUT and CPUC Period, SSC	Measured at crossing point V_{OX}	4.998500	5.026634	ns
$T_{PERIODAbs}$	100-MHz CPUT and CPUC Absolute period	Measured at crossing point V_{OX}	9.912001	10.08800	ns
$T_{PERIODAbs}$	133-MHz CPUT and CPUC Absolute period	Measured at crossing point V_{OX}	7.412751	7.587251	ns
$T_{PERIODAbs}$	166-MHz CPUT and CPUC Absolute period	Measured at crossing point V_{OX}	5.913201	6.086801	ns
$T_{PERIODAbs}$	200-MHz CPUT and CPUC Absolute period	Measured at crossing point V_{OX}	4.913500	5.086500	ns
$T_{PERIODSSAbs}$	100-MHz CPUT and CPUC Absolute period, SSC	Measured at crossing point V_{OX}	9.912001	10.13827	ns
$T_{PERIODSSAbs}$	133-MHz CPUT and CPUC Absolute period, SSC	Measured at crossing point V_{OX}	7.412751	7.624950	ns
$T_{PERIODSSAbs}$	166-MHz CPUT and CPUC Absolute period, SSC	Measured at crossing point V_{OX}	5.913201	6.116960	ns
$T_{PERIODSSAbs}$	200-MHz CPUT and CPUC Absolute period, SSC	Measured at crossing point V_{OX}	4.913500	5.111634	ns
T_{CCJ}	CPUT/C Cycle to Cycle Jitter	Measured at crossing point V_{OX}	–	85	ps
T_{CCJ2}	CPU2_ITP Cycle to Cycle Jitter	Measured at crossing point V_{OX}	–	125	ps
T_{SKEW2}	CPU2_ITP to CPU0 Clock Skew	Measured at crossing point V_{OX}	–	150	ps
T_R / T_F	CPUT and CPUC Rise and Fall Time	Measured from V_{OL} = 0.175 to V_{OH} = 0.525V	175	700	ps
T_{RFM}	Rise/Fall Matching	Determined as a fraction of $2*(T_R - T_F)/(T_R + T_F)$	–	20	%
ΔT_R	Rise Time Variation		–	125	ps
ΔT_F	Fall Time Variation		–	125	ps
V_{HIGH}	Voltage High	Math averages *Figure 15*	660	850	mV
V_{LOW}	Voltage Low	Math averages *Figure 15*	–150	–	mV
V_{OX}	Crossing Point Voltage at 0.7V Swing		250	550	mV

AC Electrical Specifications (continued)

Parameter	Description	Condition	Min.	Max.	Unit
V_{OVS}	Maximum Overshoot Voltage		–	V_{HIGH} + 0.3	V
V_{UDS}	Minimum Undershoot Voltage		–0.3	–	V
V_{RB}	Ring Back Voltage	See *Figure 15*. Measure SE	–	0.2	V
SRC					
T_{DC}	SRCT and SRCC Duty Cycle	Measured at crossing point V_{OX}	45	55	%
T_{PERIOD}	100-MHz SRCT and SRCC Period	Measured at crossing point V_{OX}	9.997001	10.00300	ns
$T_{PERIODSS}$	100-MHz SRCT and SRCC Period, SSC	Measured at crossing point V_{OX}	9.997001	10.05327	ns
$T_{PERIODAbs}$	100-MHz SRCT and SRCC Absolute Period	Measured at crossing point V_{OX}	9.872001	10.12800	ns
$T_{PERIODSSAbs}$	100-MHz SRCT and SRCC Absolute Period, SSC	Measured at crossing point V_{OX}	9.872001	10.17827	ns
T_{SKEW}	Any SRCT/C to SRCT/C Clock Skew	Measured at crossing point V_{OX}	–	100	ps
T_{CCJ}	SRCT/C Cycle to Cycle Jitter	Measured at crossing point V_{OX}	–	125	ps
L_{ACC}	SRCT/C Long Term Accuracy	Measured at crossing point V_{OX}	–	300	ppm
T_R / T_F	SRCT and SRCC Rise and Fall Time	Measured from V_{OL} = 0.175 to V_{OH} = 0.525V	175	700	ps
T_{RFM}	Rise/Fall Matching	Determined as a fraction of $2*(T_R - T_F)/(T_R + T_F)$	–	20	%
ΔT_R	Rise TimeVariation		–	125	ps
ΔT_F	Fall Time Variation		–	125	ps
V_{HIGH}	Voltage High	Math averages *Figure 15*	660	850	mV
V_{LOW}	Voltage Low	Math averages *Figure 15*	–150	–	mV
V_{OX}	Crossing Point Voltage at 0.7V Swing		250	550	mV
V_{OVS}	Maximum Overshoot Voltage		–	V_{HIGH} + 0.3	V
V_{UDS}	Minimum Undershoot Voltage		–0.3	–	V
V_{RB}	Ring Back Voltage	See *Figure 15*. Measure SE	–	0.2	V
PCI/PCIF					
T_{DC}	PCI Duty Cycle	Measurement at 1.5V	45	55	%
T_{PERIOD}	Spread Disabled PCIF/PCI Period	Measurement at 1.5V	29.99100	30.00900	ns
$T_{PERIODSS}$	Spread Enabled PCIF/PCI Period, SSC	Measurement at 1.5V	29.9910	30.15980	ns
$T_{PERIODAbs}$	Spread Disabled PCIF/PCI Period	Measurement at 1.5V	29.49100	30.50900	ns
$T_{PERIODSSAbs}$	Spread Enabled PCIF/PCI Period, SSC	Measurement at 1.5V	29.49100	30.65980	ns
T_{HIGH}	PCIF and PCI high time	Measurement at 2.4V	12.0	–	ns
T_{LOW}	PCIF and PCI low time	Measurement at 0.4V	12.0	–	ns
T_R / T_F	PCIF/PCI rising and falling Edge Rate	Measured between 0.8V and 2.0V	1.0	4.0	V/ns
T_{SKEW}	Any PCI clock to Any PCI clock Skew	Measurement at 1.5V	–	500	ps
T_{CCJ}	PCIF and PCI Cycle to Cycle Jitter	Measurement at 1.5V	–	500	ps
DOT					
T_{DC}	DOT96T and DOT96C Duty Cycle	Measured at crossing point V_{OX}	45	55	%
T_{PERIOD}	DOT96T and DOT96C Period	Measured at crossing point V_{OX}	10.41354	10.41979	ns
$T_{PERIODAbs}$	DOT96T and DOT96C Absolute Period	Measured at crossing point V_{OX}	10.16354	10.66979	ns
T_{CCJ}	DOT96T/C Cycle to Cycle Jitter	Measured at crossing point V_{OX}	–	250	ps
L_{ACC}	DOT96T/C Long Term Accuracy	Measured at crossing point V_{OX}	–	100	ppm

AC Electrical Specifications (continued)

Parameter	Description	Condition	Min.	Max.	Unit
T_R / T_F	DOT96T and DOT96C Rise and Fall Time	Measured from V_{OL} = 0.175 to V_{OH} = 0.525V	175	700	ps
T_{RFM}	Rise/Fall Matching	Determined as a fraction of $2*(T_R - T_F)/(T_R + T_F)$	–	20	%
ΔT_R	Rise Time Variation		–	125	ps
ΔT_F	Fall Time Variation		–	125	ps
V_{HIGH}	Voltage High	Math averages *Figure 15*	660	850	mV
V_{LOW}	Voltage Low	Math averages *Figure 15*	–150	–	mV
V_{OX}	Crossing Point Voltage at 0.7V Swing		250	550	mV
V_{OVS}	Maximum Overshoot Voltage		–	V_{HIGH} + 0.3	V
V_{UDS}	Minimum Undershoot Voltage		–0.3	–	V
V_{RB}	Ring Back Voltage	See *Figure 15*. Measure SE	–	0.2	V
USB					
T_{DC}	Duty Cycle	Measurement at 1.5V	45	55	%
T_{PERIOD}	Period	Measurement at 1.5V	20.83125	20.83542	ns
$T_{PERIODAbs}$	Absolute Period	Measurement at 1.5V	20.48125	21.18542	ns
T_{HIGH}	USB high time	Measurement at 2.4V	8.094	10.036	ns
T_{LOW}	USB low time	Measurement at 0.4V	7.694	9.836	ns
T_R / T_F	Rising and Falling Edge Rate	Measured between 0.8V and 2.0V	1.0	2.0	V/ns
T_{CCJ}	Cycle to Cycle Jitter	Measurement at 1.5V	–	350	ps
REF					
T_{DC}	REF Duty Cycle	Measurement at 1.5V	45	55	%
T_{PERIOD}	REF Period	Measurement at 1.5V	69.8203	69.8622	ns
$T_{PERIODAbs}$	REF Absolute Period	Measurement at 1.5V	68.82033	70.86224	ns
T_R / T_F	REF Rising and Falling Edge Rate	Measured between 0.8V and 2.0V	1.0	4.0	V/ns
T_{CCJ}	REF Cycle to Cycle Jitter	Measurement at 1.5V	–	1000	ps
ENABLE/DISABLE and SET-UP					
T_{STABLE}	Clock Stabilization from Power-up		–	1.8	ms
T_{SS}	Stopclock Set-up Time		10.0	–	ns
T_{SH}	Stopclock Hold Time		0	–	ns

Test and Measurement Set-up

For PCI Single-ended Signals and Reference

The following diagram shows the single-ended PCI outputs.

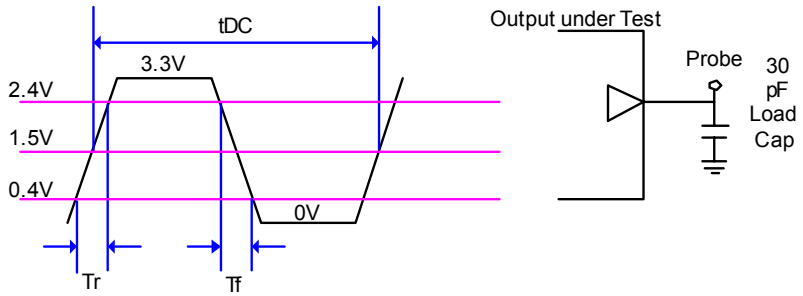


Figure 14. Single-ended PCI Lumped Load Configuration

The following diagram shows the test load configuration for the differential CPU and SRC outputs.

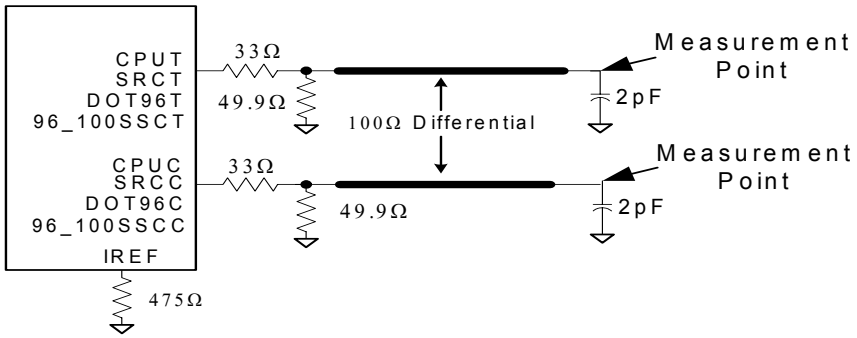


Figure 15. 0.7V Differential Clock Load Configuration

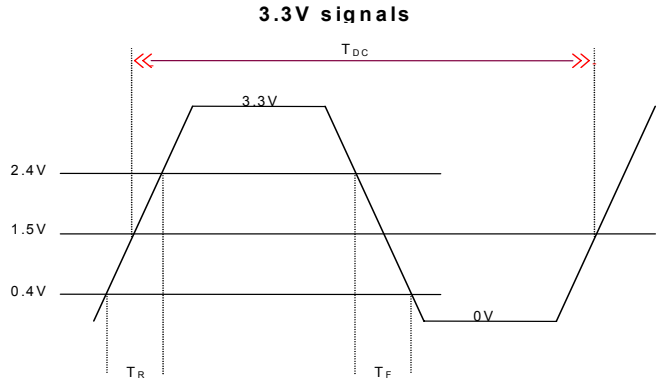


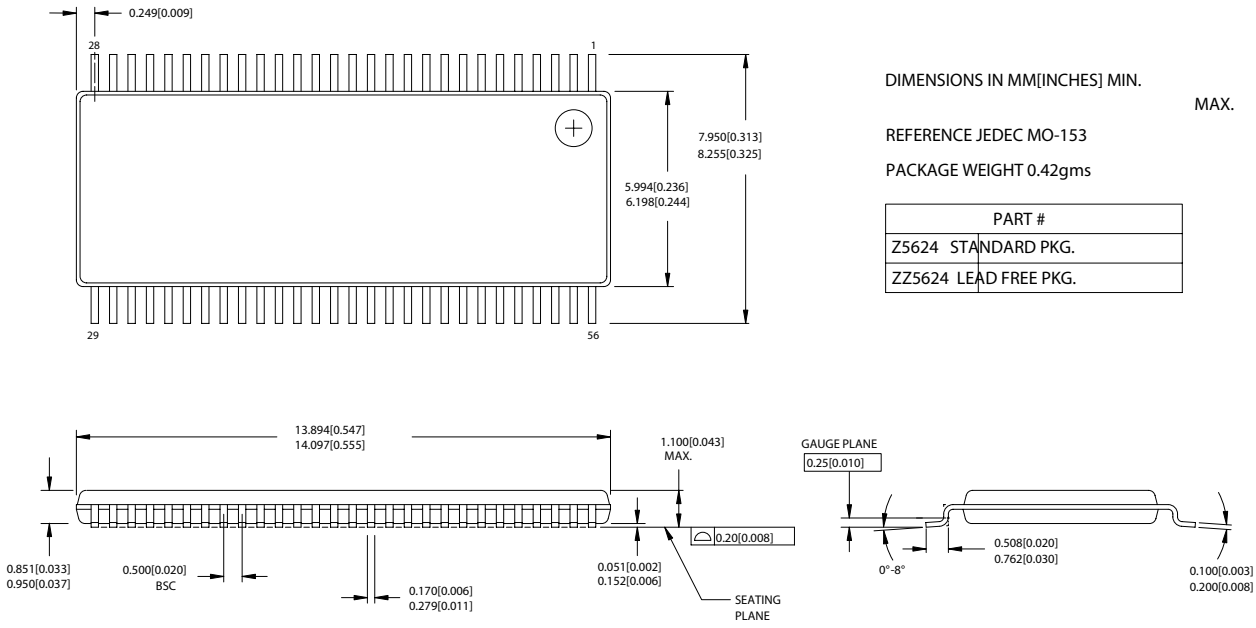
Figure 16. Single-ended Output Signals (for AC Parameters Measurement)

Ordering Information

Part Number	Package Type	Product Flow
Lead-free		
CY28442ZXC-2	56-pin TSSOP	Commercial, 0° to 85°C
CY28442ZXC-2T	56-pin TSSOP – Tape and Reel	Commercial, 0° to 85°C

Package Diagrams

56-Lead Thin Shrunk Small Outline Package, Type II (6 mm x 12 mm) Z56



Document History Page

Document Title: CY28442-2 Clock Generator for Intel® Alviso Chipset Document Number: 38-07691				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	237627	See ECN	RGL	New Data Sheet
*A	378059	See ECN	RGL	Minor Change: Corrected typo in the label of the diagram from PLL4 to PLL3
*B	390510	See ECN	RGL	Removed Preliminary