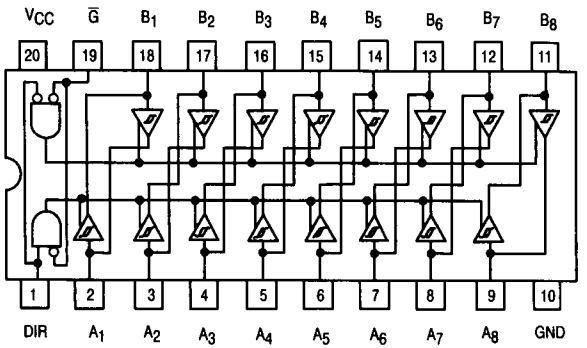
MOTOROLA

Octal Bus Transceivers With 3-State Outputs (Non-Inverting)

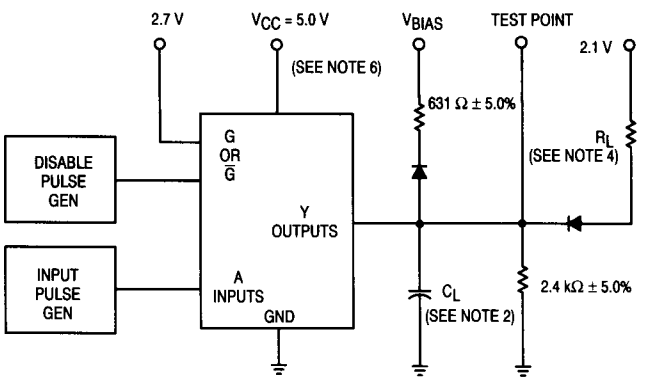
ELECTRICALLY TESTED PER:
MPG54LS645

The 54LS645 is designed for asynchronous two-way communication between data buses. Control function implementation minimizes external timing requirements. The 54LS645 allows data transmission from A bus to B or from the B bus depending upon the logic level of the direction control (DIR) input. Enable input ($\overline{G}$) can disable the device so that the buses are effectively isolated.

LOGIC DIAGRAM



AC TEST CIRCUIT



REFERENCE NOTES ON PAGE 5-415

Military 54LS645

AVAILABLE AS:

1) JAN: N/A
2) SMD: N/A
3) 883: 54LS645/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: R
CERFLAT: S
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 732-03	FLATS 737-02	LCC 756A-02	BURN-IN (COND. A)
DIR	1	1	1	V_{CC}
A_1	2	2	2	V_{CC}
A_2	3	3	3	V_{CC}
A_3	4	4	4	V_{CC}
A_4	5	5	5	V_{CC}
A_5	6	6	6	V_{CC}
A_6	7	7	7	V_{CC}
A_7	8	8	8	V_{CC}
A_8	9	9	9	V_{CC}
GND	10	10	10	GND
B_8	11	11	11	V_{CC}
B_7	12	12	12	V_{CC}
B_6	13	13	13	V_{CC}
B_5	14	14	14	V_{CC}
B_4	15	15	15	V_{CC}
B_3	16	16	16	V_{CC}
B_2	17	17	17	V_{CC}
B_1	18	18	18	V_{CC}
$\overline{G}$	19	19	19	V_{CC}
V_{CC}	20	20	20	V_{CC}

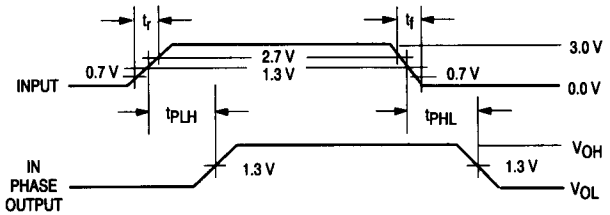
BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

TRUTH TABLE

Control Inputs		Operation
$\overline{G}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

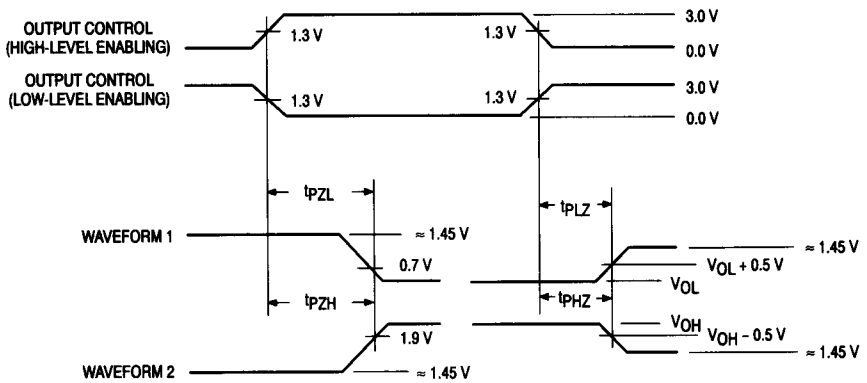
VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



SWITCH POSITIONS

Symbol	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS



NOTES:

1. The pulse generator has the following characteristics: V_{GEN} = 3.0 V, PRR = 1.0 MHz, t_r = 15 ns, $t_f \leq$ 6.0 ns, Z_{OUT} = 50 Ω.
2. C_L = 50 pF ± 10%, including scope probe, wiring and stray capacitance.
3. Voltage measurements are to be made with respect to network ground terminal.
4. R_L = 110 Ω ± 5.0%.
5. Clock pulse characteristics: $t_{p(CLK)}$ = 20 ns, t_{setup} = 20 ns.
6. The diode and resistor shown within the dotted area are optional. When the diode and resistor are used. V_{BIAS} shall be 5.5 V for all tests except for t_{PHZ}; for t_{PHZ} test, V_{BIAS} shall be – 0.6 V.
7. All diodes are 1N3064 or equivalent.

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+ 25°C		+ 125°C		– 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.4		2.4		2.4		V	V_{CC} = 4.5 V, I_{OH} = – 3.0 mA, V_{IH} = 2.0 V (other inputs are open), DIR = 2.0 V or 0.7 V, $\overline{G}$ = 0.7 V.
V_{OH1}	Logical "1" Output Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V, I_{OH} = – 12 mA, V_{IH} = 2.0 V (other inputs are open), DIR = 2.0 V or 0.5 V, $\overline{G}$ = 0.5 V.
V_{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 12 mA, V_{IL} = 0.7 V (other inputs are open), DIR = 2.0 V or 0.7 V, $\overline{G}$ = 0.7 V.
V_{IC}	Input Clamping Voltage		– 1.5					V	V_{CC} = 4.5 V, I_{IN} = – 18 mA, all other inputs are open, $\overline{G}$ = open, 5.5 V or (– 18 mA).
I_{IH}	Logical "1" Input Current		20		20		20	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs are open, $\overline{G}$ = open, 5.5 V or (2.7 V).
I_{IHH}	Logical "1" Input Current		100		100		100	µA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, other inputs are open, $\overline{G}$ = open or 5.5 V.
I_{IL}	Logical "0" Input Current	– 5.0	– 240	– 5.0	– 240	– 5.0	– 240	µA	V_{CC} = 5.5 V, V_{IN} = 0.4 V, other inputs are open, DIR = (0.4 V), 4.5 V or GND, $\overline{G}$ = open, 5.5 V or (0.4 V).
I_{OS}	Output Short Circuit Current	– 40	– 225	– 40	– 225	–40	– 225	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V (other inputs are open), V_{OUT} = GND, DIR = 5.5 V or GND, $\overline{G}$ = GND.
I_{OZH}	Output Off Current High		20		20		20	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs are open.
I_{OZL}	Output Off Current Low		– 200		– 200		– 200	µA	V_{CC} = 5.5 V, V_{IL} = 0.4 V, other inputs are open.
I_{CCH}	Power Supply Current		70		70		70	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V (all inputs), $\overline{G}$ & DIR = GND.
I_{CCL}	Power Supply Current		90		90		90	mA	V_{CC} = 5.5 V, V_{IN} = GND (all inputs).
I_{CCZ}	Power Supply Current Off		95		95		95	mA	V_{CC} = 5.5 V, all inputs are open, $\overline{G}$ = 5.5 V.
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V_{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 5.0 V, V_{INL} = 0.4 V, and V_{INH} = 2.4 V.

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		− 55°C			
	Switching Parameters:	Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL} t_{PHL}	Propagation Delay /Data-Output A to B	2.0 —	17 15	2.0 —	22 19	2.0 —	22 19	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 110 Ω. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.
t_{PLH} t_{PLH}	Propagation Delay /Data-Output A to B	2.0 —	17 15	2.0 —	22 19	2.0 —	22 19	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 110 Ω. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.
t_{PLZ} t_{PLZ}	Propagation Delay Output Disable Time, $\overline{G}$, DIR to A	2.0 —	30 25	2.0 —	39 34	2.0 —	39 34	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 110 Ω. V_{CC} = 5.0 V, C_L = 5.0 pF.
t_{PHZ} t_{PHZ}	Propagation Delay Output Disable Time, $\overline{G}$, DIR to A	2.0 —	30 25	2.0 —	39 34	2.0 —	39 34	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 110 Ω. V_{CC} = 5.0 V, C_L = 5.0 pF.
t_{PZL} t_{PZL}	Propagation Delay Output Enable Time $\overline{G}$, DIR to A	2.0 —	45 40	2.0 —	58 53	2.0 —	58 53	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 110 Ω. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.
t_{PZH} t_{PZH}	Propagation Delay Output Enable Time $\overline{G}$, DIR to A	2.0 —	45 40	2.0 —	58 53	2.0 —	58 53	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 110 Ω. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.