LM48560 Evaluation Board

This user's guide describes the characteristics, operation, and use of the LM48560 Evaluation Module (EVM). A complete schematic diagram, printed-circuit board layouts, and bill of materials (BOM) are included in this document.

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1 Introduction

To help the user investigate and evaluate the LM48560 performance and capabilities, a fully-populated demonstration board was created. Figure 1 shows the board. Connected to an external power supply (2.7 V ≤ V_{DD} ≤ 5.5 V) and a signal source, the LM48560 demonstration board easily exercises the amplifier's features.

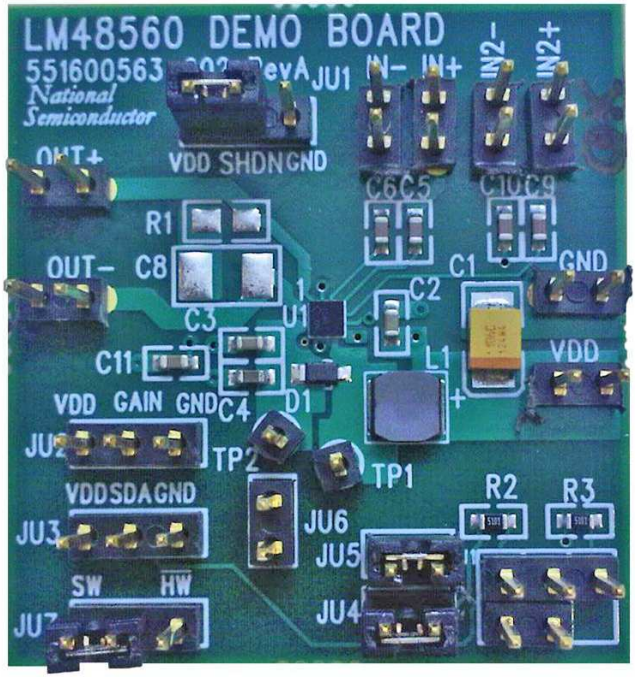

Figure 1. LM48560 Demonstration Board

2 Quick Start Guide

2.1 Hardware Mode

Use the following steps to set up the EVM board in hardware mode:

Step 1. Short pins 1 (VDD) and 2 of JU1 for normal operation.

Step 2. Short pins 2 and 3 (GND) of JU7 to set the device in hardware mode.

Step 3. Short pins 1 and 2 of JU3 to select IN2 and enable boost.

Step 4. Short pins 1 and 2 of JU2 for gain of 30 V/V.

Step 5. Connect a power supply (2.7 V–5.5 V) and ground reference, respectively, to the VDD and GND headers on the demo board.

Step 6. Connect a differential audio input to IN2+ and IN2–.

Step 7. Power on the board and observe the output on OUT+ and OUT–.

2.2 Software Mode

Use the following steps to set up the EVM board in software mode:

Step 1. Short pins 1 (VDD) and 2 of JU1 for normal operation.

Step 2. Short pins 1 (VDD) and 2 of JU7 to set the device in software mode

Step 3. Short pins 1 (VDD) and 2 of JU3 to select IN2 and enable boost.

Step 4. Short pins 2 and 3 (GND) of JU2 for 24-dB gain.

Step 5. Connect a power supply (2.7 V–5.5 V) and ground reference, respectively, to the VDD and GND headers on the demo board.

Step 6. Connect a differential audio input on IN2+ and IN2–.

Step 7. Connect a USB/I^2C board to the LM48560 demo board.

Step 8. Connect the USB/I^2C board to a PC.

Step 9. Turn on the power supply.

Step 10. Launch the LM48560 software GUI (SNAC051).

Step 11. Verify that the bottom left corner of the GUI reads “USB Connected ALL ACK”. If the GUI reads “USB I/O error NAK” the device has not been acknowledged, please double check connections.

Step 12. Select the following:

- INPUT SELECT = INPUT 1
- BOOST = ON
- TURN ON TIME = NORMAL
- GAIN = 0dB

3 General Description

The LM48560 is a high-voltage, high-efficiency, Class H driver for ceramic speakers and piezo actuators. The LM48560’s Class H architecture offers significant power savings compared to traditional Class AB amplifiers. The device provides 30Vp-p output drive while consuming just 4 mA of quiescent current from a 3.6-V supply.

The LM48560 features two fully-differential inputs with separate gain settings, and a selectable control interface. In software control mode, the gain control and device modes are configured through the I^2C interface. In hardware control mode, the gain and input mux are configured through a pair of logic inputs. The LM48560 has a low power shutdown mode that reduces quiescent current consumption to 0.1 µA.

4 Board Features

The LM48560 high voltage class H ceramic speaker driver with automatic level control demonstration board has all of the necessary connections using 0.100” headers connectors to apply the power supply voltage, audio input signals, and audio output (speaker). The amplified audio signal is only available on the audio output header.

5 Operating Conditions

Table 1 lists the temperature range and supply voltage conditions for the EVM.

Table 1. Operating Conditions

Temperature Range: $T_{MIN} \le T_A \le T_{MAX}$	$-40°C \le T_A \le 85°C$
Supply Voltage (V_{DD})	$2.7\ V \le V_{DD} \le 5.5\ V$

6 Application Circuit Schematic

Figure 2 shows the demonstration board schematic.

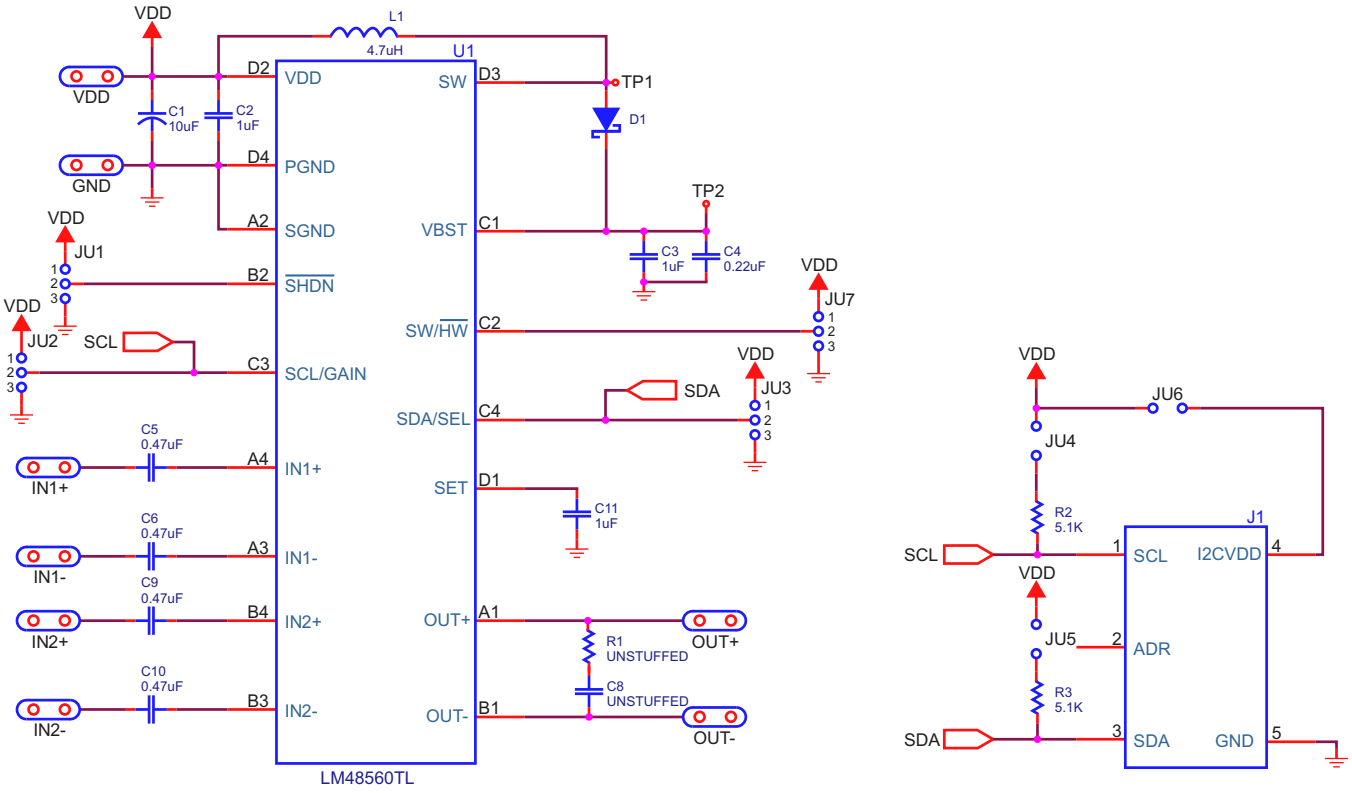

Figure 2. Demonstration Board Schematic

7 Connections

Table 2 describes the connections on the EVM board.

Table 2. Connections

Designator	Function	Notes
VDD	VDD	Power supply
GND	GND	Ground reference
OUT+	OUTPUT	Positive output terminal
OUT–	OUTPUT	Negative output terminal
IN1+	INPUT 1	Positive input terminal 1
IN1–	INPUT 1	Negative input terminal 1
IN2+	INPUT 2	Positive input terminal 2
IN2–	INPUT 2	Negative input terminal 2
JU1	Shutdown	Short pin 1 (VDD) and pin 2 for normal operation. Short pin 2 and pin 3 (GND) for device shutdown.
JU2	SCL/Gain Select	Hardware mode: Short pin 2 to pin 1 (VDD) for higher gain. Short pin 2 to pin 3 (GND) for lower gain. Software mode: Keep pins 1-3 open. Pin 2 = SCL for I^2C communication
JU3	SDA/Input Select	Hardware mode: Short pin 2 to pin 1 (VDD) to select IN2. Short pin 2 to pin 3 (GND) to select IN1. Software mode: Keep pins 1-3 open. Pin 2 = SDA for I^2C communication
JU4	SCL Pullup	Short JU4 to connect pullup resistor to VDD. Open to use external I^2C supply voltage
JU5	SDA pullup	Short JU5 to connect pullup resistor to VDD. Open to use external I^2C supply voltage
JU6	I^2C VDD	Short JU6 to use VDD as I^2C VDD. Open to use external I^2C supply voltage
JU7	SW/HW	Hardware Mode: Short pins 2 and 3 (GND) Software Mode: Short pins 1 (VDD) and 2

8 PCB Layout Guidelines

Minimize trace impedance of the power, ground and all output traces for optimum performance. Voltage loss due to trace resistance between the LM48560 and the load results in decreased output power and efficiency. Trace resistance between the power supply and ground has the same effect as a poorly regulated supply; increased ripple and reduced peak output power. Use wide traces for power supply inputs and amplifier outputs to minimize losses due to trace resistance, as well as route heat away from the device. Proper grounding improves audio performance, minimizes crosstalk between channels and prevents switching noise from interfering with the audio signal. Use of power and ground planes is recommended.

Place all digital components and route digital signal traces as far as possible from analog components and traces. Do not run digital and analog traces in parallel on the same PCB layer. If digital and analog signal lines must cross either over or under each other, ensure that they cross in a perpendicular fashion.

9 Bill Of Materials

Table 3 details the EVM BOM.

Table 3. LM48560 Bill of Materials

Designator	Description	Part Number	Footprint	Value	Qty
U1	LM48560TL IC	LM48560TL/NOPB			1
C1	CAP_TANTALUM-CHIP_B	TPSB106K016R0800	B case	10uF	1
C4	CAP_0603_CERAMIC-CHIP	GCM188R71H224KA64D	603	0.22uF	1
C8	1210 Ceramic Capacitor	C3225X7R1E685K	1210	UNSTUFFED	0
C2, C3	CAP_0603_CERAMIC-CHIP	GRM188R61E105KA12D	603	1uF	2
C11	CAP_0603_CERAMIC-CHIP	GRM188R71H104KA93D	603	0.1uF	1
C5,C6,C9,C10	CAP_0603_CERAMIC-CHIP	GRM188R61A474KA61D	603	0.47uF	4
D1	Schottky Diode	PD3S120L-7	PowerDI 323	20V	1
GND, IN+, IN-, IN2+, IN2-, JU4, JU5, JU6, OUT+, OUT-, VDD	2-pin Header	87220-2	100 mil		11
J1	2-pin Header + 3-pin Header		100 mil		2
JU1, JU2, JU3, JU7	3-pin Header	87220-3	100 mil		4
L1	INDUCTOR_CHIP_1515_MURATA	LQH44PN4R7MP0L	1515	4.7uH	1
R1	RES_0805_CHIP	ERJ-P06J100V	805	UNSTUFFED	0
R2, R3	603 Thick Film Resistor	CRCW06035K10JNEA	603	5.1k	2
TP1, TP2	TESTPOINT-PC5000	87220-1	100 mil		2

10 Example Initialization Register Setting

Table 4 provides an initialization register setting example.

Table 4. Example Initialization Register Setting

Register	Data	Data (Binary)	Description
0x00h	0x01h	00000011	Turn on time = 15 ms. Input 1 selected. Boost enabled, device enabled
0x01h	0x00h	00000000	Release time = 0.5 s. Attack time = 0.83 ms. Voltage limit disabled. (Release/Attack time depends on Cset, more details in LM48560 datasheet (SNAS513))
0x02h	0x00h	00000000	Gain = 21 dB (Gain depends on boost enable/disable)

11 Demonstration Board PCB Layout

Figure 3 through Figure 11 show the different layers used to create the LM48560 demonstration board. Figure 3 is the top silk screen that shows component locations on the board's top surface. Figure 5 is the top layer, Figure 6 is layer 2, Figure 7 is layer 3, and Figure 11 is the bottom layer.

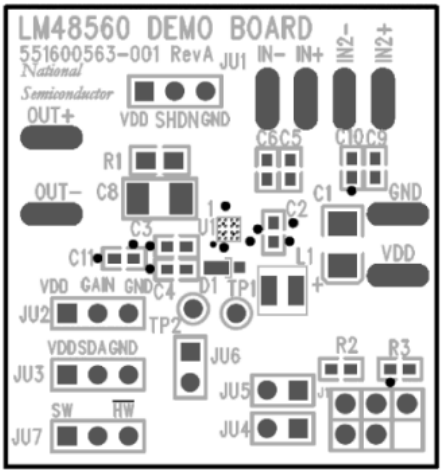

Figure 3. Top Silk Screen

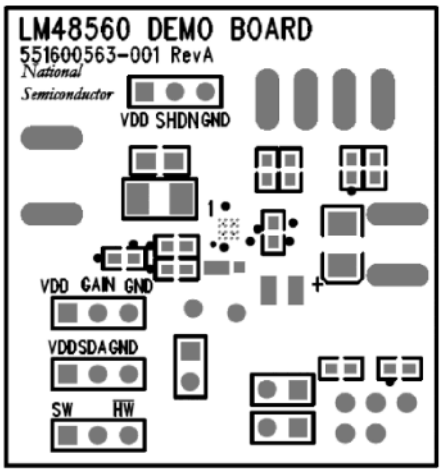

Figure 4. Solder Mask Top

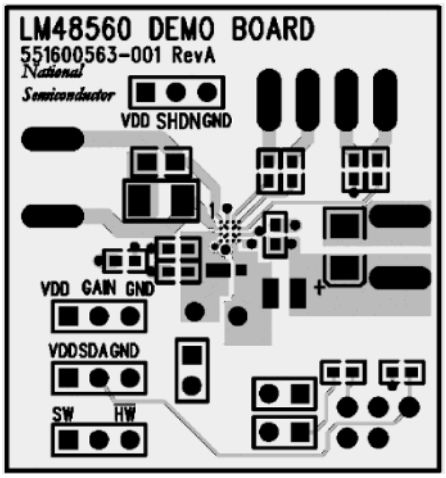

Figure 5. Top Layer

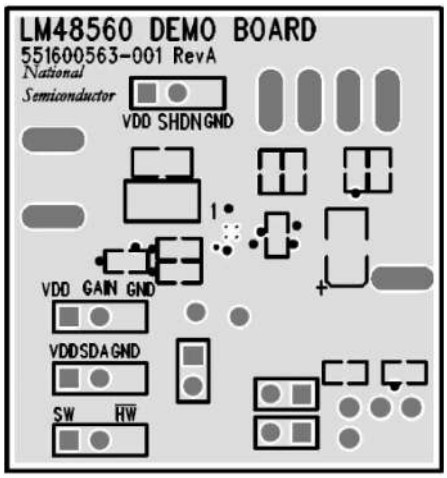

Figure 6. Layer 2

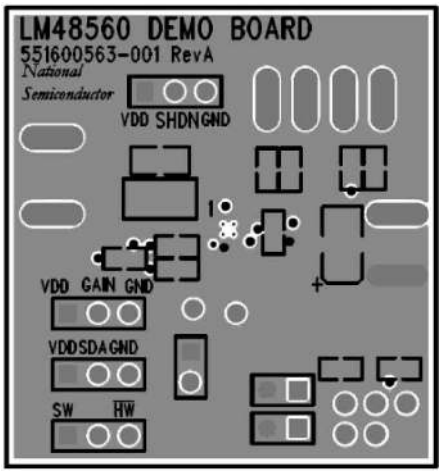

Figure 7. Layer 3

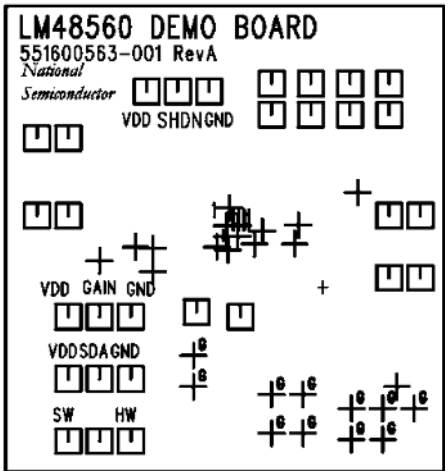

Figure 8. Drill Drawing

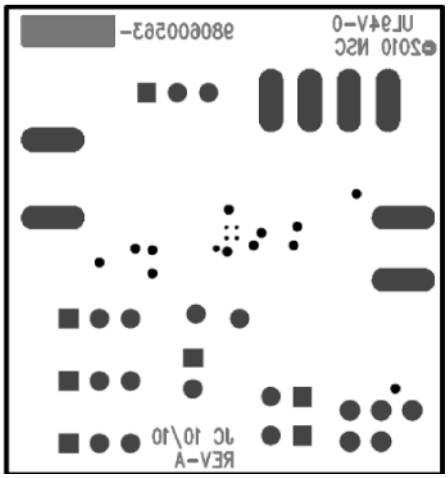

Figure 9. Silk Bottom

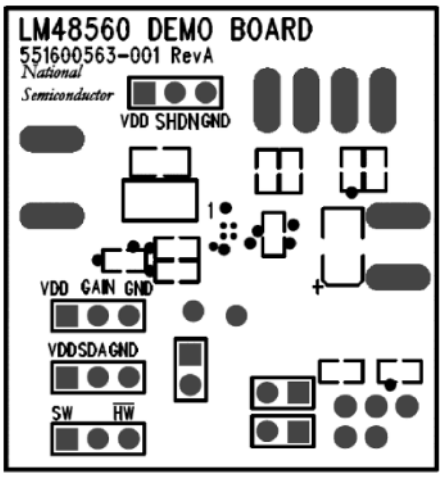

Figure 10. Solder Mask Bottom

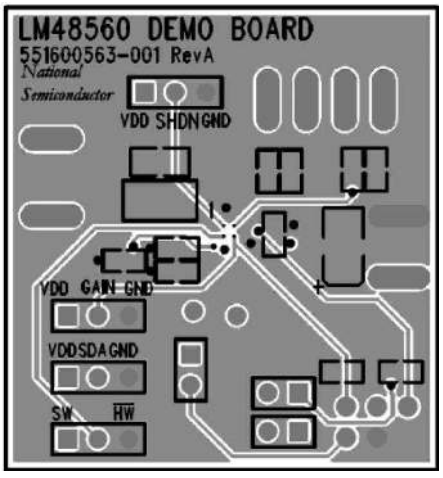

Figure 11. Bottom Layer

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      Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

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- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

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3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210*

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Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

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2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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