TAS5342LA 100-W Stereo Digital Amplifier Power Stage

1 Features

- Total Power Output (Bridge Tied Load)
  - 2 × 100 W at 10% THD+N Into 4 Ω
  - 2 × 80 W at 10% THD+N Into 6 Ω
  - 2 × 65 W at 10% THD+N Into 8 Ω
- Total Power Output (Single Ended)
  - 4 × 40 W at 10% THD+N Into 3 Ω
  - 4 × 30 W at 10% THD+N Into 4 Ω
- Total Power Output (Parallel Mode)
  - 1 × 200 W at 10% THD+N Into 2 Ω
  - 1 × 160 W at 10% THD+N Into 3 Ω
- >110 dB SNR (A-Weighted With TAS5518 Modulator)
- <0.1% THD+N (1 W, 1 kHz)
- Supports PWM Frame Rates of 192 kHz to 432 kHz
- Resistor-Programmable Current Limit
- Integrated Self-Protection Circuitry, Including:
  - Under Voltage Protection
  - Overtemperature Warning and Error
  - Overload Protection
  - Short-Circuit Protection
  - PWM Activity Detector
- Standalone Protection Recovery
- Power-On Reset (POR) to Eliminate System Power-Supply Sequencing
- High-Efficiency Power Stage (>90%) With 110-mΩ Output MOSFETs
- Thermally Enhanced Package 44-Pin HTSSOP (DDV)
- Error Reporting, 3.3-V and 5-V Compliant
- EMI Compliant When Used With Recommended System Design

2 Applications

- Mini/Micro Audio System
- DVD Receiver
- Home Theater

3 Description

The TAS5342LA is a high-performance, integrated stereo digital amplifier power stage designed to drive a 4-Ω bridge-tied load (BTL) at up to 100 W per channel with low-harmonic distortion, low-integrated noise, and low-idle current.

The TAS5342LA has a complete protection system integrated on-chip, safeguarding the device against a wide range of fault conditions that could damage the system. These protection features are short-circuit protection, over-current protection, under voltage protection, over temperature protection, and a loss of PWM signal (PWM activity detector).

A power-on-reset (POR) circuit is used to eliminate power-supply sequencing that is required for most power-stage designs.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TAS5342LA	HTSSOP (44)	14.00 mm × 6.10 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

BTL Output Power vs Supply Voltage

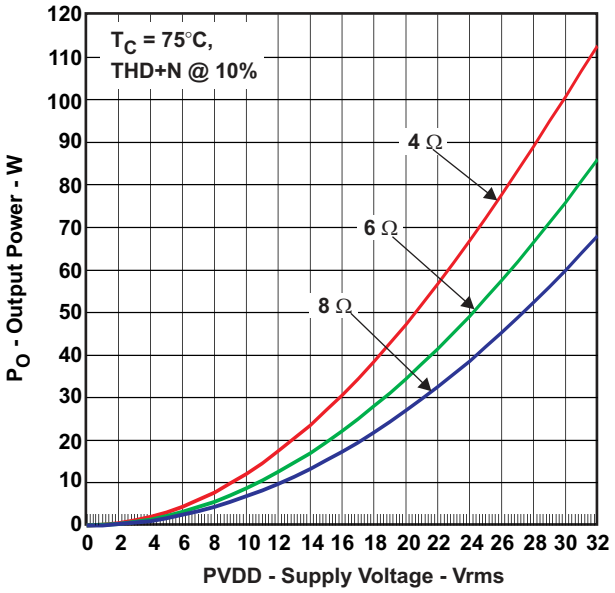


Table of Contents

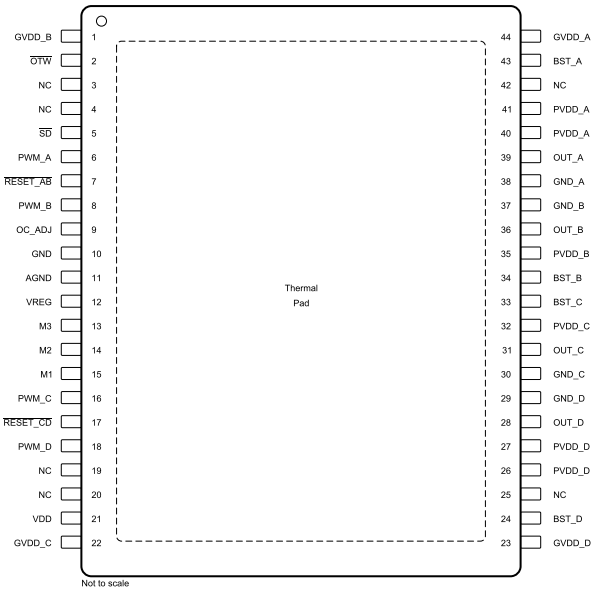
4 Revision History

Changes from Original (November 2008) to Revision A **Page**

- Added *Pin Configuration and Functions*, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted the *Ordering Information* table; see the POA at the end of the datasheet. ... 5
- Added the *Thermal Information* table ... 5

5 Pin Configuration and Functions

DDV Package
44-Pin HTTSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	11	P	Analog ground
BST_A	43	P	Bootstrap pin, A-Side
BST_B	34	P	Bootstrap pin, B-Side
BST_C	33	P	Bootstrap pin, C-Side
BST_D	24	P	Bootstrap pin, D-Side
GND	10	P	Ground
GND_A	38	P	Power ground for half-bridge A
GND_B	37	P	Power ground for half-bridge B
GND_C	30	P	Power ground for half-bridge C
GND_D	29	P	Power ground for half-bridge D
GVDD_A	44	P	Gate-drive voltage supply; A-Side
GVDD_B	1	P	Gate-drive voltage supply; B-Side
GVDD_C	22	P	Gate-drive voltage supply; C-Side
GVDD_D	23	P	Gate-drive voltage supply; D-Side
M1	15	I	Mode selection pin (LSB)
M2	14	I	Mode selection pin
M3	13	I	Mode selection pin (MSB)
NC	3, 4, 19, 20, 25, 42	–	No connect. Pins may be grounded.
OC_ADJ	9	O	Analog overcurrent programming pin
$\overline{\text{OTW}}$	2	O	Overtemperature warning signal, open-drain, active-low
OUT_A	39	O	Output, half-bridge A
OUT_B	36	O	Output, half-bridge B

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
OUT_C	31	O	Output, half-bridge C
OUT_D	28	O	Output, half-bridge D
PVDD_A	40, 41	P	Power supply input for half-bridge A
PVDD_B	35	P	Power supply input for half-bridge B
PVDD_C	32	P	Power supply input for half-bridge C
PVDD_D	26, 27	P	Power supply input for half-bridge D
PWM_A	6	I	PWM Input signal for half-bridge A
PWM_B	8	I	PWM Input signal for half-bridge B
PWM_C	16	I	PWM Input signal for half-bridge C
PWM_D	18	I	PWM Input signal for half-bridge D
$\overline{\text{RESET\_AB}}$	7	I	Reset signal for half-bridge A and half-bridge B, active-low
$\overline{\text{RESET\_CD}}$	17	I	Reset signal for half-bridge C and half-bridge D, active-low
$\overline{\text{SD}}$	5	O	Shutdown signal, open-drain, active-low
VDD	21	P	Input power supply
VREG	12	P	Internal voltage regulator

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
VDD to AGND		–0.3	13.2	V
GVDD_X to AGND		–0.3	13.2	V
PVDD_X to GND_X (2)		–0.3	46	V
OUT_X to GND_X (2)		–0.3	46	V
BST_X to GND_X (2)		–0.3	59.2	V
BST_X to GVDD_X (2)		–0.3	46	V
VREG to AGND		–0.3	4.2	V
GND_X to GND		–0.3	0.3	V
GND_X to AGND		–0.3	0.3	V
GND to AGND		–0.3	0.3	V
PWM_X, OC_ADJ, M1, M2, M3 to AGND		–0.3	4.2	V
$\overline{\text{RESET\_X}}$, $\overline{\text{SD}}$, $\overline{\text{OTW}}$ to AGND		–0.3	7	V
Maximum continuous sink current ($\overline{\text{SD}}$, $\overline{\text{OTW}}$)			9	mA
Minimum pulse duration, low			30	ns
Maximum operating junction temperature range, T_J		0	125	°C
Storage temperature, T_{stg}		–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) These voltages represent the DC voltage and peak AC waveform measured at the terminal of the device in all conditions.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
PVDD_X	Half-bridge supply voltage		0	32	34	V
GVDD_X	Supply voltage for logic regulators and gate-drive circuitry		10.8	12	13.2	V
VDD	Digital regulator supply voltage		10.8	12	13.2	V
R_L (BTL)	Resistive load impedance (no Cycle-by-Cycle current control), recommended demodulation filter		3	4		Ω
R_L (SE)			2.25	3		
R_L (PBTL)			1.5	2		
L_{Output} (BTL)	Output-filter inductance	Minimum output inductance under short-circuit condition	5	10		µH
L_{Output} (SE)			5	10		
L_{Output} (PBTL)			5	10		
f_S	PWM frame rate		192	384	432	kHz
t_{LOW}	Minimum low-state pulse duration per PWM Frame, noise shaper enabled		30			nS
C_{PVDD}	PVDD close decoupling capacitors			0.1		µF
C_{BST}	Bootstrap capacitor, selected value supports PWM frame rates from 192 kHz to 432 kHz			33		nF
R_{OC}	Over-current programming resistor	Resistor tolerance = 5%	22	22	47	kΩ
$R_{EXT-PULLUP}$	External pullup resistor to 3.3 V to 5.0 V for $\overline{SD}$ or $\overline{OTW}$		3.3	4.7		kΩ
T_J	Junction temperature		0		125	°C

6.4 Thermal Information

THERMAL METRIC (1)		TAS5342LA DDV (HTSSOP) 44 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	41.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	18.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	17.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

PVDD_x = 32 V, GVDD_X = 12 V, VDD = 12 V, T_C (Case temperature) = 25°C, f_S = 384 kHz, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL VOLTAGE REGULATOR AND CURRENT CONSUMPTION						
VREG	Voltage regulator, only used as a reference node	VDD = 12 V	3	3.3	3.6	V
IVDD	VDD supply current	Operating, 50% duty cycle		7.1	17	mA
		Idle, reset mode		5.6	11	
IGVDD_X	Gate supply current per half-bridge	50% duty cycle		5.9	12	mA
		Reset mode		1	1.8	
IPVDD_X	Half-bridge idle current	50% duty cycle, without output filter or load		10.5	20	mA
		Reset mode, no switching		594	713	µA
OUTPUT STAGE MOSFETs						
$R_{DSon,LS}$	Drain-to-source resistance, Low Side	T_J = 25°C, excludes metallization resistance		110	125	mΩ
$R_{DSon,HS}$	Drain-to-source resistance, High Side			110	125	mΩ
I/O PROTECTION						
$V_{uvp,G}$	Undervoltage protection limit, GVDD_X			9.5		V
$V_{uvp,hyst}$ (1)	Undervoltage protection limit, GVDD_X			250		mV
BST_{uvpF}	Puts device into RESET when BST voltage falls below limit			6.11		V
BST_{uvpR}	Brings device out of RESET when BST voltage rises above limit			7.25		V
OTW(1)	Overtemperature warning		115	125	135	°C
OTW_{HYST} (1)	Temperature drop needed below $\overline{OTW}$ temp. for $\overline{OTW}$ to be inactive after the $\overline{OTW}$ event			25		°C
OTE(1)	Overtemperature error threshold		145	155	165	°C
$OTE\text{-}OTW_{differential}$ (1)	$\overline{OTE}$ - $\overline{OTW}$ differential, temperature delta between $\overline{OTW}$ and $\overline{OTE}$			30		°C
OLPC	Overload protection counter	f_S = 384 kHz		1.25		ms
I_{OC}	Overcurrent limit protection	Resistor—programmable, high-end, R_{OC} = 22 kΩ with 1 ms pulse, T_C= 75°C	7.9	8.4		A
I_{OCT}	Overcurrent response time			150		ns
$t_{ACTIVITY\ DETECTOR}$	Time for PWM activity detector to activate when no PWM is present	Lack of transistion of any PWM input		13.2		µS
I_{PD}	Output pulldown current of each half-bridge	Connected when $\overline{RESET}$ is active to provide bootstrap capacitor charge. Not used in SE mode.		3		mA
STATIC DIGITAL SPECIFICATIONS						
V_{IH}	High-level input voltage	PWM_A, PWM_B, PWM_C, PWM_D, M1, M2, M3, RESET_AB, RESET_CD	2			V
V_{IL}	Low-level input voltage				0.8	V
$I_{Leakage}$	Input leakage current				100	µA
OTW/SHUTDOWN (SD)						
R_{INT_PU}	Internal pullup resistance, $\overline{OTW}$ to VREG, $\overline{SD}$ to VREG		20	26	32	kΩ
V_{OH}	High-level output voltage	Internal pullup resistor	3	3.3	3.6	V
		External pullup of 4.7 kΩ to 5 V	4.5		5	
V_{OL}	Low-level output voltage	I_O = 4 mA		0.2	0.4	V
FANOUT	Device fanout $\overline{OTW}$, $\overline{SD}$	No external pullup		30		Devices

(1) Specified by design

6.6 Audio Specifications (BTL)

Audio performance is recorded as a chipset consisting of a TAS5518 pwm processor (modulation index limited to 97.7%) and a TAS5342LA power stage. PCB and system configuration are in accordance with recommended guidelines. Audio frequency = 1 kHz, PVDD_x = 32 V, GVDD_x = 12 V, R_L = 4 Ω, f_S = 384 kHz, R_{OC} = 22 kΩ, T_C = 75°C, Output Filter: L_{DEM} = 10 μH, C_{DEM} = 470 nF, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_{OMAX}	Maximum Power Output	R_L = 4 Ω, 10% THD+N, clipped input signal		100		W
		R_L = 6 Ω, 10% THD+N, clipped input signal		80		
		R_L = 8 Ω, 10% THD+N, clipped input signal		65		
P_O	Unclipped Power Output	R_L = 4 Ω, 0 dBFS, unclipped input signal		80		W
		R_L = 6 Ω, 0 dBFS, unclipped input signal		64		
		R_L = 8 Ω, 0 dBFS, unclipped input signal		50		
THD+N	Total harmonic distortion + noise	0 dBFS; AES17 filter		0.4%		
		1 W; AES17 filter		0.09%		
V_n	Output integrated noise	A-weighted, AES17 filter, Auto mute disabled		55		μV
SNR	Signal-to-noise ratio (1)	A-weighted, AES17 filter, Auto mute disabled		110		dB
DNR	Dynamic range	A-weighted, input level = –60 dBFS, AES17 filter		110		dB
DC Offset	Output offset voltage			±15		mV
P_{idle}	Power dissipation due to idle losses (IPVDD_X)	P_O = 0 W, all halfbridges switching (2)		3		W

(1) SNR is calculated relative to 0-dBFS input level.
(2) Actual system idle losses are affected by core losses of output inductors.

6.7 Audio Specifications (Single-Ended Output)

Audio performance is recorded as a chipset consisting of a TAS5086 pwm processor (modulation index limited to 97.7%) and a TAS5342LA power stage. PCB and system configuration are in accordance with recommended guidelines. Audio frequency = 1 kHz, PVDD_x = 32 V, GVDD_x = 12 V, R_L = 4 Ω, f_S = 384 kHz, R_{OC} = 22 kΩ, T_C = 75°C, Output Filter: L_{DEM} = 20 μH, C_{DEM} = 1 μF, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_{OMAX}	Maximum Power Output	R_L = 3 Ω, 10% THD+N, clipped input signal		40		W
		R_L = 4 Ω, 10% THD+N, clipped input signal		30		
P_O	Unclipped Power Output	R_L = 3 Ω, 0 dBFS, unclipped input signal		30		
		R_L = 4 Ω, 0 dBFS, unclipped input signal		25		
THD+N	Total harmonic distortion + noise	0 dBFS; AES17 filter		0.4%		
		1 W; AES17 filter		0.09%		
V_n	Output integrated noise	A-weighted, AES17 filter, Auto mute disabled		35		μV
SNR	Signal-to-noise ratio (1)	A-weighted, AES17 filter, Auto mute disabled		109		dB
DNR	Dynamic range	A-weighted, input level = –60 dBFS AES17 filter		109		dB
P_{idle}	Power dissipation due to idle losses (IPVDD_X)	P_O = 0 W, all half bridges switching (2)		3		W

(1) SNR is calculated relative to 0-dBFS input level.
(2) Actual system idle losses are affected by core losses of output inductors.

6.8 Audio Specifications (PBTL)

Audio performance is recorded as a chipset consisting of a TAS5518 pwm processor (modulation index limited to 97.7%) and a TAS5342LA power stage. PCB and system configuration are in accordance with recommended guidelines. Audio frequency = 1 kHz, PVDD_x = 32 V, GVDD_x = 12 V, R_L = 3 Ω, f_S = 384 kHz, R_{OC} = 22 kΩ, T_C = 75°C, Output Filter: L_{DEM} = 10 µH, C_{DEM} = 1 uF, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_{OMAX}	Maximum Power Output	R_L = 2 Ω, 10% THD+N, clipped input signal		200		W
		R_L = 3 Ω, 10% THD+N, clipped input signal		160		
P_O	Unclipped Power Output	R_L = 2 Ω, 0 dBFS, unclipped input signal		150		W
		R_L = 3 Ω, 0 dBFS, unclipped input signal		120		
THD+N	Total harmonic distortion + noise	0 dBFS; AES17 filter		0.4%		
		1 W; AES17 filter		0.09%		
V_n	Output integrated noise	A-weighted, AES17 filter, Auto mute disabled		45		µV
SNR	Signal-to-noise ratio(1)	A-weighted, AES17 filter, Auto mute disabled		110		dB
DNR	Dynamic range	A-weighted, input level = –60 dBFS AES17 filter		110		dB
DC Offset	Outuput offset voltage			±15		mV
P_{idle}	Power dissipation due to idle losses (IPVDD_X)	P_O = 0 W, all half bridges switching(2)		3		W

(1) SNR is calculated relative to 0-dBFS input level.
(2) Actual system idle losses are affected by core losses of output inductors.

6.9 Typical Characteristics

6.9.1 BTL Configuration

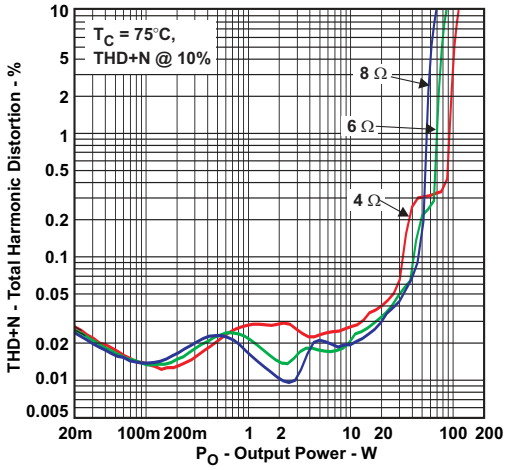


Figure 1. Total Harmonic Distortion + Noise vs Output Power

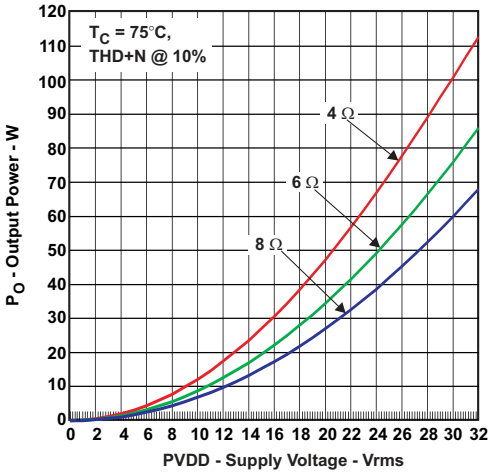


Figure 2. Output Power vs Supply Voltage

BTL Configuration (continued)

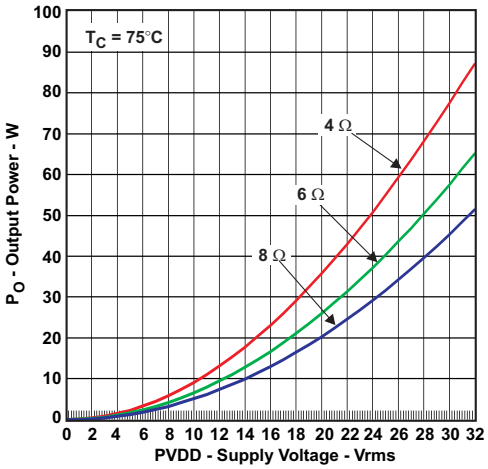


Figure 3. Unclipped Output Power vs Supply Voltage

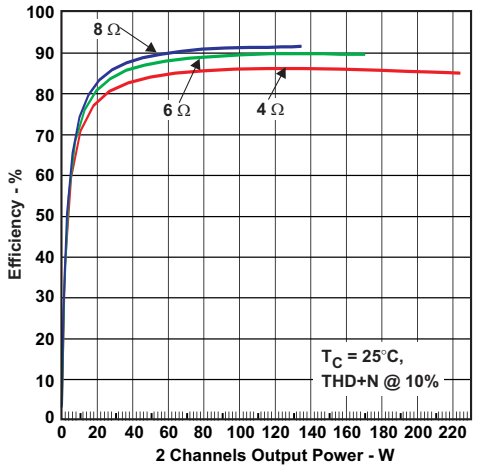


Figure 4. System Efficiency vs Output Power

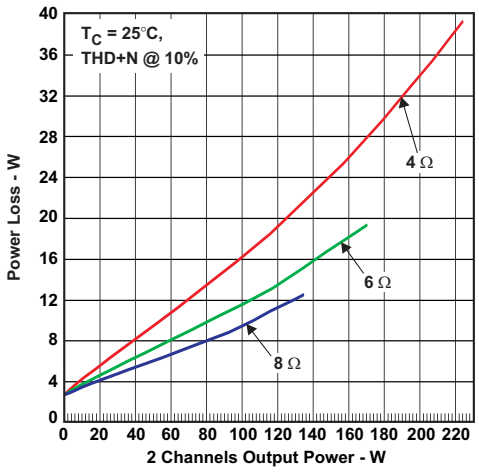


Figure 5. System Power Loss vs Output Power

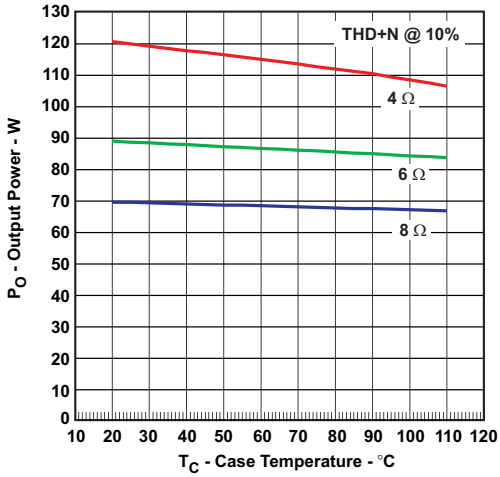


Figure 6. System Output Power vs Case Temperature

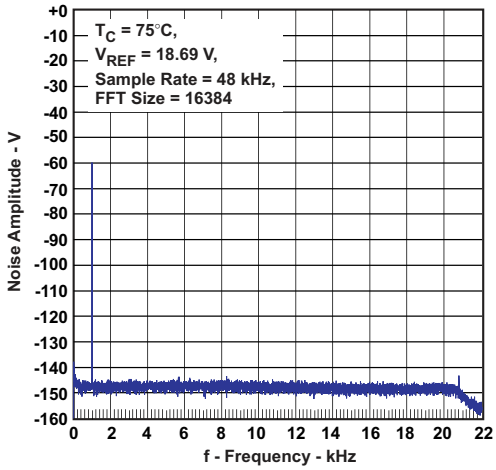


Figure 7. Noise Amplitude vs Frequency

6.9.2 SE Configuration

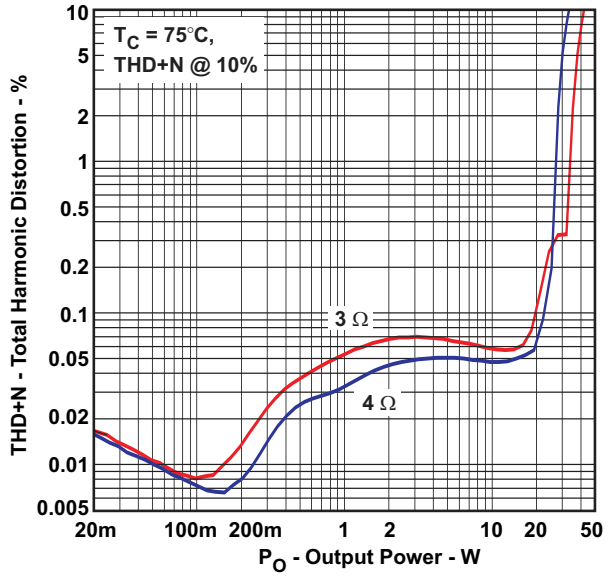


Figure 8. Total Harmonic Distortion + Noise vs Output Power

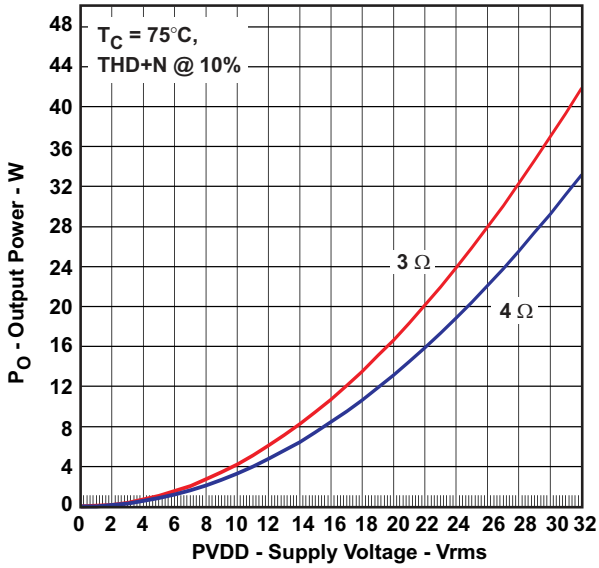


Figure 9. Output Power vs Supply Voltage

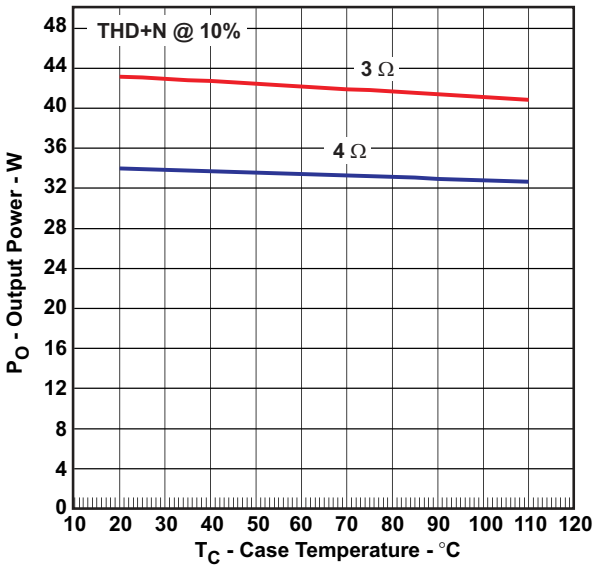


Figure 10. Output Power vs Case Temperature

6.9.3 PBTL Configuration

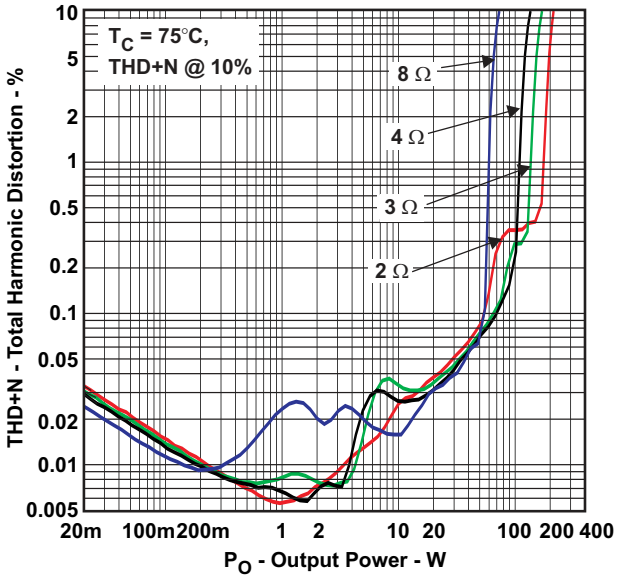


Figure 11. Total Harmonic Distortion + Noise vs Output Power

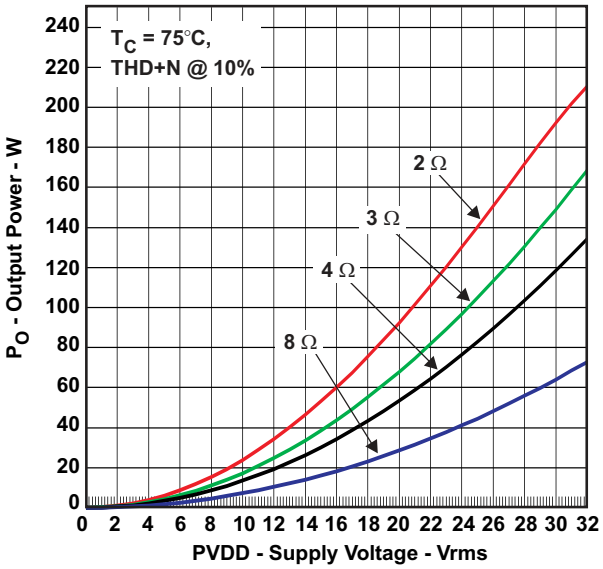


Figure 12. Output Power vs Supply Voltage

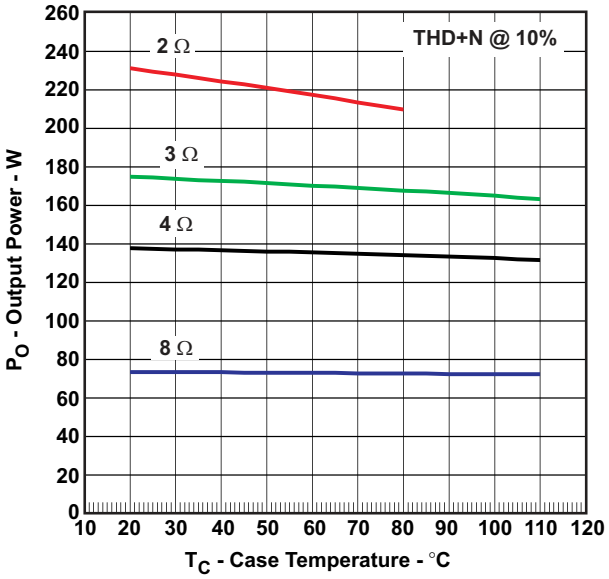


Figure 13. System Output Power vs Case Temperature

7 Detailed Description

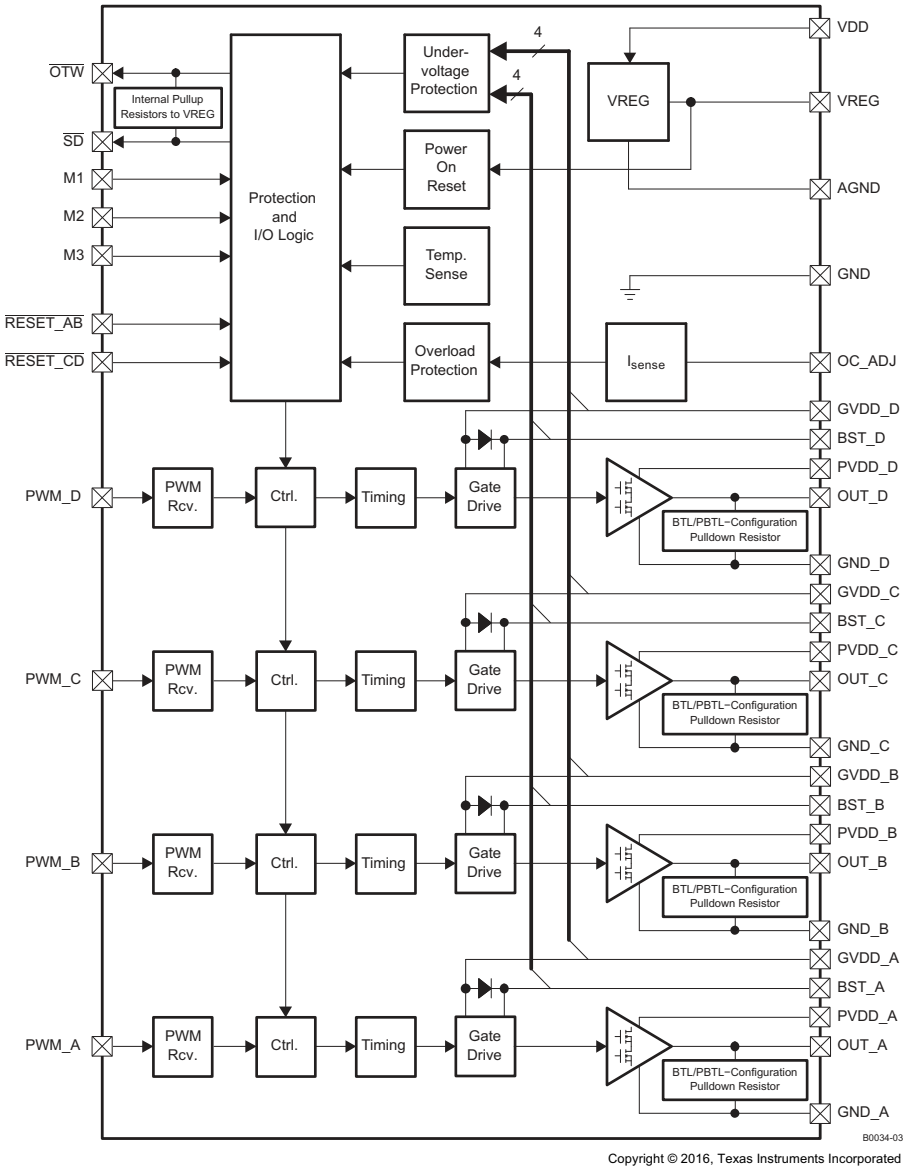
7.1 Overview

TAS5342LA is a PWM input, Class-D audio amplifier. The output of the TAS5342LA can be configured for single-ended, bridge-tied load (BTL) or parallel BTL (PBTL) output. Independent supply rails provide improved audio performance, one for audio power output (PVDD) and the other for gate drive and analog control (GVDD and VDD).

The TAS5342LA contains a protection system that safeguards the device against short circuits, overload, over-temperature, and under-voltage conditions. An error reporting system provides feedback under fault conditions.

Figure 14 shows typical connections for BTL outputs. A detailed schematic can be viewed in (*TAS5342LDDV6EVM User Guide*).

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Mid Z Sequence Compatibility

The TAS5342LA is compatable with the Mid Z sequence of the TAS5086 Modulator. The Mid Z Sequence is a series of pulses that is generated by the modulator. This sequence causes the power stage to slowly enable its outputs as it begins to switch.

By slowly starting the PWM switching, the impulse response created by the onset of switching is reduced. This impulse response is the acoustic artifact that is heard in the output transducers (loudspeakers) and is commonly termed "click" or "pop".

The low acoustic artifact noise of the TAS5342LA will be further decreased when used in conjunction with the TAS5086 modulator with the Mid Z Sequence enabled.

The Mid Z sequence is primarily used for the single-ended output configuration. It facilitates a "softer" PWM output start after the split cap output configuration is charged.

7.3.2 Device Protection System

The TAS5342LA contains advanced protection circuitry carefully designed to facilitate system integration and ease of use, as well as to safeguard the device from permanent failure due to a wide range of fault conditions such as short circuits, overload, overtemperature, and undervoltage. The TAS5342LA responds to a fault by immediately setting the power stage in a high-impedance (Hi-Z) state and asserting the $\overline{SD}$ pin low. In situations other than overload and over-temperature error ($\overline{OTE}$), the device automatically recovers when the fault condition has been removed, that is, the supply voltage has increased.

The device will function on errors, as shown in Table 1.

Table 1. Device Protection

BTL MODE		PBTL MODE		SE MODE	
Local Error In	Turns Off	Local Error In	Turns Off	Local Error In	Turns Off
A	A + B	A	A + B + C + D	A	A + B
B		B		B	
C	C + D	C		C	C + D
D		D		D	

Bootstrap UVP does not shutdown according to the table, it shutsdown the respective halfbridge.

7.3.3 Use Of TAS5342LA In High-Modulation-Index Capable Systems

This device requires at least 30 ns of low time on the output per 384-kHz PWM frame rate in order to keep the bootstrap capacitors charged. As an example, if the modulation index is set to 99.2% in the TAS5508, this setting allows PWM pulse durations down to 10 ns. This signal, which does not meet the 30-ns requirement, is sent to the PWM_X pin and this low-state pulse time does not allow the bootstrap capacitor to stay charged. The TAS5342LA device requires limiting the TAS5508 modulation index to 97.7% to keep the bootstrap capacitor charged under all signals and loads.

The TAS5342LA contains a bootstrap capacitor under voltage protection circuit (BST_UVP) that monitors the voltage on the bootstrap capacitors. When the voltage on the bootstrap capacitors is less than required for proper control of the High-Side MOSFETs, the device will initiate bootstrap capacitor recharge sequences until the bootstrap capacitors are properly charged for robust operation. This function may be activated with PWM pulses less than 30 nS.

Therefore, TI strongly recommends using a TI PWM processor, such as TAS5518, TAS5086 or TAS5508, with the modulation index set at 97.7% to interface with TAS5342LA.

Feature Description (continued)

7.3.4 Overcurrent (OC) Protection With Current Limiting and Overload Detection

The device has independent, fast-reacting current detectors with programmable trip threshold (OC threshold) on all high-side and low-side power-stage FETs. See the following table for OC-adjust resistor values. The detector outputs are closely monitored by two protection systems. The first protection system controls the power stage in order to prevent the output current from further increasing, that is, it performs a current-limiting function rather than prematurely shutting down during combinations of high-level music transients and extreme speaker load impedance drops. If the high-current situation persists, that is, the power stage is being overloaded, a second protection system triggers a latching shutdown, resulting in the power stage being set in the high-impedance (Hi-Z) state. Current limiting and overload protection are independent for half-bridges A and B and, respectively, C and D. That is, if the bridge-tied load between half-bridges A and B causes an overload fault, only half-bridges A and B are shut down.

- For the lowest-cost bill of materials in terms of component selection, the OC threshold measure should be limited, considering the power output requirement and minimum load impedance. Higher-impedance loads require a lower OC threshold.
- The demodulation-filter inductor must retain at least 5 μH of inductance at twice the OC threshold setting.

Unfortunately, most inductors have decreasing inductance with increasing temperature and increasing current (saturation). To some degree, an increase in temperature naturally occurs when operating at high output currents, due to core losses and the dc resistance of the inductor copper winding. A thorough analysis of inductor saturation and thermal properties is strongly recommended.

Setting the OC threshold too low might cause issues such as lack of enough output power and/or unexpected shutdowns due to too-sensitive overload detection.

TI recommends following the external component selection and PCB layout as given in the *Application and Implementation* section.

For added flexibility, the OC threshold is programmable within a limited range using a single external resistor connected between the OC_ADJ pin and AGND. (See the *Electrical Characteristics* section of this data sheet for information on the correlation between programming-resistor value and the OC threshold.) It should be noted that a properly functioning overcurrent detector assumes the presence of a properly designed demodulation filter at the power-stage output. Short-circuit protection is not provided directly at the output pins of the power stage but only on the speaker terminals (after the demodulation filter). It is required to follow certain guidelines when selecting the OC threshold and an appropriate demodulation inductor:

Table 2. Overcurrent Resistor Selection

OC-Adjust Resistor Values (kΩ)	Max. Current Before OC Occurs (A), T_C=75°C
22	8.4 A
33	6.8 A
47	5.3 A

The reported maximum peak current in the table above is measured with continuous current in 1 Ω, one channel active and the other one muted.

7.3.5 Pin-To-Pin Short Circuit Protection System (PPSC)

The PPSC detection system protects the device from permanent damage in the case that a power output pin (OUT_X) is shorted to GND_X or PVDD_X. For comparison the OC protection system detects an over current after the demodulation filter where PPSC detects shorts directly at the pin before the filter. PPSC detection is performed at startup, that is, when VDD is supplied, consequently a short to either GND_X or PVDD_X after system startup will not activate the PPSC detection system. When PPSC detection is activated by a short on the output, all half bridges are kept in a Hi-Z state until the short is removed, the device then continues the startup sequence and starts switching. The detection is controlled globally by a two step sequence. The first step ensures that there are no shorts from OUT_X to GND_X, the second step tests that there are no shorts from OUT_X to PVDD_X. The total duration of this process is roughly proportional to the capacitance of the output LC

Feature Description (continued)

filter. The typical duration is < 15 ms/μF. While the PPSC detection is in progress, $\overline{SD}$ is kept low, and the device will not react to changes applied to the $\overline{RESET}$ pins. If no shorts are present the PPSC detection passes, and $\overline{SD}$ is released. A device reset will not start a new PPSC detection. PPSC detection is enabled in BTL and PBTL output configurations, the detection is not performed in SE mode. To make sure not to trip the PPSC detection system it is recommended not to insert resistive load to GND_X or PVDD_X.

7.3.6 Overtemperature Protection

The TAS5342LA has a two-level temperature-protection system that asserts an active-low warning signal ($\overline{OTW}$) when the device junction temperature exceeds 125°C (nominal) and, if the device junction temperature exceeds 155°C (nominal), the device is put into thermal shutdown, resulting in all half-bridge outputs being set in the high-impedance (Hi-Z) state and $\overline{SD}$ being asserted low. OTE is latched in this case. To clear the OTE latch, either $\overline{RESET\_AB}$ or $\overline{RESET\_CD}$ must be asserted. Thereafter, the device resumes normal operation.

7.3.7 Undervoltage Protection (UVP) and Power-On Reset (POR)

The UVP and POR circuits of the TAS5342LA fully protect the device in any power-up or down and brownout situation. While powering up, the POR circuit resets the overload circuit (OLP) and ensures that all circuits are fully operational when the GVDD_X and VDD supply voltages reach stated in the *Electrical Characteristics* table. Although GVDD_X and VDD are independently monitored, a supply voltage drop below the UVP threshold on any VDD or GVDD_X pin results in all half-bridge outputs immediately being set in the high-impedance (Hi-Z) state and $\overline{SD}$ being asserted low. The device automatically resumes operation when all supply voltages have increased above the UVP threshold.

7.3.8 Error Reporting

The $\overline{SD}$ and $\overline{OTW}$ pins are both active-low, open-drain outputs. Their function is for protection-mode signaling to a PWM controller or other system-control device.

Any fault resulting in device shutdown is signaled by the $\overline{SD}$ pin going low. Likewise, $\overline{OTW}$ goes low when the device junction temperature exceeds 125°C (see Table 3).

Table 3. Error Reporting

$\overline{SD}$	$\overline{OTW}$	DESCRIPTION
0	0	Overtemperature (OTE) or overload (OLP) or undervoltage (UVP)
0	1	Overload (OLP) or undervoltage (UVP)
1	0	Junction temperature higher than 125°C (overtemperature warning)
1	1	Junction temperature lower than 125°C and no OLP or UVP faults (normal operation)

Note that asserting either $\overline{RESET\_AB}$ or $\overline{RESET\_CD}$ low forces the $\overline{SD}$ signal high, independent of faults being present. TI recommends monitoring the $\overline{OTW}$ signal using the system microcontroller and responding to an overtemperature warning signal by, for example, turning down the volume to prevent further heating of the device resulting in device shutdown (OTE).

To reduce external component count, an internal pullup resistor to 3.3 V is provided on both $\overline{SD}$ and $\overline{OTW}$ outputs. Level compliance for 5-V logic can be obtained by adding external pullup resistors to 5 V (see the *Electrical Characteristics* section of this data sheet for further specifications).

Feature Description (continued)

7.3.9 Device Reset

Two reset pins are provided for independent control of half-bridges A/B and C/D. When $\overline{\text{RESET\_AB}}$ is asserted low, all four power-stage FETs in half-bridges A and B are forced into a high-impedance (Hi-Z) state. Likewise, asserting $\overline{\text{RESET\_CD}}$ low forces all four power-stage FETs in half-bridges C and D into a high-impedance state. Thus, both reset pins are well suited for hard-muting the power stage if needed.

In BTL modes, to accommodate bootstrap charging prior to switching start, asserting the reset inputs low enables weak pulldown of the half-bridge outputs. In the SE mode, the weak pulldowns are not enabled, and it is therefore recommended to ensure bootstrap capacitor charging by providing a low pulse on the PWM inputs when reset is asserted high.

Asserting either reset input low removes any fault information to be signalled on the $\overline{\text{SD}}$ output, that is, $\overline{\text{SD}}$ is forced high.

A rising-edge transition on either reset input allows the device to resume operation after an overload fault. To ensure thermal reliability, the rising edge of reset must occur no sooner than 4 ms after the falling edge of $\overline{\text{SD}}$.

7.4 Device Functional Modes

Protection modes are selected by shorting M1, M2, and M3 to VREG or GND.

Table 4. Protection Mode Selection Pins

MODE PINS			MODE NAME	PWM INPUT (1)	DESCRIPTION
M3	M2	M1			
0	0	0	BTL mode 1	2N	All protection systems enabled
0	0	1	BTL mode 2	2N	Latching shutdown on, PWM activity detector and OLP disabled
0	1	0	BTL mode 3	1N	All protection systems enabled
0	1	1	PBTL mode	1N / 2N (2)	All protection systems enabled
1	0	0	SE mode 1	1N	All protection systems enabled (3)
1	0	1	SE mode 2	1N	Latching shutdown on, PWM activity detector and OLP disabled (3)
1	1	0	Reserved		
1	1	1			

(1) The 1N and 2N naming convention is used to indicate the number of PWM lines to the power stage per channel in a specific mode.
(2) PWM_D is used to select between the 1N and 2N interface in PBTL mode (Low = 1N; High = 2N). PWM_D is internally pulled low in PBTL mode. PWM_A is used as the PWM input in 1N mode and PWM_A and PWM_B are used as inputs for the 2N mode
(3) PPSC detection system disabled.

7.4.1 System Power-Up/Power-Down Sequence

7.4.1.1 Powering Up

The TAS5342LA does not require a power-up sequence. The outputs of the H-bridges remain in a high-impedance state until the gate-drive supply voltage (GVDD_X) and VDD voltage are above the undervoltage protection (UVP) voltage threshold (see the *Electrical Characteristics* section of this data sheet). Although not specifically required, it is recommended to hold RESET_AB and RESET_CD in a low state while powering up the device. This allows an internal circuit to charge the external bootstrap capacitors by enabling a weak pulldown of the half-bridge output.

When the TAS5342LA is being used with TI PWM modulators such as the TAS5518, no special attention to the state of RESET_AB and RESET_CD is required, provided that the chipset is configured as recommended.

7.4.1.2 Powering Down

The TAS5342LA does not require a power-down sequence. The device remains fully operational as long as the gate-drive supply (GVDD_X) voltage and VDD voltage are above the undervoltage protection (UVP) voltage threshold (see the *Electrical Characteristics* section of this data sheet). Although not specifically required, it is a good practice to hold RESET_AB and RESET_CD low during power down, thus preventing audible artifacts including pops or clicks.

When the TAS5342LA is being used with TI PWM modulators such as the TAS5518, no special attention to the state of RESET_AB and RESET_CD is required, provided that the chipset is configured as recommended.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

TAS5342LA can be configured either in stereo BTL mode, 4 channel SE mode, or mono PBTL mode, depending on output power conditions and system design.

8.2 Typical Applications

8.2.1 Typical Differential (2N) BTL Application

The following schematics and PCB layouts illustrate "best practices" in the use of the TAS5342LA.

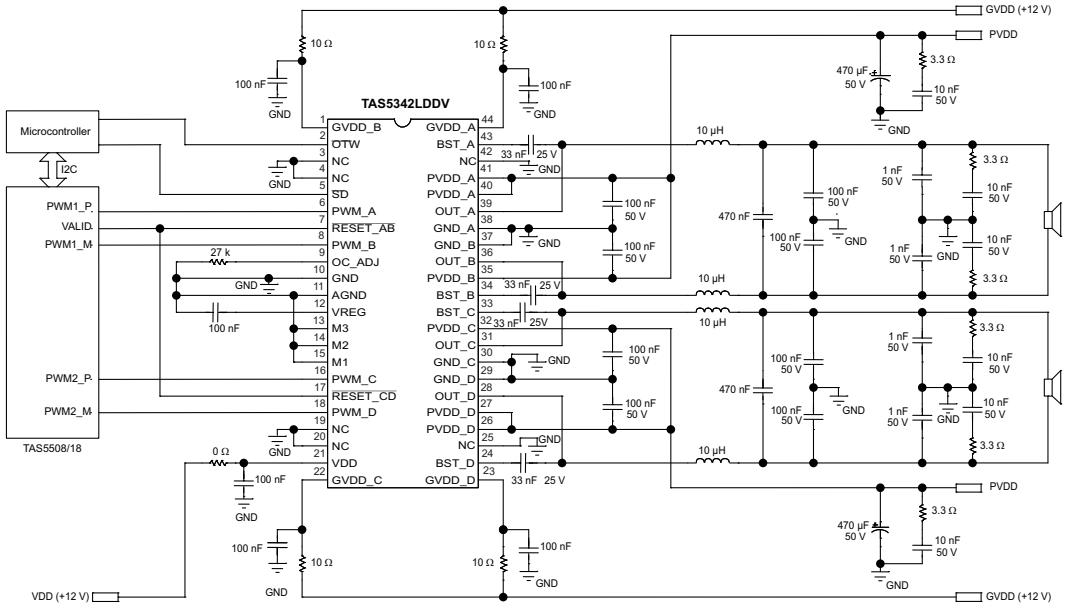


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Figure 14. Typical Differential (2N) BTL Application With AD Modulation Filters

8.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 5 as the input parameters.

Table 5. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Low Power (pull-up) supply	3.3 V
Mid Power Supply (GVDD, VDD)	12 V
High Power Supply (PVDD)	12 V – 36 V
PWM Inputs	INPUT A = 0 – 3.3 V PWM
	INPUT_B = 0 – 3.3 V PWM
	INPUT_C = 0 – 3.3 V PWM
	INPUT_D = 0 – 3.3 V PWM
Speaker Impedance	4 Ω – 8 Ω

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 PCB Material Recommendation

FR-4 Glass Epoxy material with 2 oz. (70 μm) is recommended for use with the TAS5342LA. The use of this material can provide for higher power output, improved thermal performance, and better EMI margin (due to lower PCB trace inductance.

8.2.1.2.2 P_{VDD} Capacitor Recommendation

The large capacitors used in conjunction with each full-birdge, are referred to as the PVDD Capacitors. These capacitors should be selected for proper voltage margin and adequate capacitance to support the power requirements. In practice, with a well designed system power supply, 1000 μF, 50-V supports more applications. The PVDD capacitors should be low ESR type because they are used in a circuit associated with high-speed switching.

8.2.1.2.3 Decoupling Capacitor Recommendations

In order to design an amplifier that has robust performance, passes regulatory requirements, and exhibits good audio performance, good quality decoupling capacitors should be used. In practice, X7R should be used in this application.

The voltage of the decoupling capacitors should be selected in accordance with good design practices. Temperature, ripple current, and voltage overshoot must be considered. This fact is particularly true in the selection of the 0.1 μF that is placed on the power supply to each half-bridge. It must withstand the voltage overshoot of the PWM switching, the heat generated by the amplifier during high power output, and the ripple current created by high power output. A minimum voltage rating of 50-V is required for use with a 32 V power supply.

8.2.1.3 Application Curves

Relevant performance plots for TAS5342LA are shown in the *BTL Configuration*.

Table 6. Performance Plots, Typical BTL Configurations

PLOT TITLE	FIGURE NUMBER
Total Harmonic Distortion + Noise vs. Output power	Figure 1
Output Power vs. Supply Voltage	Figure 2
Unclipped Output Power vs. Supply Voltage	Figure 3
System Efficiency vs. Output Power	Figure 4
System Power Loss vs. Output Power	Figure 5
System Output Power vs. Case Temperature	Figure 6
Noise Amplitude vs. Frequency	Figure 7

8.2.2 Typical Non-Differential (1N) BTL

Design Requirements Typical Non-Differential BTL.

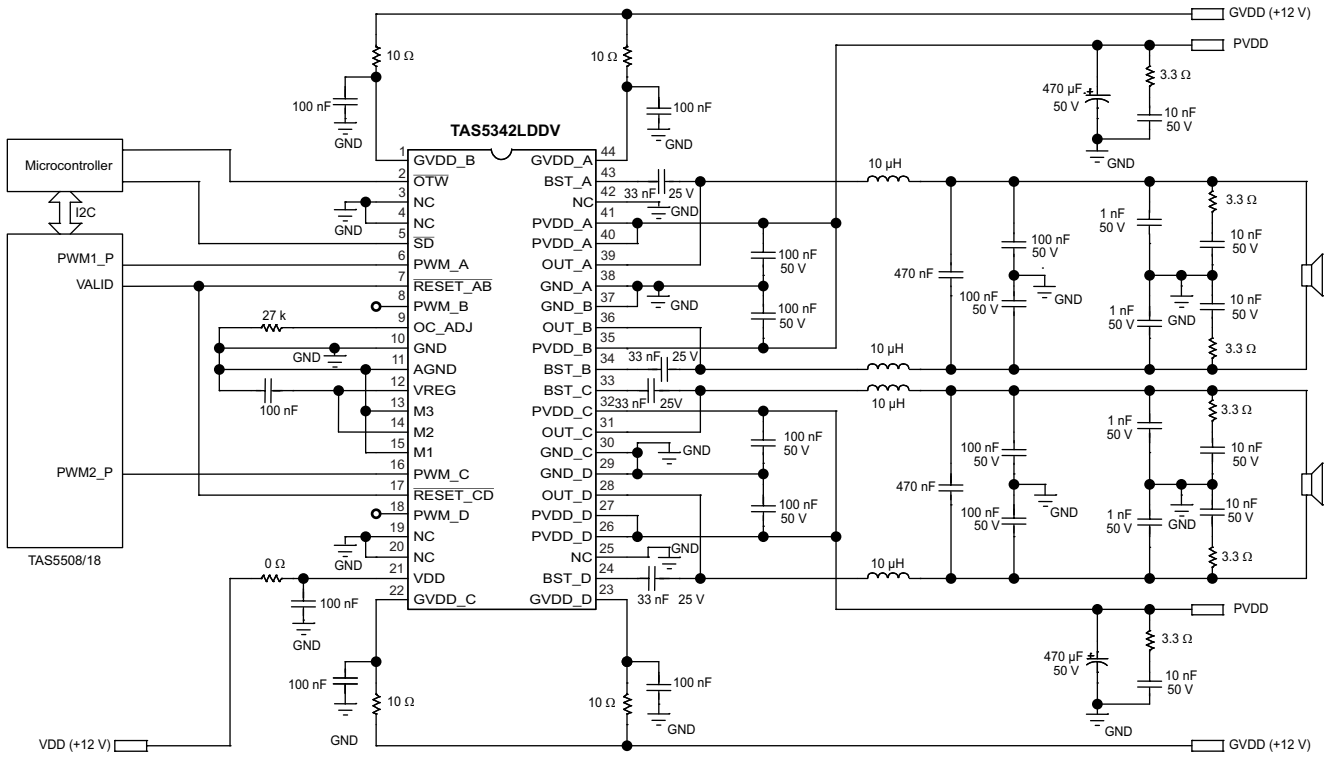

Figure 15. Typical Non-Differential (1N) BTL Application With AD Modulation Filters

8.2.2.1 Design Requirements

For this design example, use the parameters listed in Table 7 as the input parameters.

Table 7. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Low Power (pull-up) supply	3.3 V
Mid Power Supply (GVDD, VDD)	12 V
High Power Supply (PVDD)	12 V – 36 V
PWM Inputs	INPUT A = 0 – 3.3 V PWM
	INPUT_B = N/C
	INPUT_C = 0 – 3.3 V PWM
	INPUT_D = N/C
Speaker Impedance	4 Ω – 8 Ω

8.2.2.2 Application Curves

Relevant performance plots for TAS5342LA are shown in the *BTL Configuration*.

Table 8. Performance Plots, Typical BTL Configurations

PLOT TITLE	FIGURE NUMBER
Total Harmonic Distortion + Noise vs. Output power	Figure 1
Output Power vs. Supply Voltage	Figure 2
Unclipped Output Power vs. Supply Voltage	Figure 3
System Efficiency vs. Output Power	Figure 4
System Power Loss vs. Output Power	Figure 5
System Output Power vs. Case Temperature	Figure 6
Noise Amplitude vs. Frequency	Figure 7

8.2.3 Typical SE Application

Design Requirements Typical SE

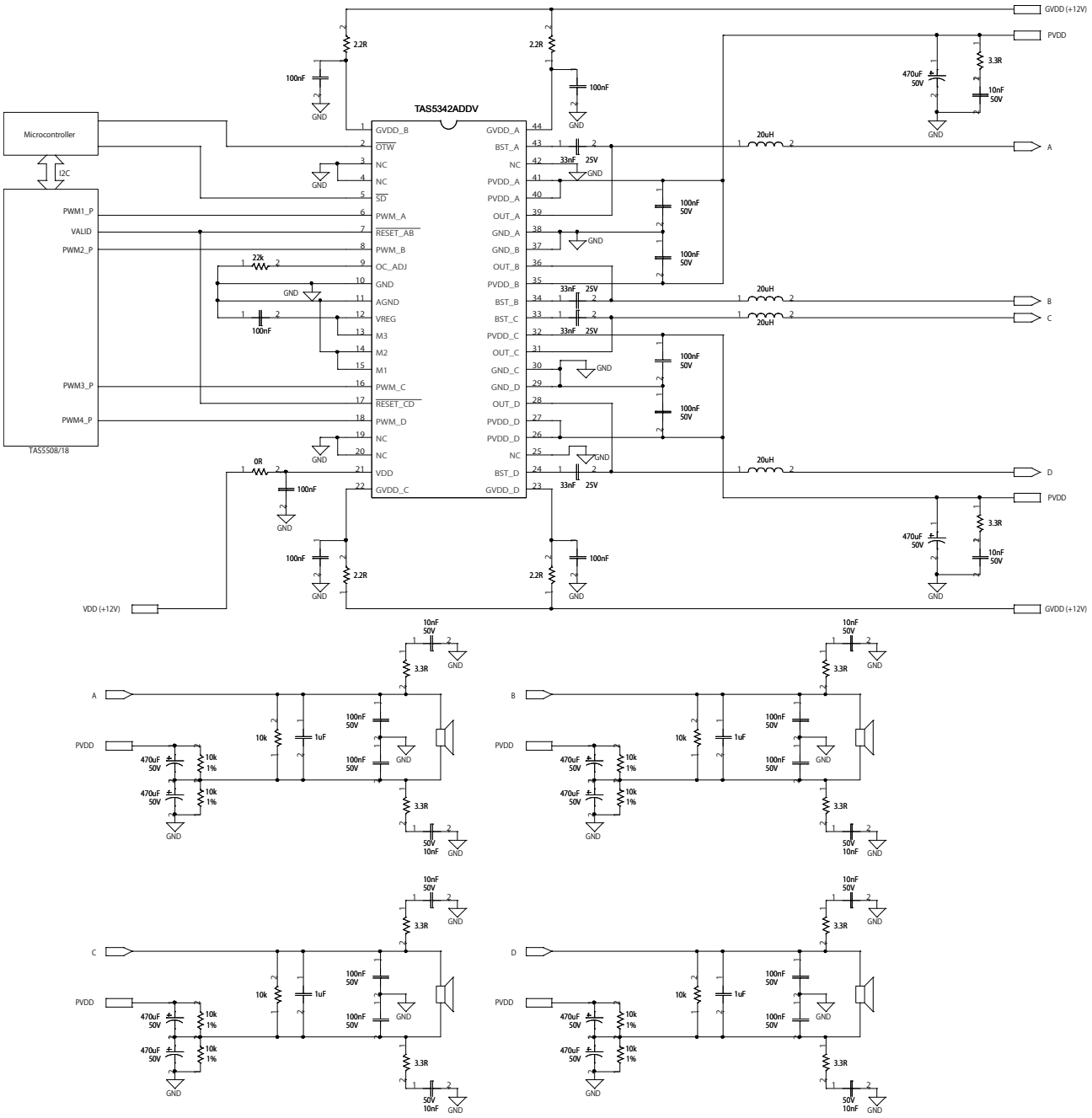

Figure 16. Typical SE Application

8.2.3.1 Design Requirements

For this design example, use the parameters listed in Table 9 as the input parameters.

Table 9. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Low Power (pull-up) supply	3.3 V
Mid Power Supply (GVDD, VDD)	12 V
High Power Supply (PVDD)	12 V – 36 V
PWM Inputs	INPUT A = 0 – 3.3 V PWM
	NPUT B = 0 – 3.3 V PWM
	INPUT_C = 0 – 3.3 V PWM
	NPUT D = 0 – 3.3 V PWM
Speaker Impedance	3 Ω – 4 Ω

8.2.3.2 Application Curves

Relevant performance plots for TAS5342LA are shown in the *SE Configuration*.

Table 10. Performance Plots, Typical SE Configurations

PLOT TITLE	FIGURE NUMBER
Total Harmonic Distortion + Noise vs. Output power	Figure 8
Output Power vs. Supply Voltage	Figure 9
Power Output vs. Case Temperature	Figure 10

8.2.4 Typical Differential (2N) PBTL Application

Design Requirements Typical Differential PBTL

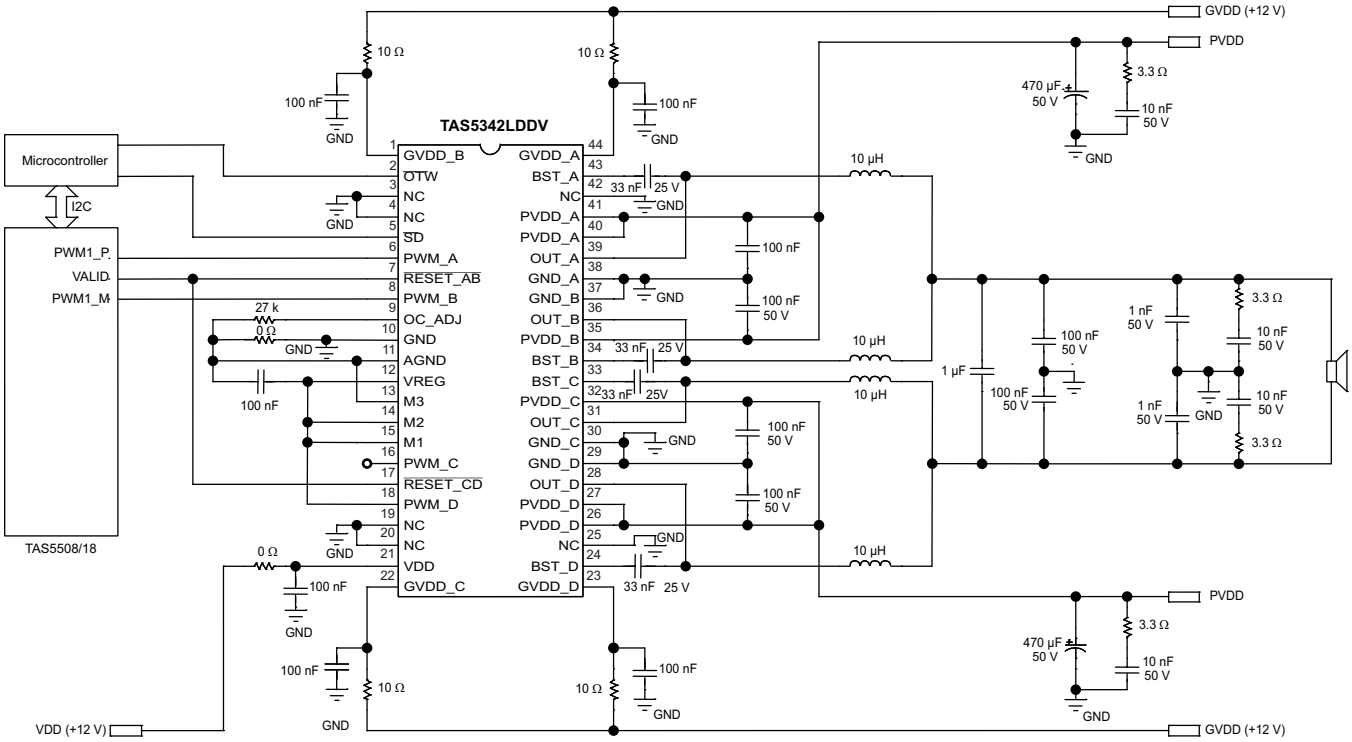

Figure 17. Typical Differential (2N) PBTL Application With AD Modulation Filters

8.2.4.1 Design Requirements

For this design example, use the parameters listed in Table 11 as the input parameters.

Table 11. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Low Power (pull-up) supply	3.3 V
Mid Power Supply (GVDD, VDD)	12 V
High Power Supply (PVDD)	12 V – 36 V
PWM Inputs	INPUT A = 0 – 3.3 V PWM
	INPUT_B = N/C
	INPUT_C = N/C
	INPUT_D = GND
Speaker Impedance	2 Ω – 3 Ω

8.2.4.2 Application Curves

Relevant performance plots for TAS5342LA are shown in the *PBTL Configuration*.

Table 12. Performance Plots, Typical PBTL Configurations

PLOT TITLE	FIGURE NUMBER
Total Harmonic Distortion + Noise vs. Output power	Figure 11
Output Power vs. Supply Voltage	Figure 12
Power Output vs. Case Temperature	Figure 13

8.2.5 Typical Non-Differential (1N) PBTL

Design Requirements Typical Non-Differential PBTL.

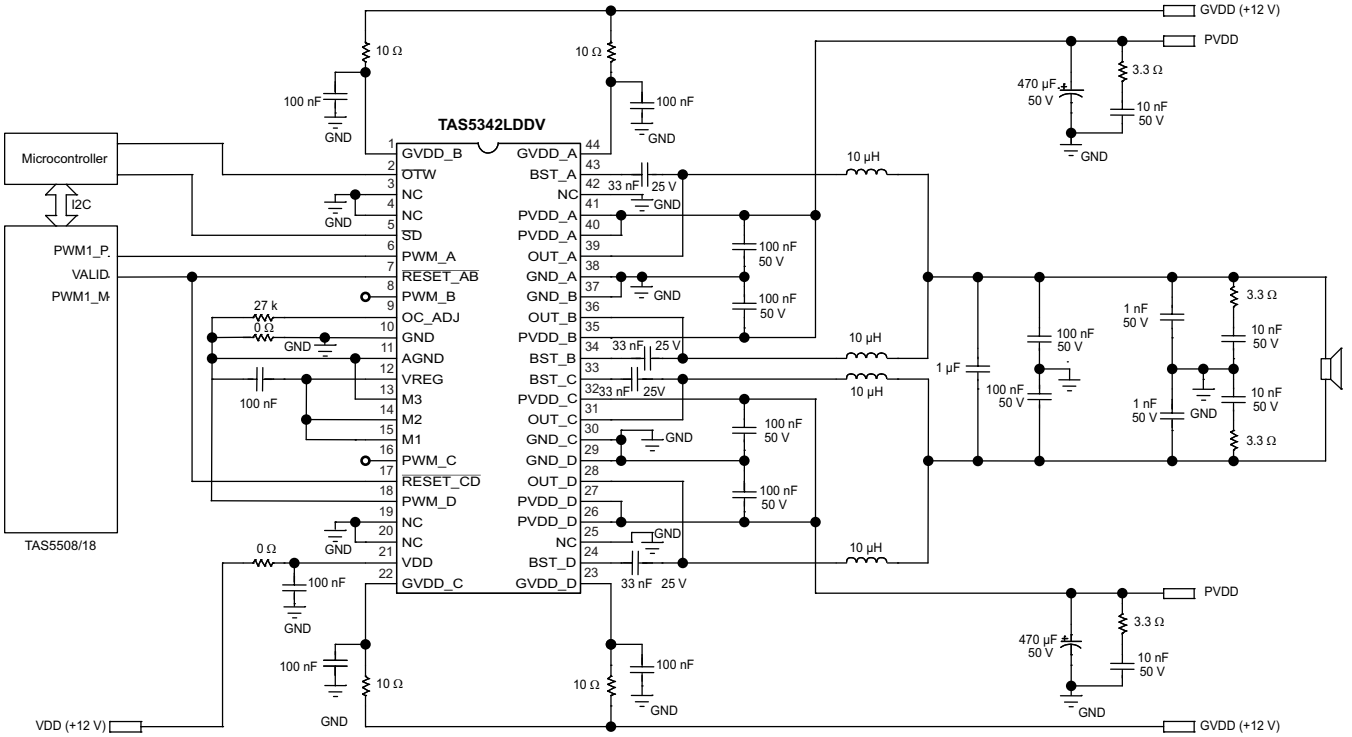

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Figure 18. Typical Non-Differential (1N) PBTL Application

8.2.5.1 Design Requirements

For this design example, use the parameters listed in Table 13 as the input parameters.

Table 13. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Low Power (pull-up) supply	3.3 V
Mid Power Supply (GVDD, VDD)	12 V
High Power Supply (PVDD)	12 V – 36 V
PWM Inputs	INPUT A = 0 – 3.3 V PWM
	INPUT_B = N/C
	INPUT_C = N/C
	INPUT_D = GND
Speaker Impedance	2 Ω – 3 Ω

8.2.5.2 Application Curves

Relevant performance plots for TAS5342LA are shown in the *PBTL Configuration*.

Table 14. Performance Plots, Typical PBTL Configurations

PLOT TITLE	FIGURE NUMBER
Total Harmonic Distortion + Noise vs. Output power	Figure 11
Output Power vs. Supply Voltage	Figure 12
Power Output vs. Case Temperature	Figure 13

8.3 Systems Examples

A block diagram for a typical audio system using the TAS5342LA is shown in Figure 19. The TAS5518 is an 8 channel digital audio PWM processor.

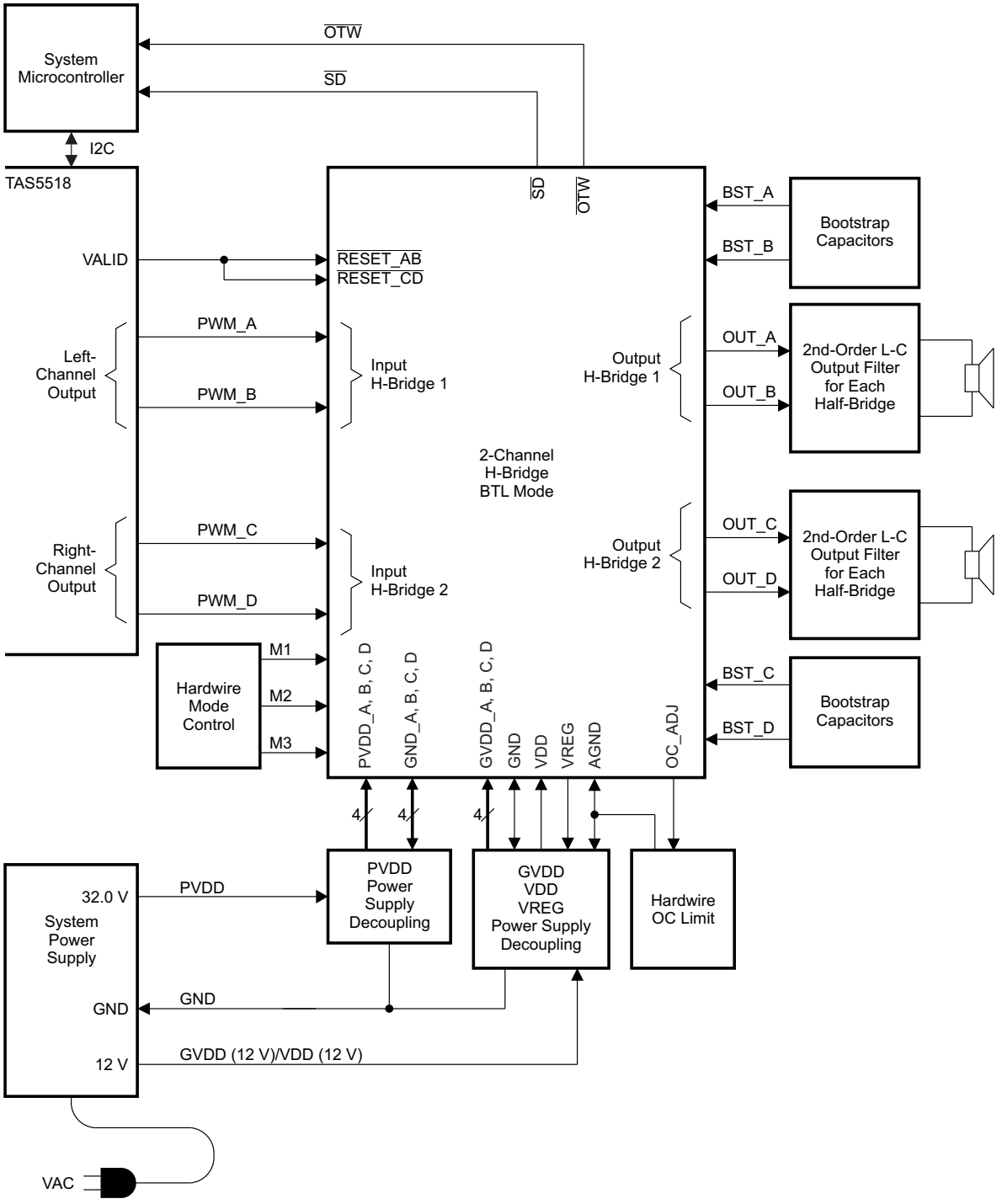

Figure 19. Typical Audio System

9 Power Supply Recommendations

To facilitate system design, the TAS5342LA needs only a 12-V supply in addition to the (typical) 32-V power-stage supply. An internal voltage regulator provides suitable voltage levels for the digital and low-voltage analog circuitry. Additionally, all circuitry requiring a floating voltage supply, for example, the high-side gate drive, is accommodated by built-in bootstrap circuitry requiring only an external capacitor for each half-bridge.

In order to provide outstanding electrical and acoustical characteristics, the PWM signal path including gate drive and output stage is designed as identical, independent half-bridges. For this reason, each half-bridge has separate gate drive supply (GVDD_X), bootstrap pins (BST_X), and power-stage supply pins (PVDD_X). Furthermore, an additional pin (VDD) is provided as supply for all common circuits. Although supplied from the same 12-V source, it is highly recommended to separate GVDD_A, GVDD_B, GVDD_C, GVDD_D, and VDD on the printed-circuit board (PCB) by RC filters (see application diagram for details). These RC filters provide the recommended high-frequency isolation. Special attention should be paid to placing all decoupling capacitors as close to their associated pins as possible. In general, inductance between the power supply pins and decoupling capacitors must be avoided. (See reference board documentation for additional information.)

For a properly functioning bootstrap circuit, a small ceramic capacitor must be connected from each bootstrap pin (BST_X) to the power-stage output pin (OUT_X). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive power-supply pin (GVDD_X) and the bootstrap pin. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a suitable voltage supply for the high-side gate driver. In an application with PWM switching frequencies in the range from 352 kHz to 384 kHz, it is recommended to use 33-nF ceramic capacitors, size 0603 or 0805, for the bootstrap supply. These 33-nF capacitors ensure sufficient energy storage, even during minimal PWM duty cycles, to keep the high-side power stage FET (LDMOS) fully turned on during the remaining part of the PWM cycle. In an application running at a reduced switching frequency, generally 192 kHz, the bootstrap capacitor might need to be increased in value.

Special attention should be paid to the power-stage power supply; this includes component selection, PCB placement, and routing. As indicated, each half-bridge has independent power-stage supply pins (PVDD_X). For optimal electrical performance, EMI compliance, and system reliability, it is important that each PVDD_X pin is decoupled with a 100-nF ceramic capacitor placed as close as possible to each supply pin. It is recommended to follow the PCB layout of the TAS5342LA reference design. For additional information on recommended power supply and required components, see the application diagrams given previously in this data sheet.

The 12-V supply should be from a low-noise, low-output-impedance voltage regulator. Likewise, the 32-V power-stage supply is assumed to have low output impedance and low noise. The power-supply sequence is not critical as facilitated by the internal power-on-reset circuit. Moreover, the TAS5342LA is fully protected against erroneous power-stage turnon due to parasitic gate charging. Thus, voltage-supply ramp rates (dV/dt) are non-critical within the specified range (see the *Recommended Operating Conditions* section of this data sheet).

10 Layout

10.1 Layout Guidelines

- Use an unbroken ground plane to have good low impedance and inductance return path to the power supply for power and audio signals.
- Maintain a contiguous ground plane from the ground pins to the PCB area surrounding the device for as many of the ground pins as possible, since the ground pins are the best conductors of heat in the package.
- PCB layout, audio performance and EMI are linked closely together.
- Routing the audio input should be kept short and together with the accompanied audio source ground.
- The small bypass capacitors on the PVDD lines of the DUT be placed as close the PVDD pins as possible.
- A local ground area underneath the device is important to keep solid to minimize ground bounce.
- Orient the passive component so that the narrow end of the passive component is facing the TAS5342LA device, unless the area between two pads of a passive component is large enough to allow copper to flow between the two pads.
- Avoid placing other heat producing components or structures near the TAS5342LA device.
- Avoid cutting off the flow of heat from the TAS5342IA device to the surrounding ground areas with traces or via strings, especially on output side of device.

10.2 Layout Example

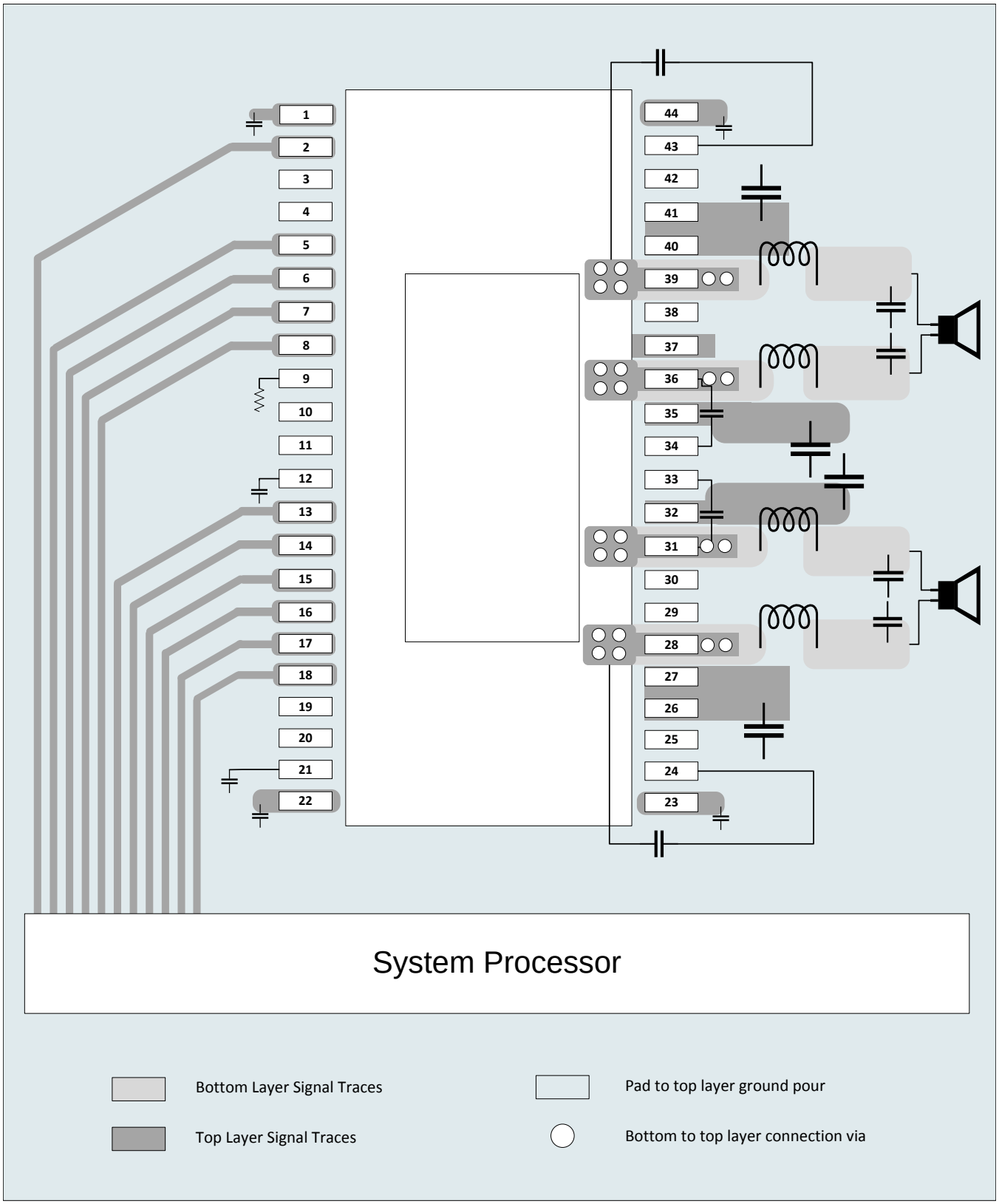

Figure 20. Example Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *TAS5342LDDV6EVM User Guide* (SLAU243)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TAS5342LADDV	ACTIVE	HTSSOP	DDV	44	35	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 70	TAS5342LA	Samples
TAS5342LADDVR	ACTIVE	HTSSOP	DDV	44	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 70	TAS5342LA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

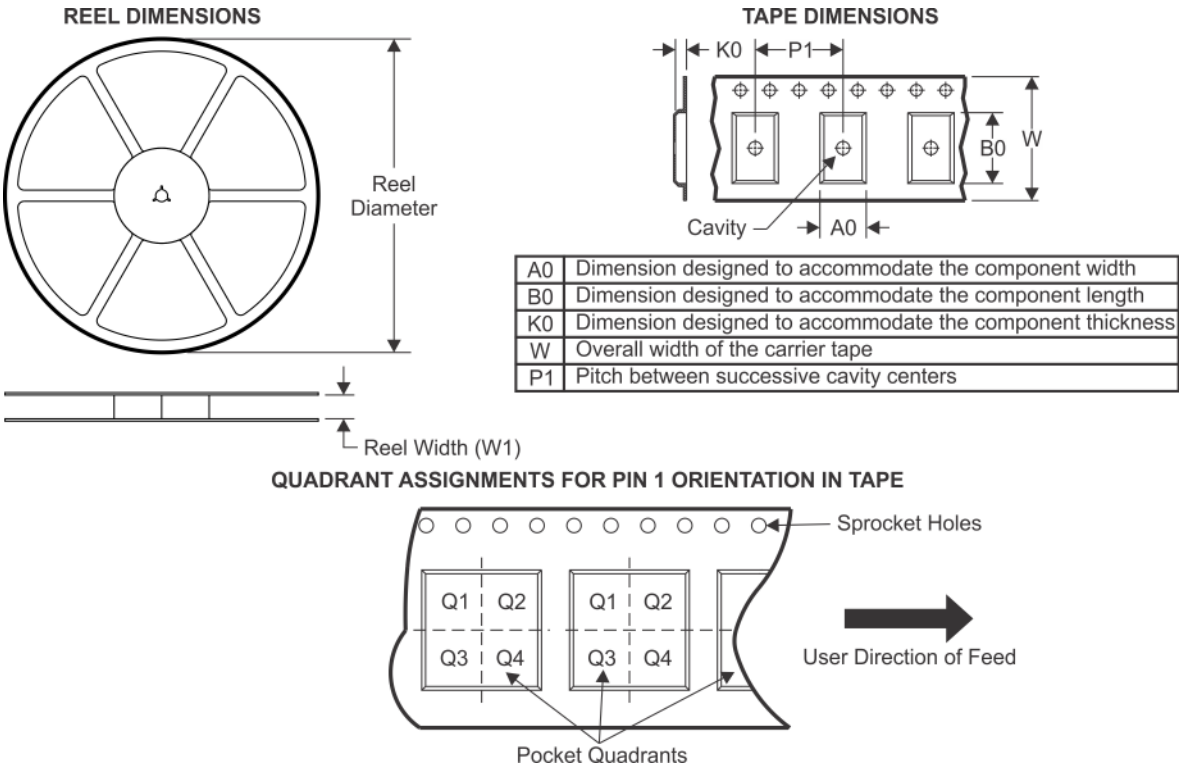
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

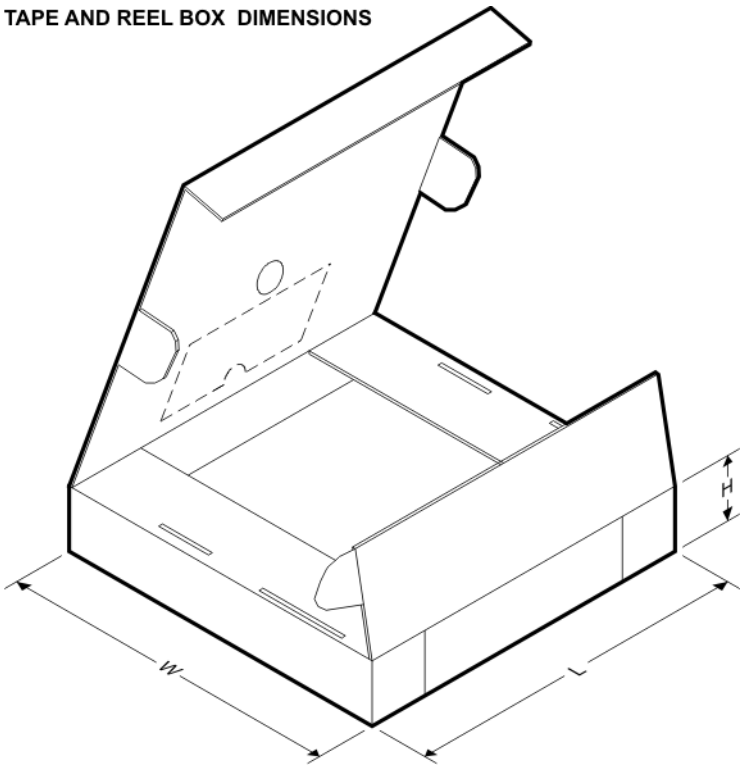


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS5342LADDVR	HTSSOP	DDV	44	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1

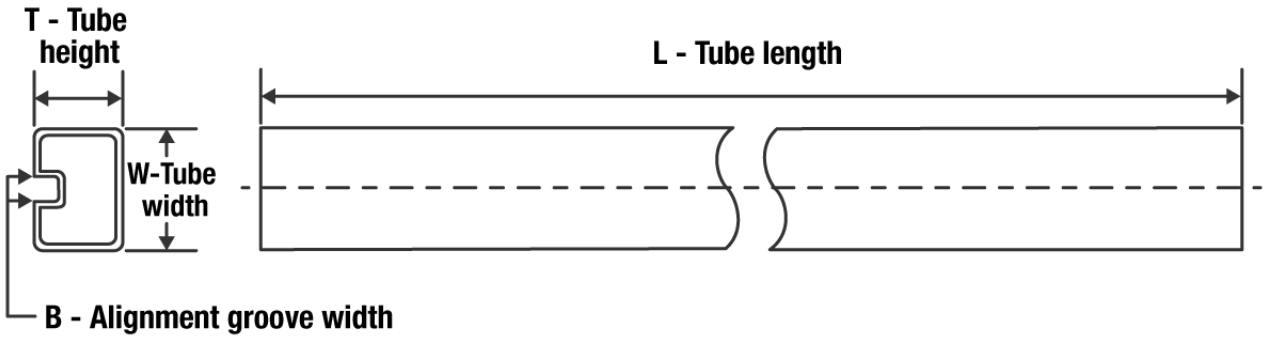
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS5342LADDVR	HTSSOP	DDV	44	2000	350.0	350.0	43.0

TUBE

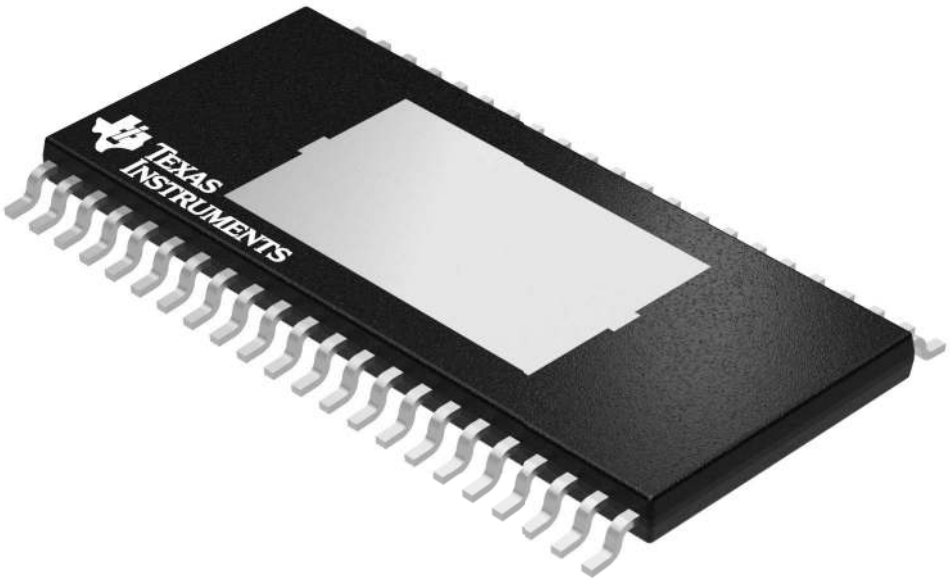


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TAS5342LADDV	DDV	HTSSOP	44	35	530	11.89	3600	4.9

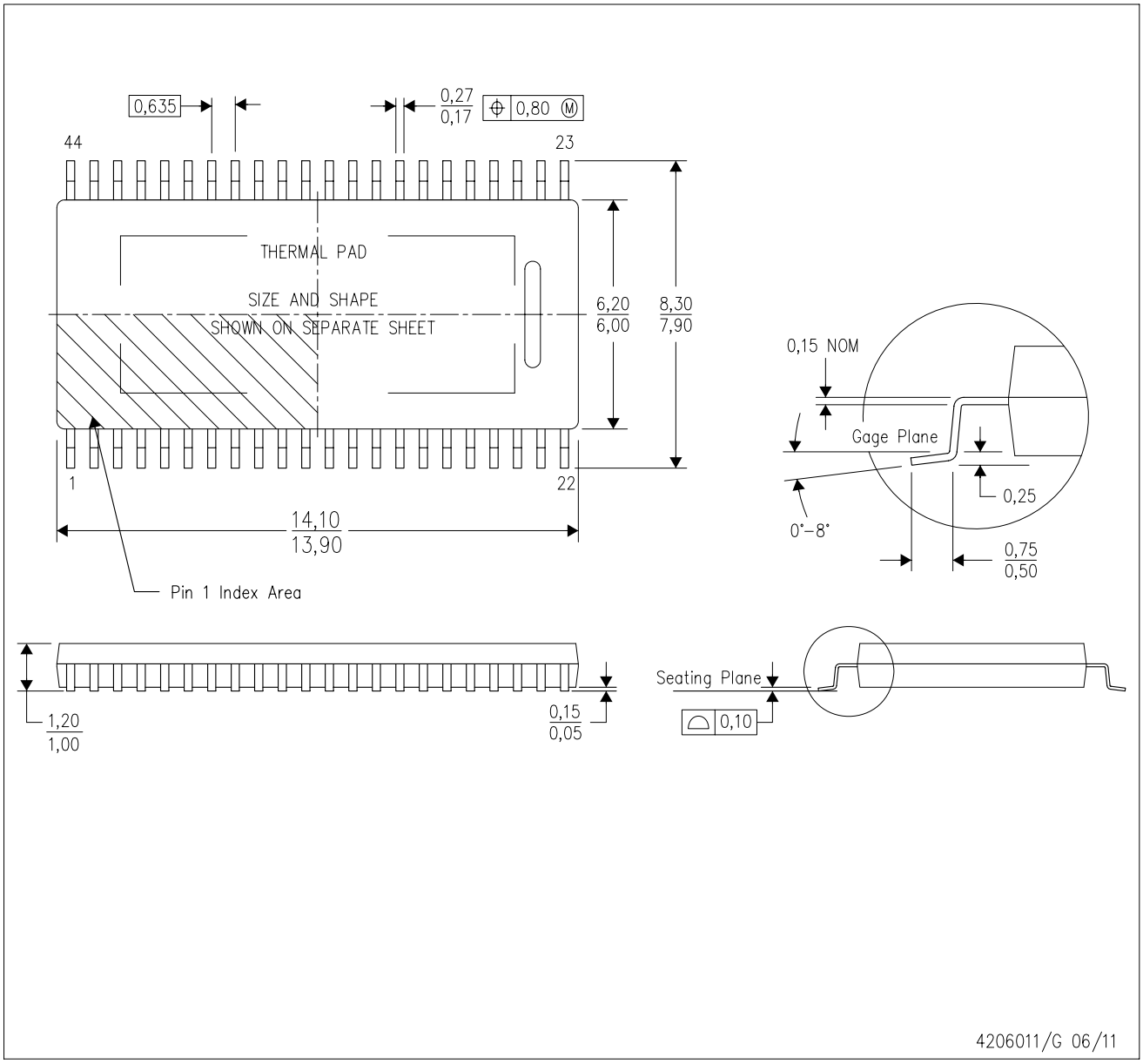
DDV 44 PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DDV (R–PDSO–G44) PowerPAD™ PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be attached directly to an external heatsink. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>. See the product data sheet for details regarding the exposed thermal pad dimensions.

PowerPAD is a trademark of Texas Instruments.

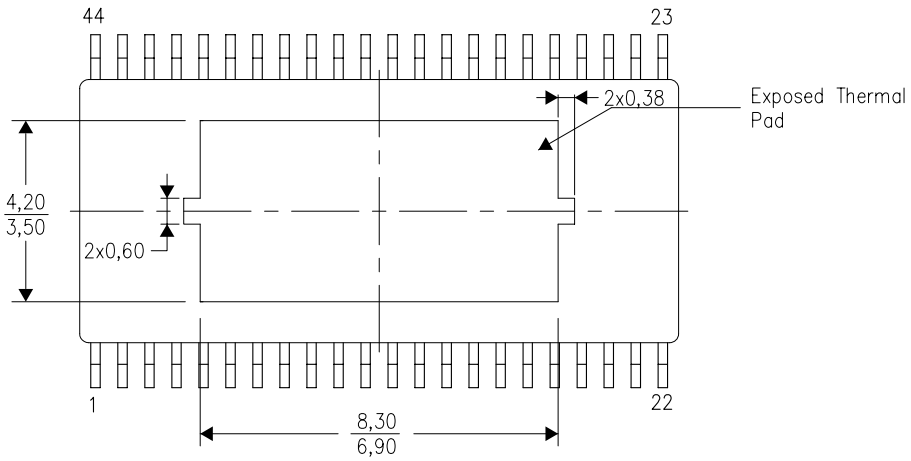
DDV (R–PDSO–G44) PowerPAD ™SMALL OUTLINE PACKAGE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206975–2/D 07/11

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

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