

Dual P-Channel 60-V (D-S) 175° MOSFET

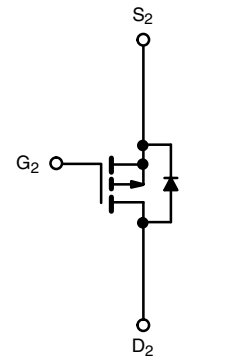
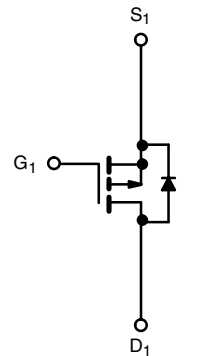
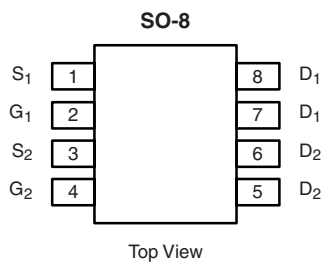
| PRODUCT SUMMARY | | |
|-----------------|-----------------------------|-----------|
| V_{DS} (V) | $R_{DS(on)}$ (Ω) | I_D (A) |
| - 60 | 0.120 at $V_{GS} = - 10$ V | - 3.1 |
| | 0.150 at $V_{GS} = - 4.5$ V | - 2.8 |

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE
Available



Ordering Information: Si4948BEY-T1-E3 (Lead (Pb)-free)
Si4948BEY-T1-GE3 (Lead (Pb)-free and Halogen-free)

| ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted | | | | |
|--|----------------|---------------|--------------|-------|
| Parameter | Symbol | 10 s | Steady State | Unit |
| Drain-Source Voltage | V_{DS} | - 60 | | V |
| Gate-Source Voltage | V_{GS} | ± 20 | | |
| Continuous Drain Current ($T_J = 150$ °C) ^a | I_D | $T_A = 25$ °C | - 3.1 | - 2.4 |
| | | $T_A = 70$ °C | - 2.6 | - 2.0 |
| Pulsed Drain Current (10 μ s Pulse Width) | I_{DM} | - 25 | | A |
| Continuous Source Current (Diode Conduction) ^a | I_S | - 2 | - 1.1 | |
| Avalanche Current | I_{AS} | 15 | | |
| Single Pulse Avalanche Energy | E_{AS} | 11 | | mJ |
| Maximum Power Dissipation ^a | P_D | $T_A = 25$ °C | 2.4 | 1.4 |
| | | $T_A = 70$ °C | 1.7 | 0.95 |
| Operating Junction and Storage Temperature Range | T_J, T_{stg} | - 55 to 175 | | °C |

| THERMAL RESISTANCE RATINGS | | | | | |
|--|------------|---------------|---------|------|------|
| Parameter | Symbol | Typical | Maximum | Unit | |
| Maximum Junction-to-Ambient ^a | R_{thJA} | $t \leq 10$ s | 53 | 62.5 | °C/W |
| | | Steady State | 85 | 110 | |
| Maximum Junction-to-Foot | R_{thJF} | 30 | 37 | | |

Notes:

a. Surface Mounted on 1" x 1" FR4 board.



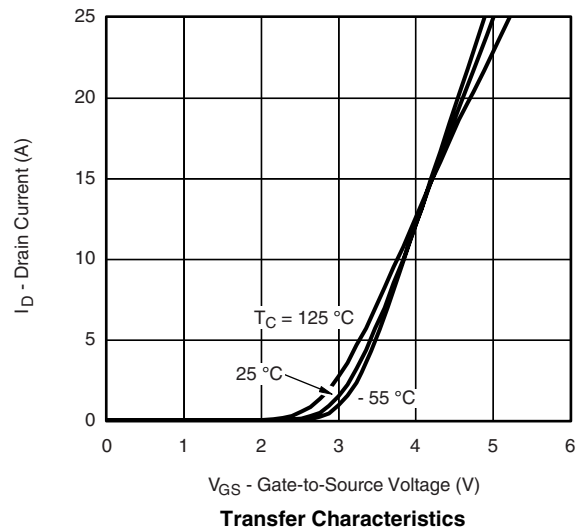
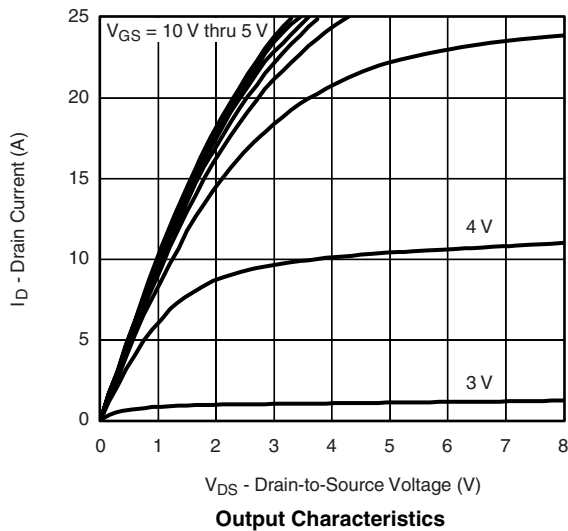
| SPECIFICATIONS $T_J = 25^\circ\text{C}$, unless otherwise noted | | | | | | |
|--|--------------|--|------|-------|-----------|---------------|
| Parameter | Symbol | Test Conditions | Min. | Typ. | Max. | Unit |
| Static | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$ | -1 | | -3 | V |
| Gate-Body Leakage | I_{GSS} | $V_{DS} = 0\ \text{V}, V_{GS} = \pm 20\ \text{V}$ | | | ± 100 | nA |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS} = -60\ \text{V}, V_{GS} = 0\ \text{V}$ | | | -1 | μA |
| | | $V_{DS} = -60\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 70^\circ\text{C}$ | | | -10 | |
| On-State Drain Current ^a | $I_{D(on)}$ | $V_{DS} = -5\ \text{V}, V_{GS} = -10\ \text{V}$ | -25 | | | A |
| Drain-Source On-State Resistance ^a | $R_{DS(on)}$ | $V_{GS} = -10\ \text{V}, I_D = -3.1\ \text{A}$ | | 0.100 | 0.120 | Ω |
| | | $V_{GS} = -4.5\ \text{V}, I_D = -0.2\ \text{A}$ | | 0.126 | 0.150 | |
| Forward Transconductance ^a | g_{fs} | $V_{DS} = -15\ \text{V}, I_D = -3.1\ \text{A}$ | | 8.5 | | S |
| Diode Forward Voltage ^a | V_{SD} | $I_S = -2\ \text{A}, V_{GS} = 0\ \text{V}$ | | -0.8 | -1.2 | V |
| Dynamic^b | | | | | | |
| Total Gate Charge | Q_g | $V_{DS} = -30\ \text{V}, V_{GS} = -10\ \text{V}, I_D = -3.1\ \text{A}$ | | 14.5 | 22 | nC |
| Gate-Source Charge | Q_{gs} | | | 2.2 | | |
| Gate-Drain Charge | Q_{gd} | | | 3.7 | | |
| Gate Resistance | R_g | $f = 1\ \text{MHz}$ | | 14 | | Ω |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD} = -30\ \text{V}, R_L = 30\ \Omega$ $I_D \cong -1\ \text{A}, V_{GEN} = -10\ \text{V}, R_g = 6\ \Omega$ | | 10 | 15 | ns |
| Rise Time | t_r | | | 15 | 22 | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | 50 | 75 | |
| Fall Time | t_f | | | 35 | 55 | |
| Source-Drain Reverse Recovery Time | t_{rr} | $I_F = -2\ \text{A}, dI/dt = 100\ \text{A}/\mu\text{s}$ | | 30 | 50 | |

Notes:

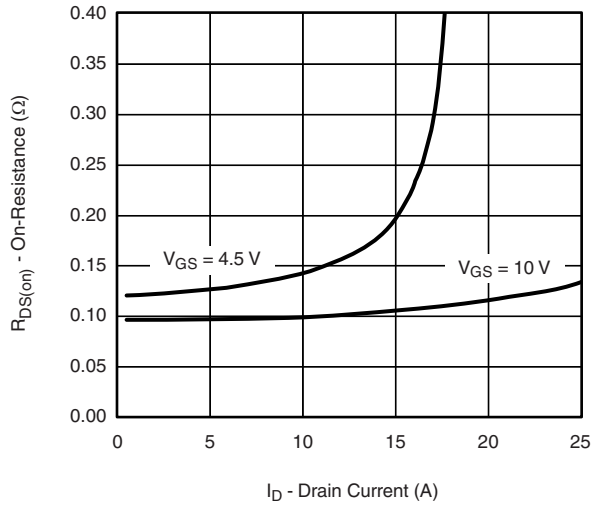
- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

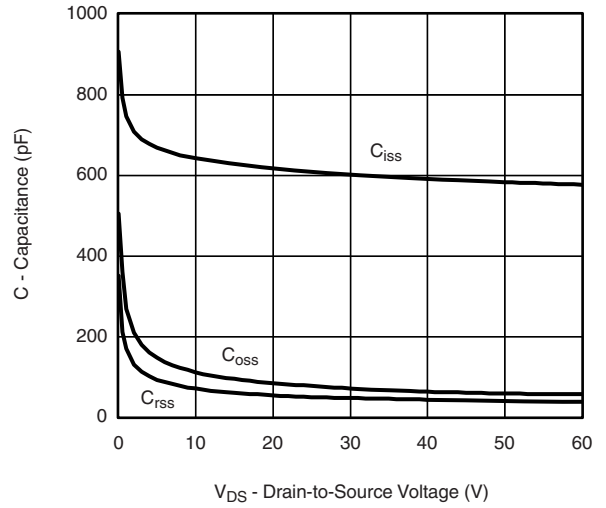
TYPICAL CHARACTERISTICS 25°C , unless otherwise noted



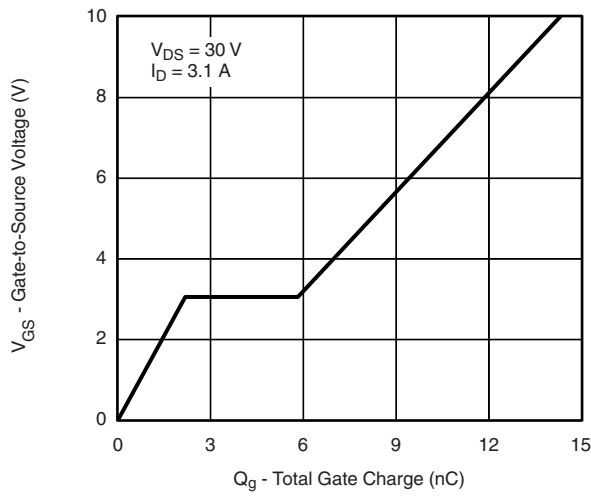
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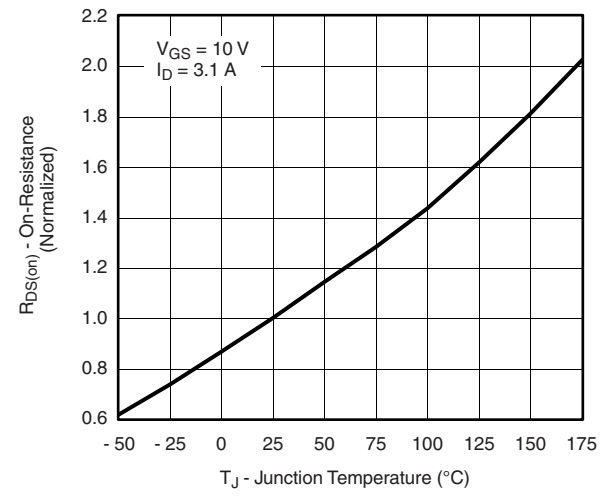
On-Resistance vs. Drain Current



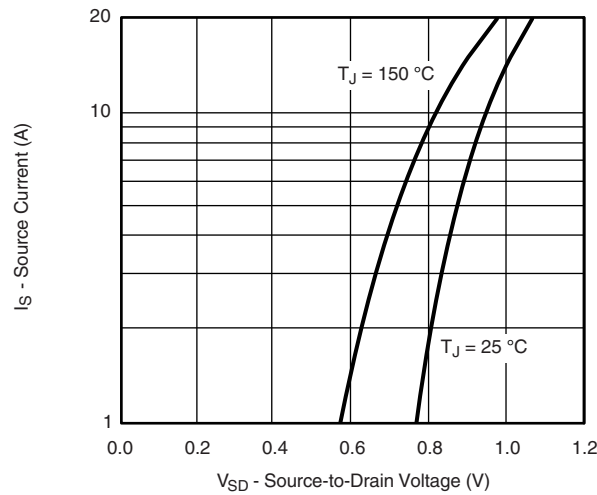
Capacitance



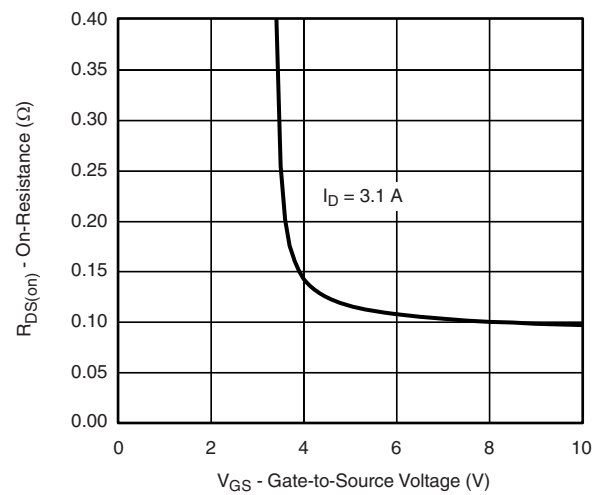
Gate Charge



On-Resistance vs. Junction Temperature

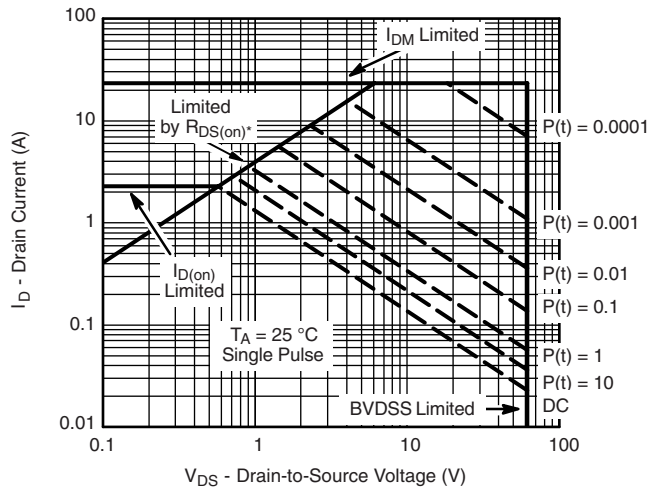
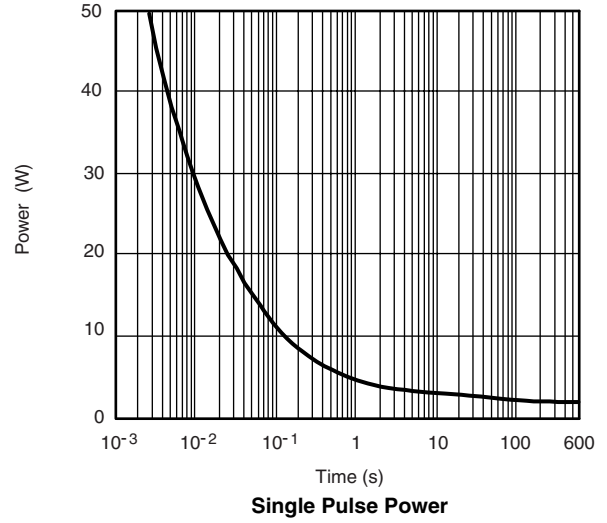
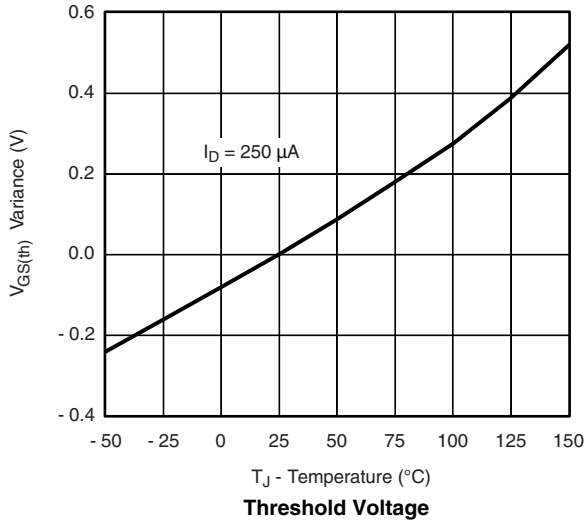


Source-Drain Diode Forward Voltage

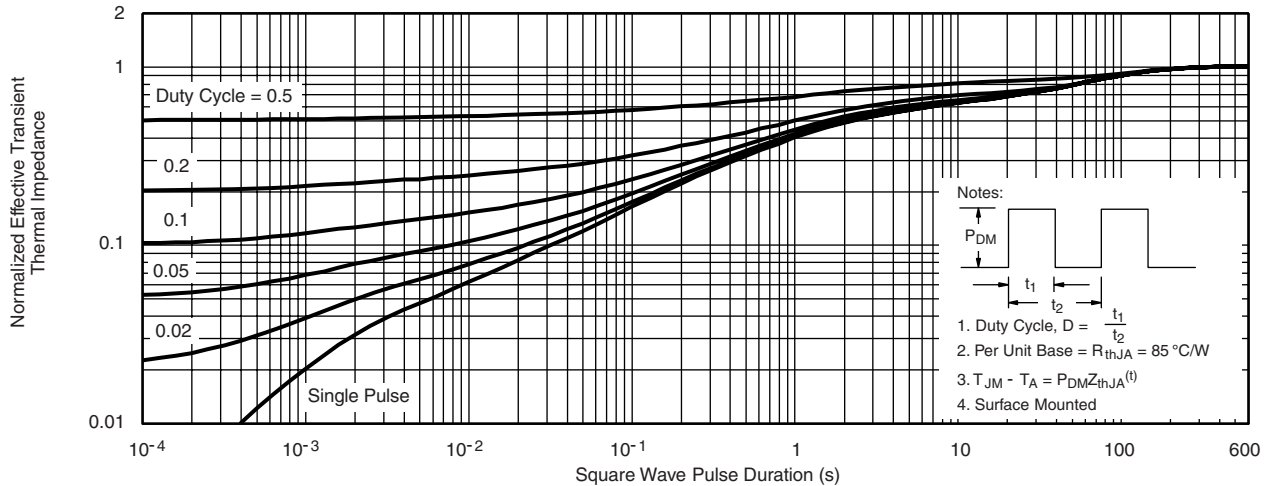


On-Resistance vs. Gate-to-Source Voltage

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

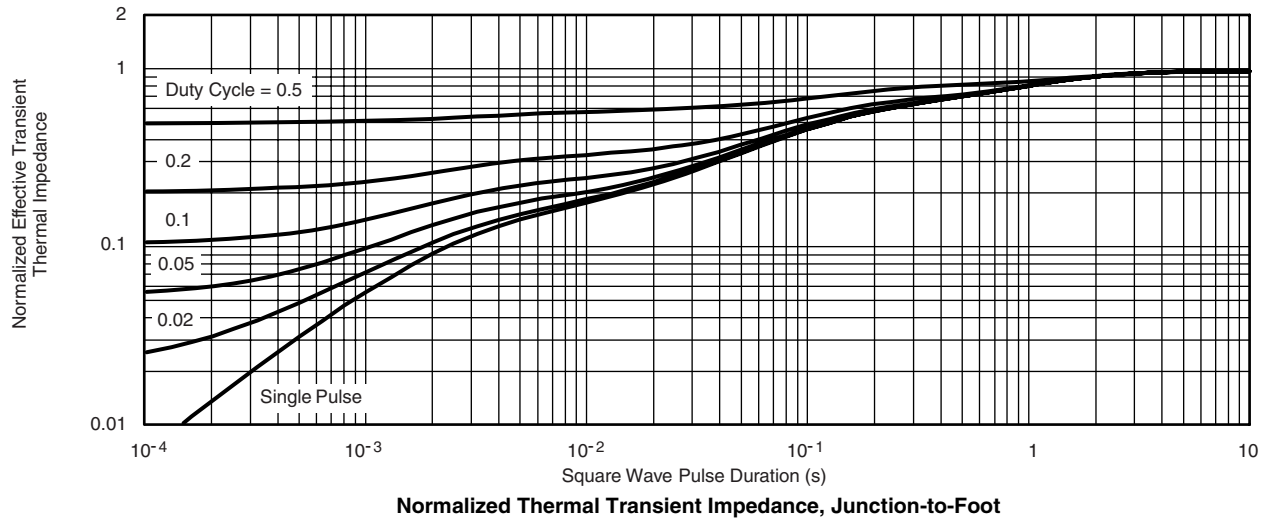


* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



- Notes:
1. Duty Cycle, $D = \frac{t_1}{t_2}$
 2. Per Unit Base = $R_{thJA} = 85 \text{ }^\circ\text{C/W}$
 3. $T_{JM} - T_A = P_{DM} Z_{thJA}^{(t)}$
 4. Surface Mounted

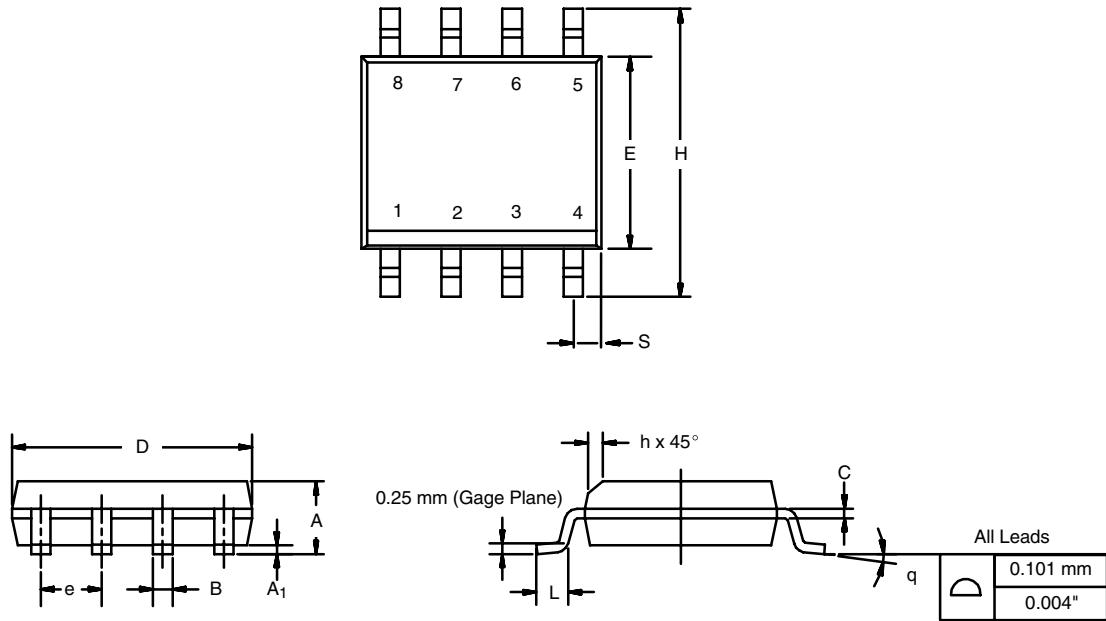
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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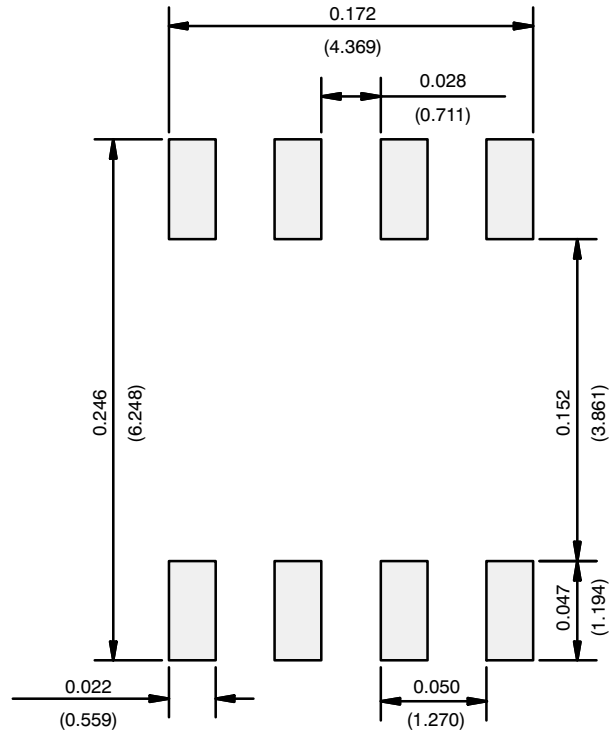
SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



| DIM | MILLIMETERS | | INCHES | |
|--------------------------------|-------------|------|-----------|-------|
| | Min | Max | Min | Max |
| A | 1.35 | 1.75 | 0.053 | 0.069 |
| A ₁ | 0.10 | 0.20 | 0.004 | 0.008 |
| B | 0.35 | 0.51 | 0.014 | 0.020 |
| C | 0.19 | 0.25 | 0.0075 | 0.010 |
| D | 4.80 | 5.00 | 0.189 | 0.196 |
| E | 3.80 | 4.00 | 0.150 | 0.157 |
| e | 1.27 BSC | | 0.050 BSC | |
| H | 5.80 | 6.20 | 0.228 | 0.244 |
| h | 0.25 | 0.50 | 0.010 | 0.020 |
| L | 0.50 | 0.93 | 0.020 | 0.037 |
| q | 0° | 8° | 0° | 8° |
| S | 0.44 | 0.64 | 0.018 | 0.026 |
| ECN: C-06527-Rev. I, 11-Sep-06 | | | | |
| DWG: 5498 | | | | |

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

[Return to Index](#)



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