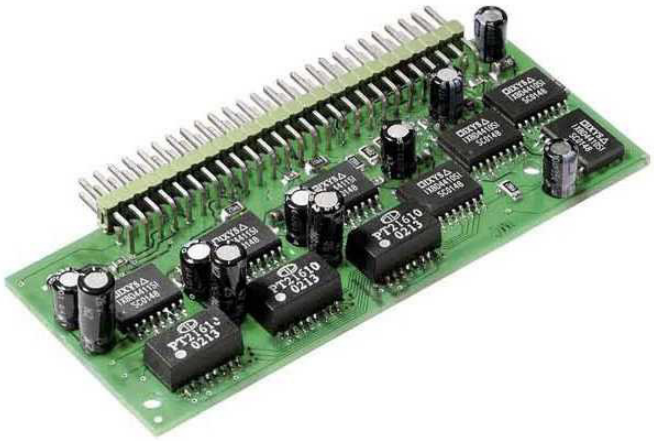
Driver Unit for Converter-Brake-Inverter Modules

Preliminary data

Application and Features

The driver board constitutes a high performance interface between drive controller and power section of a variable speed AC drive, consisting of six plus one transistors for a three phase inverter with constant voltage DC link and a brake chopper. Pinout is especially matched to IXYS MUBW...7/8 or corresponding industry standard IGBT modules.

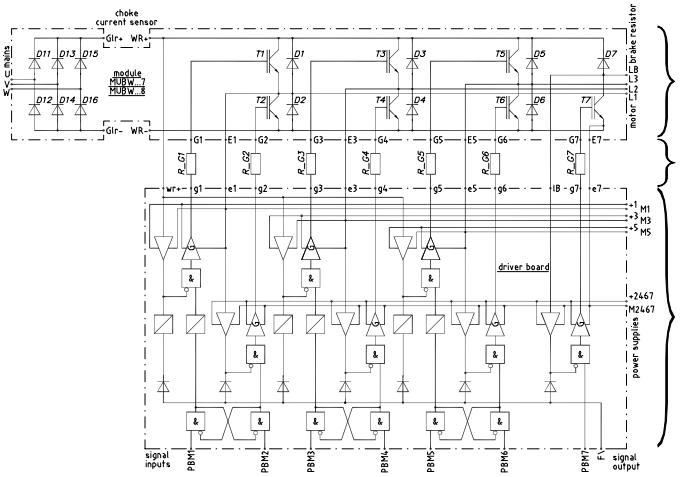


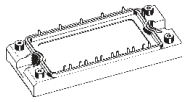
The board provides:
- logic interface to the controller
  - one control signal for each transistor
  - feedback signal for fault condition
- magnetically isolated signal transmission from ground referenced low side to high side potentials and vice versa with high du/dt immunity
- one drive output to each transistor
  - high current gate drive with negative off-voltage generated on board
  - U_{CEsat} supervision for overcurrent protection
- protection schemes against
  - overcurrent/short circuit
  - cross conduction
  - supply under- or overvoltage
- power supply inputs for
  - either a single ground referenced supply voltage and bootstrap circuits for the high side drivers
  - or one single ground referenced and three single high side supply voltages

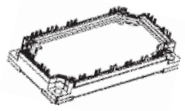
It is intended for use as turn-key interface between controller and power section.

The board uses IXYS proprietary driver IC chipset IXBD4410/ IXBD4411, where IXBD4410 is the low and IXBD4411 the high side driver – see also the respective data sheet.

Funtional Block Diagram







Logic Interfaces

Logic interface comprises seven input signals PBM1 to PBM7:

- PBM1 controls transistor T1, PBM2 controls transistor T2; cross conduction interlock prevents both transistors from being turned on at the same time.
- PBM3 controls transistor T3, PBM4 controls transistor T4; cross conduction interlock prevents both transistors from being turned on at the same time.
- PBM5 controls transistor T5, PBM6 controls transistor T6; cross conduction interlock prevents both transistors from being turned on at the same time.
- PBM7 controls brake transistor T7.

All PBM signals have the following properties:

- They are ground referenced, i.e. refer to potential of minus DC link.
- Logic 1 turns the transistor on, logic 0 turns it off.
- The signals are TTL/CMOS compatible.
- A pull down resistor of 4,7 kΩ is provided on board.

Further, an output F\ signal indicating fault status is provided, see section Protection Schemes

Symbol	Definitions	Ratings	
v_{DD}	Input Voltage (PBM1...7)	-0.5...V_{DD} +0.5	V
I_{in}	Input Current (PBM1...7)	±10	A
t_p	min. high/low pulse width for PBM1/3/5	1	µs

Isolated Signal Transmission

In the driver unit the high-side ICs are isolated from the low-side ICs by magnetic barriers. There are two magnetic transmission channels between the low- and high-side ICs for bidirectional communication. One sends a signal from the low-side IXBD4410 IC up to the high-side IXBD4411 IC and the other sends a signal back from the high-side to the low-side IC. The signal that is sent up controls the IXBD4411 gate-drive output. The signal sent from the IXBD4411 back to the IXBD4410 indicates a high-side fault has occurred which is detected at the IXBD4410 IC. Magnetically coupled signal transmission leads to high immunity against disturbances caused by voltage change rates du/dt, which necessarily occur in power electronic phaseleg circuits.

Symbol	Definitions	Max. Ratings	
L_{Gb} / L_{GI}	maximum common mode dv/dt	±50	V/ns

Symbol	Definitions/Conditions	Characteristic Values min.	typ.	max.	
d_S	creepage distance on board between high & low side potential	2			mm

422

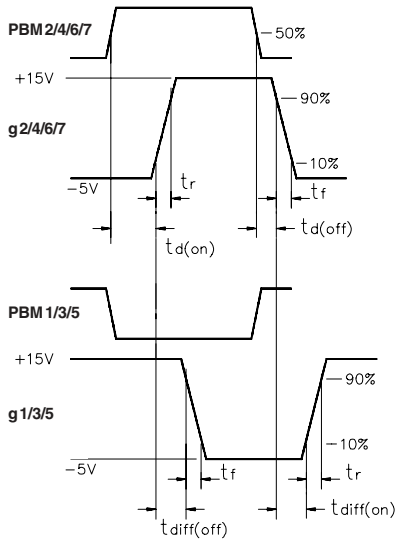
Transistor Drive

The driver unit provides the necessary gate drive signals to fully control the grounded-emitter low-side power devices as well as the floating-emitter high-side power devices including a negative-going, off-state gate drive signal for improved turn-off of IGBTs: Both the IXBD4410 and IXBD4411 ICs contain on-board negative charge pumps to provide negative gate drive V_{EE}, which ensures turn-off of the high- or low-side power device in the presence of currents induced by power device Miller capacitance or from inductive ground transients. These charge pumps provide -5 V relative to the local driver ground when V_{DD} is at +15 V, and at average currents of 25mA.

Symbol	Definitions	Max. Ratings	
I_o (rev)	peak reverse output current g1...g7	2	A

Symbol	Definitions/Conditions		Characteristic Values (T_{VJ} = 25°C, V_{DD} = 15 V unless otherwise specified) min.	typ.	max.	
VEE Supply (referred to M2467/M1/M3/M5)						
V_{EE}	output voltage; I_C = 1mA; C_S = 1µF		-5	-6.5	-7.5	V
I_{out}	output current; V_{out} = 0,7 • V_{EE}		-20	-25		mA
Output g1...g7 Characteristics						
V_{oh}	HI Output/I_o = -5 mA		V_{DD}-0.05			V
V_{ol}	LO Output/I_o = 5 mA			V_{EE}+0.05		V
R_o	Output HI Res./I_o = -0.1 A			3	5	Ω
R_o	Output LO Res./I_o = 0.1 A			3	4	Ω
I_{pk}	Peak Output Current/C_L = 10 nF		1.5	2		A
Switching times						
$t_{d(on)}$	4410 Turn-on delay time;	C_L = 1 nF		110	175	ns
t_r	Rise time;	C_L = 10 nF		70	100	ns
		C_L = 1 nF		15	20	ns
$t_{d(off)}$	4410 Turn-off delay time	C_L = 1 nF		70	150	ns
t_f	Fall time	C_L = 10 nF		70	150	ns
		C_L = 1 nF		15	20	ns
$t_{dlh(off)}$	4410 Turn-on delay time vs. 4411 Turn-off delay time	C_L = 1 nF		60	150	ns
$t_{dlh(on)}$	4410 Turn-on delay time vs. 4411 Turn-off delay time	C_L = 1 nF		60	150	ns

Waveform reference



422

On board gate resistors of R_{Gint} = 4,7 Ω are provided between the outputs of the IXBD4410/4411 ICs and the respective terminals g1...g7. Total gate resistance R_G for operation of the IGBTs should be adjusted by addition of an external gate resistor R_{Gext} in each gate wire on the printed circuit board, connecting the driver unit and the CBI module, according to:
$R_G = R_{Gint} + R_{Gext}$
It is recommended to use total gate resistors R_G for inverter and brake chopper as specified in the respective module data sheets. Circuitry according to figure 1 may be added to adjust current and voltage change rates during commutations and for protection purposes.

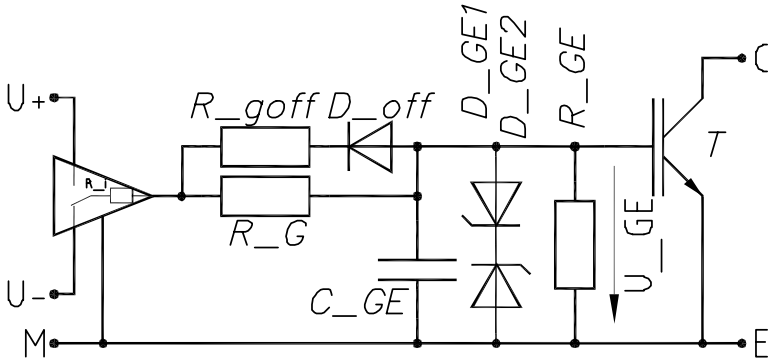


Figure 1: optional gate circuitry between driver unit and CBI module

Protection Schemes

To assure maximum protection for the power devices, the driver unit incorporates the following IGBT protection schemes:

- protection from cross conduction of the half bridge, see section Logic Interfaces
- power device overcurrent or desaturation protection: The IXBD4410/4411 IC will turn off the driven device, supposed to be turned on since at least 3 µs typ., within 150 ns of sensing an output overcurrent or desaturation condition, i. e. U_{CE} >10 V typ. Measurement is taken with a resistive voltage divider, limiting device blocking and thus DC link voltage to U_Z = 800V.
- under-voltage gate-drive lockout on the low- and/or high- side drivers whenever the respective positive power supply V_{DD} falls below 9.5 V typically
- over-voltage gate-drive lockout on the low- and high- side drivers whenever the respective negative power supply V_{EE} rises above -3 V typically, cf. section Transistor Drive
- During power-up, the chipset's gate-drive outputs will be low (off), until the voltage reaches the supply voltage trip points.

During a status fault, high side or low side driver IC of the concerned phaselegs keep their respective outputs off at V_{EE} as long as supplied. The overcurrent fault condition is latched, which is reset on the next positive transition of the respective input PBM1...PBM7, provided that the fault condition is not applicable any more.
Further the driver unit provides a logic compatible fault indication: Activation of open drain output F\ indicates a fault in any of the low or high side drivers. This signal can be utilised by a superceeding control unit on ground – i.e. DC link minus – potential, e.g. a microprocessor. The high level when F\ is not activated should be supplied by an external pull up resistor connected to the appropriate supply voltage.

Symbol	Definitions	Max. Ratings	
V_{DD}/V_{EE}	Supply Voltage	-0.5 ... 24	V

Symbol	Definitions/Conditions	Characteristic Values (T_{VJ} = 25°C, V_{DD} = 15 V unless otherwise specified) min.	typ.	max.	
V_{DD} Undervoltage Lockout					
V_{uv}	Drop out	9.5	10.5	11.5	V
V_{uh}	Hysteresis	0.1	0.15	0.3	V
VEE Supply (referred to M2467/M1/M3/M5)					
V_{EEF}	Over-voltage fault indication	-4.8		-3	V
Open Drain Fault Output (referred to M2467)					
V_{oh}	HI output / R_{pu} = 10 kΩ to V_{DD}	V_{DD}-0.05			V
V_{ol}	LO output / I_o = 4 mA		0.3	0.5	V
Quiescent Power Supply Current per Driver IC					
I_{DD}	V_{DD} current / V_{in}= V_{DD} or LG, I_o = 0			20	mA

422

Power Supply

One power supply with a single, ground referenced voltage V_{DD} is required for all four low side drivers within the driver unit together. It shall be connected between the terminals +2467 (plus) and M2467 (ground).

The high side drivers for transistors T1, T3 and T5 can be supplied in one of the following ways:

- power supplies on separate potentials
  - Those typically make use of additional secondary windings of the transformer which is used in an existing auxiliary switched mode power supply anyway. However only one output voltage can be controlled in this case.
  - Alternatively, DC-DC converters with high insulation voltage might be used.
- bootstrap circuit

  The circuit is exemplary shown for a phase-leg in figure 2:
  - When low side transistor T2 or diode D2 is conducting, high side ground M1 is on potential of low side ground M2 plus saturation voltage U_{CEsat} of T2 or minus forward voltage U_F of D2. Plus of low side driver supply +2 thus can charge the buffer capacitor for the high side driver supply C_{V1} via high voltage diode D_B and current limiting resistor R_B.
  - When low side transistor T2 and diode D2 are off, high side transistor T1 can be driven with the charge stored in C_{V1}. When T1 or D1 are conducting, bootstrap diode is blocking about DC link voltage.

It should thus be noted that

- regular turn on of T2 or D2 is mandatory for operation of this circuit, otherwise there is no supply for T1 driver
- T1 driver supply voltage level is quite inaccurate, also depending on T2 U_{CEsat} or D2 U_F respectively
- bootstrap diode D_B has to be rated for operation with DC link voltage
- bootstrap resistor R_B should be sized in a way that charging of C_{V1} is effectuated within the minimum on time of T2 or D2 respectively
- bootstrap diode D_B and resistor R_B have to sustain the charging current peaks.

Bootstrap circuits for the three high side drivers can easily be placed on the printed circuit board, the driver unit is connected to, between pins +2467 and +1 or +3 or +5 respectively.

Generally, supply voltage levels of V_{DD} = 15 V are recommended.

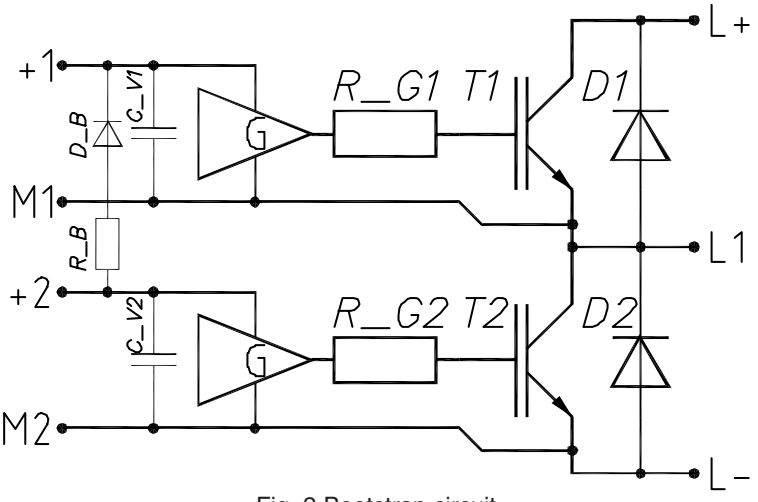


Fig. 2 Bootstrap circuit

Symbol	Definitions/Conditions	Characteristic Values (T_{VJ} = 25°C, V_{DD} = 15 V unless otherwise specified) min.	typ.	max.	
Quiescent Power Supply Current					
I_{DD}	V_{DD} Current/V_{in} = V_{DD} or LG, I_D = 0			20	mA

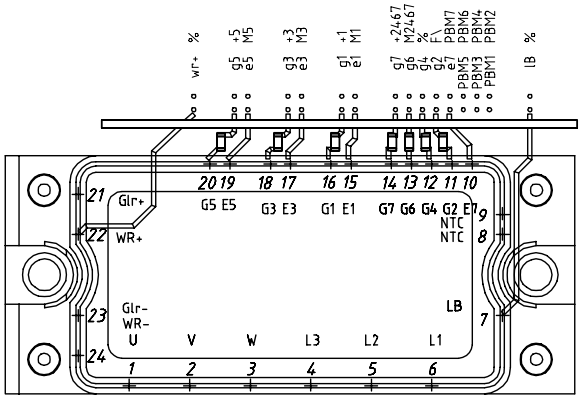
422

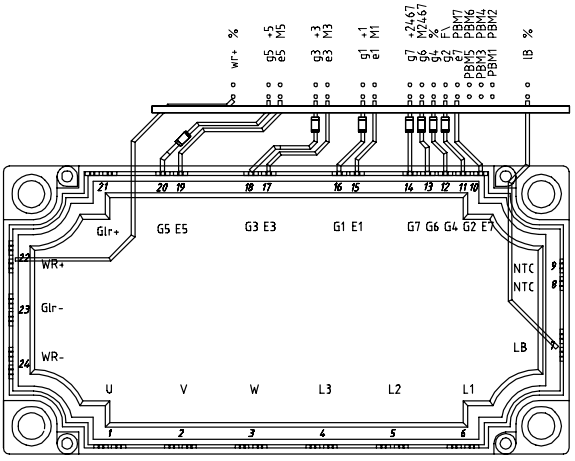
Dimensions, Pinout and Assembly

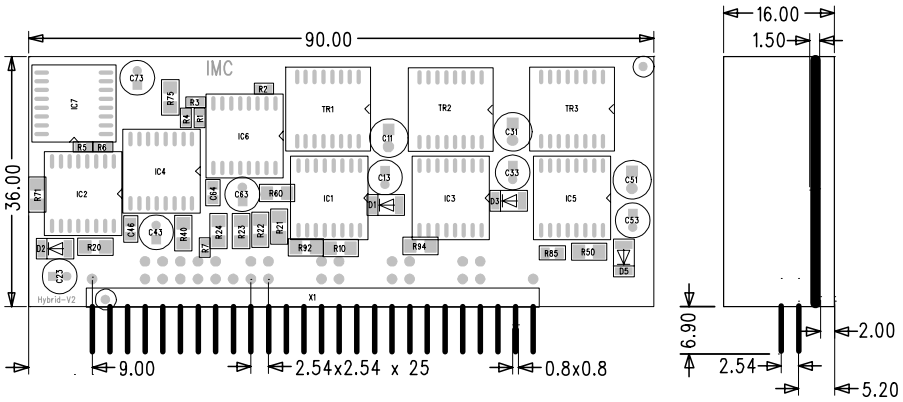
The driver unit has been realised as a printed circuit board with a two row connector according to figure 3. The pinout indicated in figure 4 is arranged in a way that

- wires connecting the gate outputs g1...g7/e1/e3/e5/e7 of driver unit with the control inputs G1..G7/E1/E3/E5/E7 of CBI module on the power printed circuit board can be routed with a simple shape; an arrangement of wires and SMD gate resistors – cf. section Transistor Drive – for two types of industry standard modules is proposed in figure 4
- neighbouring pins in the 2,54 mm grid carry electrically close potentials while different high potentials are separated by one additional pin being not connected; this also facilitates external wiring with sufficient spacing for isolation
- power supplies or bootstrap circuits according to section Power Supply can be easily connected
- all logic interface signal pins according to section Logic Interfaces are grouped together.

The pins should be sodered into the power printed circuit board. Use appropriate wave solder or manual techniques, not a reflow process which may damage the solder connections of the driver unit itself. It may be recommendable to additionally mechanically fix the driver unit depending on the environment, especially when vibrations occur.







Operating Conditions

The driver unit shall be operated within the specification of all components it consists of, e.g. driver IC's or electrolytic capacitors.

Symbol	Definitions	Max. Ratings	
T_A	Operating Ambient Temperature	-40 ... 85	°C
T_{JM}	Maximum Junction Temperature of IXBD4410/11 ICs	150	°C
T_{stg}	Storage Temperature Range	-40 ... 85	°C

422