National Semiconductor

MICROCIRCUIT DATA SHEET

MJLP2951-X REV 1B1

Original Creation Date: 08/01/95
Last Update Date: 05/19/98
Last Major Revision Date: 01/21/97

ADJUSTABLE MICROPOWER VOLTAGE REGULATORS

General Description

The LP2951 is a micropower voltage regulator with very low quiescent curent (75 uA typ.) and very low dropout voltage (typ. 40 mV at light loads and 380 mV at 100mA). They are ideally suited for use in battery-powered systems. Furthermore, the quiescent current of the LP2951 increases only slightly in dropout, prolonging battery life.

The 8-Lead LP2951 is available in plastic, ceramic dual-in-line, or metal can packages and offers additional system functions.

One such feature is an error flag output which warns of a low output voltage, often due to falling batteries on the input. It may be used for a power-on reset. A second feature is the logic-compatible shutdown input which enables the regulator to be switched on and off. Also, the part may be pin-strapped for a 5V output or programmed from 1.24V to 29V with an external pair of resistors.

Careful design of the LP2951 has minimized all contributions to the error budget. This includes a tight initial tolerance (.5% typ.), extremely good load and line regulation (.05% typ.) and a very low output voltage temperature coefficient, making the part useful as a low-power voltage reference.

Industry Part Number

LP2951

Prime Die

LP2951

Controlling Document

See Features Page REV C

NS Part Numbers

JL2951BGA*
JL2951BPA**
JL2951S2A***
JL2951SGA****
JL2951SPA*****

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{o}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- SMD : 5962-3870501BGA*, BPA**, S2A***, SGA****, SPA*****.

(Absolute Maximum Ratings)
(Note 1)

Power Dissipation (Note 2)		
METAL CAN		675mW at +25 C
CERDIP		1.0W at +25 C
LCC		1.25W at +25 C
CERAMIC SOIC		1.0W at +25 C
Lead Temperature (Soldering, 10 seconds)		260 C
Storage Temperature Range		-65 C to +150 C
Operating Junction Temp Range		
LP2951		-55 C to +160 C
Input Supply Voltage		-0.3 to +30V
Feedback Input Voltage (Note 3, 4)		-1.5 to +30V
Shutdown Input Voltage (Note 3)		-0.3 to +30V
Error Comparator Out. Voltage (Note 3)		-0.3 to +30V
Thermal Resistance		
ThetaJA		
METAL CAN	(Still Air @ 0.5W)	163 C/W
	(500LF/Min Air flow @ 0.5W)	95 C/W
CERDIP	(Still Air @ 0.5W)	131 C/W
	(500LF/Min Air flow @ 0.5W)	75 C/W
LCC	(Still Air @ 0.5W)	95 C/W
	(500LF/Min Air flow @ 0.5W)	66 C/W
CERAMIC SOIC	(Still Air @ 0.5W)	215 C/W
	(500LF/Min Air flow @ 0.5W)	130 C/W
ThetaJC		
METAL CAN		51 C/W
CERDIP		21 C/W
LCC		24 C/W
CERAMIC SOIC		24 C/W
Package Weight (Typical)		TBD
ESD Rating		500V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation msut be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA)/ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: May exceed input supply voltage.

Note 4: When used in dual-supply systems where the output terminal sees loads returned to a negative supply, the output voltage should be diode-clamped to ground.

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vout = 5V (Nominal), Cload = 3.3uF, Vsd = 0.6V, Vin = 6V, Il = -100uA

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vo	Output Voltage	Vin = 6V, Il = -100uA			4.975	5.025	V	1
					4.94	5.06	V	2, 3
Voline	Line Regulation	6V ≤ Vin ≤ 30V, Il = -1mA			-5	5	mV	1
		6V ≤ Vin ≤ 30V, Il = -1mA			-25	25	mV	2, 3
Voload	Load Regulation	-100uA ≤ Il ≤ -100mA, Vin = 6V			-5	5	mV	1
		-100uA ≤ Il ≤ -100mA, Vin = 6V			-25	25	mV	2, 3
Vd	Dropout Voltage	Il = -100mA				450	mV	1
						600	mV	2, 3
		Il = -100uA				80	mV	1
						150	mV	2, 3
Ig	Ground Current	Il = -100mA, Vin = 6V				12	mA	1
						14	mA	2, 3
		Il = -100uA, Vin = 6V				120	uA	1
						140	uA	2, 3
		Il = -100uA, Vout = 15V, Vin = 30V				120	uA	1
						140	uA	2, 3
		Il = -100uA, Vin = 30V, Vout = 15V				15	mA	1
						20	mA	2, 3
Igdiff	Ground Current Change	6V ≤ Vin ≤ 30V, Il = -100uA			-30	30	uA	1
		6V ≤ Vin ≤ 30V, Il = -100uA			-50	50	uA	2, 3
Igdo	Dropout Ground Current	Vin = 4.5V, Il = -100uA				170	uA	1
						200	uA	2, 3
Vlt	Error Comparator Lower Threshold Voltage	Vin = 6V, Il = -100uA	1		0	0.8	mV	1, 2, 3
Vut	Error Comparator Upper Threshold Voltage	Vin = 6V, Il = -100uA	1		2	30	mV	1, 2, 3
Vrth	Thermal Regulation	Vin = 30V, Il = -50mA, 2mS ≤ T ≤ 10mS			-12.5	12.5	mV	1
Isc	Current Limit	Vout = 0V, Vin = 6V				200	mA	1
						220	mA	2, 3

Electrical Characteristics

DC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vout = 5V (Nominal), Cload = 3.3uF, Vsd = 0.6V, Vin = 6V, Il = -100uA

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Igsc	Ground Current At Current Limit	Vout = 0V, Vin = 6V				20	mA	1
						25	mA	2, 3
Vref	Reference Voltage				1.22	1.25	V	1
					1.20	1.26	V	2, 3
Vrline	Reference Voltage Line Regulation	2.3V ≤ Vin ≤ 30V			-1.9	1.9	mV	1
		2.3V ≤ Vin ≤ 30V			-10	10	mV	2, 3
Vrload	Reference Voltage Output Regulation	1.2V ≤ Vout ≤ 29V, Vin = 30V			-1.2	1.2	mV	1
		1.2V ≤ Vout ≤ 29V, Vin = 30V			-5	5	mV	2, 3
Ifb	Feedback Pin Bias Current					40	nA	1
						60	nA	2, 3
Ioh	Error Comparator Output Leakage Current	Vo = 30V				1	uA	1
						2	uA	2, 3
Vol	Error Comparator Output Low Voltage	Vin = 4.5V, Vsd = 2V				250	mV	1
						400	mV	2, 3
Isd	Shutdown Pin Input Current	Vsd = 2.4V				50	uA	1
						100	uA	2, 3
		Vsd = 30V				600	uA	1
						750	uA	2, 3
Vsdl	Shutdown Input Logic Voltage	(LOW)	1			0.6	V	1, 2, 3
Vsdh	Shutdown Input Logic Voltage	(HIGH)	1		2		V	1, 2, 3
Ilkg	Regular Output Bias Current In Shutdown	Vsd = 2V, Vin = 30V, Il = 0mA			-10	10	uA	1
					-20	20	uA	2, 3

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vin = 6V, Cload = 3.3uF, Vsd = 0.6V

Rr	Ripple Rejection	f = 120Hz, Vin = 0.1Vrms			50		dB	4
Vnoise	Output Noise	C1 = 1uF				600	uVrms	7
		C1 = 3.3uF				250	uVrms	7

Electrical Characteristics

DC PARAMETERS: DRIFT VALUES

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vout = 5V (Nominal), Cload = 3.3uF, Vsd = 0.6V, Vin = 6V, Il = -100uA. "Delta calculations performed on JAN S and QMLV devices at group B, subgroup 5 ONLY."

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Ig	Ground Current	Il = -100uA, Vin = 6V			-6.5	6.5	uA	1
Vref	Reference Voltage				-0.0055	0.0055	V	1

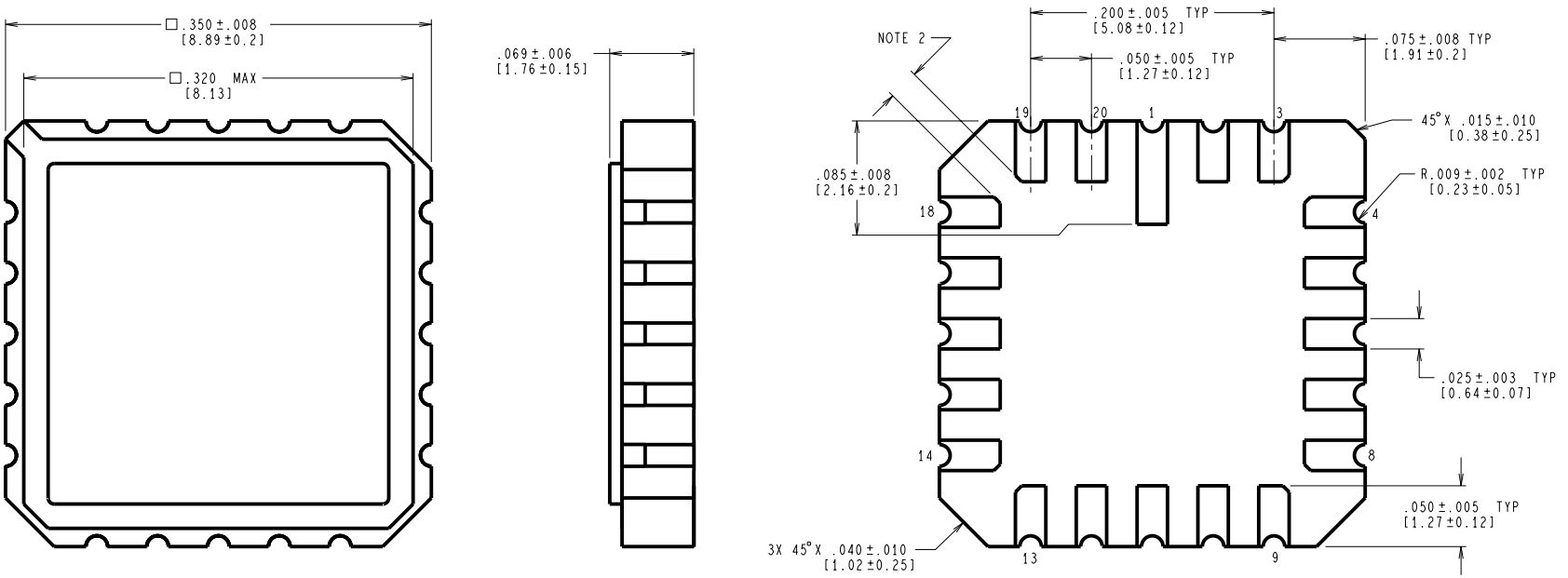
Note 1: Parameter tested go-no-go only.

Graphics and Diagrams

GRAPHICS#	DESCRIPTION
05810HRA2	METAL CAN (H), TO-99, 8LD, .200 DIA P.C. (B/I CKT)
06059HRA2	CERDIP (J), 8 LEAD (B/I CKT)
06146HRA2	LCC (E), TYPE C, 20 TERMINAL(B/I CKT)
06341HRA1	CERPACK (W), 10 LEAD (B/I CKT)
E20ARE	LCC (E), TYPE C, 20 TERMINAL(P/P DWG)
H08CRF	METAL CAN (H), TO-99, 8LD, .200 DIA P.C. (P/P DWG)
J08ARL	CERDIP (J), 8 LEAD (P/P DWG)
P000205A	METAL CAN (H), 8 LEAD (PINOUT)
P000206A	CERDIP (J), 8 LEAD (PINOUT)
P000251B	LCC (E), 20 LEAD (PINOUT)
P000374A	CERAMIC SOIC (WG), 10 LEAD (PINOUT)
WG10ARC	CERAMIC SOIC (WG), 10 LEAD (P/P DWG)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
E	REVISE AND REDRAW.	10005	02/10/94	DEG/



NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH TO BE ONE OF THE FOLLOWING:

   a. 50 MICROINCHES/12.7 MICROMETERS MINIMUM GOLD PLATING OVER 50-350 MICROINCHES/1.27-8.89 MICROMETERS NICKEL.

   b. SOLDER DIP.
   SOLDER THICKNESS PER LATEST REVISION OF MIL-STD-1835.

2. CORNER PADS MAY HAVE A 45°X.020IN/0.51mm MAXIMUM CHAMFER TO ACCOMPLISH THE .015IN/0.38mm DIMENSION.

4. REFERENCE JEDEC REGISTRATION MS-004, VARIATION CB, DATED 7/90.

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MIL/AERO
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: Dwayne Grady	02/10/94
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION
INCH [MM]

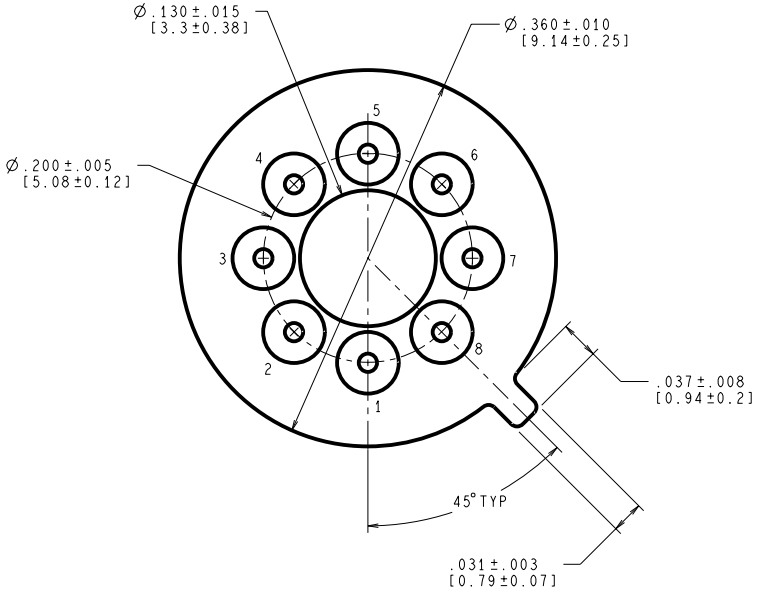
NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

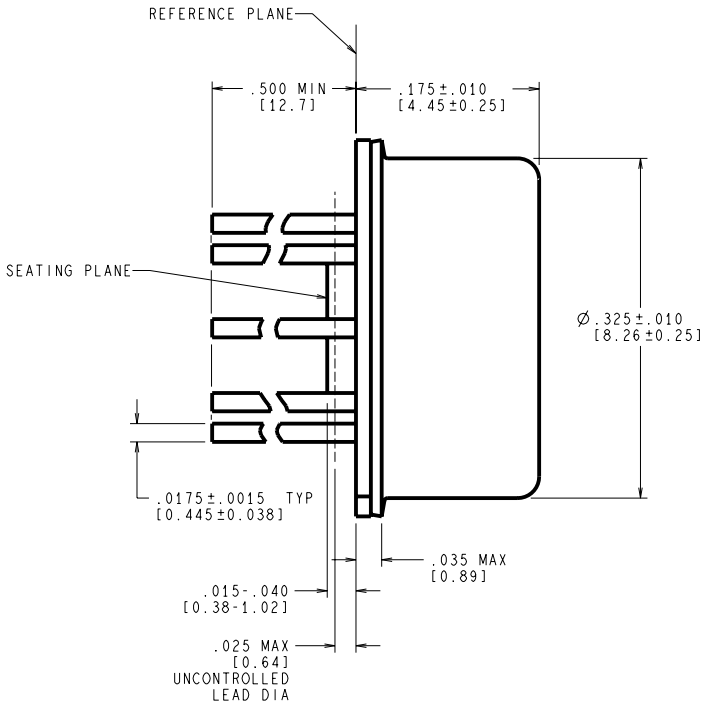
LEADLESS CHIP CARRIER, TYPE C, 20 TERMINAL

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-E20A	E

DO NOT SCALE DRAWING | SHEET 1 of 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
F	REVISE & REDRAW PER CURRENT STANDARD; UPDATE MIL/AERO STAMP & TITLE.	11002	06/22/95	MS/





CONTROLLING DIMENSION IS INCH
VALUES IN [] ARE MILLIMETERS

MIL-I-38535
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEADS TO BE LOCATED WITHIN .007 IN/ 0.18 mm OF THEIR TRUE POSITIONS RELATIVE TO A MAXIMUM WIDTH TAB.
2. STANDARD METAL CAN TYPE: SOLID BASE WITH CERAMIC STANDOFF.
3. APPLIES TO MIL-AERO AND LINEAR PRODUCTS.
4. REFERENCE JEDEC REGISTRATION TO-99, JEDEC PUBLICATION No.95.

APPROVALS	DATE
DRAWN: MARTA SUCHY	06/22/95
DFTG. CHK.	
ENGR. CHK.	

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

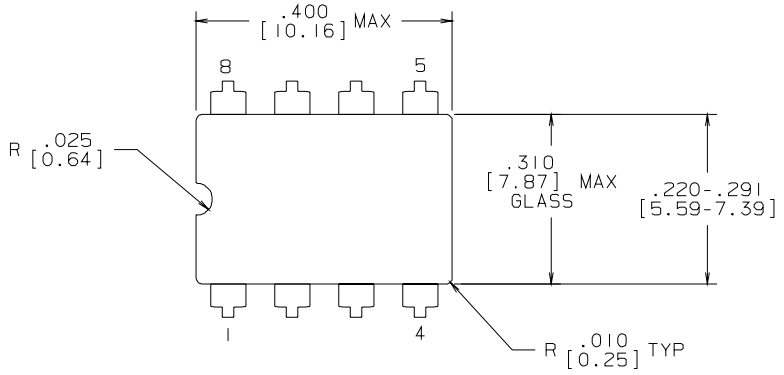
METAL CAN, TO-99, 8 LEAD, .200 DIA P.C.

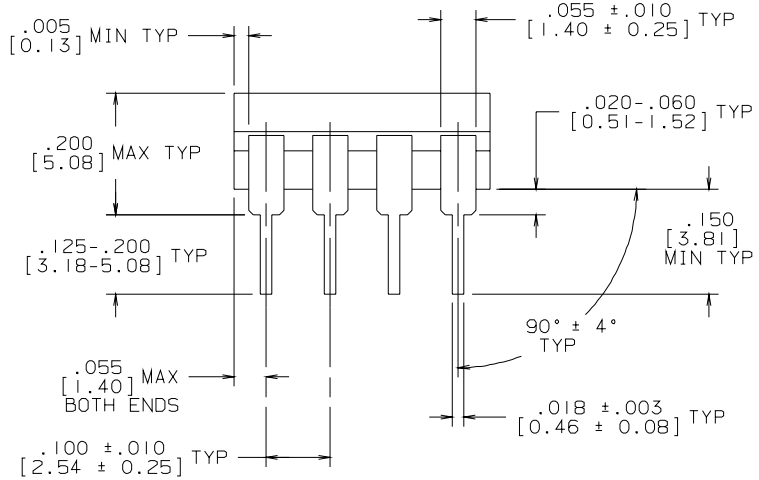
PROJECTION — INCH [MM]

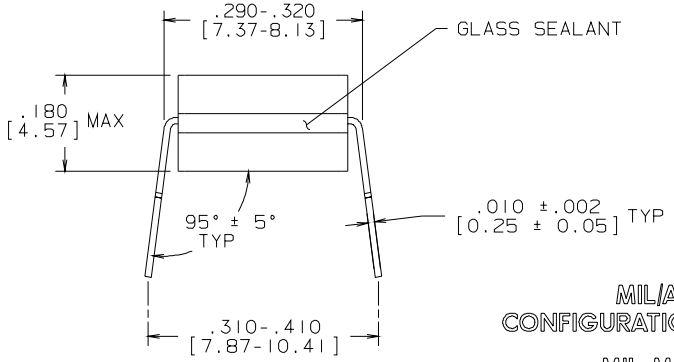
SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-H08C	F

DO NOT SCALE DRAWING — SHEET 1 of 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE PER CURRENT STD; REDRAW	I0002	09/21/93	TL/







MIL/AERO
CONFIGURATION CONTROL

MIL-M-38510
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AA, DATED 04/1981.

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN T. LEQUANG	09/21/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

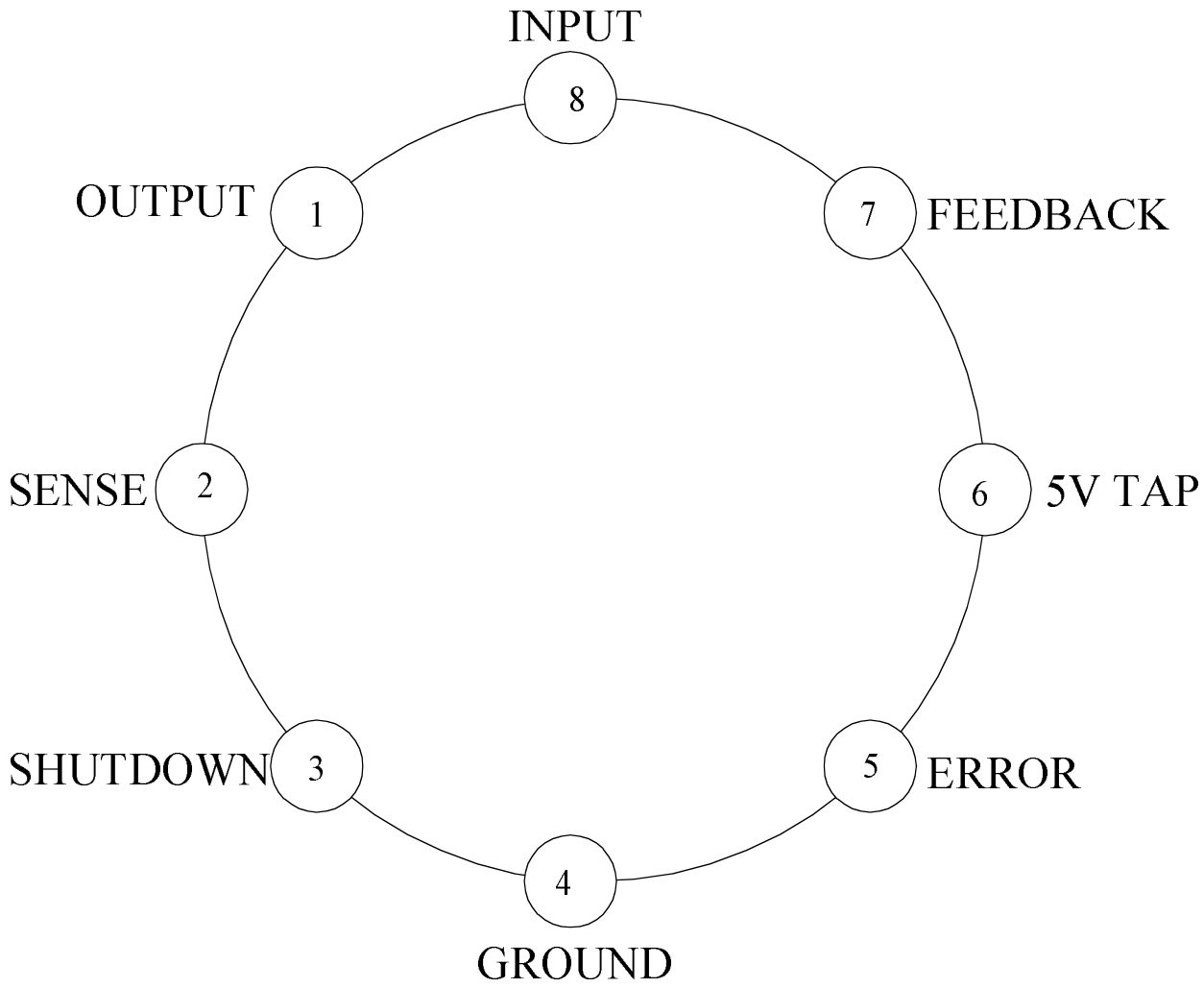
INCH
[MM]

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 8 LEAD

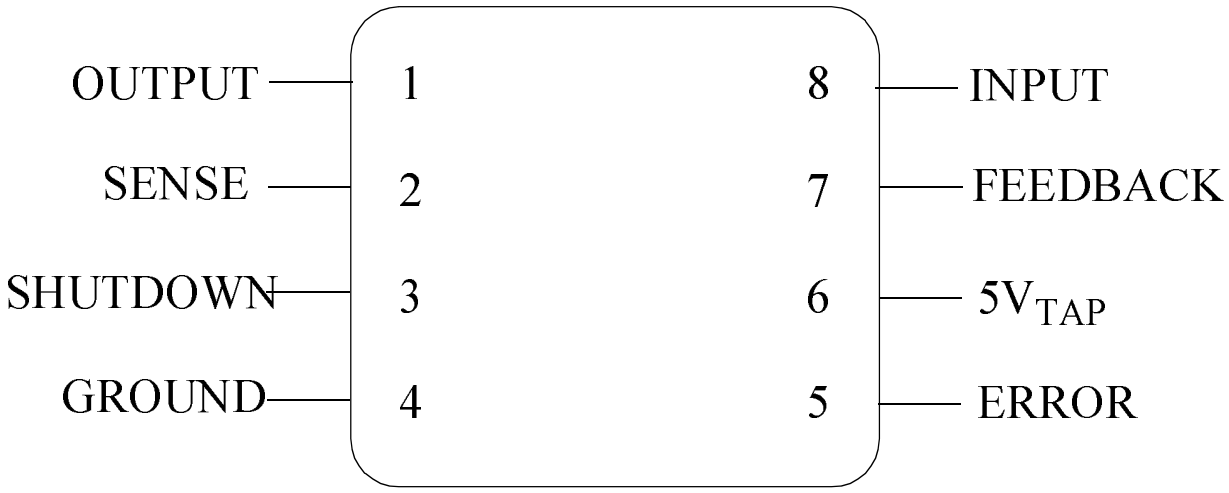
SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J08A	L

DO NOT SCALE DRAWING | SHEET 1 OF 1



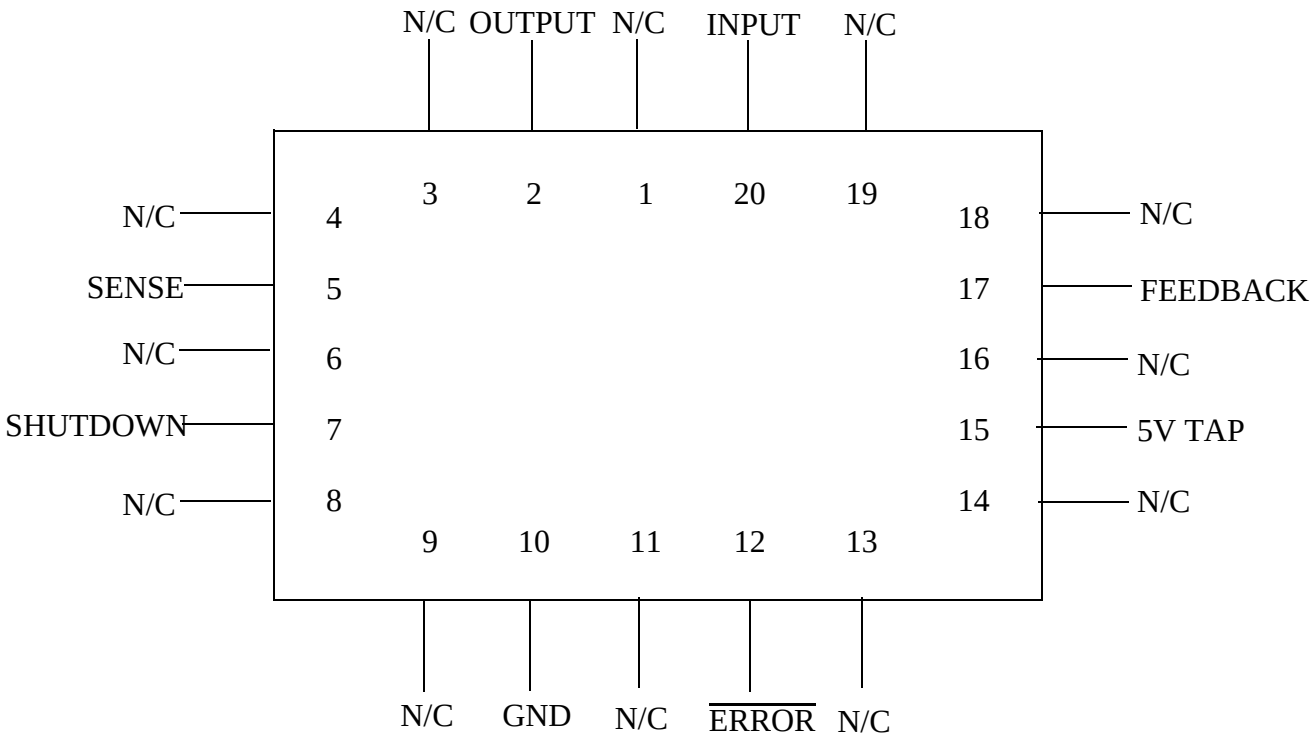
LP2951H
8 - PIN METAL CAN
CONNECTION DIAGRAM
TOP VIEW
P000205A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



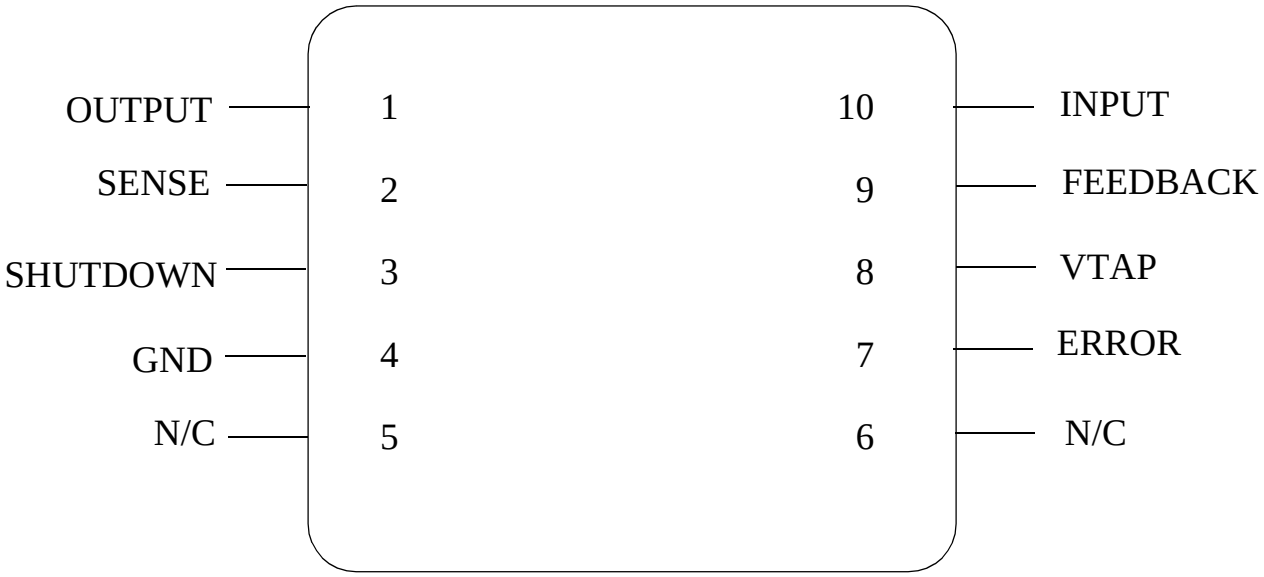
LP2951J
8 - LEAD DIP
CONNECTION DIAGRAM
TOP VIEW
P000206A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



LP2951E
20 - LEAD LCC
CONNECTION DIAGRAM
TOP VIEW
P000251B

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



LP2951WG

10 - LEAD CERAMIC SOIC

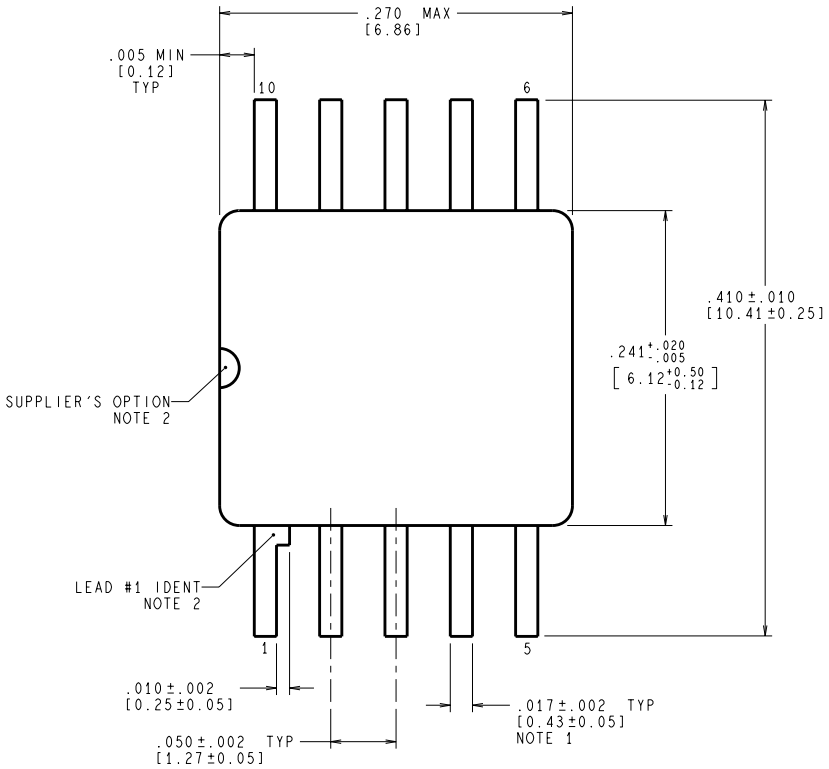
CONNECTION DIAGRAM

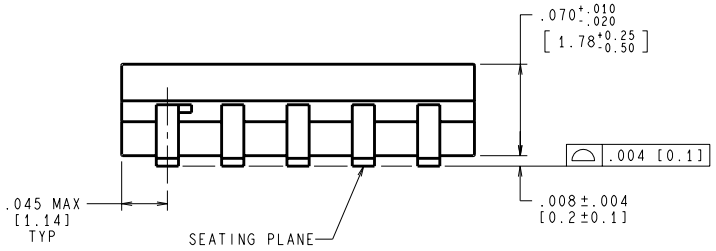
TOP VIEW

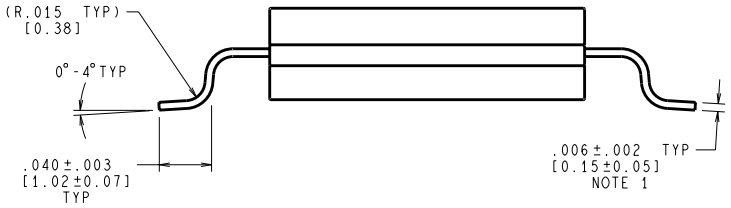
P000374A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	11374	02/29/1996	MS/KH
B	LD PITCH TOL WAS ±.005; CHANGE LD RADIUS TO REF DIM; REMOVE THE OTHER R.006±.002 DIM .040±.003 WAS .037±.003	11441	04/19/1996	MS/KH
C	R .015[0.38] WAS R .006[0.15]	11838	10/08/1997	TL/







NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-PRF-38535 TO A MINIMUM THICKNESS OF 200 MICROINCHES/ 5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE. MAXIMUM LIMIT MAY BE INCREASED BY .003 IN/ 0.08mm AFTER LEAD FINISH APPLIED.
2. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE
3. NO JEDEC REGISTRATION AS OF FEBRUARY 1996.

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MIL-PRF-38535
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: MARTA SUCHY	02/29/96
DFTG. CHK.	
ENGR. CHK.	

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

CERPACK, 10 LEAD, GULL WING

PROJECTION
INCH [MM]

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	(SC)MKT-WG10A	C

DO NOT SCALE DRAWING | SHEET 1 of 1

Revision History

Rev	ECN #	Rel Date	Originator	Changes
1B1	M0002867	05/19/98	Barbara Lopez	Update MDS: MJLP2951-X Rev. 1A0 to MJLP2951-X Rev. 1B1. Updated SMD number to add suffixes. Updated NSID to add astericks associated with SMD suffix. Updated power dissipation, lead temperature, junction temperature, thermal resistance and ESD rating. Changed note 1 to Absolute note, updated note 2 to power dissipation note. Added graphics for all packages. Added Package Weights.