

# NTD65N03R

## Power MOSFET 25 V, 65 A, Single N-Channel, DPAK

### Features

- Low  $R_{DS(on)}$
- Ultra Low Gate Charge
- Low Reverse Recovery Charge
- Pb-Free Packages are Available

### Applications

- Desktop CPU Power
- DC-DC Converters
- High and Low Side Switch

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	$V_{DSS}$	25	V	
Gate-to-Source Voltage	$V_{GS}$	$\pm 20$	V	
Continuous Drain Current ( $R_{\theta JC}$ ) Limited by Die	$I_D$	$T_C = 25^\circ\text{C}$	65	A
		$T_C = 85^\circ\text{C}$	45	A
Continuous Drain Current ( $R_{\theta JC}$ ) Limited by Wire	$I_D$	$T_C = 25^\circ\text{C}$	32	A
		$T_C = 25^\circ\text{C}$	$P_D$	50
Power Dissipation ( $R_{\theta JC}$ )				
Continuous Drain Current (Note 1)	$I_D$	$T_A = 25^\circ\text{C}$	11.4	A
		$T_A = 85^\circ\text{C}$	8.9	A
Power Dissipation (Note 1)	$P_D$	1.88	W	
Continuous Drain Current (Note 2)	$I_D$	$T_A = 25^\circ\text{C}$	9.5	A
		$T_A = 85^\circ\text{C}$	7.4	A
Power Dissipation (Note 2)	$P_D$	1.3	W	
Pulsed Drain Current	$t_p = 10 \mu\text{s}$	$I_{DM}$	130	A
Operating Junction and Storage Temperature	$T_J, T_{stg}$	-55 to 175	$^\circ\text{C}$	
Drain-to-Source (dv/dt)	dv/dt	2.0	V/ns	
Source Current (Body Diode)	$I_S$	2.1	A	
Single Pulse Drain-to-Source Avalanche Energy ( $V_{DD} = 24 \text{ V}, V_{GS} = 10 \text{ V}, I_L = 12 \text{ A}, L = 1.0 \text{ mH}, R_G = 25 \Omega$ )	$E_{AS}$	71.7	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	$T_L$	260	$^\circ\text{C}$	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).
2. Surface-mounted on FR4 board using the minimum recommended pad size (Cu area = 0.15 in sq [1 oz] including traces).

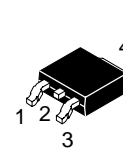
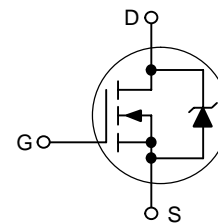


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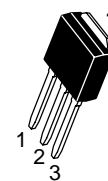
<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	$I_D$ MAX
25 V	6.5 m $\Omega$ @ 10 V	65 A
	9.7 m $\Omega$ @ 4.5 V	

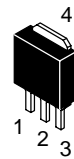
### N-Channel



CASE 369AA  
DPAK  
(Bend Lead)  
STYLE 2

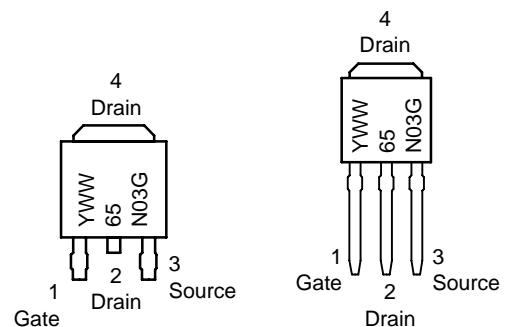


CASE 369D  
DPAK  
(Straight Lead)  
STYLE 2



CASE 369AC  
3 IPAK  
(Straight Lead)

### MARKING DIAGRAMS & PIN ASSIGNMENTS



Y = Year  
WW = Work Week  
65N03 = Device Code  
G = Pb-Free Package

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

# NTD65N03R

## THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	2.5	°C/W
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	80	
Junction-to-Ambient – Steady State (Note 4)	$R_{\theta JA}$	115	

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	25	29.5		V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			19.2		mV/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 20\text{ V}$	$T_J = 25^\circ\text{C}$		1.5	$\mu\text{A}$
			$T_J = 125^\circ\text{C}$		10	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA

### ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.0	1.74	2.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			4.8		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 30\text{ A}$		6.5	8.4	m $\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 30\text{ A}$		9.7	14.6	
Forward Transconductance	$g_{FS}$	$V_{DS} = 15\text{ V}, I_D = 15\text{ A}$		27		mHos

### CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = 20\text{ V}$		1177	1400	pF
Output Capacitance	$C_{oss}$			555		
Reverse Transfer Capacitance	$C_{rss}$			218		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 5.0\text{ V}, V_{DS} = 10\text{ V}, I_D = 30\text{ A}$		12.2	16	nC
Threshold Gate Charge	$Q_{G(TH)}$			1.5		
Gate-to-Source Charge	$Q_{GS}$			2.95		
Gate-to-Drain Charge	$Q_{GD}$			6.08		

### SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 10\text{ V}, V_{DS} = 25\text{ V}, I_D = 30\text{ A}, R_G = 3.0\ \Omega$		6.3		ns
Rise Time	$t_r$			18.6		
Turn-Off Delay Time	$t_{d(off)}$			20.3		
Fall Time	$t_f$			8.8		

### DRAIN-SOURCE DIODE CHARACTERISTICS

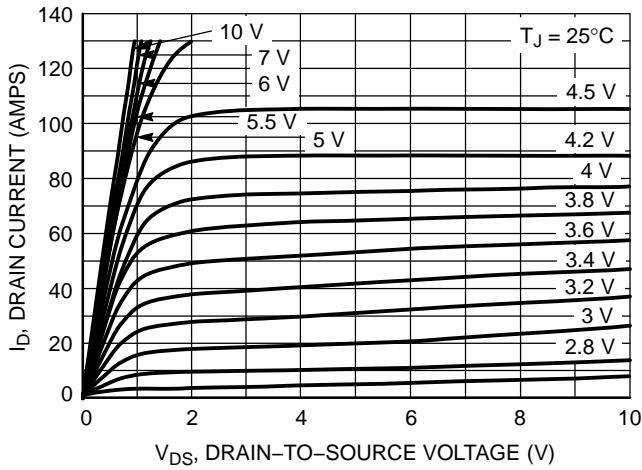
Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_S = 20\text{ A}$	$T_J = 25^\circ\text{C}$	0.85	1.1	V
			$T_J = 125^\circ\text{C}$	0.72		
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, di_S/dt = 100\text{ A}/\mu\text{s}, I_S = 20\text{ A}$		28.8		ns
Charge Time	$t_a$			12.8		
Discharge Time	$t_b$			16		
Reverse Recovery Time	$Q_{RR}$			20		nC

### PACKAGE PARASITIC VALUES

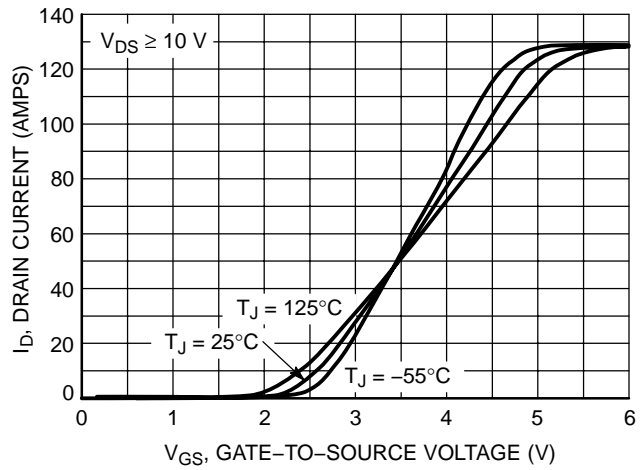
Source Inductance	$L_S$	$T_A = 25^\circ\text{C}$		2.49		nH
Drain Inductance	$L_D$			0.02		
Gate Inductance	$L_G$			3.46		
Gate Resistance	$R_G$			1.75		

- Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).
- Surface-mounted on FR4 board using the minimum recommended pad size (Cu area = 0.15 in sq [1 oz] including traces).
- Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .
- Switching characteristics are independent of operating junction temperatures.

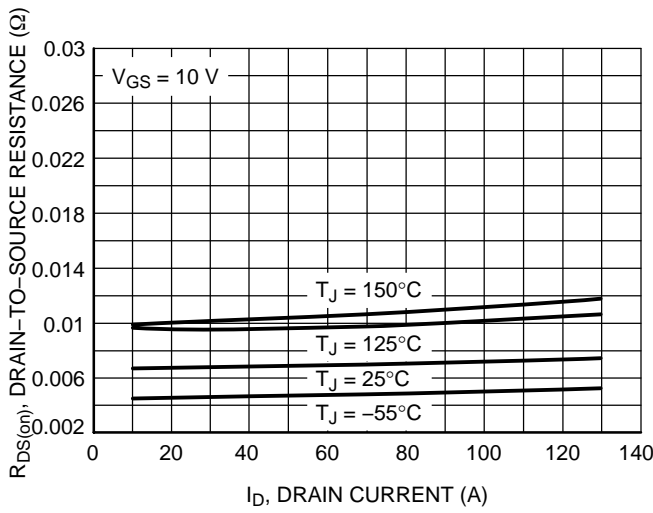
# NTD65N03R



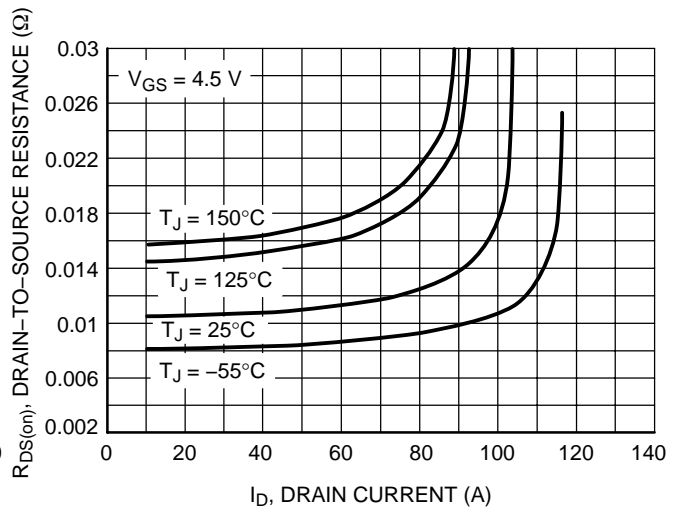
**Figure 1. On-Region Characteristics**



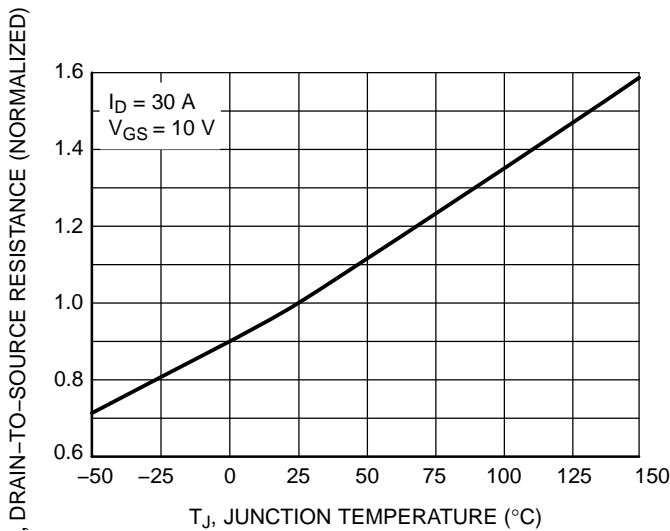
**Figure 2. Transfer Characteristics**



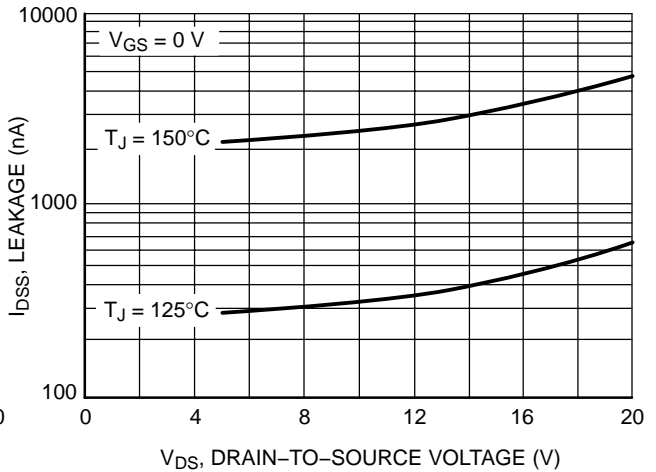
**Figure 3. On-Resistance versus Drain Current and Temperature**



**Figure 4. On-Resistance versus Drain Current and Temperature**



**Figure 5. On-Resistance Variation with Temperature**



**Figure 6. Drain-to-Source Leakage Current versus Voltage**

# NTD65N03R

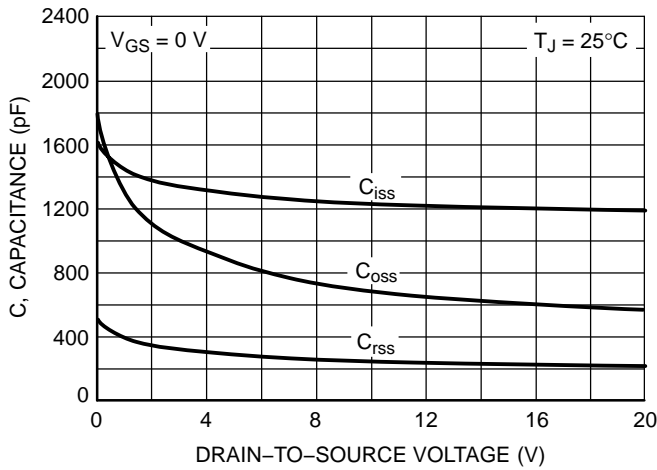


Figure 7. Capacitance Variation

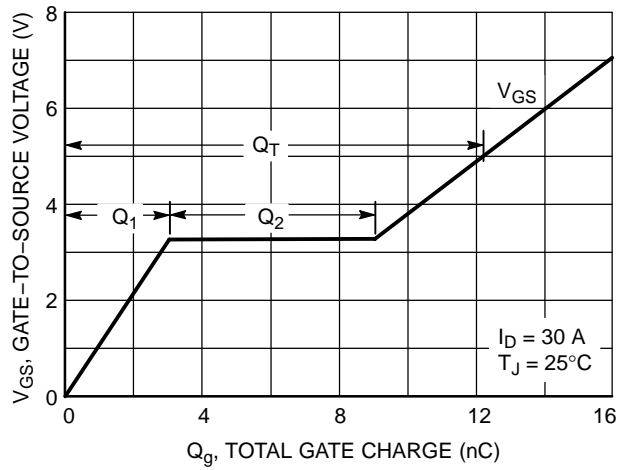


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

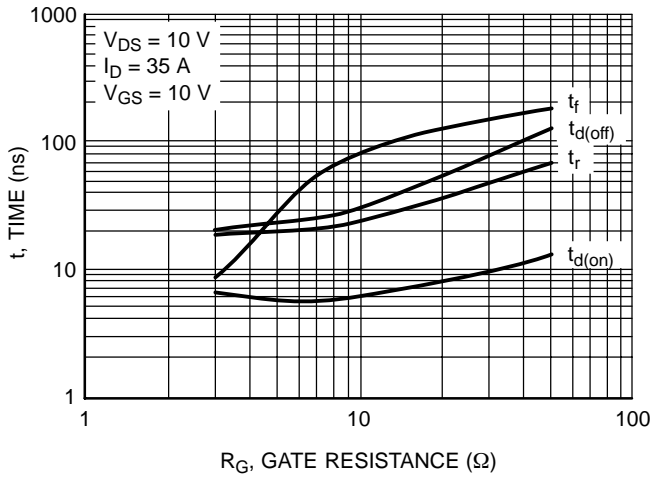


Figure 9. Resistive Switching Time Variation versus Gate Resistance

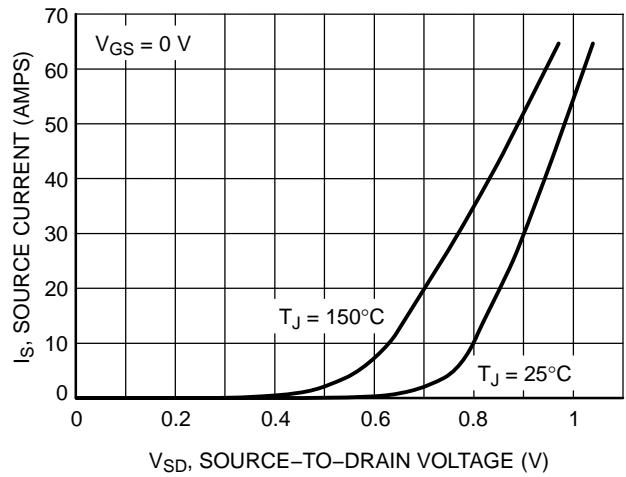


Figure 10. Diode Forward Voltage versus Current

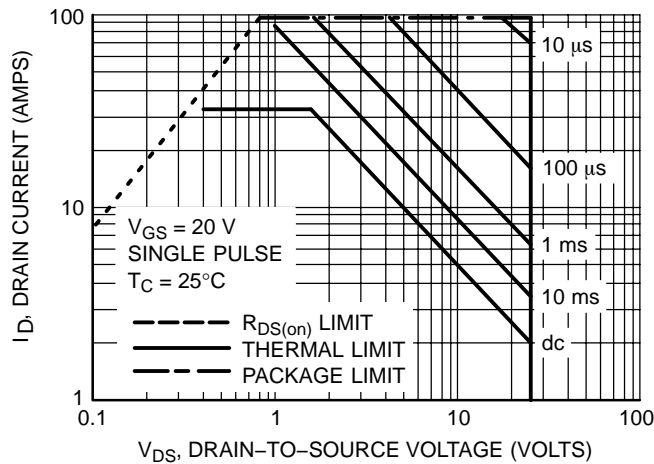


Figure 11. Maximum Rated Forward Biased Safe Operating Area

# NTD65N03R

## ORDERING INFORMATION

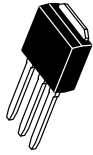
Order Number	Package	Shipping†
NTD65N03R	DPAK-3	75 Units / Rail
NTD65N03RG	DPAK-3 (Pb-Free)	75 Units / Rail
NTD65N03RT4	DPAK-3	2500 / Tape & Reel
NTD65N03RT4G	DPAK-3 (Pb-Free)	2500 / Tape & Reel
NTD65N03R-1	DPAK-3 Straight Lead	75 Units / Rail
NTD65N03R-1G	DPAK-3 Straight Lead (Pb-Free)	75 Units / Rail
NTD65N03R-35	DPAK Straight Lead Trimmed (3.5 ± 0.15 mm)	75 Units / Rail
NTD65N03R-35G	DPAK Straight Lead Trimmed (3.5 ± 0.15 mm) (Pb-Free)	75 Units / Rail

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

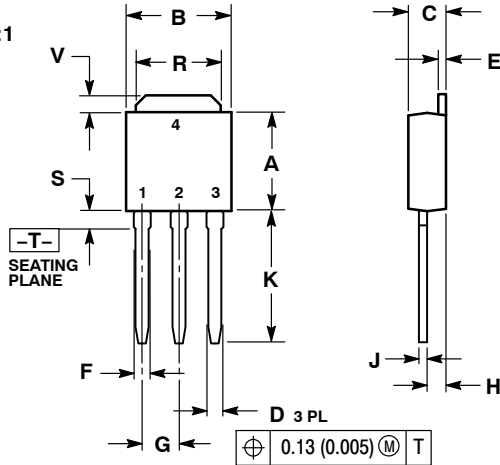
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### IPAK CASE 369D-01 ISSUE C

DATE 15 DEC 2010

SCALE 1:1

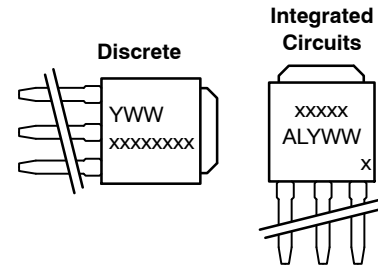


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090	BSC	2.29	BSC
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

- |  |   |  |  |
|--|---|--|--|
| <p>STYLE 1:<br/>PIN 1. BASE<br/>2. COLLECTOR<br/>3. EMITTER<br/>4. COLLECTOR</p> | <p>STYLE 2:<br/>PIN 1. GATE<br/>2. DRAIN<br/>3. SOURCE<br/>4. DRAIN</p> | <p>STYLE 3:<br/>PIN 1. ANODE<br/>2. CATHODE<br/>3. ANODE<br/>4. CATHODE</p>      | <p>STYLE 4:<br/>PIN 1. CATHODE<br/>2. ANODE<br/>3. GATE<br/>4. ANODE</p> |
| <p>STYLE 5:<br/>PIN 1. GATE<br/>2. ANODE<br/>3. CATHODE<br/>4. ANODE</p>         | <p>STYLE 6:<br/>PIN 1. MT1<br/>2. MT2<br/>3. GATE<br/>4. MT2</p>        | <p>STYLE 7:<br/>PIN 1. GATE<br/>2. COLLECTOR<br/>3. EMITTER<br/>4. COLLECTOR</p> |  |

### MARKING DIAGRAMS



- xxxxxxxx = Device Code  
A = Assembly Location  
IL = Wafer Lot  
Y = Year  
WW = Work Week

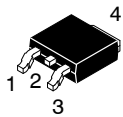
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<b>DESCRIPTION:</b>	<b>IPAK (DPAK INSERTION MOUNT)</b>	<b>PAGE 1 OF 1</b>

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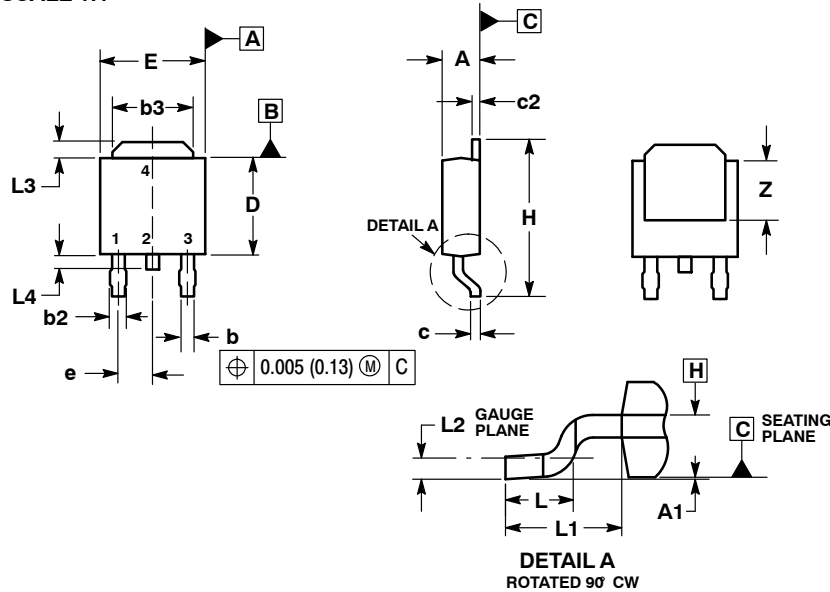
# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

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SCALE 1:1



### DPAK (SINGLE GAUGE)

#### CASE 369AA-01

#### ISSUE B

DATE 03 JUN 2010

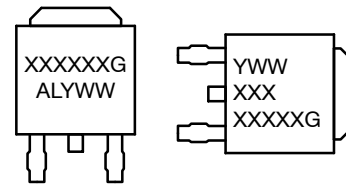
**NOTES:**

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: INCHES.
- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b<sub>3</sub>, L<sub>3</sub> and Z.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
- DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b <sub>2</sub>	0.030	0.045	0.76	1.14
b <sub>3</sub>	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c <sub>2</sub>	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L <sub>1</sub>	0.108 REF		2.74 REF	
L <sub>2</sub>	0.020 BSC		0.51 BSC	
L <sub>3</sub>	0.035	0.050	0.89	1.27
L <sub>4</sub>	---	0.040	---	1.01
Z	0.155	---	3.93	---

- |   |  |   |   |
|---|--|---|---|
| <p><b>STYLE 1:</b><br/>PIN 1. BASE<br/>2. COLLECTOR<br/>3. EMITTER<br/>4. COLLECTOR</p> | <p><b>STYLE 2:</b><br/>PIN 1. GATE<br/>2. DRAIN<br/>3. SOURCE<br/>4. DRAIN</p> | <p><b>STYLE 3:</b><br/>PIN 1. ANODE<br/>2. CATHODE<br/>3. ANODE<br/>4. CATHODE</p>      | <p><b>STYLE 4:</b><br/>PIN 1. CATHODE<br/>2. ANODE<br/>3. GATE<br/>4. ANODE</p> |
| <p><b>STYLE 5:</b><br/>PIN 1. GATE<br/>2. ANODE<br/>3. CATHODE<br/>4. ANODE</p>         | <p><b>STYLE 6:</b><br/>PIN 1. MT1<br/>2. MT2<br/>3. GATE<br/>4. MT2</p>        | <p><b>STYLE 7:</b><br/>PIN 1. GATE<br/>2. COLLECTOR<br/>3. EMITTER<br/>4. COLLECTOR</p> |   |

### GENERIC MARKING DIAGRAM\*



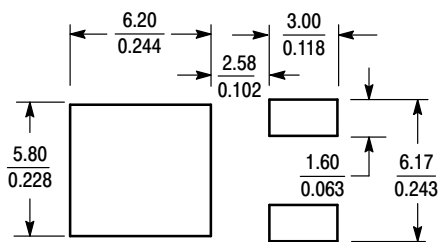
IC

Discrete

- XXXXXX = Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking.

### SOLDERING FOOTPRINT\*



SCALE 3:1 (mm/inches)

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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<b>DESCRIPTION:</b>	<b>DPAK (SINGLE GAUGE)</b>	<b>PAGE 1 OF 1</b>

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