

IX2R11

500 Volt, 2 Ampere High & Low-side Driver for N-Channel MOSFETs and IGBTs

Features

- Floating High Side Driver with boot-strap power supply along with a Low Side Driver.
- Fully operational to 500V
- $\pm 50\text{V/ns}$ dV/dt immunity
- Gate drive power supply range: 10 - 35V
- Undervoltage lockout for both output drivers
- Separate logic power supply range: 3.3V to V_{CL}
- Built using the advantages and compatibility of CMOS and IXYS HDMOS™ processes
- Latch-Up protected over entire operating range
- Matched propagation delay for both outputs
- High peak output current: 2A
- Low output impedance
- Low power supply current
- Immune to negative voltage transients

Applications

- Driving MOSFETs and IGBTs in half-bridge circuits
- High voltage, high side and low side drivers
- Motor Controls
- Switch Mode Power Supplies (SMPS)
- DC to DC Converters
- Class D Switching Amplifiers

General Description

The IX2R11 High Side and Low Side Driver is for driving N-channel MOSFETs and IGBTs with high side and low side outputs, whose input signals reference the low side. The High Side driver can control a MOSFET or IGBT connected to a positive bus voltage up to 500V. The logic input stages are compatible with TTL or CMOS, have built-in hysteresis and are fully immune to latch up over the entire operating range. The IX2R11 can withstand dV/dt on the output side up to $\pm 50\text{V/ns}$.

The IX2R11 comes in either the 16-PIN SOIC package (IX2R11S3) or the 14-PIN DIP through-hole package (IX2R11P7).

Ordering Information	
Part Number	Package Type
IX2R11P7	14-PIN DIP
IX2R11S3	16-PIN SOIC

Warning: The IX2R11 is ESD sensitive.

Precaution: When performing the High-Voltage tests, adequate safety precautions should be taken.

* Operational voltage rating of 500V determined in a typical half-bridge circuit configuration (refer to Figure 10 and Figure 11). Operational voltage in other circuit configurations may vary

Figure 1. Typical Circuit Connection

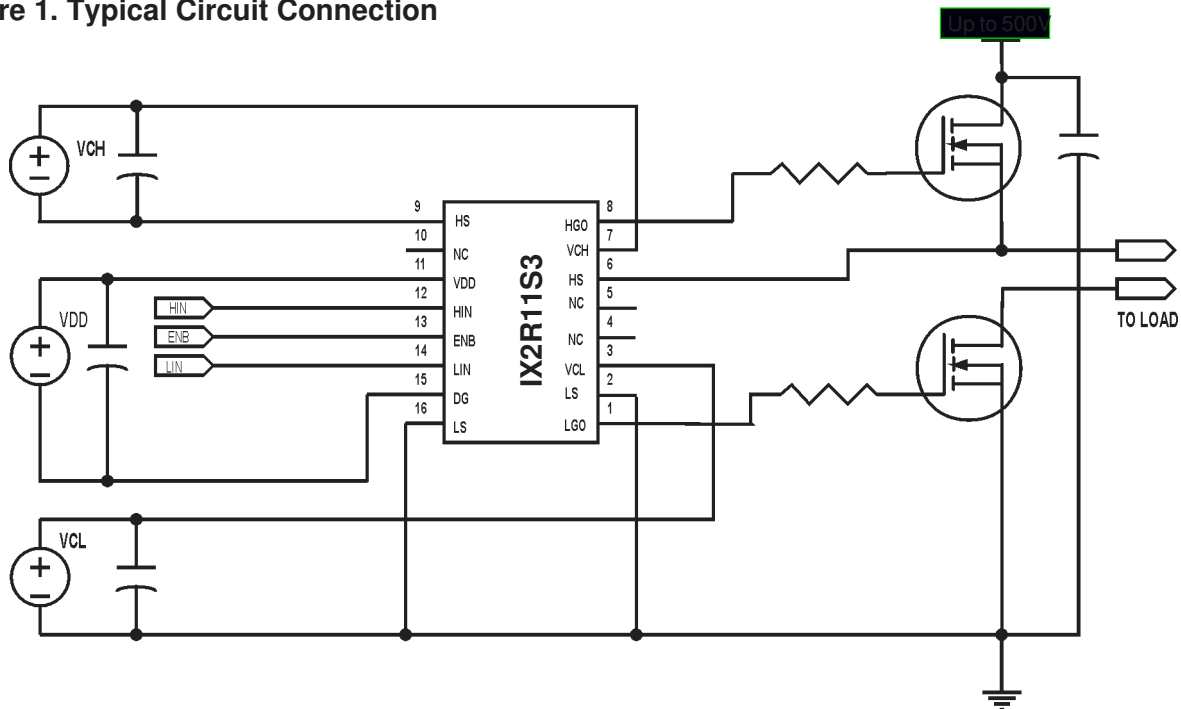
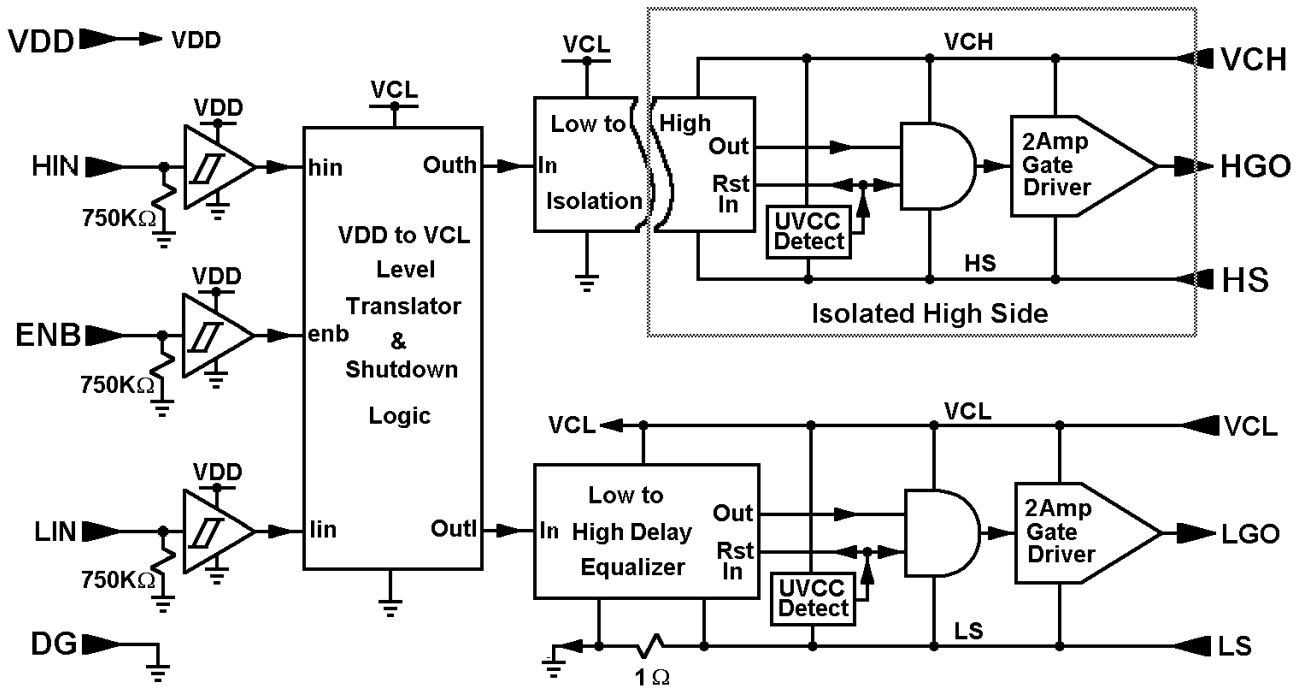
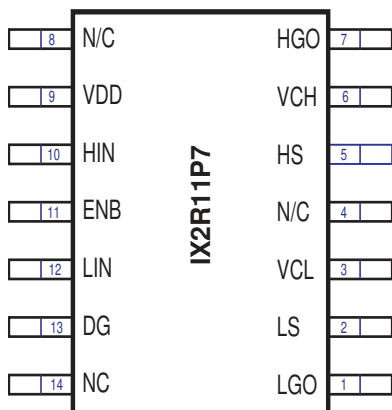
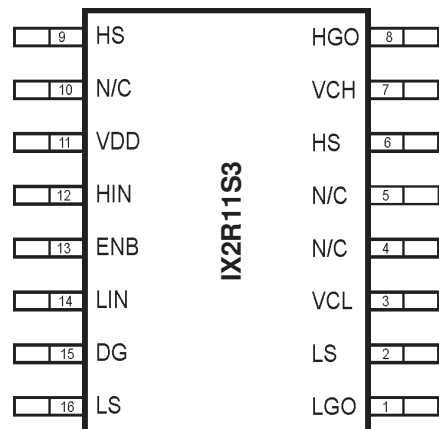


Figure 2 - IX2R11 Functional Block Diagram

Pin Description And Configuration

SYMBOL	FUNCTION	DESCRIPTION
V _{DD}	Logic Supply	Positive power supply for the chip CMOS functions
HIN	HS Input	High side Input signal, TTL or CMOS compatible; HGO in phase
LIN	LS Input	Low side Input signal, TTL or CMOS compatible; LGO in phase
ENB	Enable	Chip enable, active low. When driven high, both outputs go low.
DG	Ground	Logic reference ground
V _{CH}	Supply Voltage	High side power supply, referenced to HS
HGO	Output	High side driver output
HS	Return	High side voltage return
V _{CL}	Supply Voltage	Low side power supply, referenced to LS
LGO	Output	Low side driver output
LS	Ground	Low side return

14-PIN DIP

16-PIN SOIC


Absolute Maximum Ratings*

Symbol	Definition	Min	Max	Units
V_{CH}	High side floating supply voltage	-0.3	+35	V
V_{HS}	High side floating supply offset voltage	-200	+500	V
V_{HGO}	High side floating output voltage	$V_{HS} - 0.3$	$V_{CH} + 0.3$	V
V_{CL}	Low side fixed supply voltage	-0.3	+35	V
V_{LGO}	Low side output voltage	-0.3	$V_{CL} + 0.3$	V
V_{DD}	Logic supply voltage	-0.3	$V_{CL} + 0.3$	V
V_{DG}	Logic supply offset voltage	$V_{LS} - 1$	$V_{LS} + 1$	V
V_{IN}	Logic input voltage(HIN, LIN, ENB)	$V_{LS} - 0.3$	$V_{CL} + 0.3$	V
dV_{HS}/dt	Allowable offset supply voltage transient	---	50	V/ns
P_D	Package power dissipation@ $T_{AMBIENT} \leq 25^{\circ}C$	---	1.25	W
P_D	Package power dissipation@ $T_{CASE} \leq 25^{\circ}C$	---	2.5	W
R_{THJA}	Thermal resistance, junction-to-ambient	---	100	$^{\circ}C/W$
R_{THJC}	Thermal resistance, junction-to-case	---	50	$^{\circ}C/W$
T_J	Junction Temperature	---	150	$^{\circ}C$
T_S	Storage temperature	-55	150	$^{\circ}C$
T_L	Lead temperature (soldering, 10 secs.)	---	300	$^{\circ}C$

Recommended Operating Conditions

Symbol	Definition	Min	Max	Units
V_{CH}	High side floating supply absolute voltage	$V_{HS} + 10$	$V_{HS} + 20$	V
V_{HS}	High side floating supply offset voltage	-250	+500	V
V_{HGO}	High side floating output voltage	V_{HS}	$V_{HS} + V_{CH}$	V
V_{CL}	Low side fixed supply voltage	10	20	V
V_{LGO}	Low side output voltage	0	V_{CL}	V
V_{DD}	Logic supply voltage	$V_{DG} + 3$	$V_{DG} + V_{CL}$	V
V_{DG}	Logic supply offset voltage	$V_{LS} - 0.3$	$V_{LS} + 0.3$	V
V_{IN}	Logic input voltage(HIN, LIN, ENB)	V_{DG}	V_{DD}	V
T_A	Ambient Temperature	-40	125	$^{\circ}C$

***Note:** Operating the device beyond parameters with listed “absolute maximum ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Dynamic Electrical Characteristics*

Symbol	Definition	Test Conditions	Min	Typ	Max	Units
t_{on}	Turn-on propagation delay	$C_{load} = 1nF$ $V_{DD}, V_{CL}, V_{CH}=15V$	---	140	170	ns
t_{off}	Turn-off propagation delay	$C_{load} = 1nF$ $V_{DD}, V_{CL}, V_{CH}=15V$	---	100	120	ns
t_{enb}	Enable delay, active low	$V_{DD}=15V$ $V_{CL}, V_{CH}=18V$	---	90	110	ns
t_r	Turn-on rise time	$C_{load} = 1nF$ $V_{CH}, V_{CL}=15V$	---	8	11	ns
t_f	Turn-off fall time	$C_{load} = 1nF$ $V_{CH}, V_{CL}=15V$	---	7	10	ns
t_{dm}	Delay matching, HS & LS turn-on/off		---	30	40	ns

Static Electrical Characteristics

Symbol	Definition	Test Conditions	Min	Typ	Max	Units
V_{INH}	Logic "1" input voltage	$V_{DD}, V_{CL}, V_{CH}=15V$	9.5	9.8	---	V
V_{INL}	Logic "0" input voltage	$V_{DD}, V_{CL}, V_{CH}=15V$	---	5.8	6	V
V_{HLGO} / V_{HHGO}	High level output voltage, $V_{CH}-V_{HGO}$ or $V_{CL}-V_{LGO}$	$I_O = 20mA$	---	0.3	1	V
V_{LLGO} / V_{LHGO}	Low level output voltage, V_{HGO} or V_{LGO}	$I_O = 20mA$	---	0.04	0.1	V
I_{HL}	HS to LS bias (leakage) current.	V_{HS} Offset = 600V	---	100	150	μA
I_{QHS}	Quiescent V_{CH} supply current	$V_{IN} = 0V, V_{CH} = 15V$	---	700	1000	μA
I_{QLS}	Quiescent V_{CL} supply current	$V_{IN} = 0V, V_{CL} = 15V$	---	160	300	μA
I_{QDD}	Quiescent V_{DD} supply current	$V_{IN} = 0V, V_{DD} = 15V$	---	0.2	5	μA
I_{IN+}	Logic "1" input bias current	$V_{IN} = V_{DD} = 15V$	---	11	25	μA
I_{IN-}	Logic "0" input bias current	$V_{IN} = 0V$	---	---	1	μA
V_{CHUV+}	V_{CH} supply under-voltage positive going threshold.		7	8.1	9	V
V_{CHUV-}	V_{CH} supply under-voltage negative going threshold.		7	8	9	V
V_{CLUV+}	V_{CL} supply under-voltage positive going threshold		9	9.9	11	V
V_{CLUV-}	V_{CL} supply under-voltage negative going threshold.		8.2	9.2	10.5	V
I_{GO+}	HS or LS output high short circuit sourcing current; $V_{GO} = 15V, PW < 10\mu s$		2	2.5	---	A
I_{GO-}	HS or LS output low short circuit sinking current; $V_{GO} = 0V, PW < 10\mu s$		---	-2.5	-2	A

* These characteristics are guaranteed by design only. Tested on a sample basis.

Timing Waveform Definitions

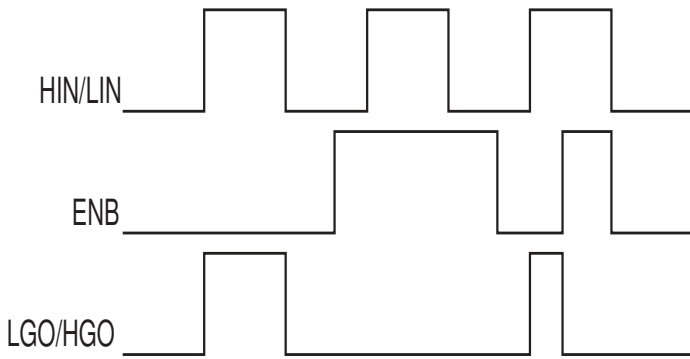


Figure 3. INPUT/OUTPUT Timing Diagram

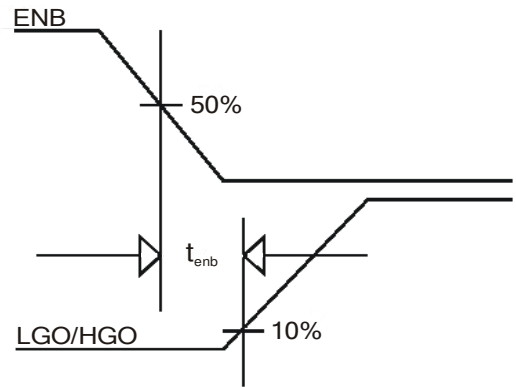


Figure 4. ENABLE Waveform Definitions

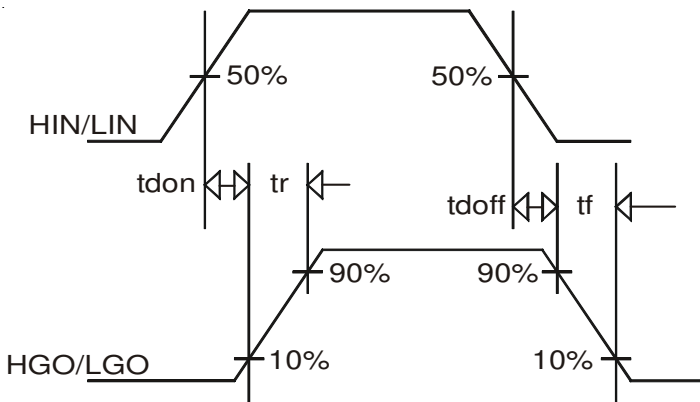


Figure 5. Definitions of Switching Time Waveforms

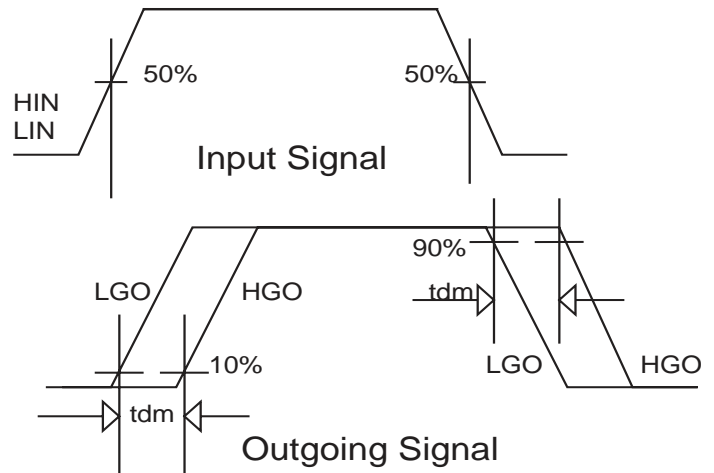


Figure 6. Definitions of Delay Matching Waveforms

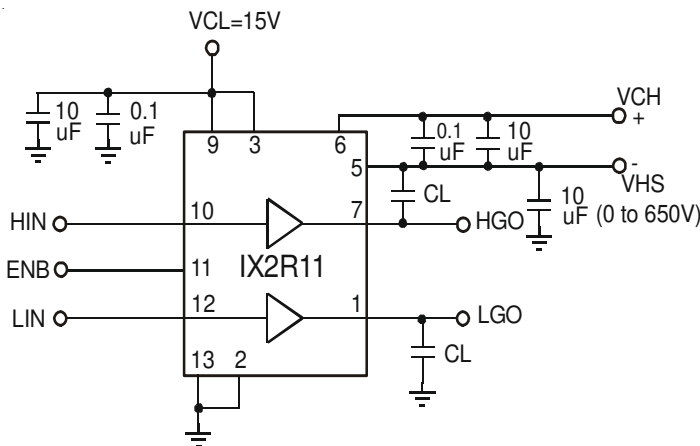


Figure 7. Switching Time Test Circuit

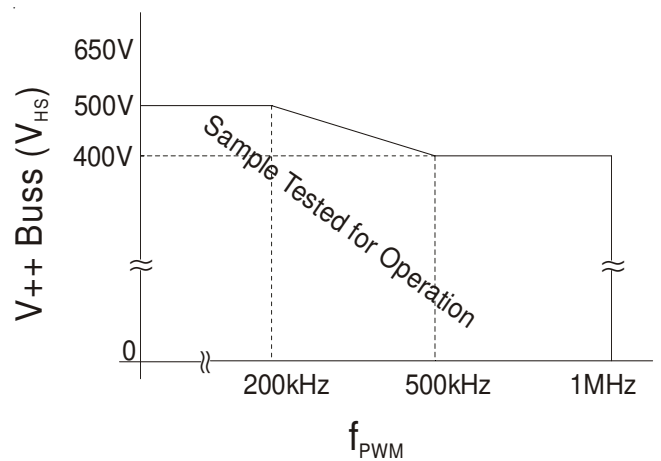


Figure 8. Device operating range: Buss voltage vs. Frequency Tested in typical circuit configuration (refer to Figures 10 & 11)

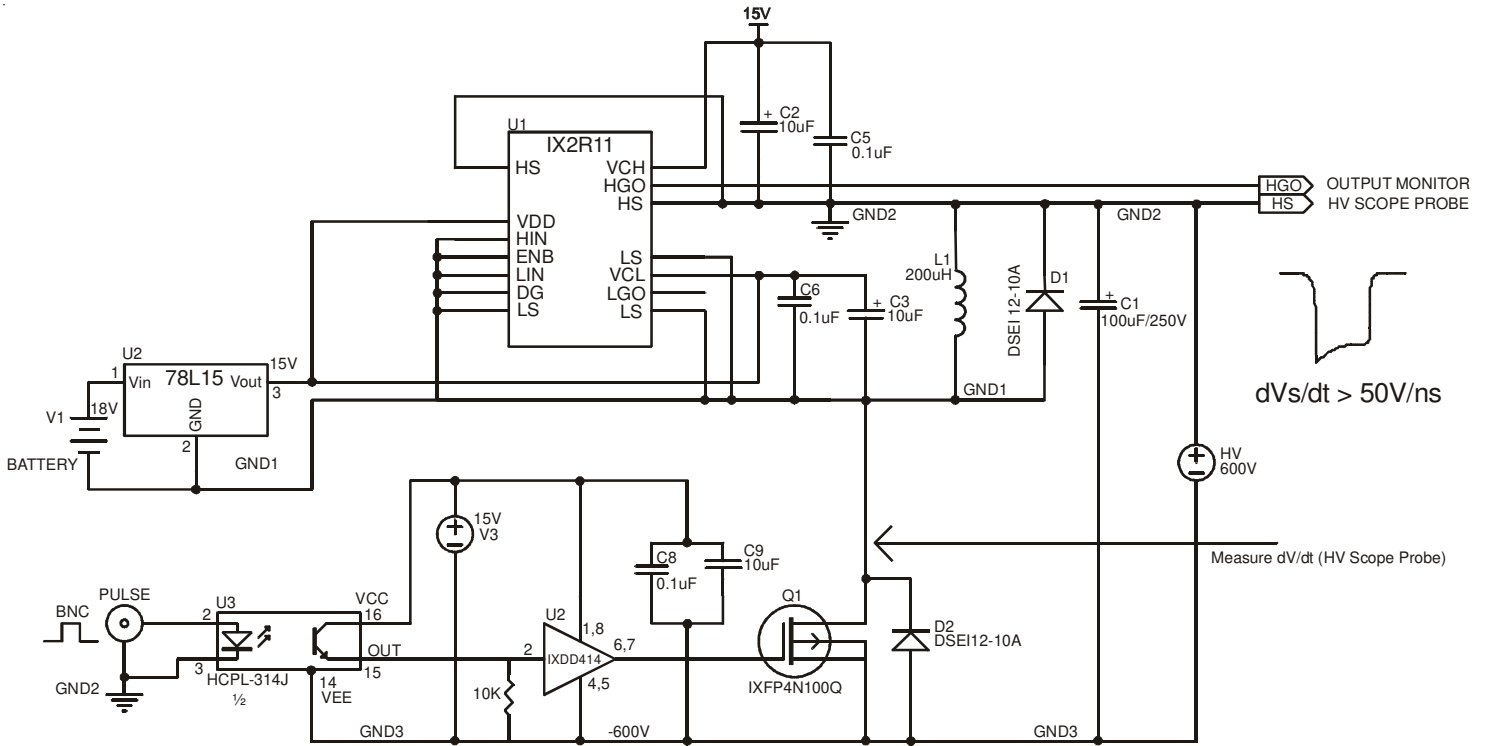


Figure 9. Test circuit for allowable offset supply voltage transient.

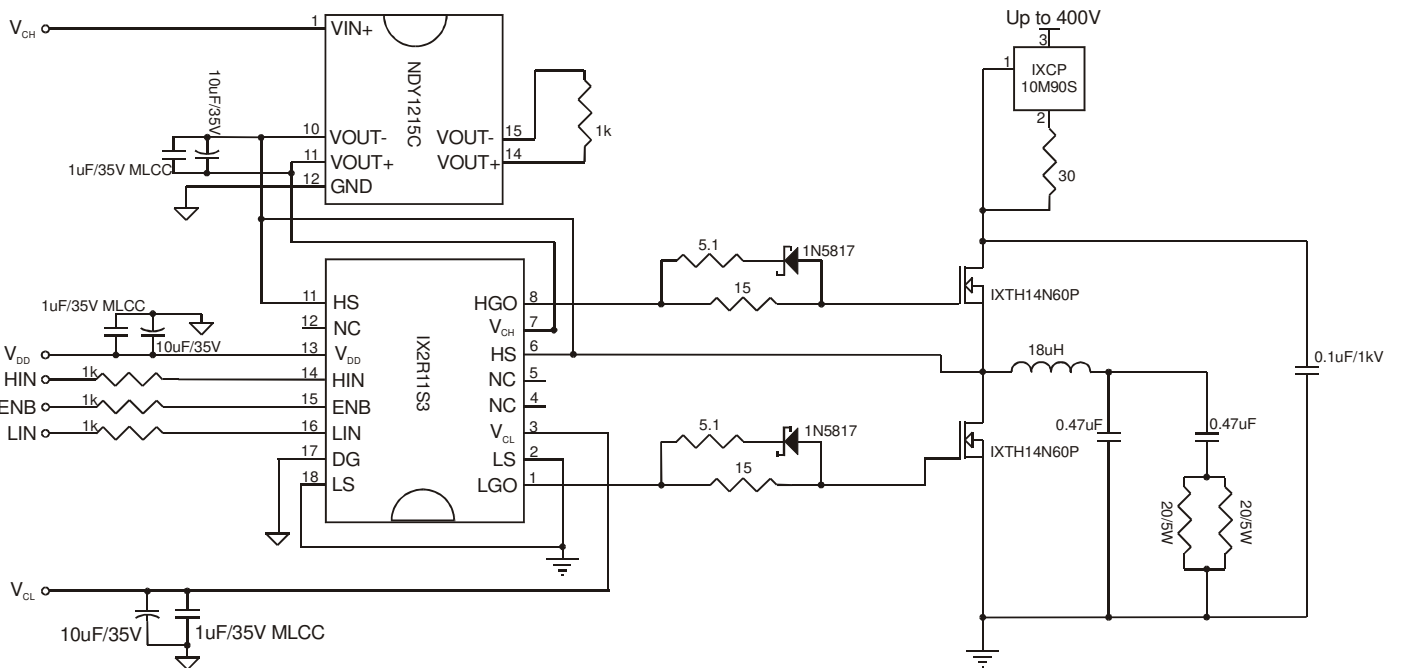


Figure 10. Test circuit for high frequency, 750kHz, operation.

$$V_{DD}, V_{CH}, V_{CL} = 15V$$

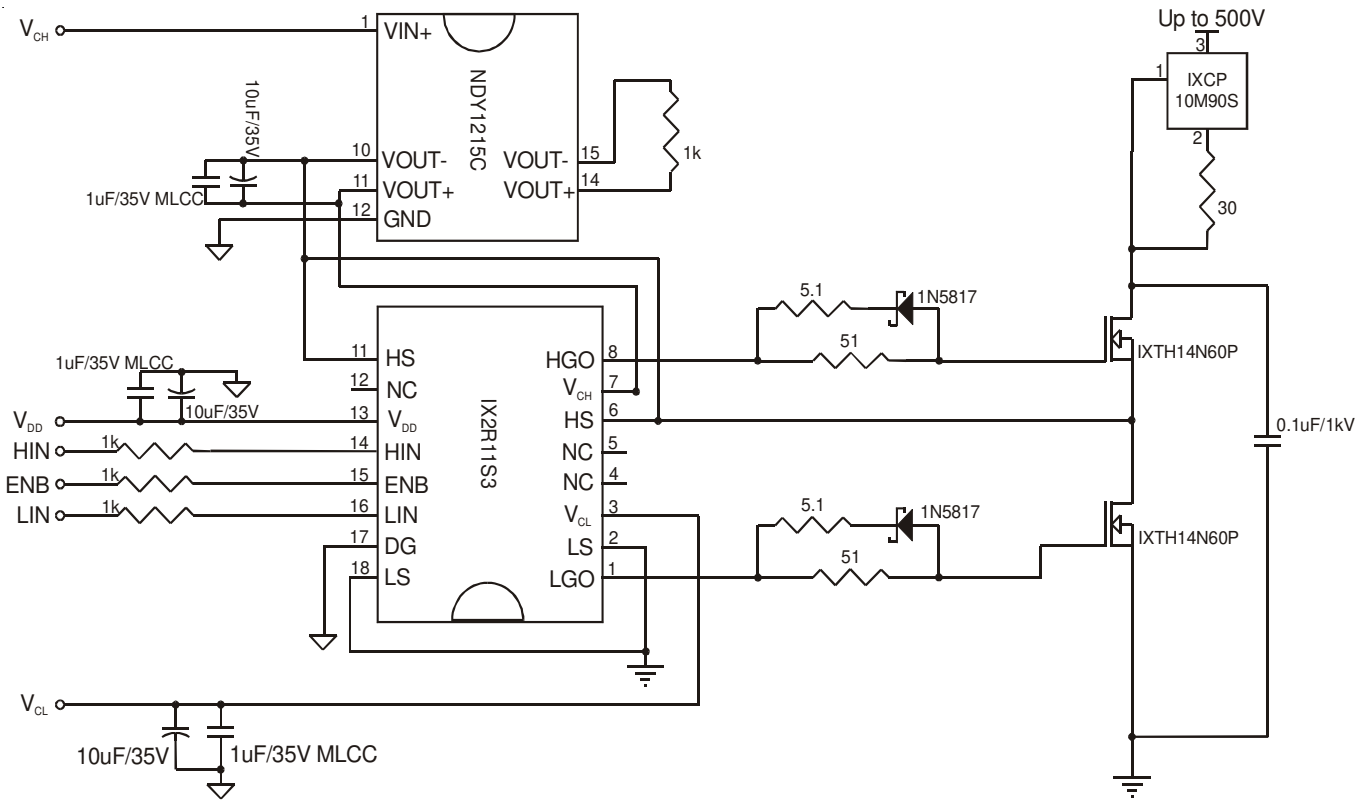


Figure 11. Test circuit for low frequency, 75kHz, operation.
 $V_{DD}, V_{CH}, V_{CL} = 15V$

Figure 12
 Rise Times vs. V_{CL} , V_{CH} Supply Voltage
 $C_{LOAD} = 1000pF$ $V_{DD} = 5V$

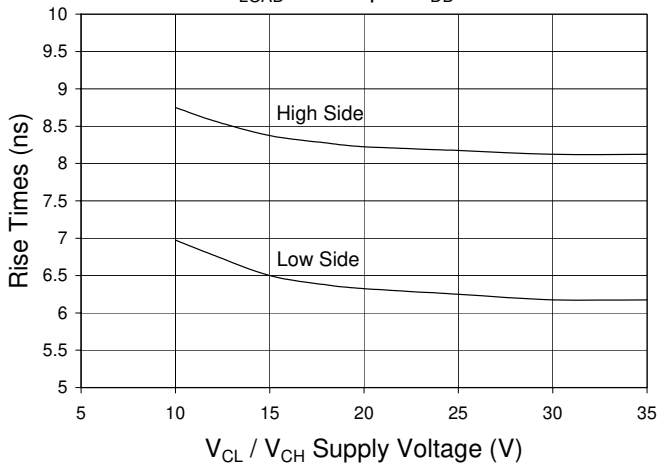


Figure 13
 Fall Times vs. V_{CL} , V_{CH} Supply Voltage
 $C_{LOAD} = 1000pF$ $V_{DD} = 5V$

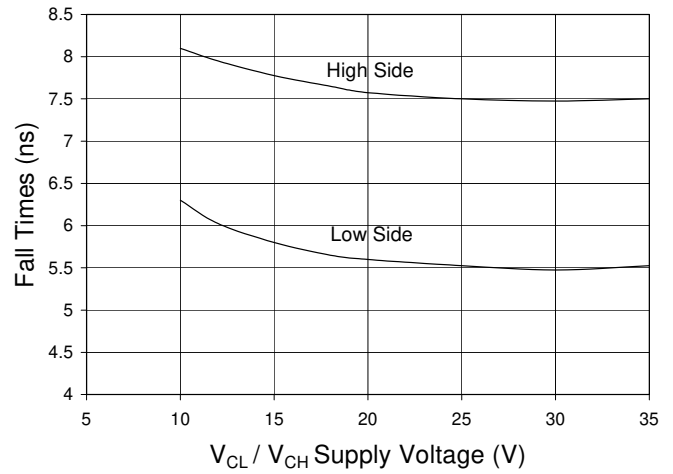


Figure 14
 Rise Times vs. Temperature
 $C_{LOAD} = 1000pF$ $V_{DD}, V_{CL}, V_{CH} = 15V$

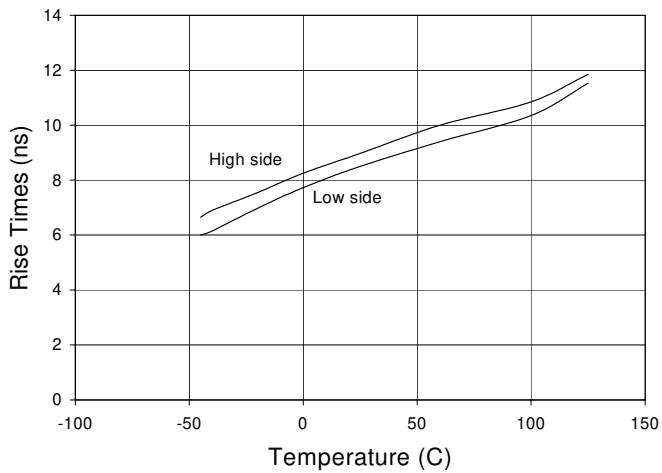


Figure 15
 Fall Times vs. Temperature
 $C_{LOAD} = 1000pF$ $V_{DD}, V_{CL}, V_{CH} = 15V$

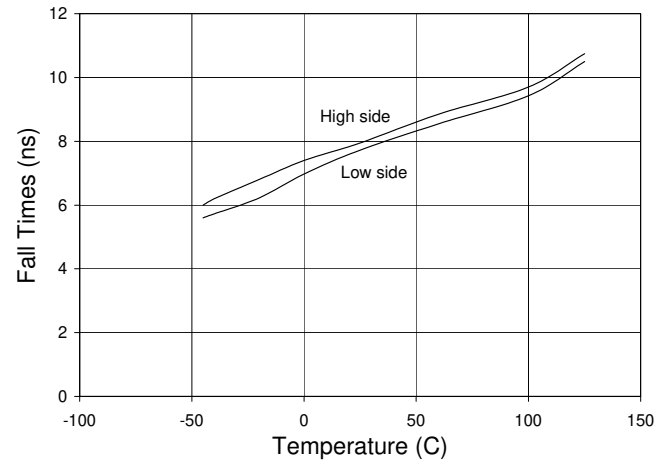


Figure 16
 Input Threshold vs. V_{DD} Supply Voltage

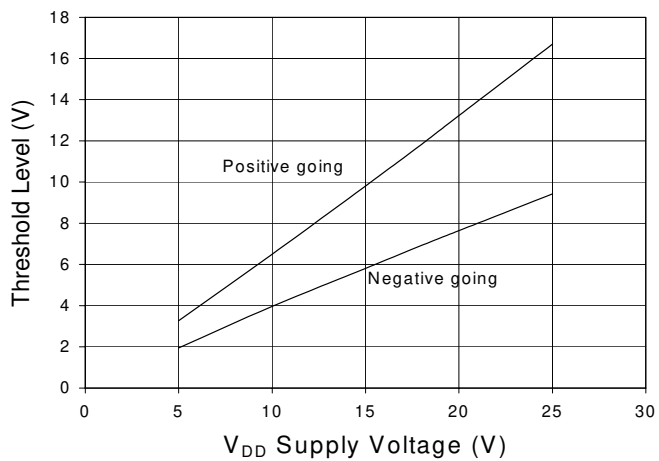


Figure 17
 Input Threshold Level vs. Temperature
 $V_{DD}, V_{CL}, V_{CH} = 15V$

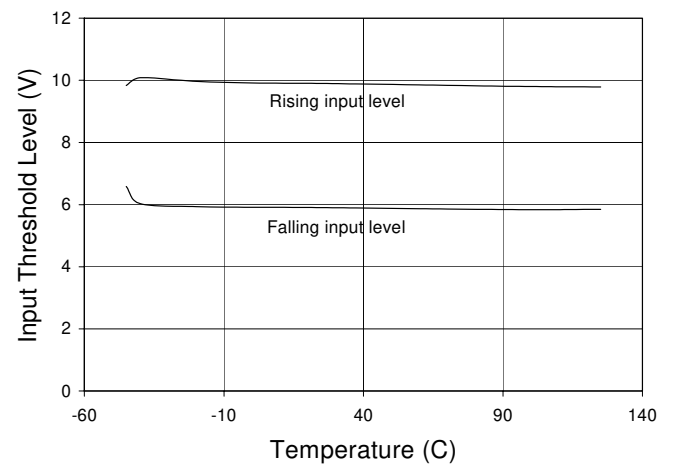


Figure 18
Turn On Propagation Delay vs. V_{CL} , V_{CH} Voltage
 $V_{DD} = 5V$

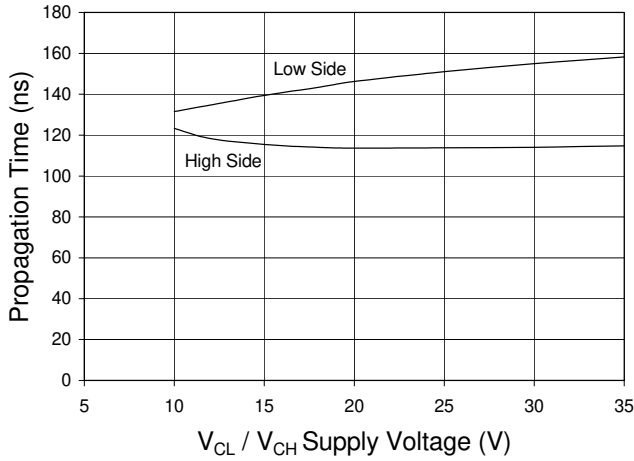


Figure 19
Turn Off Propagation Delay vs. V_{CL} , V_{CH} Voltage
 $V_{DD} = 5V$

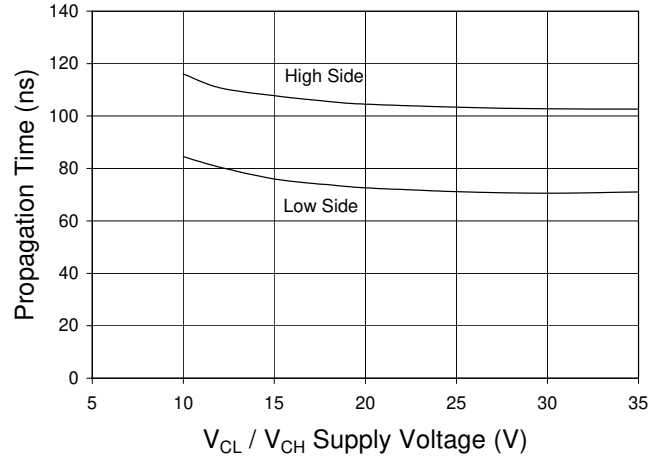


Figure 20
Turn On Propagation Delay vs. V_{DD} Supply Voltage

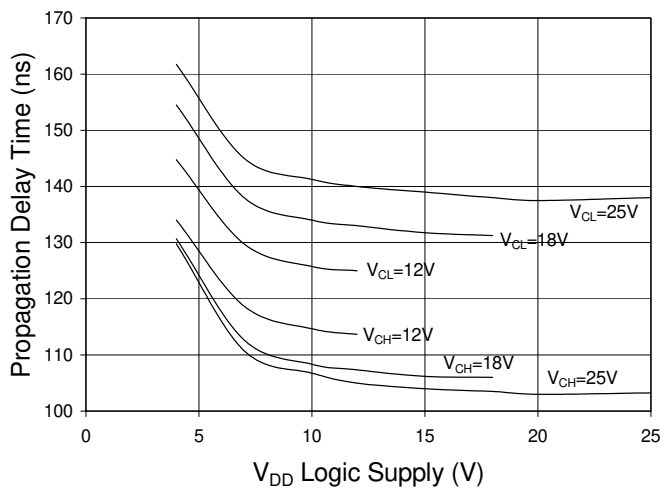


Figure 21
Turn Off Propagation Delay vs. V_{DD} Supply Voltage

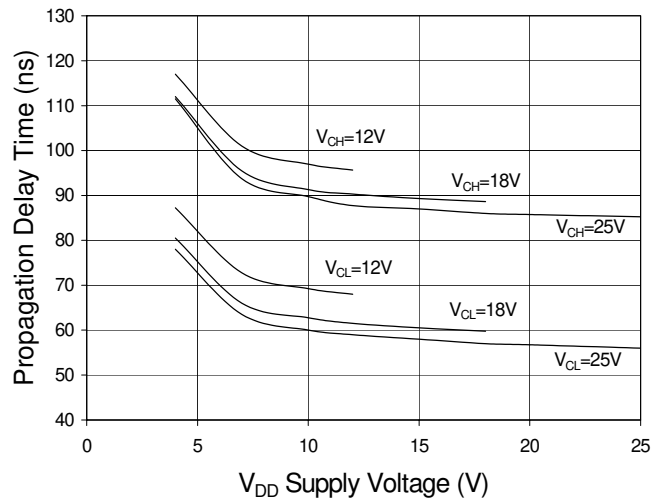


Figure 22
Turn On Propagation Delay vs. Temperature
 $V_{DD}, V_{CL}, V_{CH} = 15V$

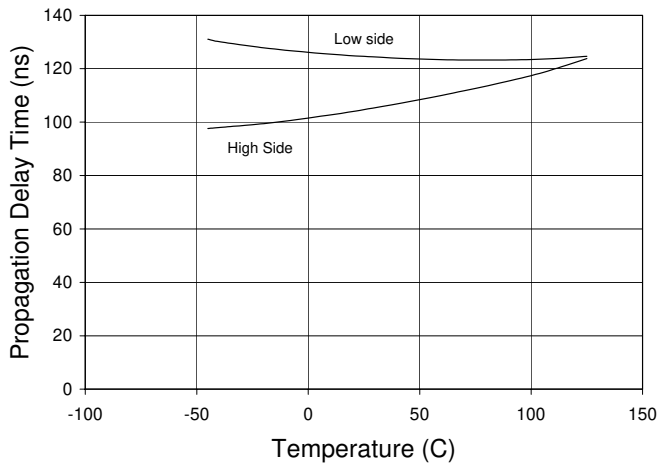


Figure 23
Turn Off Propagation Delay vs. Temperature
 $V_{DD}, V_{CL}, V_{CH} = 15V$

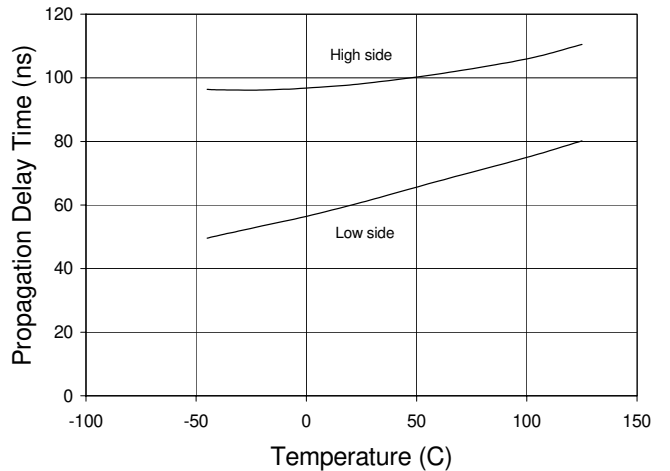


Figure 24
Enable Threshold vs. V_{DD} Logic Supply Voltage
Active Low Enable

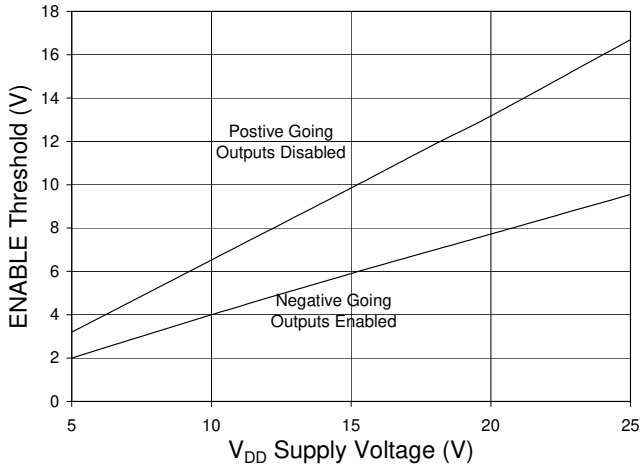


Figure 25
ENABLE Shut Off Delay vs. V_{DD} Supply Voltage

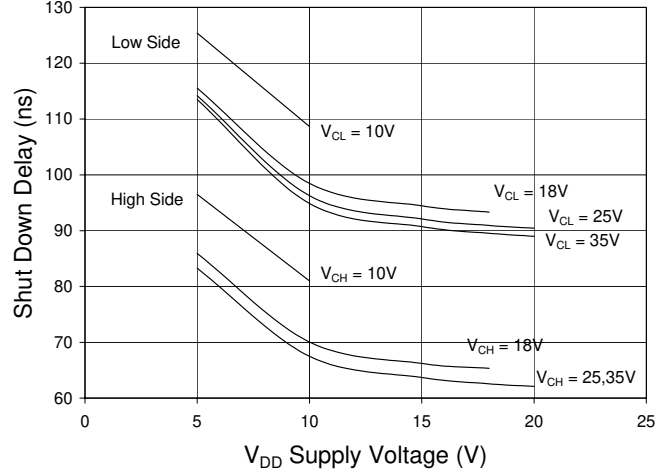


Figure 26
ENABLE Shutdown Delay vs. Temperature
 $V_{DD}, V_{CL}, V_{CH} = 15V$

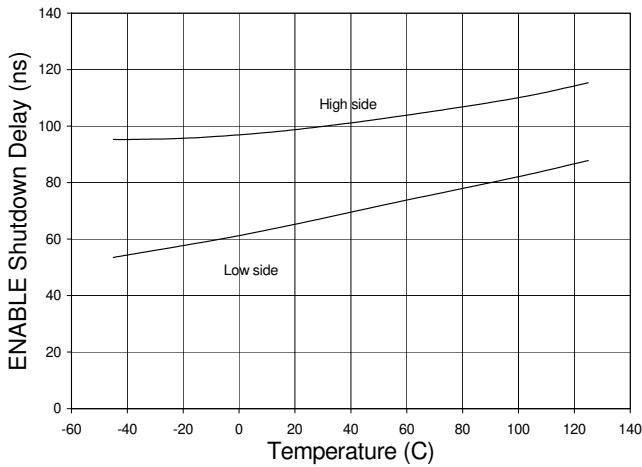


Figure 27
Quiescent Supply Currents vs. Supply Voltages
 $V_{INL}, V_{INH} = 0V$

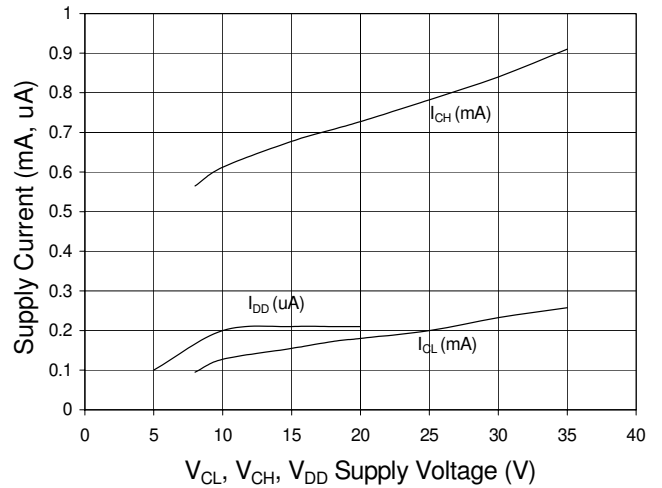


Figure 28
Quiescent Supply Current vs. Temperature
 $V_{DD}, V_{CL}, V_{CH} = 15V \quad V_{INL}, V_{INH} = 0V$

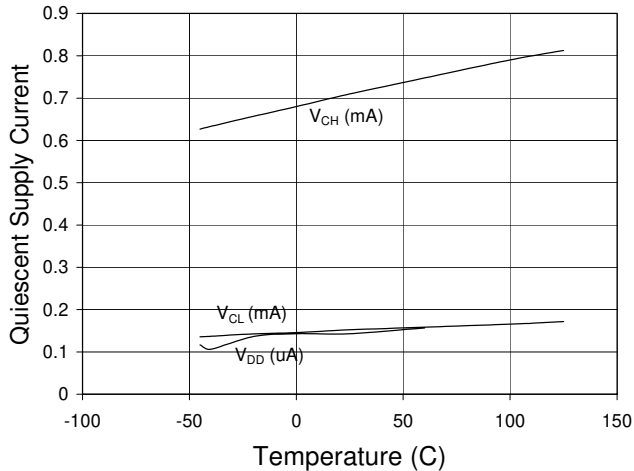


Figure 29
LIN, HIN Input Bias Current vs. V_{DD} Supply Voltage

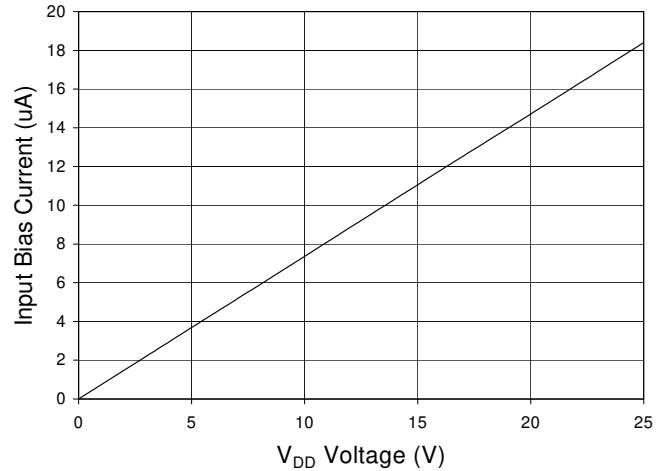


Figure 30

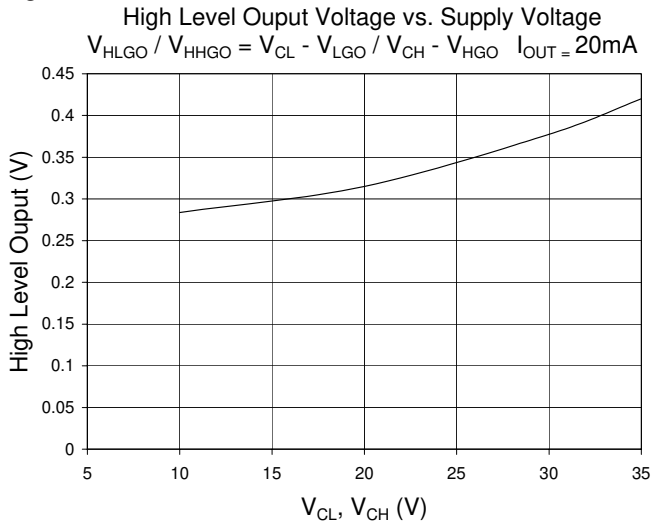


Figure 31

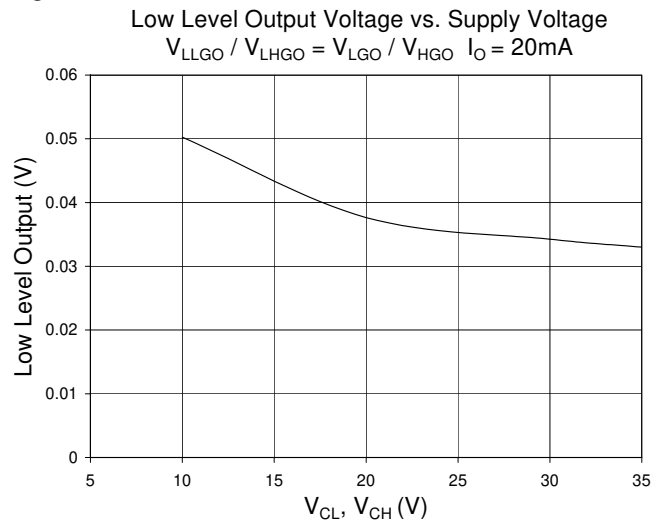


Figure 32

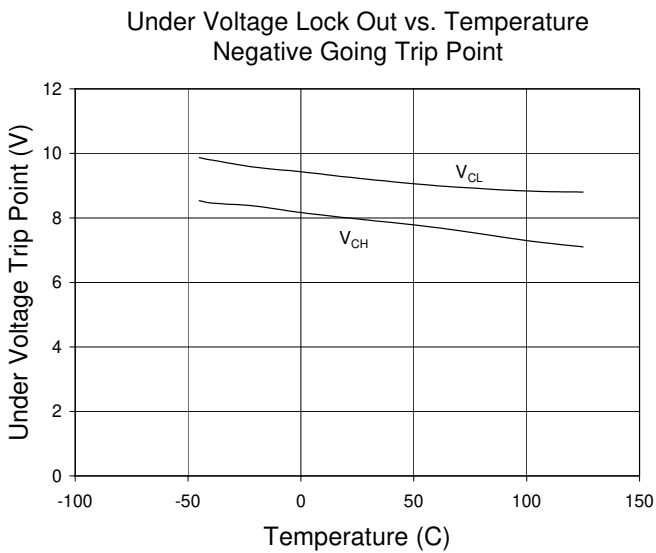


Figure 33

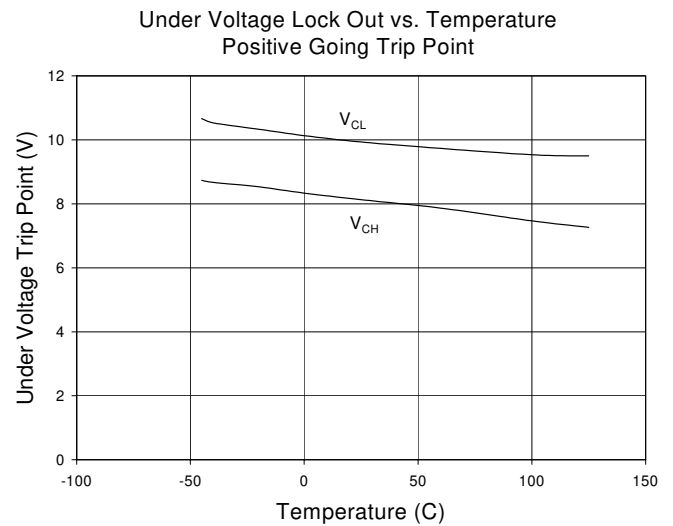


Figure 34

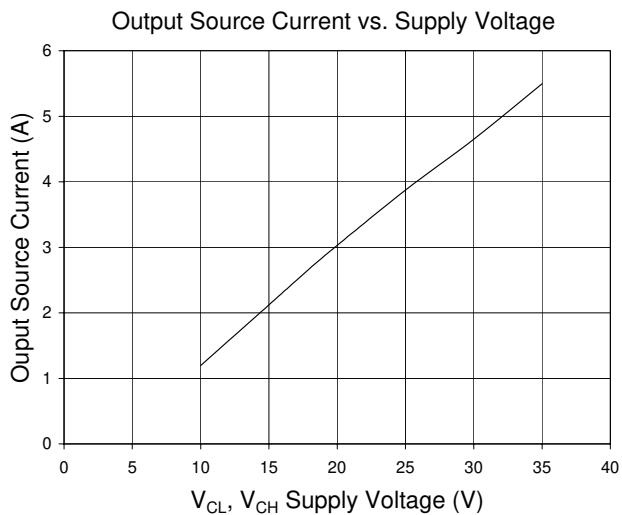


Figure 35

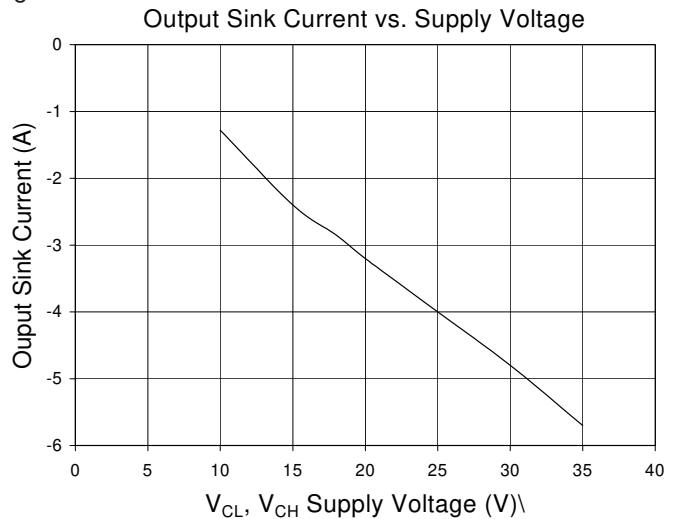


Figure 36

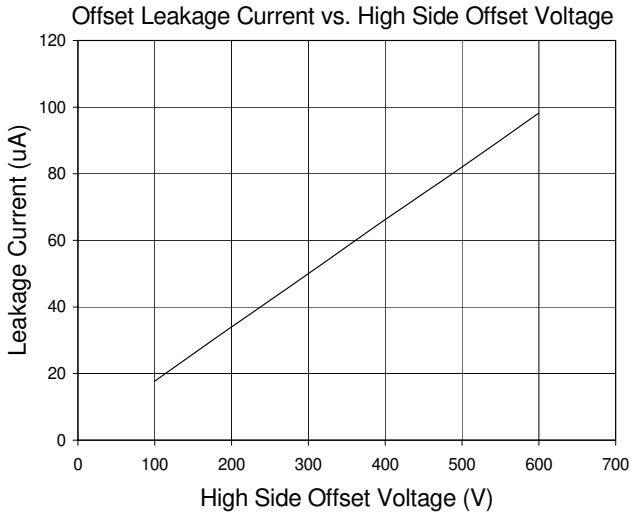


Figure 37

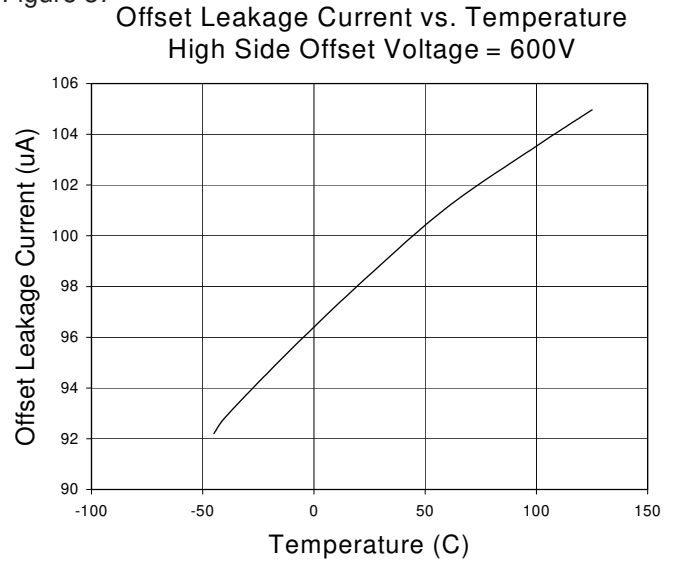


Figure 38

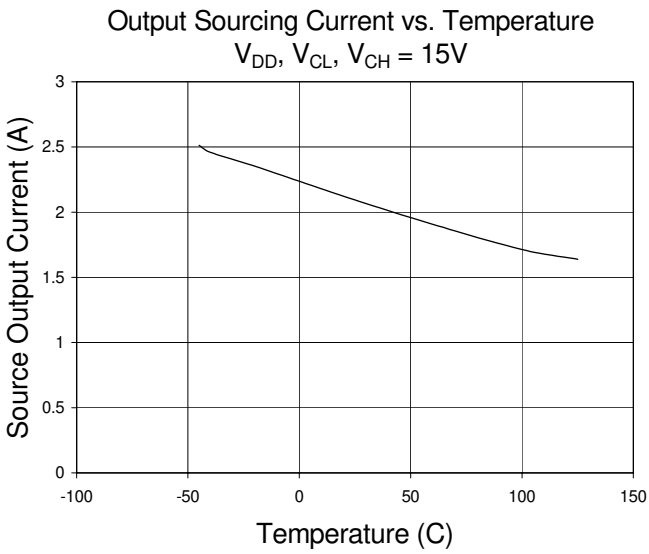
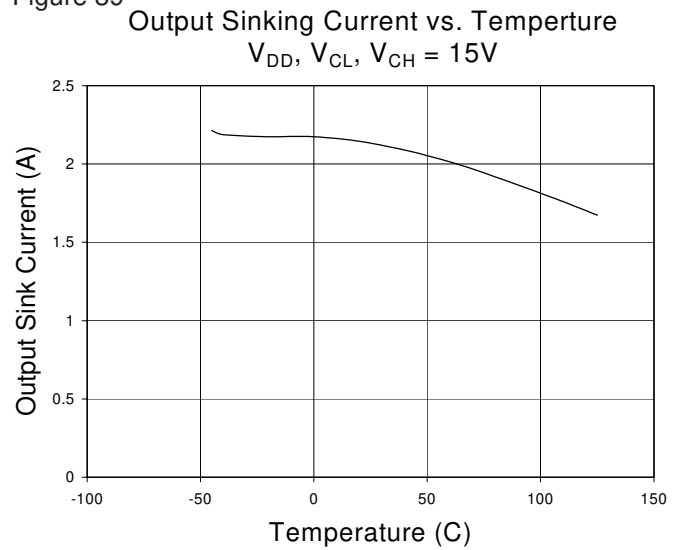
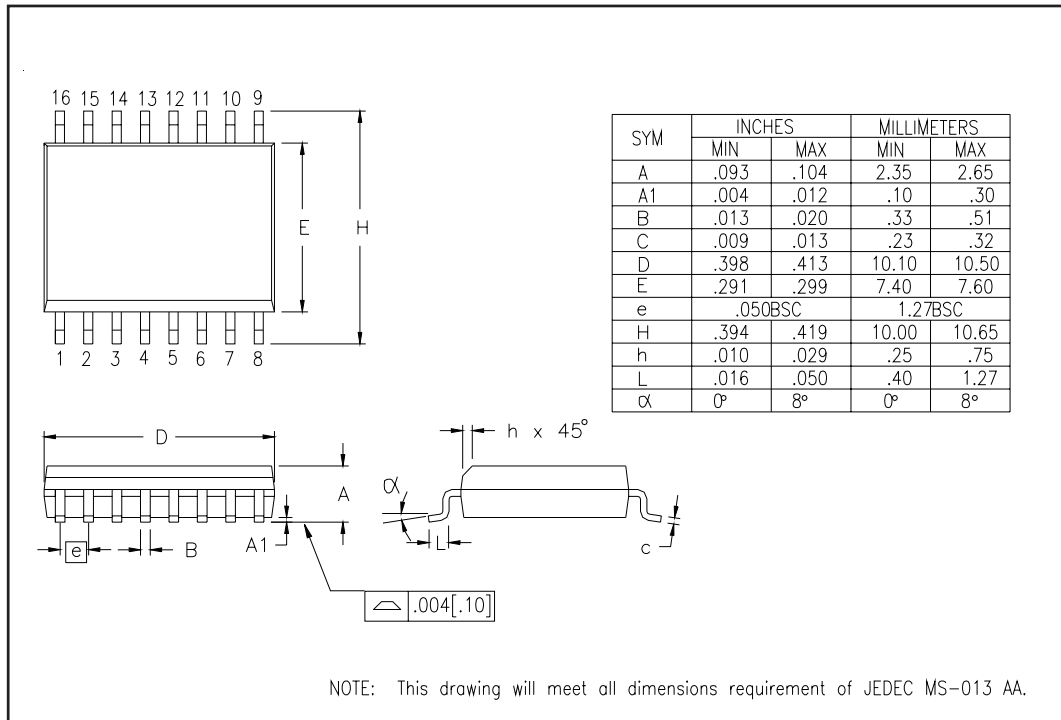


Figure 39



IX2R11S3 Package Outline

IX2R11P7 Package Outline
